Features

- **High performance ULC family suitable for large-sized CPLDs and FPGAs**
- **From 40K gates up to 780K gates supported**
- **Pin counts to over 976 pins**
- **Any pin–out matched due to limited number of dedicated pads**
- **Full range of packages: DIP, SOIC, LCC/PLCC, PQFP/TQFP, BGA, PGA/PPGA**
- **Low quiescent current: 0.3 nA/gate**
- **Available in Commercial, Industrial, and Military grades**
- **0.35 µm Drawn CMOS, 3 and 4 Metal Layers**
- **Library Optimised for Synthesis, Floor Plan & Automatic Test Pattern Generation (ATPG)**
- **High Speed Performances:**
  - **150 ps Typical Gate Delay @3.3V**
  - **Typical 600 MHz Toggle Frequency @3.3V**
  - **Typical 360 MHz Toggle Frequency @2.5V**
- **High System Frequency Skew Control:**
  - **Clock Tree Synthesis Software**
- **Low Power Consumption:**
  - **0.25 µW/Gate/ MHz @3.3V**
  - **0.18 µW/Gate/ MHz @2.5V**
- **Power on Reset**
- **Standard 2, 4, 6, 8,10, 12 and 18mA I/Os**
- **CMOS/TTL/PCI Interface**
- **ESD (2 kV) and Latch-up Protected I/O**
- **High Noise & EMC Immunity:**
  - **I/O with Slew Rate Control**
  - **Internal Decoupling**
  - **Signal Filtering between Periphery & Core**

Description

The UA1 series of ULCs is well suited for conversion of large sized CPLDs and FPGAs on applications which do not require large memories (see UA1E datasheet for application with memories) .Typically, ULC die size is 50% smaller than the equivalent FPGA die size.

Devices are implemented in high–performance CMOS technology with 0.35µm (drawn) channel lengths, and are capable of supporting flip–flop toggle rates of 200 MHz at 3.3V and 180 MHz at 2.5V, and input to output delays as fast as 150ps at 3.3V. The architecture of the UA1 series allows for efficient conversion of many PLD architecture and FPGA device types with higher IO count.

Conversion to the UA1 series of ULC can provide a significant reduction in operating power when compared to the original PLD or FPGA. This is especially true when compared to many PLD and CPLD architecture devices, which typically consume 100mA or more even when not being clocked. The UA1 series has a very low standby consumption of 0.3nA/gate typically commercial temperature, which would yield a standby current of 42µA on a 144,000 gates design. Operating consumption is a strict function of clock frequency, which typically results in a power reduction of 50% to 90% depending on the device being compared.

The UA1 series provides several options for output buffers, including a variety of drive levels up to 18mA. Schmitt trigger inputs are also an option. A number of techniques are used for improved noise immunity and reduced EMC emissions, including: several independent power supply busses and internal decoupling for isolation; slew rate limited outputs are also available if required.

0.35 µm ULC Series

UA1

4327E–ULC–04/08

The UA1 series is designed to allow conversion of high performance 3.3V devices as well as 2.5V devices. Support of mixed supply conversions is also possible, allowing optimal trade–offs between speed and power consumption.

Architecture

The basic element of the UA1 family is called a cell. One cell can typically implement between one to four FPGA gates. Cells are located contiguously through out the core of the device, with routing resources provided in three to four metal layers above the cells. Some cell blockage does occur due to routing, and utilization will be significantly greater with three metal routing than two. The sizes listed in the Product Outline are estimated usable amounts using three metal layers. I/O cells are provided at each pad, and may be configured as inputs, outputs, I/Os, V_{DD} or V_{SS} as required to match any FPGA or PLD pinout.

In order to improve noise immunity within the device, separate V_{DD} and V_{SS} busses are provided for the internal cells and the I/O cells.

I/O buffer interfacing

I/O Flexibility

All I/O buffers may be configured as input, output, bi-directional, oscillator or supply. A level translator could be located close to each buffer.

I/O Options

Inputs

Each input can be programmed as TTL, CMOS, or Schmitt Trigger, with or without a pull up or pull down resistor.

Fast Output Buffer

Fast output buffers are able to source or sink 2 to 18mA at 3.3V according to the chosen option. 36mA achievable, using 2 pads.

Slew Rate Controlled Output Buffer

In this mode, the p– and n–output transistors commands are delayed, so that they are never set “ON” simultaneously, resulting in a low switching current and low noise. These buffers are dedicated to very high load drive.

2.5V Compatibility

The UA1 series of ULC’s is fully capable of supporting high–performance operation at 2.5V or 3.3V. The performance specifications of any given ULC design however, must be explicitly specified as 2.5V, 3.3V or both.

Power Supply and Noise Protection

The speed and density of the UA1 technology cause large switching current spikes, for example when:

- 16 high current output buffers switch simultaneously, or
- 10% of the 700 000 gates are switching within a window of 1ns.

Sharp edges and high currents cause some parasitic elements in the packaging to become significant. In this frequency range, the package inductance and series resistance should be taken into account. It is known that an inductor slows down the setting time of the current and causes voltage drops on the power supply lines. These drops can affect the behavior of the circuit itself or disturb the external application (ground bounce).

In order to improve the noise immunity of the UA1 core matrix, several mechanisms have been implemented inside the UA1 arrays. Two types of protection have been added: one to limit the I/O buffer switching noise and the other to protect the I/O buffers against the switching noise coming from the matrix.

I/O buffers switching protection

Three features are implemented to limit the noise generated by the switching current:

- The power supplies of the input and output buffers are separated.
- The rise and fall times of the output buffers can be controlled by an internal regulator.
- A design rule concerning the number of buffers connected on the same power supply line has been imposed.

Matrix switching current protection

This noise disturbance is caused by a large number of gates switching simultaneously. To allow this without impacting the functionality of the circuit, three new features have been added:

- Decoupling capacitors are integrated directly on the silicon to reduce the power supply drop.
- A power supply network has been implemented in the matrix. This solution reduces the number of parasitic elements such as inductance and resistance and constitutes an artificial V_{DD} and Ground plane. One mesh of the network supplies approximately 150 cells.
- A low pass filter has been added between the matrix and the input to the output buffer. This limits the transmission of the noise coming from the ground or the V_{DD} supply of the matrix to the external world via the output buffers.

Absolute Maximum Ratings[1]

Max SupplyVoltage (V_{DD})	4.0V
Max SupplyVoltage (V_{DD5})	6.0V
Input Voltage (V_{IN})	V_{DD} + 0.5V
Input Voltage 5V Tolerant/Compliant	V_{DD5} + 0.5V
Storage Temperature	-65° to 150°C
Operating Ambient Temperature	-55° to 125°C

Note: 1. Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
This value is based on the maximum allowable die temperature and the thermal resistance of the package.

Recommended Operating Range

V_{DD}	2.5V ± 5% or 3.3V ± 5%
V_{DD5}	5V ± 5%
Operating Temperature	
Commercial	0° to 70°C
Industrial	-40° to 85°C
Military	-55° to 125°C

DC Characteristics

2.5V Supply for Core and Periphery

Symbol	Parameter	Buffer	Min	Typ	Max	Unit	Conditions
TA	Operating Temperature	All	-40		+85	℃	
VDD	SupplyVoltage	All	2.3	2.5	2.7	V	
I_{IH}	High level input current	CMOS			10	µA	$V_{IN} = V_{DD}, V_{DD} = V_{DD}(max)$
		PCI			10		
I_{IL}	Low Level input current	CMOS	-10			µA	$V_{IN} = V_{SS}, V_{DD} = V_{DD}$ (max)
		PCI					
I_{OZ}	High-Impedance State Output Current	All	-10		10	µA	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ (max), No Pull-up
I_{OS}	Output short-circuit current	PO11		9		mA	$V_{OUT} = V_{DD}, V_{DD} = V_{DD}$ (max) $V_{OUT} = V_{SS}, V_{DD} = V_{DD}$ (max)
		PO11		6			
V_{IH}	High-level InputVoltage	CMOS	$0.7V_{DD}$			V	
		PCI	$0.475V_{DD}$				
		CMOS Schmitt	$0.7V_{DD}$	1.5			
V_{IL}	Low-Level InputVoltage	CMOS			$0.3V_{DD}$	V	
		PCI			$0.325V_{DD}$		
		CMOS Schmitt		1.0	$0.3V_{DD}$		
V_{hys}	Hysteresis	CMOS Schmitt		0.5		V	
V_{OH}	High-Level output voltage	PO11	$0.7V_{DD}$			V	I_{OH} = 1.4mA, $V_{DD} = V_{DD}$ (min) I_{OH} = -500µA
		PCI	$0.9V_{DD}$				
V_{OL}	Low-Level output voltage	PO11			0.4	V	I_{OL} = 1.4mA, $V_{DD} = V_{DD}$ (min) I_{OL} = 1.5mA
		PCI			$0.1V_{DD}$		

3.3V Supply for Core and Periphery

Symbol	Parameter	Buffer	Min	Typ	Max	Unit	Conditions
TA	Operating Temperature	All	-40		+85	℃	
V_{DD}	SupplyVoltage	All	3.0	3.3	3.6	V	
I_{IH}	High level input current	CMOS			10	µA	V_{IN} = V_{DD},V_{DD} = V_{DD}(max)
		PCI			10		
I_{IL}	Low Level input current	CMOS	-10			µA	V_{IN} = V_{SS},V_{DD} = V_{DD}(max)
		PCI					
I_{OZ}	High-Impedance State Output Current	All	-10		10	µA	V_{IN} = V_{DD} or V_{SS}, V_{DD} = V_{DD} (max), No Pull-up
I_{OS}	Output short-circuit current	PO11		14		mA	V_{OUT} = V_{DD},V_{DD} = V_{DD} (max) V_{OUT} = V_{SS},V_{DD} = V_{DD} (max)
		PO11		-9			
V_{IH}	High-level InputVoltage	CMOS, LVTTL	2.0			V	
		PCI	0.475V_{DD}				
		CMOS Schmitt	2.0	1.7			
V_{IL}	Low-Level InputVoltage	CMOS			0.8	V	
		PCI			0.325V_{DD}		
		CMOS/TTL-level Schmitt		1.1	0.8		
V_{hys}	Hysteresis	TTL-level Schmitt		0.6		V	
V_{OH}	High-Level output voltage	PO11	0.7V_{DD}			V	I_{OH} = 2mA,V_{DD} = V_{DD} (min) I_{OH} = -500µA
		PCI	0.9V_{DD}				
V_{OL}	Low-Level output voltage	PO11			0.4	V	I_{OL} = 2mA ,V_{DD} = V_{DD} (min) I_{OL} = 1.5mA
		PCI			0.1V_{DD}		

3.3V or 5V Supply for Periphery, 3.3V for Core

Symbol	Parameter	Buffer	Min	Typ	Max	Unit	Conditions
TA	Operating Temperature	All	-55		+125	℃	
V_{DD}	SupplyVoltage	5V Tolerant	3.0	3.3	3.6	V	
V_{DD5}	SupplyVoltage	5V Compliant	4.5	5.0	5.5	V	
I_{IH}	High level input current	CMOS			10	µA	$V_{IN} = V_{DD}, V_{DD} = V_{DD}$(max)
		PCI			10		
I_{IL}	Low Level input current	CMOS	-10			µA	$V_{IN} = V_{SS}, V_{DD} = V_{DD}$(max)
		PCI					
I_{OZ}	High-Impedance State Output Current	All	-10		10	µA	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ (max), No Pull-up
I_{OS}	Output short-circuit current	PO11V		8		mA	$V_{OUT} = V_{DD}, V_{DD} = V_{DD}$ (max) $V_{OUT} = V_{SS}, V_{DD} = V_{DD}$ (max)
		PO11V		-7			
V_{IH}	High-level InputVoltage	PICV, PICV5	2.0	5.0	5.5	V	
		PCI	$0.475V_{DD}$	5.0	5.5		
		CMOS/TTL-level Schmitt	2.0	1.7			
V_{IL}	Low-Level InputVoltage	PICV, PICV5		$0.5V_{DD}$	0.8	V	
		PCI			$0.325V_{DD}$		
		CMOS/TTL-level Schmitt		1.1	0.8		
V_{hys}	Hysteresis	TTL-level Schmitt		0.6		V	
V_{OH}	High-Level output voltage	PO11V	$0.7V_{DD}$			V	I_{OH} = -1.7mA I_{OH} = -1.7mA
		PO11V5	$0.7V_{DD5}$				
V_{OL}	Low-Level output voltage	PO11V			0.5	V	I_{OL} = 1.7mA
		PO11V5			0.5		

I/O Buffer

Symbol	Parameter	Typ	Unit	Conditions
C_{IN}	Capacitance, Input Buffer (Die)	2.4	pF	3.3V
C_{OUT}	Capacitance, Output Buffer (Die)	5.6	pF	3.3V
$C_{I/O}$	Capacitance, Bidirectional	6.6	pF	3.3V

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