



U74HCT14

CMOS IC

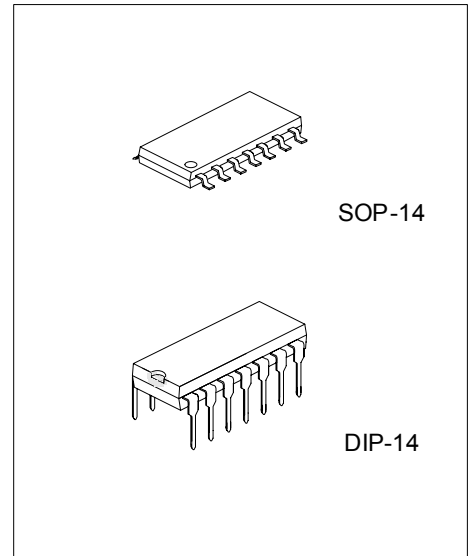
HIGH-SPEED CMOS LOGIC HEX INVERTING SCHMITT TRIGGER

DESCRIPTION

The UTC **74HCT14** each contain six inverting Schmitt triggers in one package. Each of them perform the Boolean function $Y=\overline{A}$.

FEATURES

- * Widely range of input rise and fall time
- * high noise immunity
- * Fan-out parameters(over temperature range)
up to 10 LSTTL Loads
- * Low power consumption
- * Wide range operation 4.5V ~ 5.5V



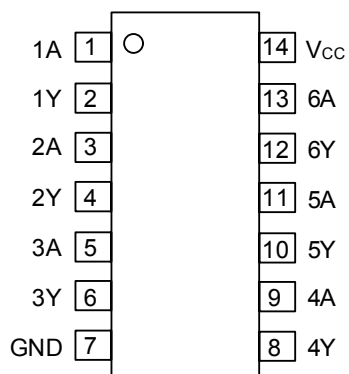
*Pb-free plating product number: 74HCT14L

ORDERING INFORMATION

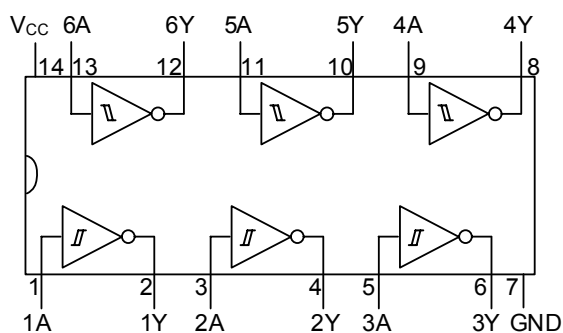
Order Number		Package	Packing
Normal	Lead Free Plating		
U74HCT14-D14-T	U74HCT14L-D14-T	DIP-14	Tube
U74HCT14-S14-R	U74HCT14L-S14-R	SOP-14	Tape Reel
U74HCT14-S14-T	U74HCT14L-S14-T	SOP-14	Tube

U74HCT14L-D14-T	(1)Packing Type (2)Package Type (3)Lead Plating	(1) R: Tape Reel, T: Tube (2) D14: DIP-14, S14: SOP-14 (3) L: Lead Free Plating, Blank: Pb/Sn
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PIN CONFIGURATION



FUNCTIONAL DIAGRAM



TRUTH TABLE

INPUT(A)	OUTPUT(Y)
L	H
H	L

H=High level

L=Low Level

■ LOGIC DIAGRAM

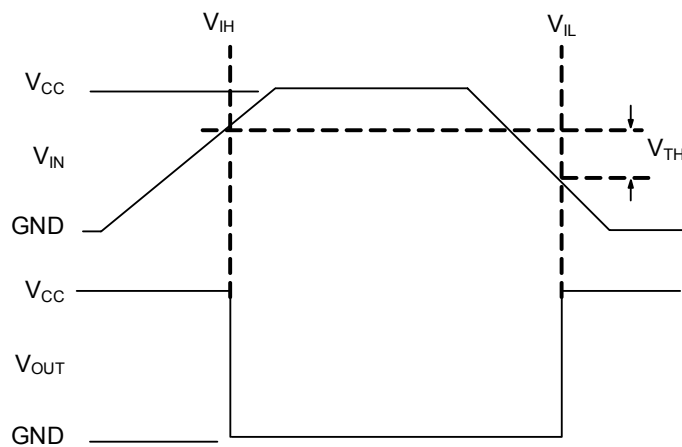
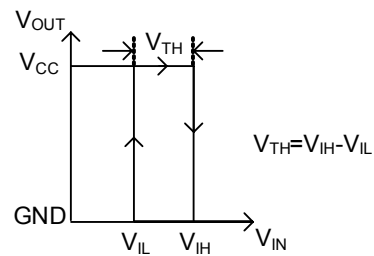
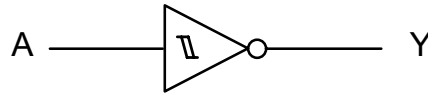


Figure 1. Hysteresis Definition, Characteristic, And Test Setup

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
DC Supply Voltage		V_{CC}	-0.5V~7V	V
DC Input Clamp Current	For $V_{IN} < -0.5V$ or $V_{IN} > V_{CC} + 0.5V$	I_{IK}	± 20	mA
DC Output Clamp Current	For $V_{OUT} < -0.5V$ or $V_{OUT} > V_{CC} + 0.5V$	I_{OK}	± 20	mA
DC Drain Current, per Output	For $-0.5V < V_{OUT} < V_{CC} + 0.5V$	I_{OUT}	± 25	mA
DC Output Source or Sink Current per Output Pin	For $V_{OUT} > -0.5V$ or $V_{OUT} < V_{CC} + 0.5V$	I_{OUT}	± 25	mA
DC V_{CC} or Ground Current		I_{CC}	± 50	mA
Operating Supply Voltage Range		V_{CC}	4.5~5.5	V
Operating DC Input or Output Voltage		V_{IN}, V_{OUT}	0V~ V_{CC}	V
Operating Temperature		T_{OPR}	-40 ~ +85	
Storage Temperature		T_{STG}	-65 ~ +150	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Thermal Resistance Junction Ambient	DIP-14	θ_{JA}	80	/W
	SOP-14		86	

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Switch Points	V_{IH}	$V_{CC}=4.5V$	1.7		1.79	V
		$V_{CC}=5.5V$	1.94		1.96	V
	V_{IL}	$V_{CC}=4.5V$	0.82		0.94	V
		$V_{CC}=5.5V$	0.96		1.15	V
	V_{TH}	$V_{CC}=4.5V$	0.8		0.86	V
		$V_{CC}=5.5V$	0.62		0.83	V
High Level Output Voltage CMOS Loads	V_{OH}	$V_{CC}=4.5V, V_{IN}=V_{IH}$ or $V_{IL}, I_{OUT}=-20\mu A$	4.49	4.495	4.498	V
High Level Output Voltage TTL Loads		$V_{CC}=4.5V, V_{IN}=V_{IH}$ or $V_{IL}, I_{OUT}=-4mA$	3.99	4.00	4.03	V
Low Level Output Voltage CMOS Loads	V_{OL}	$V_{CC}=4.5V, V_{IN}=V_{IH}$ or $V_{IL}, I_{OUT}=20\mu A$	0.41	0.66	1.0	mV
Low Level Output Voltage TTL Loads		$V_{CC}=4.5V, V_{IN}=V_{IH}$ or $V_{IL}, I_{OUT}=4mA$	0.18	0.185	0.19	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5V, V_{IN}=V_{CC}$ and GND			<0.1	μA
Quiescent Device Current	I_{CC}	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0mA$			<1	μA
Additional Quiescent Device	I_{CC} (Note 1)	$V_{CC}=4.5V\sim 5.5V$, One input at 2.4V Other inputs at GND or V_{CC}			25	μA
SWITCHING SPECIFICATIONS (Input $t_R, t_F = 6ns$)						
Propagation Delay, A to Y	t_{PLH}, t_{PHL}	$V_{CC}=4.5V, C_L=50pF$			30	ns
		$V_{CC}=5V, C_L=15pF$			2	ns
Output Transition Times	t_{TLH}, t_{THL}	$V_{CC}=4.5V, C_L=50pF$			12.5	ns
Input Capacitance	C_{IN}				10	pF
Power Dissipation Capacitance(Note 2,3)	C_{PD}	$V_{CC}=5V$		20		pF

Note: 1. This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .

2. C_{PD} is used to determine the dynamic power consumption, per inverter.

3. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

■ TEST WAVEFORM

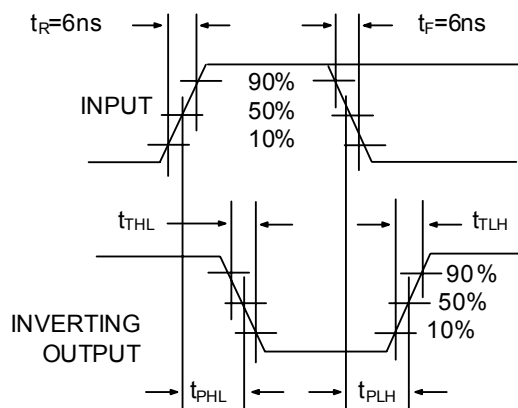


Figure 2. 74HCT14 Transition Times And Propagation Delay Times, Combination Logic

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