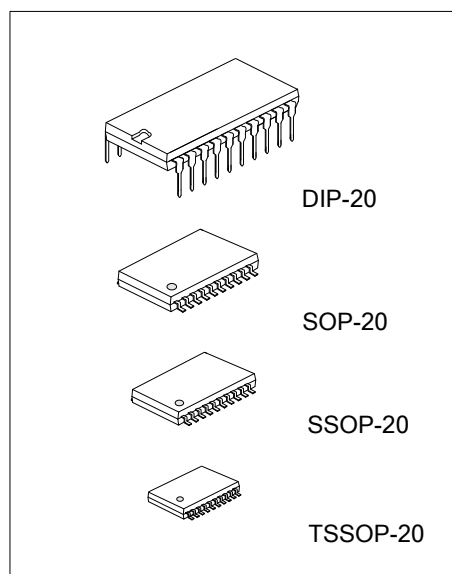


**U74HC245****CMOS IC****OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS****■ DESCRIPTION**

The **U74HC245** is designed for the asynchronous communication between data buses. While the direction-control(DIR) is high, data transmits from the A bus to the B bus. Data transmits from the B bus to the A bus if DIR is low. The output-enable( $\overline{OE}$ ) will isolate the device from the buses when high voltage is applied on it.

**■ FEATURES**

- \* Operate from 2V to 6V
- \* Max  $t_{PD}$  is 18ns at 6V

**■ ORDERING INFORMATION**

| Ordering Number |                 | Package  | Packing   |
|-----------------|-----------------|----------|-----------|
| Lead Free       | Halogen Free    |          |           |
| U74HC245L-D20-T | U74HC245G-D20-T | DIP-20   | Tube      |
| -               | U74HC245G-S20-R | SOP-20   | Tape Reel |
| -               | U74HC245G-R20-R | SSOP-20  | Tape Reel |
| -               | U74HC245G-P20-R | TSSOP-20 | Tape Reel |

|                                                                                           |                                                                                                                                                    |
|-------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>U74HC245L-D20-T</p> <p>(1) Packing Type<br/>(2) Package Type<br/>(3) Green Package</p> | <p>(1) R: Tape Reel, T: Tube<br/>(2) D20: DIP-20, P20: TSSOP-20, R20: SSOP-20, S20: SOP-20<br/>(3) L: Lead Free, G: Halogen Free and Lead Free</p> |
|-------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|

**■ MARKING**

| DIP-20                                                                                                                                                                    | SOP-20 / SSOP-20 / TSSOP-20                                                                                           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|
| <p>20 19 18 17 16 15 14 13 12 11<br/>UTC<br/>U74HC245<br/>L<br/>G<br/>1 2 3 4 5 6 7 8 9 10</p> <p>→ Date Code<br/>→ L: Lead Free<br/>→ G: Halogen Free<br/>→ Lot Code</p> | <p>20 19 18 17 16 15 14 13 12 11<br/>UTC<br/>U74HC245G<br/>1 2 3 4 5 6 7 8 9 10</p> <p>→ Date Code<br/>→ Lot Code</p> |

|     |    |  |    |                        |
|-----|----|--|----|------------------------|
| DIR | 1  |  | 20 | V <sub>CC</sub>        |
| A1  | 2  |  | 19 | $\overline{\text{OE}}$ |
| A2  | 3  |  | 18 | B1                     |
| A3  | 4  |  | 17 | B2                     |
| A4  | 5  |  | 16 | B3                     |
| A5  | 6  |  | 15 | B4                     |
| A6  | 7  |  | 14 | B5                     |
| A7  | 8  |  | 13 | B6                     |
| A8  | 9  |  | 12 | B7                     |
| GND | 10 |  | 11 | B8                     |

| INPUT                  |     | FUNCTION                          |
|------------------------|-----|-----------------------------------|
| $\overline{\text{OE}}$ | DIR |                                   |
| H                      | X   | Isolation                         |
| L                      | H   | Transmit data from A bus to B bus |
| L                      | L   | Transmit data from B bus to A bus |

The logic diagram shows the internal structure of the 74VHC147 decoder. It features two 3-input AND gates at the top. The left AND gate has inputs DIR (pin 1), A1 (pin 2), and a common input from pin 18. Its output is connected to pin 19 (OE). The right AND gate has inputs DIR (pin 1), A1 (pin 2), and a common input from pin 18. Its output is connected to pin 18 (B1). Below these gates, there are two inverters. The first inverter has input A1 (pin 2) and its output is connected to pin 18 (B1). The second inverter has input A1 (pin 2) and its output is connected to pin 19 (OE). The outputs of the two AND gates are also connected to pin 18 (B1) and pin 19 (OE) respectively. The diagram also shows connections for seven other channels, indicated by a bracket and the text "Seven Other channels".

# ■ **ABSOLUTE MAXIMUM RATING** (T<sub>A</sub>=25°C, unless otherwise specified)

| PARAMETER                                  | SYMBOL           | RATINGS    | UNIT |
|--------------------------------------------|------------------|------------|------|
| Supply Voltage                             | V <sub>CC</sub>  | -0.5~7.0   | V    |
| Input Clamp Current (V <sub>IN</sub> <0)   | I <sub>IK</sub>  | ±20        | mA   |
| Output Clamp Current (V <sub>OUT</sub> <0) | I <sub>OK</sub>  | ±20        | mA   |
| Output Current                             | I <sub>OUT</sub> | ±35        | mA   |
| V <sub>CC</sub> or GND Current             | I <sub>CC</sub>  | ±70        | mA   |
| Storage Temperature                        | T <sub>STG</sub> | -65 ~ +150 | °C   |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

# ■ **THERMAL DATA**

| PARAMETER           | SYMBOL   | RATINGS | UNIT |
|---------------------|----------|---------|------|
| Junction to Ambient | DIP-20   | 52      | °C/W |
|                     | SOP-20   | 80      | °C/W |
|                     | SSOP-20  | 96      | °C/W |
|                     | TSSOP-20 | 103     | °C/W |

# ■ **RECOMMENDED OPERATING CONDITIONS**

| PARAMETER                          | SYMBOL           | TEST CONDITIONS       | MIN | TYP | MAX             | UNIT |
|------------------------------------|------------------|-----------------------|-----|-----|-----------------|------|
| Supply Voltage                     | V <sub>CC</sub>  |                       | 2   | 5   | 6               | V    |
| Input Voltage                      | V <sub>IN</sub>  |                       | 0   |     | V <sub>CC</sub> | V    |
| Output Voltage                     | V <sub>OUT</sub> |                       | 0   |     | V <sub>CC</sub> | V    |
| Input Transition Rise or Fall Rate | t <sub>R</sub>   | V <sub>CC</sub> =2V   |     |     | 1000            | ns   |
|                                    |                  | V <sub>CC</sub> =4.5V |     |     | 500             | ns   |
|                                    |                  | V <sub>CC</sub> =6V   |     |     | 400             | ns   |
| Operating Temperature              | T <sub>OPR</sub> |                       | -40 |     | 85              | °C   |

# ■ **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub>=25°C, unless otherwise specified)

| PARAMETER                                          | SYMBOL               | TEST CONDITIONS                                                                   | MIN  | TYP   | MAX  | UNIT |
|----------------------------------------------------|----------------------|-----------------------------------------------------------------------------------|------|-------|------|------|
| High-level input voltage                           | V <sub>IH</sub>      | V <sub>CC</sub> =2V                                                               | 1.5  |       |      | V    |
|                                                    |                      | V <sub>CC</sub> =4.5V                                                             | 3.15 |       |      | V    |
|                                                    |                      | V <sub>CC</sub> =6V                                                               | 4.2  |       |      | V    |
| Low-level output voltage                           | V <sub>IL</sub>      | V <sub>CC</sub> =2V                                                               |      |       | 0.5  | V    |
|                                                    |                      | V <sub>CC</sub> =4.5V                                                             |      |       | 1.35 | V    |
|                                                    |                      | V <sub>CC</sub> =6V                                                               |      |       | 1.8  | V    |
| High-Level Output Voltage                          | V <sub>OH</sub>      | V <sub>CC</sub> =2V, I <sub>OH</sub> =-20μA                                       | 1.9  | 1.998 |      | V    |
|                                                    |                      | V <sub>CC</sub> =4.5V, I <sub>OH</sub> =-20μA                                     | 4.4  | 4.499 |      | V    |
|                                                    |                      | V <sub>CC</sub> =6V, I <sub>OH</sub> =-20μA                                       | 5.9  | 5.999 |      | V    |
|                                                    |                      | V <sub>CC</sub> =4.5V, I <sub>OH</sub> =-6mA                                      | 3.98 | 4.3   |      | V    |
|                                                    |                      | V <sub>CC</sub> =6V, I <sub>OH</sub> =-7.8mA                                      | 5.48 | 5.8   |      | V    |
| Low-Level Output Voltage                           | V <sub>OL</sub>      | V <sub>CC</sub> =2V, I <sub>OL</sub> =20μA                                        |      | 0.002 | 0.1  | V    |
|                                                    |                      | V <sub>CC</sub> =4.5V, I <sub>OL</sub> =20μA                                      |      | 0.001 | 0.1  | V    |
|                                                    |                      | V <sub>CC</sub> =6V, I <sub>OL</sub> =20μA                                        |      | 0.001 | 0.1  | V    |
|                                                    |                      | V <sub>CC</sub> =4.5V, I <sub>OH</sub> =6mA                                       |      | 0.17  | 0.26 | V    |
|                                                    |                      | V <sub>CC</sub> =6V, I <sub>OL</sub> =7.8mA                                       |      | 0.15  | 0.26 | V    |
| Input Current of DIR or $\overline{\text{OE}}$     | I <sub>I(LEAK)</sub> | V <sub>CC</sub> =6V, V <sub>IN</sub> =V <sub>CC</sub> or GND                      |      | ±0.1  | ±100 | nA   |
| Output OFF-state current                           | I <sub>OZ</sub>      | V <sub>CC</sub> =6V, V <sub>OUT</sub> =V <sub>CC</sub> or GND                     |      | ±0.01 | ±0.5 | μA   |
| Quiescent Supply Current                           | I <sub>Q</sub>       | V <sub>CC</sub> =6V, V <sub>IN</sub> =V <sub>CC</sub> or GND, I <sub>OUT</sub> =0 |      |       | 8    | μA   |
| Input Capacitance of DIR or $\overline{\text{OE}}$ | C <sub>IN</sub>      | V <sub>CC</sub> =6V, V <sub>IN</sub> =V <sub>CC</sub> or GND                      |      | 3     | 10   | pF   |

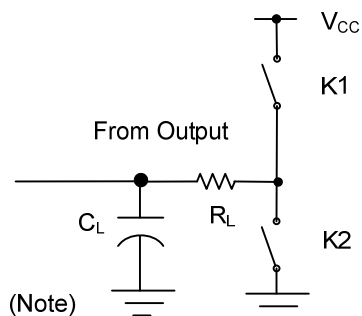
### ■ SWITCHING CHARACTERISTICS (T<sub>A</sub>=25°C, C<sub>L</sub>=50pF, R<sub>L</sub>=1kΩ, unless otherwise specified)

| PARAMETER                                                                     | SYMBOL                                                    | TEST CONDITIONS       | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------------------------|-----------------------------------------------------------|-----------------------|-----|-----|-----|------|
| Propagation delay from input (A or B) to output (B or A)                      | t <sub>PD</sub><br>(t <sub>PLH</sub> /t <sub>PHL</sub> )  | V <sub>CC</sub> =2V   |     | 40  | 105 | ns   |
|                                                                               |                                                           | V <sub>CC</sub> =4.5V |     | 15  | 21  | ns   |
|                                                                               |                                                           | V <sub>CC</sub> =6V   |     | 12  | 18  | ns   |
| 3-state output enable time from input ( $\overline{OE}$ ) to output (A or B)  | t <sub>EN</sub><br>(t <sub>PZL</sub> /t <sub>PZH</sub> )  | V <sub>CC</sub> =2V   |     | 125 | 230 | ns   |
|                                                                               |                                                           | V <sub>CC</sub> =4.5V |     | 23  | 46  | ns   |
|                                                                               |                                                           | V <sub>CC</sub> =6V   |     | 20  | 39  | ns   |
| 3-state output disable time from input ( $\overline{OE}$ ) to output (A or B) | t <sub>DIS</sub><br>(t <sub>PLZ</sub> /t <sub>PHZ</sub> ) | V <sub>CC</sub> =2V   |     | 74  | 200 | ns   |
|                                                                               |                                                           | V <sub>CC</sub> =4.5V |     | 25  | 40  | ns   |
|                                                                               |                                                           | V <sub>CC</sub> =6V   |     | 21  | 34  | ns   |
| Output transition time, (A or B)                                              | t <sub>T</sub><br>(t <sub>R</sub> /t <sub>F</sub> )       | V <sub>CC</sub> =2V   |     | 20  | 60  | ns   |
|                                                                               |                                                           | V <sub>CC</sub> =4.5V |     | 8   | 12  | ns   |
|                                                                               |                                                           | V <sub>CC</sub> =6V   |     | 6   | 10  | ns   |

### ■ OPERATING CHARACTERISTICS

| PARAMETER                     | SYMBOL          | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|-----------------|-----------------|-----|-----|-----|------|
| Power Dissipation Capacitance | C <sub>PD</sub> | No load         |     | 40  |     | pF   |

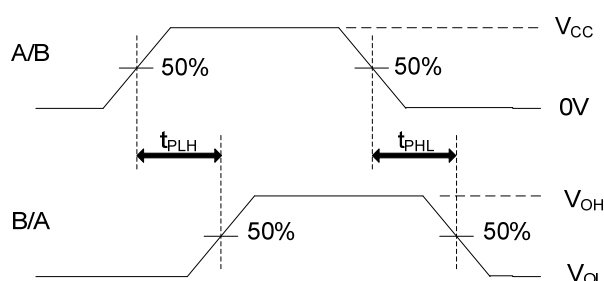
## ■ TEST CIRCUIT AND WAVEFORMS



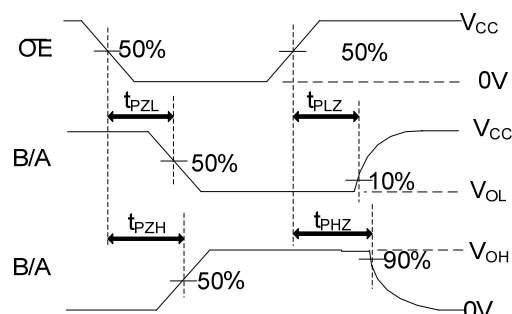
| TEST              | K1    | K2    |
|-------------------|-------|-------|
| $t_{PLH}/t_{PHL}$ | Open  | Open  |
| $t_{PHZ}/t_{PZH}$ | Open  | Close |
| $t_{PLZ}/t_{PZL}$ | Close | Open  |

Note:  $C_L$  includes probe and jig capacitance.

$$P_{RR} \leq 1\text{MHz}, Z_O = 50\Omega, t_R \leq 6\text{ns}, t_F \leq 6\text{ns}$$



Propagation Delay Times



Enable and Disable Times

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