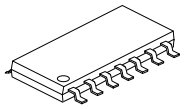
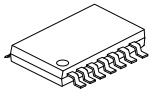
U74ACT04

CMOS IC

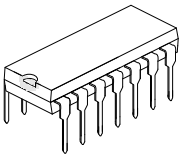
HEX INVERTERS



SOP-14



TSSOP-14



DIP-14

■ DESCRIPTION

The UTC **U74ACT04** contains six independent inverters and each of them performs the Boolean function $Y=\overline{A}$.

■ FEATURES

* Inputs are TTL Voltage Compatible

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74ACT04L-S14-R	U74ACT04G-S14-R	SOP-14	Tape Reel
U74ACT04L-P14-R	U74ACT04G-P14-R	TSSOP-14	Tape Reel
U74ACT04L-D14-T	U74ACT04G-D14-T	DIP-14	Tube

U74ACT04G-S14-L
- (1)Packing Type
- (2)Package Type
- (3)Lead Free

(1) R: Tape Reel, T: Tube
(2) S14: SOP-14, D14: DIP-14, P14: TSSOP-14
(3) G: Halogen Free, L: Lead Free

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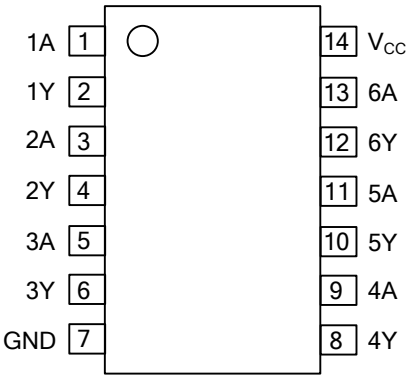
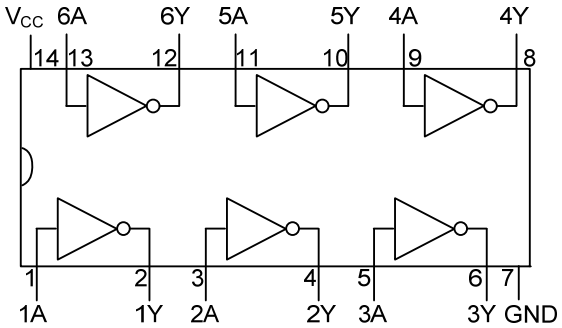
■ PIN CONFIGURATION



■ FUNCTIONAL DIAGRAM

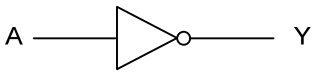


■ FUNCTION TABLE

INPUT(A)	OUTPUT(Y)
L	H
H	L

Note: H=High level; L=Low Level

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
DC Supply Voltage		V_{CC}	-0.5 ~ 7	V
Input Voltage		V_{IN}	-0.5 ~ V_{CC}+0.5	V
Output Voltage		V_{OUT}	-0.5 ~ V_{CC}+0.5	V
DC Input Clamp Current	For V_{IN} < 0 or V_{IN} > V_{CC}	I_{IK}	±20	mA
DC Output Clamp Current	For V_{OUT} < 0 or V_{OUT} > V_{CC}	I_{OK}	±20	mA
Continuous Output Current	For V_{OUT}=0 to V_{CC}	I_{OUT}	±50	mA
Continuous Current Through V_{CC} or GND			±200	mA
Operating Temperature		T_{OPR}	-40 ~ +85	°C
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-14	θ_{JA}	81	°C/W
	SOP-14		112	
	TSSOP-14		141	

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}			4.5		5.5	V
High Level Input Voltage	V_{IH}	V_{CC}=4.5~5.5V		2			V
Low Level Input Voltage	V_{IL}	V_{CC}=4.5~5.5V				0.8	V
High Level Output Voltage	V_{OH}	V_{CC}=4.5V	I_{OUT}=-50μA	4.4	4.49		V
		V_{CC}=5.5V		5.4	5.49		V
		V_{CC}=4.5V	I_{OUT}=-24 mA	3.86			V
		V_{CC}=5.5V		4.86			V
Low Level Output Voltage	V_{OL}	V_{CC}=4.5V	I_{OUT}=-50μA		0.001	0.1	V
		V_{CC}=5.5V			0.001	0.1	V
		V_{CC}=4.5V	I_{OUT}=24mA			0.36	V
		V_{CC}=5.5V				0.36	V
Input Leakage Current	$I_{I(Leak)}$	V_{CC}=5.5V, V_{IN}=V_{CC} or GND				±0.1	μA
Quiescent Device Current	I_Q	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0				2	μA
Additional quiescent Supply Current	ΔI_Q	V_{CC}=5.5V, One input at 3.4V, Other inputs at GND or V_{CC}			0.6		mA
Input Capacitance	C_{IN}	V_{CC}=5V, V_{IN}=V_{CC} or GND			4.5		pF

■ SWITCHING SPECIFICATIONS (T_A=25°C ,Input t_R, t_F = 2.5ns)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay, A to Y	t_{PLH}	V_{CC}=5±0.5V, C_L=50pF, R_L=500Ω	1	6	8.5	ns
	t_{PHL}	V_{CC}=5±0.5V, C_L=50pF, R_L=500Ω	1	5.5	8	ns
Power Dissipation Capacitance (Notes 1, 2)	C_{PD}	V_{CC}=5V, C_L=50pF,f=1MHZ		45		pF

Note 1. C_{PD} is used to determine the dynamic power consumption, per inverter.

2. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

■ TEST CIRCUITS AND WAVEFORMS

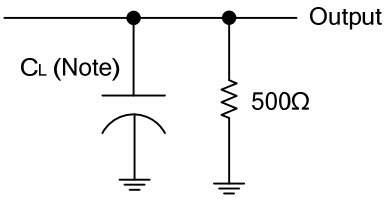


Fig.1: Load circuitry for switching times.
Note: C_L includes probe and jig capacitance.

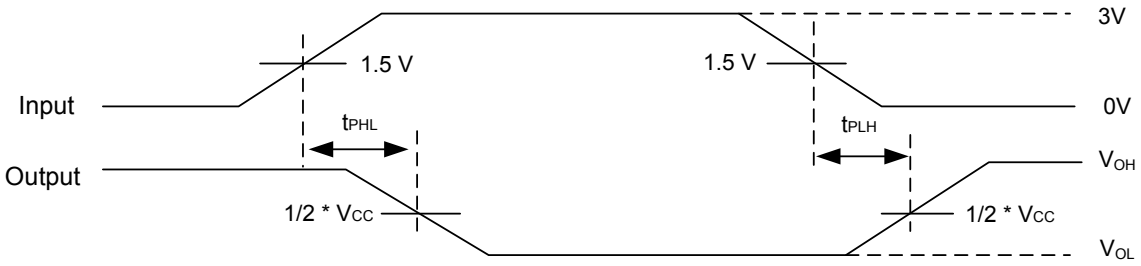


Fig.2: Propagation delay from Input(A) to Output(Y).

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