



U7313

CMOS IC

AUDIO PROCESSOR IC

■ DESCRIPTION

The **U7313** is a 3-stereo inputs and 4-speaker outputs digital audio processor which incorporates volume, tone(bass and treble) , balance(left/right)and fader(front/rear) into a single chip. Selectable input gain and loudness function are provided to build a highly effective electronic audio processor having the highest performance and reliability with the external components. The AC signal setting is obtained by resistor networks and switches which are set by programming serial input signal via I²C bus. In addition, BiCOMS processes are utilized for low distortion, low noise and low DC stepping.

The **U7313** is designed for quality audio applications in car radio and Hi-Fi systems.

■ FEATURES

- * Support I²C bus interface
- * 3 stereo inputs and selectable input gain
- * Volume control in 1.25dB/step
- * Loudness function
- * Bass and treble control
- * 4 independent speakers control
- * Independent mute function
- * Low distortion
- * Low noise and DC stepping

■ ORDERING INFORMATION

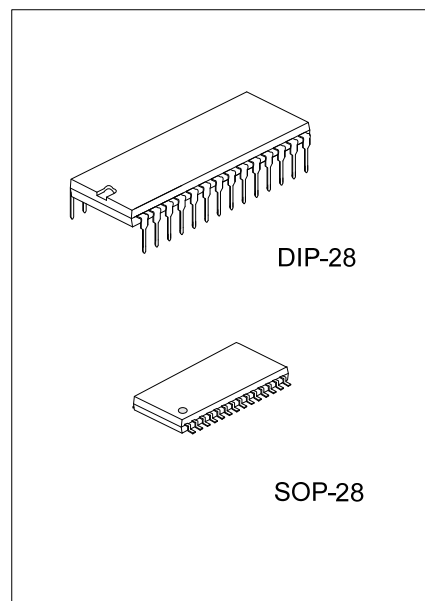
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U7313L-D28-T	U7313G-D28-T	DIP-28	Tube
U7313L-S28-R	U7313G-S28-R	SOP-28	Tape Reel
U7313L-S28-T	U7313G-S28-T	SOP-28	Tube

U7313L-D28-T

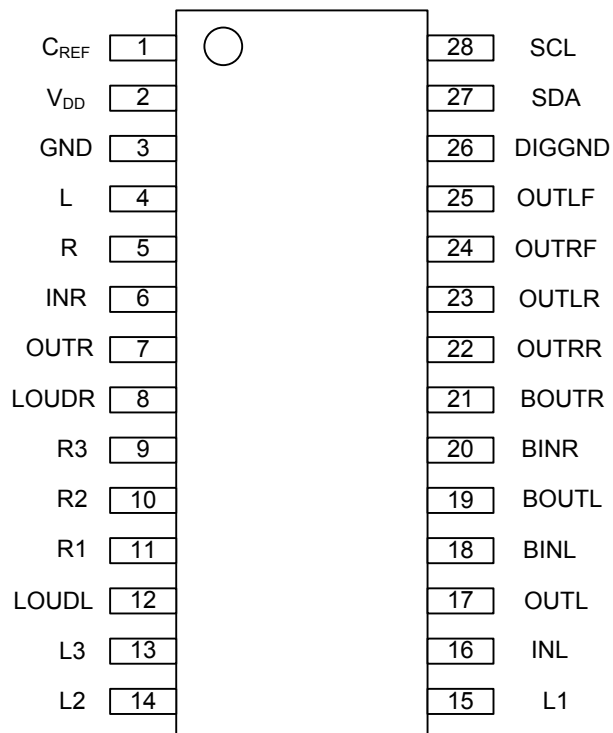


- (1)Packing Type
- (2)Package Type
- (3)Lead Free

- (1) R: Tape Reel, T: Tube
- (2) D28: DIP-28, S28: SOP-28
- (3) G: Halogen Free, L: Lead Free



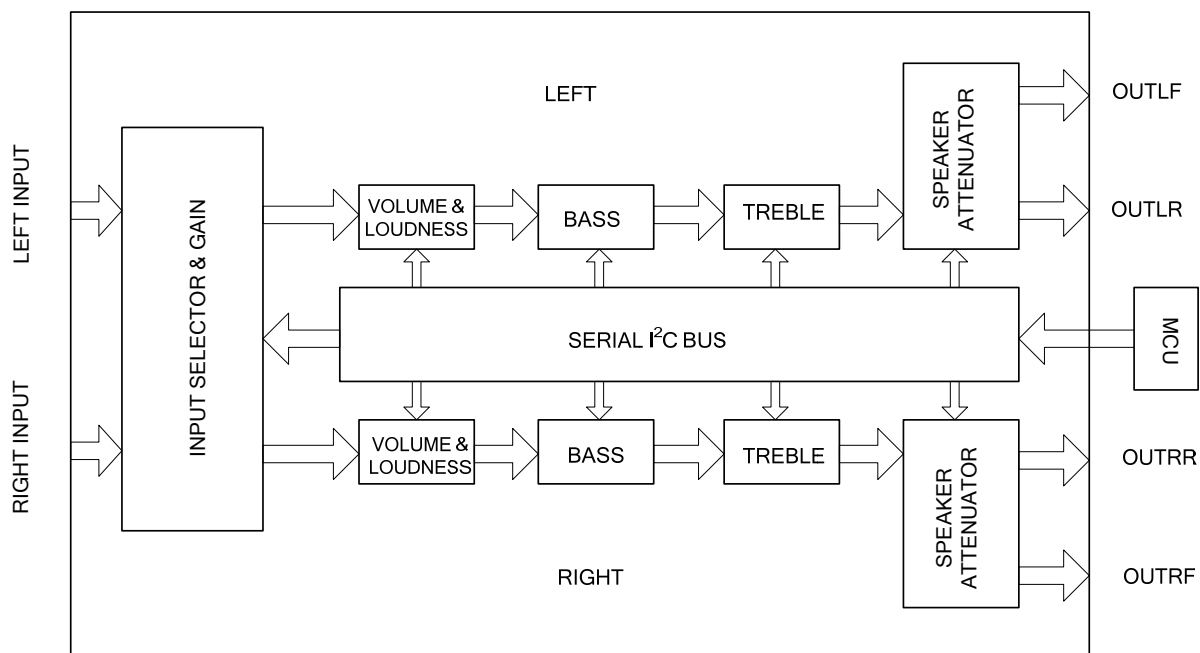
■ PIN CONFIGURATION



■ PIN DESCRIPTIONS

PIN NO.	PIN NAME	I/O	PIN DESCRIPTION
1	C _{REF}		Internal reference voltage, typical value is vdd/2, connect a capacitor to gnd to depress ripple voltage.
2	V _{DD}		Supply voltage.
3	GND		Analog gnd.
4	L	I	Connect a capacitor to gnd, the center frequency and quality of the response behavior of treble module can be chosen by the capacitor. (Left speaker)
5	R	I	Connect a capacitor to gnd, the center frequency and quality of the response behavior of treble module can be chosen by the capacitor. (Right speaker)
6	INR	I	Input of volume module.(Right speaker)
7	OUTR	O	Output of gain module.(Right speaker)
8	LOUDR	I	Connect a capacitor to gnd, change the capacitor can adjust the amplitude-frequency characteristic of loudness.(Right speaker)
9	R3	I	Channel 3 input.(Right speaker)
10	R2	I	Channel 2 input.(Right speaker)
11	R1	I	Channel 1 input.(Right speaker)
12	LOUDL	I	Connect a capacitor to gnd, change the capacitor can adjust the frequency-amplitude characteristic of loudness.(Left speaker)
13	L3	I	Channel 3 input.(Left speaker)
14	L2	I	Channel 2 input.(Left speaker)
15	L1	I	Channel 1 input.(Left speaker)
16	INL	I	Input of volume module.(Left speaker)
17	OUTL	O	Output of gain module.(Left speaker)
18	BINL	I	See the application circuit, change the capacitor and the resistor can adjust the center frequency and quality of the response behavior of bass module.(Left speaker)
19	BOUTL	I	See the application circuit, change the capacitor and the resistor can adjust the center frequency and quality of the response behavior of bass module. (Left speaker)
20	BINR	I	See the application circuit, change the capacitor and the resistor can adjust the center frequency and quality of the response behavior of bass module. (Right speaker)
21	BOUTR	I	See the application circuit, change the capacitor and the resistor can adjust the center frequency and quality of the response behavior of bass module. (Right speaker)
22	OUTRR	O	Output of the right rear speaker.
23	OUTLR	O	Output of left rear speaker.
24	OUTRF	O	Output of right front speaker.
25	OUTLF	O	Output of left front speaker.
26	DIG GND		Digital gnd of serial I ² C bus.
27	SDA	I/O	Data signal of serial I ² C bus.
28	SCL	I	Clock signal of serial I ² C bus.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage	V _{DD}	-0.5~10.2	V
Max Input Clock Speed of Serial I ² C Bus Signal	B _{CLK}	100	KBit/s
Operating Ambient Temperature	T _{OPR}	-40~+85	°C
Storage Temperature	T _{STG}	-55~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied

■ OVERALL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage	V _{DD}		6	9	10	V
Supply Current	I _S	V _{DD} =9V		8	11	mA
Ripple Rejection	RR	V _S =9V, R _L =10KΩ, R _G =600Ω	60	80		dB
Signal to Noise Ratio	S/N	All gains=0dB; V _{OUT} =1Vrms		106		dB
Total Harmonic Distortion	THD	V=1Vrms f=1KHZ		0.01	0.1	%
Channel Separation	S(channel)	f=1KHZ		103		dB
Input Gain Per Step	Au(gain)			3.75		dB/step
Volume Control Per Step	Au(volume)			1.25		dB/step
Bass Control Per Step	Au(bass)	f =100HZ		2		dB/step
Treble Control Per Step	Au(treble)	f =20KHZ		2		dB/step
Speaker Control Per Step	Au(speaker)			1.25		dB/step
Total Tracking Error	Au(error)	Au=0 to -20dB -20 to -60dB		0 0	1 2	dB

■ MODULE CHARACTERISTICS

(Ta=25°C, V_{DD}=9V, R_L=10KΩ, (gain and all control 0dB), f=1KHZ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
DC SUPPLY						
DC Supply Voltage	V _{DD}		6	9	10	V
Supply Current	I _S			8	11	mA
GAIN & INPUT SELECTOR						
Input Resistance	R _{I G}	Input1,2,3	35	50	70	KΩ
Clipping Level	V _{CL}		2	2.5		Vrms
Input Separation(input 1,2,3)	S _{IN}		80	100		dB
Output Load resistance	R _L	OUTL OUTR	2			KΩ
Gain Range	G _{IN}			11.25		dB
Min. Gain	G _{INmin}		-1	0	1	dB
Max. Gain	G _{INmax}			11.25		dB
Adjacent Gain Steps	G _{STEP}			3.75		dB
Input Noise	e _{IN}	G=11.25dB		2		uV
DC Shift Voltage Steps	V _{DC}	adjacent gain steps		4	20	mV
		G=18.75 to Av max		4		mV
VOLUME CONTROL						
Input Resistance	R _{I V}	Pin6,16	20	33	50	KΩ
Control Range	G _V		70	75	80	dB
Min. Attenuation	Au _{MIN}		-1	0	1	dB
Max. Attenuation	Au _{MAX}		70	75	80	dB
Adjacent Attenuation Steps	Au _{STEP}		0.5	1.25	1.75	dB
Attenuation Set Error	E _A	Au=0 to -20dB	-1.25	0	1.25	dB
		Au=-20 to -60dB	-3		2	dB

■ MODULE CHARACTERISTICS(Cont.)

PARAMETER		SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Tracking Error		E _T				2	dB
DC Shift Voltage Steps		V _{DC}	Adjacent attenuation steps		0	3	mV
			from 0dB to Au max		0.5	7.5	mV
BASS CONTROL							
Control Range		G _b	Center freq=100HZ	±12	±14	±16	dB
Adjacent Attenuation Steps		B _{STEP}		1	2	3	dB
Internal Feedback Resistance		R _B		34	44	58	KΩ
TREBLE CONTROL							
Control Range		G _t	Center freq=20KHZ	±13	±14	±15	dB
Adjacent Attenuation Steps		T _{STEP}		1	2	3	dB
SPEAKER ATTENUATORS							
Control Range		G _s		35	37.5	40	dB
Adjacent Attenuation Steps		S _{STEP}		0.5	1.25	1.75	dB
Attenuation Set Error		E _A				1.5	dB
Output Mute Attenuation		A _{UMUTE}		80	100		dB
DC Shift Voltage Steps		V _{DC}	adjacent attenuation steps		0	3	mV
			from 0 to mute		1	10	mV
OUTPUTS							
Clipping Level		V _{OCL}	d=0.3%	2	2.5		Vrms
Output Load Resistance		R _L		2			KΩ
Output Load Capacitance		C _L				10	nF
Output Resistance		R _{OUT}		30	75	120	Ω
Output DC Voltage		V _{OUT}		4.2	4.5	4.8	V
EFFECT OF AUDIO PROCESSING							
Output Noise		e _{N(OUT)}	BW=20-20kHz, flat output muted all gains=0dB		2.5		μV
					5	15	μV
			BW=20-20kHz , a curve all gains=0dB		3		μV
Signal to Noise Ratio		S/N	all gains=0dB; V _{OUT} =1Vrms		106		dB
Distortion		d	Au=0, V _{IN} =1Vrms		0.01	0.1	%
			Au=-20dB	V _{IN} =1Vrms	0.09		%
				V _{IN} =0.3Vrms	0.04		%
Channel Separation(left/right)		S(channel)		80	103		dB
Total Tracking Error		Au(error)	Au=0 to -20dB		0	1	dB
			Au=-20dB to -60dB		0	2	dB
I ² C BUS INPUT							
Input Voltage		Low	V _{IL}			1	V
		High	V _{IH}		3		V
Input Current		I _{IN}		-5		+5	μA
Output Voltage SDA Acknowledge		V _{OUT}	I _{OUT} =1.6mA			0.4	V

The schematic diagram shows the U7313 audio codec chip connected to an MCU. The chip has two input sections (Left and Right) and two output sections (Left and Right). The MCU is connected to the SCL, SDA, and DIGGND pins. The chip is powered by VDD and GND. Various capacitors (c1-c19) and resistors (R1, R2) are shown with their values.

Left input: Pins 15 (L1), 14 (L2), and 13 (L3) are connected to 2.2uF capacitors (c1+, c2+, c3+). Pins 11 (R1), 10 (R2), and 9 (R3) are connected to 2.2uF capacitors (c4+, c5+, c6+).

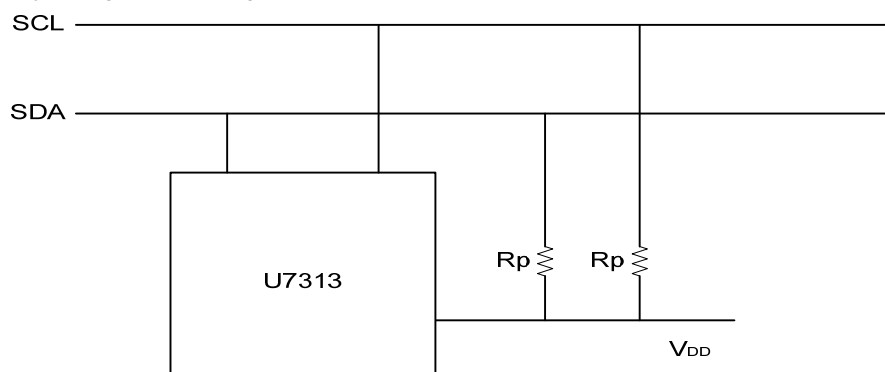
Right input: Pins 25 (OUTLF), 23 (OUTLR), 24 (OUTRF), and 22 (OUTRR) are connected to 10uF capacitors (c18, c19, c20, c21).

MCU connections: SCL (pin 28), SDA (pin 27), and DIGGND (pin 26) are connected to the MCU. The MCU is also connected to the OUTR (pin 7), INR (pin 6), LOUDR (pin 8), BOUTr (pin 21), BINR (pin 20), and R (pin 5) pins.

Power and Ground: VDD (pin 2) and GND (pin 3) are connected to the chip. A 22uF capacitor (c7) is connected between GND and CREF (pin 1). A 2.2uF capacitor (c8) is connected between OUTL (pin 17) and INL (pin 16). A 100nF capacitor (c10) is connected between LOUDL (pin 12) and 100nF (pin 19). A 5.6K resistor (R1) is connected between 100nF (pin 19) and BINL (pin 18). A 2.7nF capacitor (c16) is connected between BINL (pin 18) and L (pin 4). A 2.2uF capacitor (c9) is connected between OUTR (pin 7) and INR (pin 6). A 100nF capacitor (c11) is connected between LOUDR (pin 8) and 100nF (pin 21). A 5.6K resistor (R2) is connected between 100nF (pin 21) and BINR (pin 20). A 2.7nF capacitor (c17) is connected between BINR (pin 20) and R (pin 5).

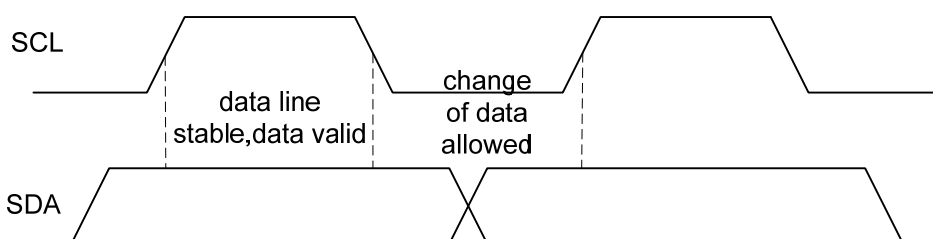
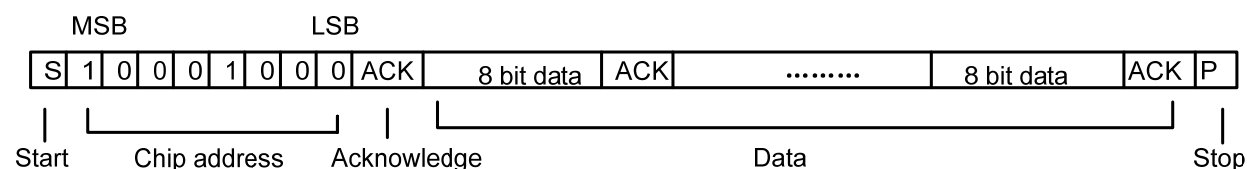
■ I²C BUS INTERFACE

The master communicated with U7313 by two lines SDA and SCL which should connect pull-up resistors to positive supply voltage. See the figure below.

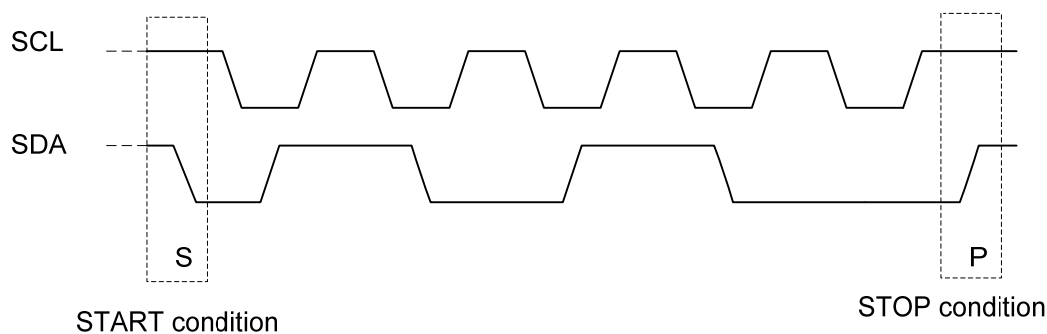


■ BYTE FORMAT

The byte transferred from SDA line should contain 8 bit binary data, and followed an acknowledge bit. The MSB is transferred first, Maximum clock speed is 100Kbit/s. Detail see the figures below.



Note: When SCL is high level, SDA data should be stable;
SDA data can be change only when the SCL is low.

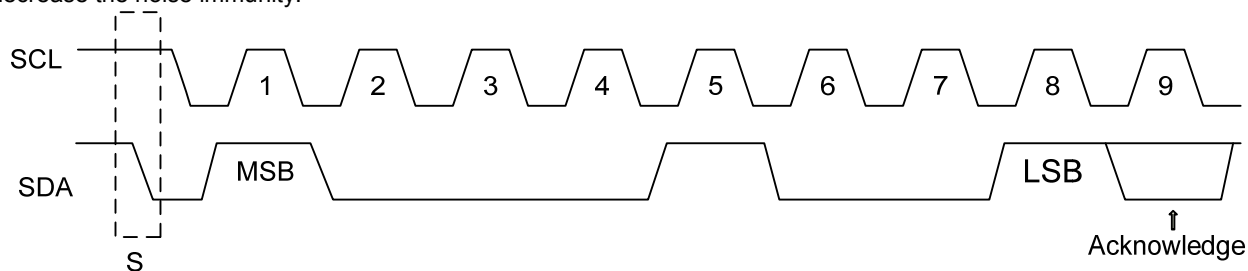


Note: When SCL is high, SDA is high to low, start to receive data.
When SCL is high, SDA is low to high, stop receiving data.

■ ACKNOWLEDGE

The master puts a resistive high level on the SDA line during the acknowledge clock pulse. The slave which acknowledge pull down the SDA line during the acknowledge clock pulse. The SDA line keep in a stable low state. The slave which has been addressed has to generate an acknowledge after receiving each byte. If the SDA line still at the high level during the ninth clock pulse time, the master can generate the stop information to abort the transfer.

If want to abort the acknowledge information, the master can stop detecting the acknowledge by waits one clock without checking, then sends the new data. This approach of course is less protected from misoperation and decrease the noise immunity.



■ FUNCTION CONTROL

Chip address

MSB					LSB		
1	0	0	0	1	0	0	0

Quick reference

MSB					LSB			FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
0	1	0	G1	G0	S2	S1	S0	Gain & Input Selector
0	1	1	0	C3	C2	C1	C0	Bass Control
0	1	1	1	C3	C2	C1	C0	Treble Control

Gain & input selector

MSB				LSB					FUNCTION
0	1	0		G1	G0	S2	S1	S0	Audio Switch
							0	0	Stereo 1
							0	1	Stereo 2
							1	0	Stereo 3
							1	1	Stereo4(nonuse)
						0			LOUDNESS ON
						1			LOUDNESS OFF
				0	0				+11.25dB
				0	1				+7.5dB
				1	0				+3.75dB
				1	1				0dB

For example:

Input: stereo 3 Gain: +3.75dB Loudness on

The 8 bit string is: 0 1 0 1 0 0 1 0

■ FUNCTION CONTROL(Cont.)

Volume control

MSB				LSB			FUNCTION(dB)	
0	0	B2	B1	B0	A2	A1		A0
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

For example: Volume -32.5dB the 8 bit string is: 0 0 0 1 1 0 1 0

Bass control

0	1	1	0	C3	C2	C1	C0	FUNCTION(dB)
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

For example: Bass control -4dB the 8 bit string is: 0 1 1 0 0 1 0 1

■ FUNCTION CONTROL(Cont.)

Treble control

0	1	1	1	C3	C2	C1	C0	FUNCTION (dB)
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

For example: Treble control -4dB the 8 bit string is: 0 1 1 1 0 1 0 1

Speaker attenuators

MSB			LSB			FUNCTION (dB)		
1	0	0	B1	B0	A2	A1	A0	SPEAKER LF
1	0	1	B1	B0	A2	A1	A0	SPEAKER RF
1	1	0	B1	B0	A2	A1	A0	SPEAKER LR
1	1	1	B1	B0	A2	A1	A0	SPEAKER RR
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

For example: Output SPEAKER RF -15dB

The 8 bit string is: 1 0 1 0 1 1 0 0

■ TYPICAL CHARACTERISTICS

Figure 1: Volume+Loudness attenuation vs. Frequency vs. Volume control (C10,C11=100nF)

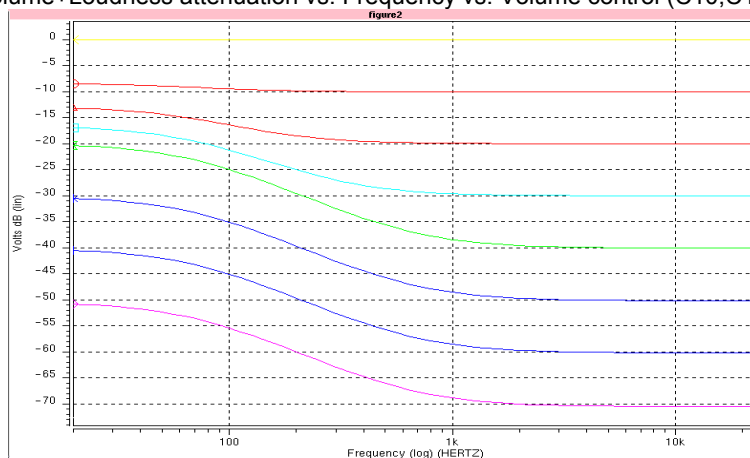


Figure 2: Volume+Loudness attenuation vs. Frequency vs. External Capacitor (Volume=-40dB)

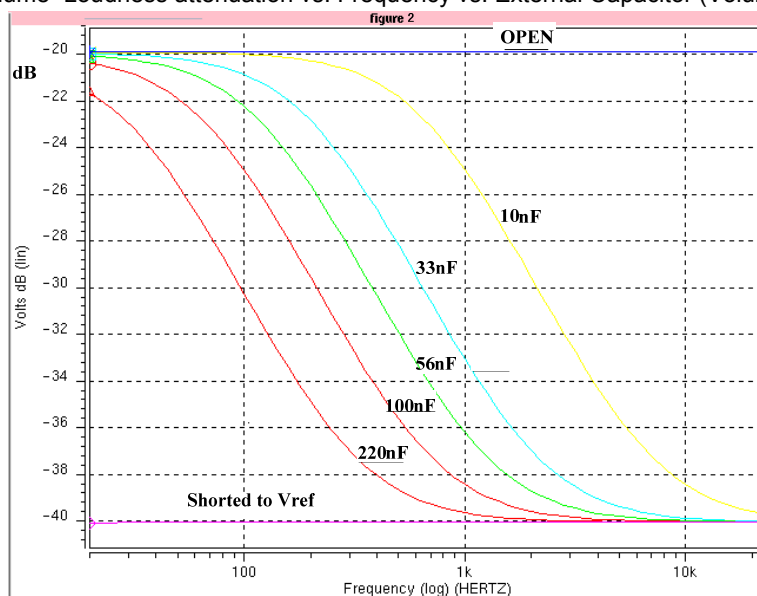
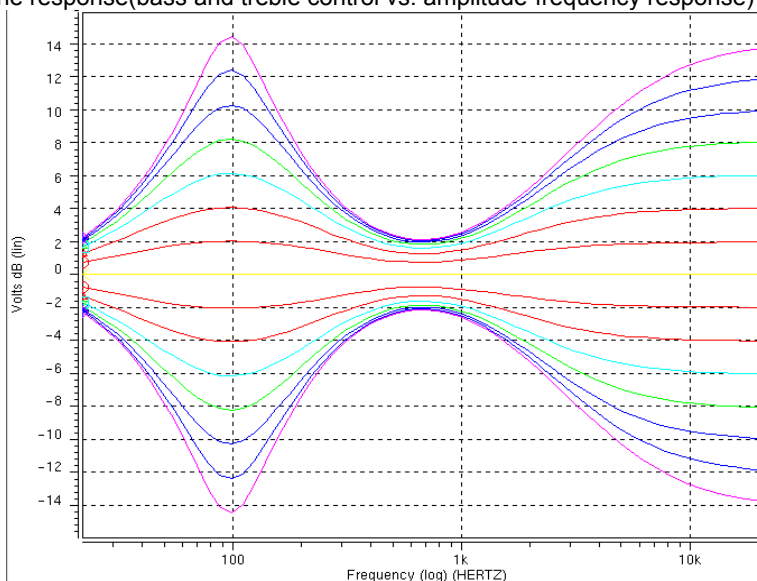


Figure 3: Tone response(bass and treble control vs. amplitude-frequency response)



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