Features

- **Supply Voltage 5V**
- **Very Low Power Consumption 125 mW**
- **Very Good Image Rejection By Means of Phase Control Loop for Precise 90° Phase Shifting**
- **Duty-cycle Regeneration for Single-ended LO Input Signal**
- **Low LO Input Level –10 dBm**
- **LO Frequency from 70 MHz to 1 GHz**
- **Power-down Mode**
- **25 dB Gain Control**
- **Very Low I/Q Output DC Offset Voltage Typically < 5 mV**

Benefits

- **Low Current Consumption**
- **Easy to Implement**
- **Perfect Performance for Large Variety of Wireless Applications**

Electrostatic sensitive device.
Observe precautions for handling.

1000-MHz Quadrature Demodulator

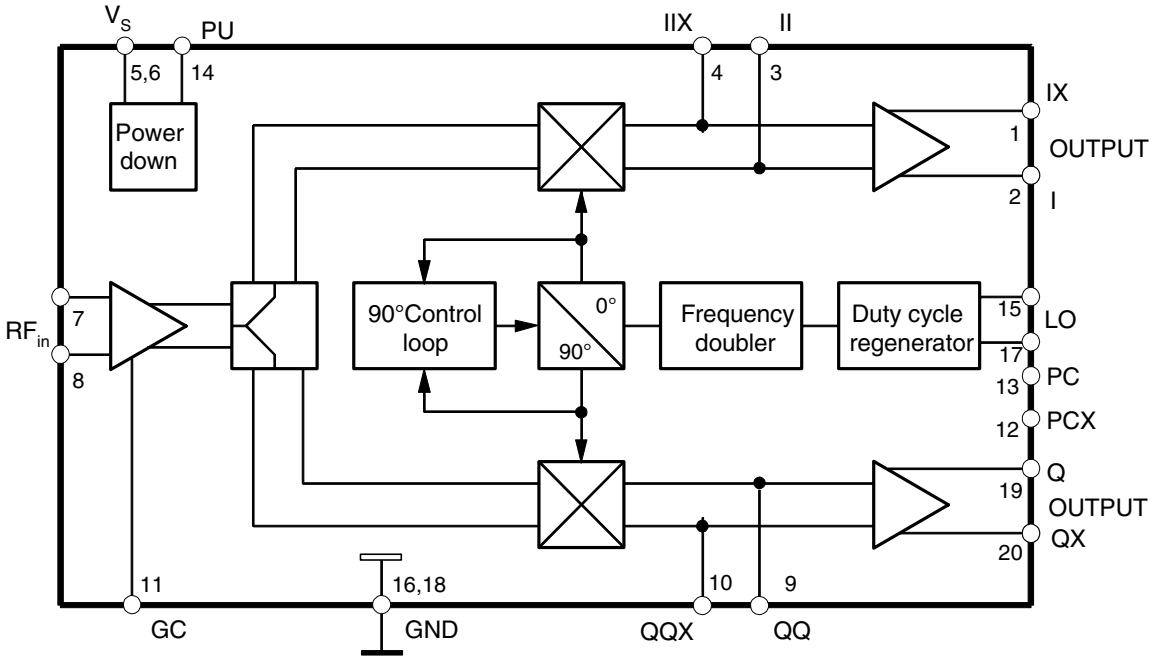
U2794B

1. Description

The silicon monolithic integrated circuit U2794B is a quadrature demodulator manufactured using Atmel's advanced UHF technology. This demodulator features a frequency range from 70 MHz to 1000 MHz, low current consumption, selectable gain, power-down mode and adjustment-free handling. The IC is suitable for direct conversion and image rejection applications in digital radio systems up to 1 GHz such as cellular radios, cordless telephones, cable TV and satellite TV systems.

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Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SSO20

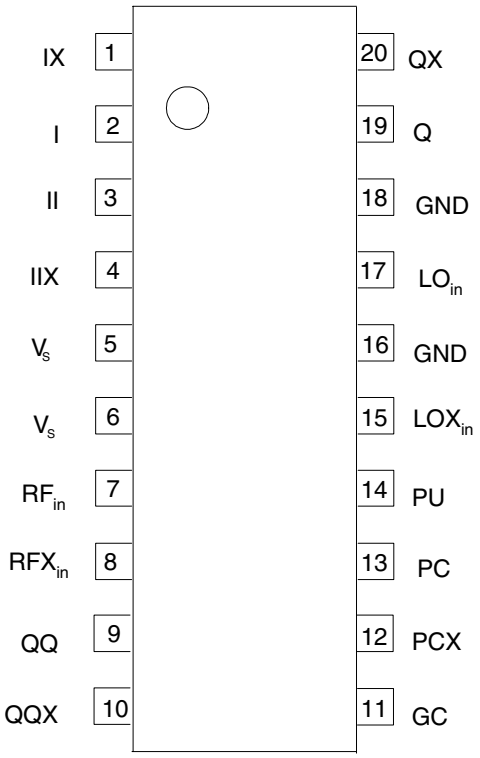


Table 2-1. Pin Description

Pin	Symbol	Function
1	IX	IX output
2	I	I output
3	II	II lowpass filter I
4	IIX	IIX lowpass filter I
5	V_S	Supply voltage
6	V_S	Supply voltage
7	RF_{in}	RF input
8	RFX_{in}	RFX input
9	QQ	QQ lowpass filter Q
10	QQX	QQX lowpass filter Q
11	GC	GC gain control
12	PCX	PCX phase control
13	PC	PC phase control
14	PU	PU power up
15	LOX_{in}	LOX input
16	GND	Ground
17	LO_{in}	LO input
18	GND	Ground
19	Q	Q output
20	QX	QX output

3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage	V_S	6	V
Input voltage	V_i	0 to V_S	V
Junction temperature	T_j	+125	°C
Storage-temperature range	T_{stg}	–40 to +125	°C

4. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO20	R_{thJA}	140	K/W

5. Operating Range

Parameters	Symbol	Value	Unit
Supply-voltage range	V_S	4.75 to 5.25	V
Ambient-temperature range	T_{amb}	–40 to +85	°C

6. Electrical Characteristics

Test conditions (unless otherwise specified); V_S = 5V, T_{amb} = 25°C, referred to test circuit
System impedance Z_O = 50Ω, f_{iLO} = 950 MHz, P_{iLO} = –10 dBm

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	Supply-voltage range		5, 6	V_S	4.75		5.25	V	A
1.2	Supply current		5, 6	I_S	22	30	35	mA	A
2	**Power-down Mode**								
2.1	"OFF" mode supply current	$V_{PU} \leq$ 0.5V V_{PU} = 1.0 V(1)	14, 5 6	I_{SPU}		≤ 1 20		µA µA	B D
3	**Switch Voltage**								
3.1	"Power ON"		14	V_{PON}	4			V	D
3.2	"Power DOWN"		14	V_{POFF}			1	V	D
4	**LO Input, LO_{in}**								
4.1	Frequency range		17	f_{iLO}	70		1000	MHz	D
4.2	Input level	(2)	17	P_{iLO}	–12	–10	–5	dBm	D
4.3	Input impedance	See Figure 6-10	17	Z_{iLO}		50		Ω	D
4.4	Voltage standing wave ratio	See Figure 6-3	17	$VSWR_{LO}$		1.2	2		D
4.5	Duty-cycle range		17	DCR_{LO}	0.4		0.6		D
5	**RF Input, RF_{in}**								
5.1	Noise figure (DSB) symmetrical output	at 950 MHz(3) at 100 MHz	7, 8	NF		12 10		dB	D
5.2	Frequency range	$f_{iRF} = f_{iLO} \pm BW_{YQ}$	7, 8	f_{iRF}	40		1030	MHz	D
5.3	–1 dB input compression point	High gain Low gain	7, 8	P_{1dBHG} P_{1dBLG}		–8 +3.5		dBm	D
5.4	Second order IIP	(4)	7, 8	IIP_{2HG}		35		dBm	D
5.5	Third order IIP	High gain Low gain	7, 8	IIP_{3HG} IIP_{3LG}		+3 +13		dBm	D
5.6	LO leakage	Symmetric input Asymmetric input	7, 8	L_{OL}		≤ –60 ≤ –55		dBm	D
5.7	Input impedance	see Figure 6-10	7, 8	Z_{iRF}		500Ω||0.8		Ω||pF	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. During power-down status a load circuitry with DC-isolation to GND is assumed, otherwise a current of I ≈ (VS –0.8V)/RI has to be added to the above power-down current for each output I, IX, Q, QX.
2. The required LO-Level is a function of the LO frequency (see Figure 6-6).
3. Measured with input matching. For 950 MHz, the optional transmission line T3 at the RF input may be used for this purpose. Noise figure measurements without using the differential output signal result in a worse noise figure.
4. Using pins 7 and 8 as a symmetric RF input, the second-order IIP can be improved.
5. Due to test board parasitics, this bandwidth may be reduced and not be equal for I, IX, Q, QX. If symmetry and full bandwidth is required, the lowpass pins 3, 4 and 9, 10 should be isolated from the board. the bandwidth of the I/Q outputs can be increased further by using a resistor between pins 3, 4, 9 and 10. These resistors shunt the internal loads of RI ~ 5.4 kΩ. The decrease in gain here has to be considered.
6. The internal current of the output emitter followers is 0.6 mA. This reduces the undistorted output voltage swing at a 50Ω load to approximately 30 mV. For low signal distortion the load impedance should be RI ≥ 5 kΩ
7. Referred to the level of the output vector $\sqrt{I^2 + Q^2}$
8. The low-gain status is achieved with an open or high-ohmic pin 11. A recommended application circuit for switching between high and low gain status is shown in Figure 6-1.

6. Electrical Characteristics (Continued)

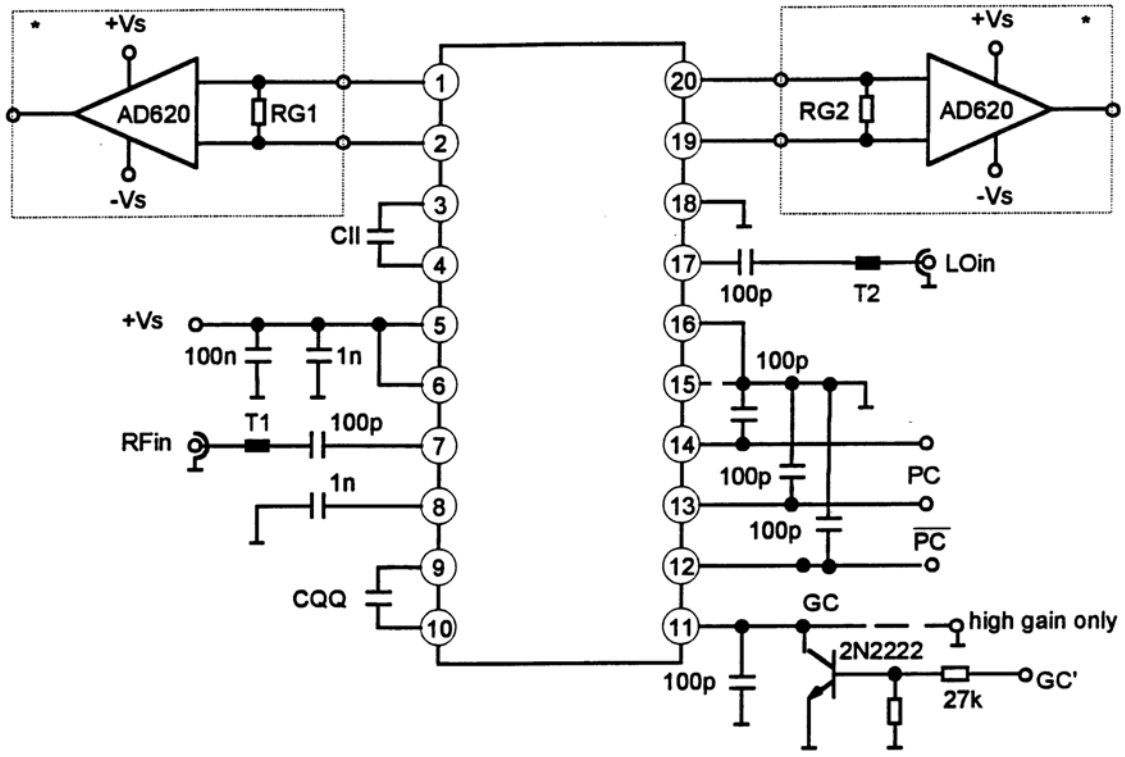
Test conditions (unless otherwise specified); V_S = 5V, T_{amb} = 25°C, referred to test circuit
System impedance Z_O = 50Ω, f_{iLO} = 950 MHz, P_{iLO} = –10 dBm

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6	**I/Q Outputs (I, IX, Q, QX) Emitter Follower I = 0.6 mA**								
6.1	3-dB bandwidth w/o external C		1, 2, 19, 20	BWI/Q	≥ 30			MHz	D
6.2	I/Q amplitude error		1, 2, 19, 20	Ae	–0.5	≤ ±0.2	+0.5	dB	B
6.3	I/Q phase error		1, 2, 19, 20	Pe	–3	≤ ±1.5	+3	Deg	B
6.4	I/Q maximum output swing	Symm. output R_L > 5 kΩ	1, 2, 19, 20	V_{PP}			2		D
6.5	DC output voltage		1, 2, 19, 20	V_{OUT}	2.5	2.8	3.1	V	A
6.6	DC output offset voltage	(6)	1, 2, 19, 20	V_{offset}		< 5		mV	Test spec.
6.7	Output impedance	see Figure 6-10	1, 2, 19, 20	Z_{out}		50		Ω	D
7	**Gain Control, GC**								
7.1	Control range power Gain high Gain low	(7)	11	GCR G_H G_L		25 23 –2		dB dBm dBm	D B D
7.2	**Switch Voltage**								
7.3	“Gain high”		11				1	V	
7.4	“Gain low”	(8)	11 < open						
7.5	**Settling Time, ST**								
7.6	Power “OFF” - “ON”			T_{SON}		< 4		µs	D
7.7	Power “ON” - “OFF”			T_{SOFF}		< 4		µs	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. During power-down status a load circuitry with DC-isolation to GND is assumed, otherwise a current of I ≈ (VS –0.8V)/RI has to be added to the above power-down current for each output I, IX, Q, QX.
2. The required LO-Level is a function of the LO frequency (see Figure 6-6).
3. Measured with input matching. For 950 MHz, the optional transmission line T3 at the RF input may be used for this purpose. Noise figure measurements without using the differential output signal result in a worse noise figure.
4. Using pins 7 and 8 as a symmetric RF input, the second-order IIP can be improved.
5. Due to test board parasitics, this bandwidth may be reduced and not be equal for I, IX, Q, QX. If symmetry and full bandwidth is required, the lowpass pins 3, 4 and 9, 10 should be isolated from the board. the bandwidth of the I/Q outputs can be increased further by using a resistor between pins 3, 4, 9 and 10. These resistors shunt the internal loads of RI ~ 5.4 kΩ The decrease in gain here has to be considered.
6. The internal current of the output emitter followers is 0.6 mA. This reduces the undistorted output voltage swing at a 50Ω load to approximately 30 mV. For low signal distortion the load impedance should be RI ≥ 5 kΩ
7. Referred to the level of the output vector $\sqrt{I^2 + Q^2}$
8. The low-gain status is achieved with an open or high-ohmic pin 11. A recommended application circuit for switching between high and low gain status is shown in Figure 6-1.

Figure 6-1. Test Circuit



* optional for single-ended tests (notice 3 dB bandwidth of AD620)
T1, T2 = transmission line $Z_O = 50\Omega$
If no GC function is required, connect Pin 11 to GND.
For high and low gain status GC´ is to be switched to GND respectively to V_S.

Figure 6-2. I and Q phase for $f_{RF} > f_{LO}$. For $f_{RF} < f_{LO}$ the phase is inverted.

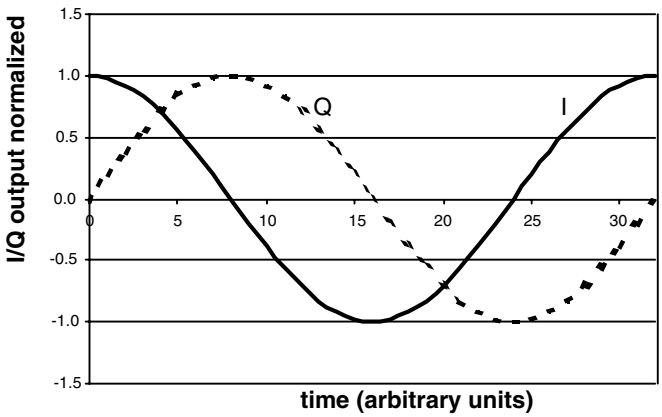


Figure 6-3. Typical VSWR Frequency Response of the LO Input

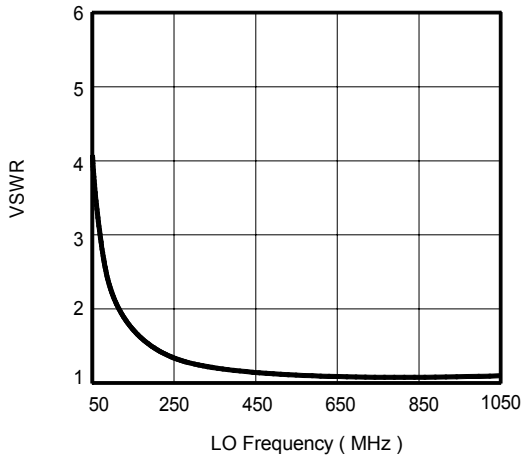


Figure 6-4. Noise Figure versus LO Frequency; o: Value at 950 MHz with RF Input Matching with T3

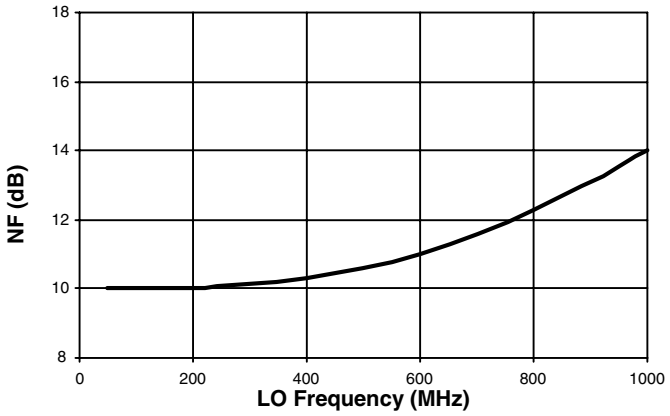


Figure 6-5. Typical Suitable LO Power Range versus Frequency

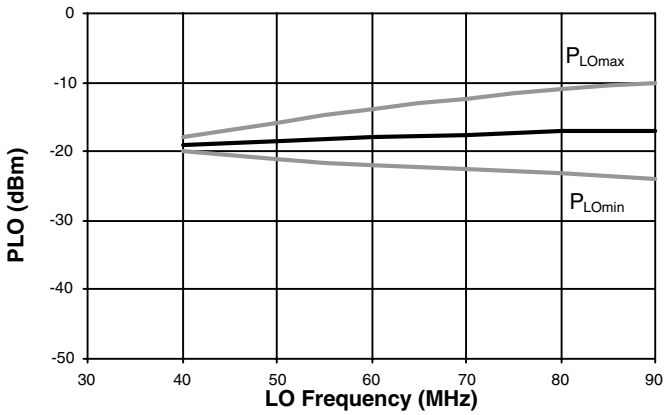


Figure 6-6. Gain versus LO Frequency; x: Value at 950 MHz with RF Input Matching with T3

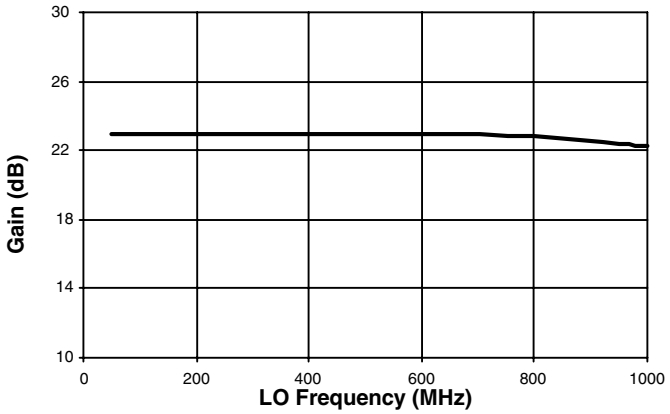


Figure 6-7. Typical Output Signal versus LO Frequency for P_{RF} = –15 dBm and PLO = –15 dBm

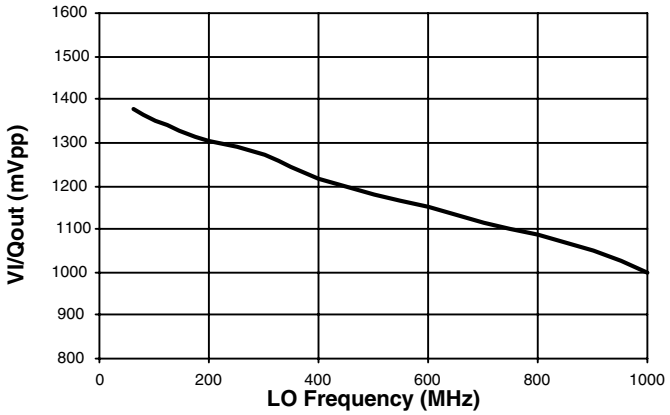


Figure 6-8. Typical Suitable LO Power Range versus Frequency

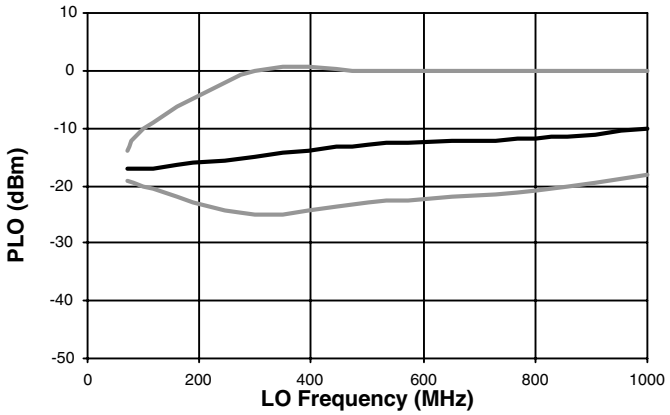


Figure 6-9. Typical Output Voltage (single ended) versus P_{RF} at T_{amb} = 25°C and PLO = –15 dBm

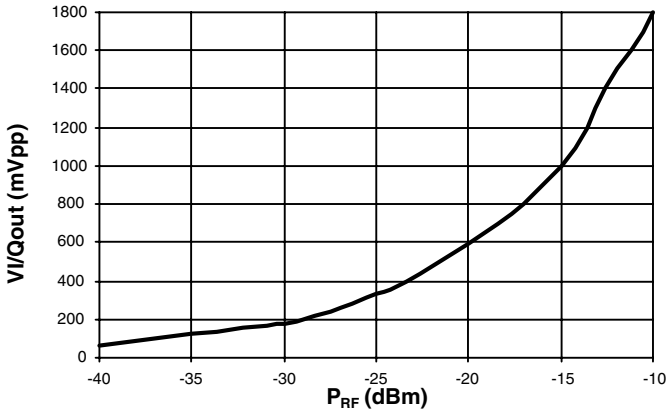
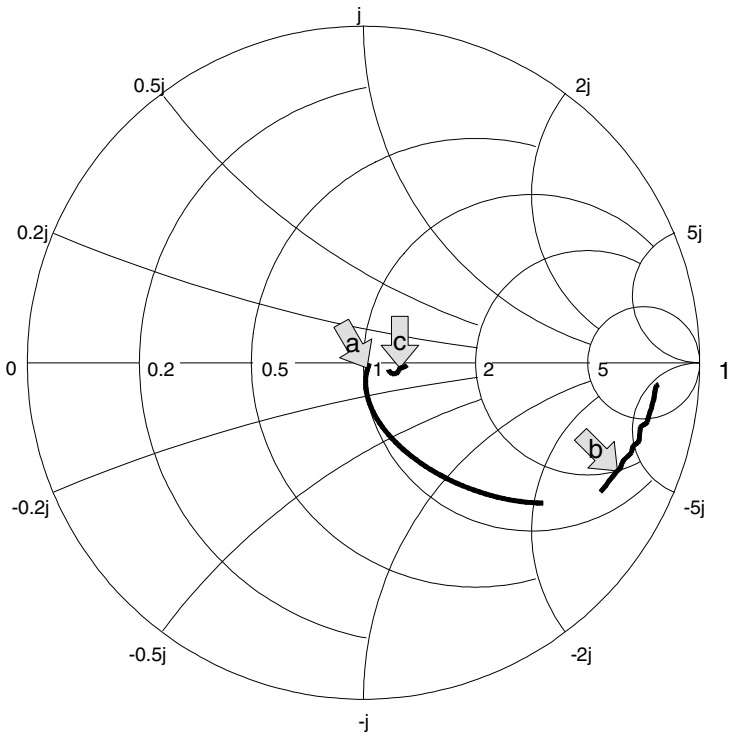


Figure 6-10. Typical S11 Frequency Response



a: LO input, LO frequency from 100 MHz to 1100 MHz, marker: 950 MHz
b: RF input, RF frequency from 100 MHz to 1100 MHz, marker: 950 MHz
c: I/Q Outputs, Baseband Frequency from 5 MHz to 55 MHz, marker: 25 MHz

Figure 6-11. Evaluation Board Layout

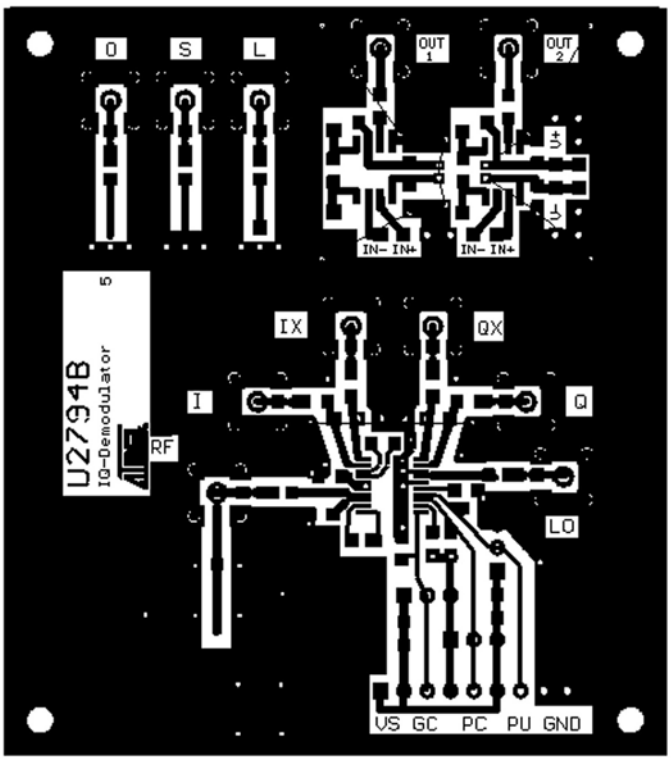
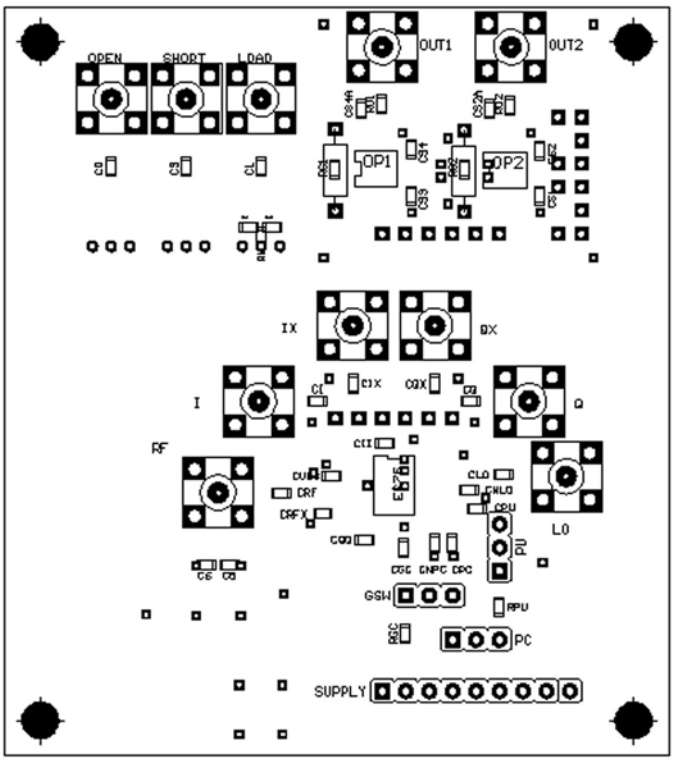


Figure 6-12. Evaluation Board



6.1 External Components

CUCC	100 nF	
CRFX	1 nF	
CLO	100 pF	
CNLO	1 nF	
CRF	100 pF	
CII, CQQ		optional external lowpass filters
T3		transmission line for RF-input matching, to connect optionally
CI, CIX		optional for AC-coupling at
CQ, CQX		baseband outputs
CPDN	100 pF	not connected
CGC	100 pF	
CPC	100 pF	not connected
CNPC	100 pF	not connected
GSW		gain switch

6.2 Calibration Part

CO, CS, CL	100 pF
RL	50Ω

6.3 Conversion to Single Ended Output

(see datasheet of AD620)

OP1, OP2		AD620
RG1, RG2		prog. gain, see datasheet, for 5.6 kΩ a gain of 1 at 50Ω is achieved together with RD1 and RD2.
RD1, RD2	450Ω	
CS1, CS2	100 nF	
CS3, CS4	100 nF	

7. Description of the Evaluation Board

Board material: epoxy; $\varepsilon r = 4.8$, thickness = 0.5 mm, transmission lines: $Z_O = 50\Omega$

The board offers the following functions:

- Test circuit for the U2794B:
  - The supply voltage and the control inputs GC, PC and PU are connected via a plug strip. The control input voltages can be generated via external potentiometers; then the inputs should be AC-grounded (time requirements in burst mode for power up have to be considered).
  - The outputs I, IX, Q, QX are DC coupled via an plug strip or can be AC-connected via SMB plugs for high frequency tests e.g. noise figure or s-parameter measurement. The Pins II, IIX, QQ, QQX allow user-definable filtering with 2 external capacitors CII, CQQ.
  - The offsets of both channels can be adjusted with two potentiometers or resistors.
  - The LO- and the RF-inputs are AC-coupled and connected via SMB plugs. If transmission line T3 is connected to the RF-input and AC-grounded at the other end, gain and noise performance can be improved (input matching to 50Ω).
  - The complementary RF-input is AC-coupled to GND (CRFX = 1 nF), the same appears to the complementary LO input (CNLO = 1 nF).
- A calibration part which allows to calibrate an s-parameter analyzer directly to the in- and output- signal ports of the U2794B.
- For single-ended measurements at the demodulator outputs, two OPs (e.g., AD620 or other) can be configured with programmable gain; together with an output-divider network RD = 450Ω to RL = 50Ω, direct measurements with 50Ω load impedances are possible at frequencies t < 100 kHz.

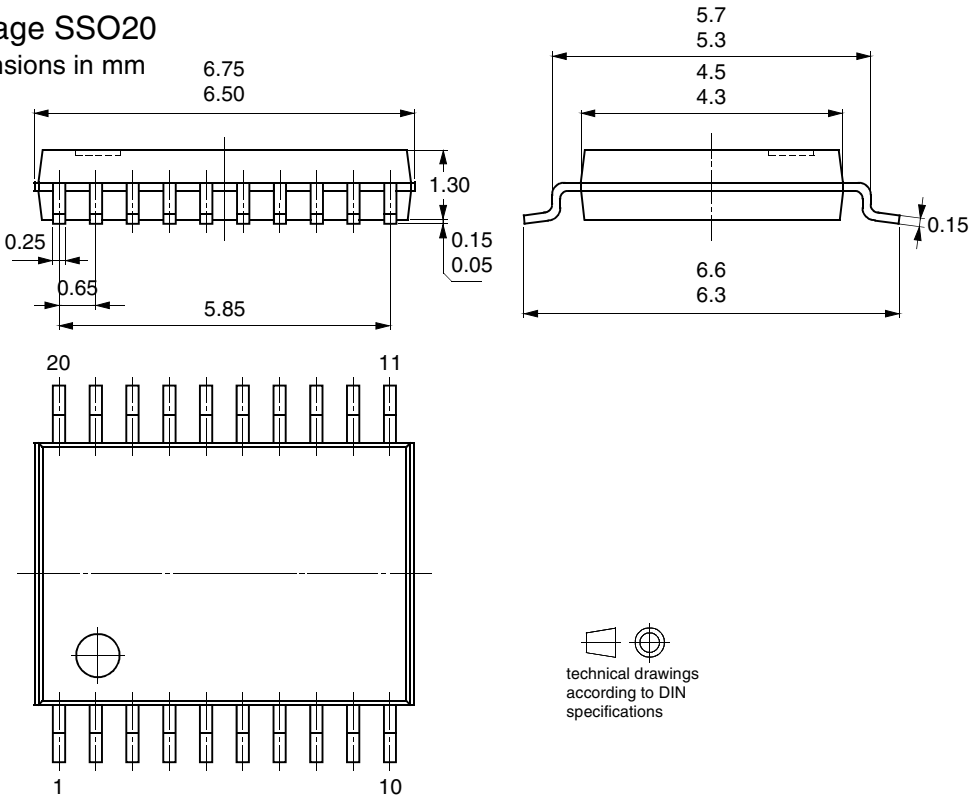
8. Ordering Information

Extended Type Number	Package	Remarks
U2794B-NFSH	SSO20	Tube, MOQ 830 pcs, Pb-free
U2794B-NFSG3H	SSO20	Taped and reeled, MOQ 4000 pcs, Pb-free

9. Package Information

Package SSO20

Dimensions in mm



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