

Microsemi®
SoC Products Group

Terrestrial FPGA and SoC Product Catalog

October 2011

Power Matters.



Microsemi®
SoC Products Group

The leader in customizable System-on-Chip devices and FPGAs for sense and control applications where **reliability**, **security**, and **power** matter.

Now, more than ever, **power matters.**

Whether you're designing at the board or system level, **Microsemi's customizable System-on-Chip (cSoC) devices and low power FPGAs are your best choice.** The unique, flash-based technology of Microsemi FPGAs, coupled with their history of reliability, sets them apart from traditional FPGAs.

Design for today's rapidly growing markets of consumer and portable medical devices, or tomorrow's environmentally friendly data centers, industrial controls and military and commercial aircraft. Only Microsemi can meet the power, size, cost and reliability targets that reduce time-to-market and enable long-term profitability.

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Please refer to www.microsemi.com/soc and appropriate product datasheets for the latest device information, valid ordering codes and more information regarding previous generations of flash and antifuse FPGAs.

SmartFusion

SmartFusion

The customizable system-on-chip (cSoC) device

SmartFusion cSoCs are the only devices that integrate FPGA fabric, an ARM® Cortex™-M3 processor and programmable analog, offering full customization, IP protection and ease-of-use. Based on Microsemi's proprietary flash process, SmartFusion cSoCs are ideal for hardware and embedded designers who need a true system-on-chip that gives more flexibility than traditional fixed-function microcontrollers without the excessive cost of soft processor cores on traditional FPGAs.

- **Available in commercial, industrial and military* grades**
- **Hard 100 MHz 32-bit ARM Cortex-M3 CPU**
- **Multi-layer AHB communications matrix with up to 16 Gbps throughput**
- **10/100 Ethernet MAC**
- **Two peripherals of each type: SPI, I2C, UART, and 32-bit timers**
- **Up to 512 KB flash and 64 KB SRAM**
- **External memory controller (EMC)**
- **8-channel DMA controller**
- **Integrated analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) with 1 percent accuracy**
- **On-chip voltage, current and temperature monitors**
- **Up to ten 15 ns high-speed comparators**
- **Analog compute engine (ACE) offloads CPU from analog processing**
- **Up to 35 analog I/Os and 169 digital GPIOs**

** Under development*

SmartFusion Devices

SmartFusion Devices		A2F060	A2F200	A2F500
FPGA Fabric	System Gates	60,000	200,000	500,000
	Tiles (D-flip-flops)	1,536	4,608	11,520
	RAM Blocks (4,608 bits)	8	8	24
Microcontroller Subsystem (MSS)	Flash (Kbytes)	128	256	512
	SRAM (Kbytes)	16	64	64
	Cortex-M3 with Memory Protection Unit (MPU)	Yes	Yes	Yes
	10/100 Ethernet MAC	No	Yes	Yes
	External Memory Controller (EMC)	24-bit address, 16-bit data	24-bit address, 16-bit data	24-bit address, 16-bit data[1]
	DMA	8 Ch	8 Ch	8 Ch
	I2C	2	2	2
	SPI	2	2	2
	16550 UART	2	2	2
	32-Bit Timer	2	2	2
	PLL	1	1	2[2]
	32 KHz Low Power Oscillator	1	1	1
	100 MHz On-Chip RC Oscillator	1	1	1
	Main Oscillator (32 KHz to 20 MHz)	1	1	1
Programmable Analog	ADCs (8-/10-/12-bit SAR)	1	2	3[4]
	DACs (12-bit sigma-delta)	1	2	3[4]
	Signal Conditioning Blocks (SCBs)	1	4	5[4]
	Comparators[3]	2	8	10[4]
	Current Monitors[3]	1	4	5[4]
	Temperature Monitors[3]	1	4	5[4]
	Bipolar High Voltage Monitors[3]	2	8	10[4]

Notes:

1. *Not available on A2F500 for the PQ208 package.*
2. *Two PLLs are available in CS288 and FG484 (one PLL in FG256 and PQ208).*
3. *These functions share I/O pins and may not all be available at the same time.*
4. *Available on FG484 only. PQ208, FG256, and CS288 packages offer the same programmable analog capabilities as A2F200.*

Package I/Os: MSS + FPGA I/Os

Device	A2F060			A2F200				A2F500			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Direct Analog Input	11	11	11	8	8	8	8	8	8	8	12
Shared Analog Input[1]	4	4	4	16	16	16	16	16	16	16	20
Total Analog Input	15	15	15	24	24	24	24	24	24	24	32
Total Analog Output	1	1	1	1	2	2	2	1	2	2	3
MSS I/Os[2,3]	21[4]	28[4]	26[4]	22	31	25	41	22	31	25	41
FPGA I/Os	33	68	66	66	78	66	94	66[5]	78	66	128
Total I/Os	70	112	108	113	135	117	161	113	135	117	204

Notes:

1. *These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.*
2. *16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for the MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.*
3. *9 MSS I/Os are primarily for 10/00 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.*
4. *10/100 Ethernet MAC is not available on A2F060.*
5. *EMC is not available on the A2F500 PQ208 package.*

Fusion

The world's first mixed signal FPGA

Fusion FPGAs integrate configurable analog, large flash memory blocks, comprehensive clock generation and management circuitry and high-performance, flash-based programmable logic in a monolithic device. The Fusion architecture can be used with soft microcontroller cores, such as the performance-optimized ARM Cortex-M1, 8051s or Microsemi's own CoreABC, the smallest soft microcontroller for FPGAs.

- Integrated A/D converter (ADC) with 8-, 10- and 12-bit resolution and 30 scalable analog input channels
- ADC accuracy better than 1 percent
- On-chip voltage, current and temperature monitors
- In-system configurable analog supports a wide variety of applications
- Up to 1 MB of user flash memory
- Extensive clocking resources
- Analog PLLs
- 1 percent RC oscillator
- Crystal oscillator circuit
- Real-time counter (RTC)
- Flash FPGA fabric
- Reprogrammable
- Live at power-up
- Maximum design security
- Ultra-low power
- Configuration memory error immune
- Clock management
- Advanced I/O standards
- User nonvolatile FlashROM

Fusion Devices

Fusion Devices		AFS090	AFS250	AFS600	AFS1500
Cortex-M1 Devices[1]			M1AFS250	M1AFS600	M1AFS1500
Pigeon Point Devices				P1AFS600[2]	P1AFS1500[2]
MicroBlade Devices				U1AFS600[3]	
General Information	System Gates	90,000	250,000	600,000	1,500,000
	Tiles (D–flip–flops)	2,304	6,144	13,824	38,400
	AES-protected ISP	Yes	Yes	Yes	Yes
	PLLs	1	1	2	2
	Globals	18	18	18	18
Memory	Flash Memory Blocks (2 Mbits)	1	1	2	4
	Total Flash Memory Bits	2 M	2 M	4 M	8 M
	FlashROM Bits	1,024	1,024	1,024	1,024
	RAM Blocks (4,608 bits)	6	8	24	60
	RAM (Kbits)	27	36	108	270
Analog and I/Os	Analog Quads	5	6	10	10
	Analog Input Channels	15	18	30	30
	Gate Driver Outputs	5	6	10	10
	I/O Banks (+ JTAG)	4	4	5	5
	Maximum Digital I/Os	75	114	172	252
	Analog I/Os	20	24	40	40

Notes:
1. *Refer to the Cortex-M1 product brief for more information.*
2. *Pigeon Point devices only offered in FG484 and FG256 packages.*
3. *MicroBlade devices only offered in FG256 package.*

Package I/Os: Single-/Double-Ended (Analog)

Fusion Mixed Signal FPGAs	AFS090	AFS250	AFS600	AFS1500
Cortex-M1 Devices		M1AFS250	M1AFS600	M1AFS1500
Pigeon Point Devices			P1AFS600[1]	P1AFS1500[1]
MicroBlade Devices			U1AFS600[2]	
QN108[3]	37/9 (16)	—	—	—
QN180[3]	60/16 (20)	65/15 (24)	—	—
PQ208[4]	—	93/26 (24)	95/46 (40)	—
FG256[5]	75/22 (20)	114/37 (24)	119/58 (40)	119/58 (40)
FG484[5]	—	—	172/86 (40)	223/109 (40)
FG676[5]	—	—	—	252/126 (40)

Notes:
1. *Pigeon Point devices only offered in FG484 and FG256 packages.*
2. *MicroBlade devices only offered in FG256 package.*
3. *These packages are available only as RoHS-compliant (QNG package specifier).*
4. *AFS250 and AFS600 PQ208 devices are not pin-compatible.*
5. *Available in RoHS-compliant and standard leaded packages.*

Extended Temperature Fusion

Mixed signal integration at extended temperatures

Microsemi Fusion mixed signal FPGAs integrate configurable analog, large flash memory blocks, comprehensive clock generation and management circuitry and high-performance, flash-based reprogrammable logic in a monolithic device. Innovative Fusion architecture can be used with Microsemi's soft microcontroller (MCU) core as well as the performance-maximized 32-bit ARM Cortex-M1 cores. Extended temperature Fusion devices operate at temperatures from 100ºC to as low as -55ºC.

Extended Temperature Fusion Devices

Extended Temperature Fusion Devices	AFS600	AFS1500
Cortex-M1 Devices	M1AFS600	M1AFS1500
System Gates	600,000	1,500,000
Tiles (D–flip–flops)	13,824	38,400
AES-Protected ISP	Yes	Yes
PLLs	2	2
Globals	18	18
Flash Memory Blocks (2 Mbits)	2	4
Total Flash Memory Bits	4 M	8 M
FlashROM Bits	1,024	1,024
RAM Blocks (4,608 bits)	24	60
RAM (kbits)	108	270
Analog Quads	10	10
Analog Input Channels	30	30
Gate Driver Outputs	10	10
I/O Banks (+ JTAG)	5	5
Maximum Digital I/Os	172	223
Analog I/Os	40	40
Package Pins FG	FG256, FG484	FG256, FG484

IGLOO/e

The ultra low power programmable solution

The IGLOO family of reprogrammable, full-featured flash FPGAs is designed to meet the demanding power, area and cost requirements of today's portable electronics. Based on nonvolatile flash technology, the 1.2 V to 1.5 V operating voltage family offers the industry's lowest power consumption—as low as 5 µW. The IGLOO family supports up to 3,000,000 system gates with up to 504 Kbits of true dual-port SRAM, up to 6 embedded PLLs and up to 620 user I/Os. Low power applications that require 32-bit processing can use the ARM Cortex-M1 processor without license fee or royalties in M1 IGLOO devices. Developed specifically for implementation in FPGAs, Cortex-M1 offers an optimal balance between performance and size to minimize power consumption.

- Ultra low power FPGAs
- Flash*Freeze technology for lowest power consumption
- 1.2 V core and I/O voltage
- 5 µW Flash*Freeze mode
- Reprogrammable
- Live at power-up
- AES-protected in-system programming (ISP)
- User nonvolatile FlashROM

IGLOO/e Devices

IGLOO Devices	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	AGLE600	AGLE3000
Cortex-M1 Devices[1]				M1AGL250		M1AGL600	M1AGL1000		M1AGLE3000
System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	3,000,000
Typical Equivalent Macrocells	256	512	1,024	2,048	—	—	—	—	—
VersaTiles (D-flip-flops)	768	1,536	3,072	6,144	9,216	13,824	24,576	13,824	75,264
Flash*Freeze Mode (typical, µW)	5	10	16	24	32	36	53	49	137
RAM (1,024 bits)	—	18	36	36	54	108	144	108	504
RAM Blocks (4,608 bits)	—	4	8	8	12	24	32	24	112
FlashROM Kbits (1,024 bits)	1	1	1	1	1	1	1	1	1
AES-Protected ISP[1]	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLLs with CCC[2]	—	1	1	1	1	1	1	6	6
VersaNet Globals[3]	6	18	18	18	18	18	18	18	18
I/O Banks	2	2	2	4	4	4	4	8	8
Maximum User I/Os (packaged device)	81	96	133	143	194	235	300	270	620
Package Pins									
UC	UC81								
CS	CS81	CS121	CS81 CS196	CS81 CS196[4]	CS196	CS281	CS281		
QN	QN48 QN68 QN132	QN132	QN132	QN132[4]					
VQ	VQ100	VQ100	VQ100	VQ100					
FG		FG144[5]	FG144	FG144	FG144 FG256 FG484	FG144 FG256 FG484	FG144 FG256 FG484	FG256 FG484	FG484 FG896

Notes:
1. *AES is not available for Cortex-M1 IGLOO devices.*
2. *AGL060 in CS121 does not support the PLL.*
3. *Six chip (main) and twelve quadrant global networks are available for AGL060 devices and above.*
4. *The M1AGL250 device does not support this package.*

I/Os Per Package

IGLOO Devices	AGL030	AGL060	AGL125	AGL250		AGL400		AGL600		AGL1000		AGLE600		AGLE3000	
Cortex-M1 Devices				M1AGL250[1]				M1AGL600		M1AGL1000				M1AGLE3000	
I/O Type	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs
QN48	34	—	—	—	—	—	—	—	—	—	—	—	—	—	—
QN68	49	—	—	—	—	—	—	—	—	—	—	—	—	—	—
UC81	66	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CS81	66	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CS121	—	96	—	—	—	—	—	—	—	—	—	—	—	—	—
VQ100	77	71	71	68	13	—	—	—	—	—	—	—	—	—	—
QN132	81	80	84	87	19	—	—	—	—	—	—	—	—	—	—
CS196	—	—	133	143	35	143	35	—	—	—	—	—	—	—	—
FG144	—	96	97	97	24	97	25	97	25	97	25	—	—	—	—
FG256	—	—	—	—	—	178	38	177	43	177	44	165	79	—	—
CS281	—	—	—	—	—	—	—	215	53	215	53	—	—	—	—
FG484	—	—	—			194	38	235	60	300	74	270	135	341	168
FG896	—	—	—	—	—	—	—	—	—	—	—	—	—	620	310

Notes:
1. *The M1AGL250 device does not support QN132 or CS196 packages.*
2. *Each used differential pair reduces the number of single-ended I/Os available by two.*

IGLOO nano

The industry's lowest power, smallest-size solution

IGLOO nano products offer groundbreaking possibilities in power, size, lead-times, operating temperature and cost. Available in logic densities from 10,000 to 250,000 gates, the 1.2 V to 1.5 V IGLOO nano devices have been designed for high-volume applications where power and size are key decision criteria. IGLOO nano devices are perfect ASIC or ASSP replacements, yet retain the historical FPGA advantages of flexibility and quick time-to-market in low power and small footprint profiles.

- **Ultra low power in Flash*Freeze mode, as low as 2 µW**
- **Variety of small footprint packages as small as 3x3 mm**
- **Zero lead-time on selected devices**
- **Known good die supported**
- **Enhanced commercial temperature**
- **Reprogrammable flash technology**
- **1.2 V to 1.5 V single voltage operation**
- **Enhanced I/O features**
- **Clock conditioning circuits (CCCs) and PLLs**
- **Embedded SRAM and nonvolatile memory (NVM)**
- **ISP and security**

IGLOO nano Devices

IGLOO nano Devices	AGLN010	AGLN020	AGLN060	AGLN125	AGLN250
System Gates	10,000	20,000	60,000	125,000	250,000
Typical Equivalent Macrocells	86	172	512	1,024	2,048
VersaTiles (D-flip-flops)	260	520	1,536	3,072	6,144
Flash*Freeze Mode (typical, µW)	2	4	10	16	24
RAM Kbits[1] (1,024 bits)	—	—	18	36	36
4,608-Bit Blocks[1]	—	—	4	8	8
FlashROM Kbits (1,024 bits)	1	1	1	1	1
AES-Protected ISP[1]	—	—	Yes	Yes	Yes
Integrated PLL in CCCs[1,2]	—	—	1	1	1
VersaNet Globals	4	4	18	18	18
I/O Banks	2	3	2	2	4
Maximum User I/Os (packaged device)	34	52	71	71	68
Known Good Die User I/Os	34	52	71	71	68
Package Pins UC CS QN VQ	UC36 QN48	UC81 CS81 QN68	 CS81 VQ100	 CS81 VQ100	 CS81 VQ100

Notes:

1. *AGLN030 and smaller devices do not support this feature.*
2. *AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs.*
3. *For higher densities and support of additional features, refer to the IGLOO and IGLOOe datasheets and FPGA fabric user's guides.*

I/Os Per Package

IGLOO nano Devices	AGLN010	AGLN020	AGLN060	AGLN125	AGLN250
Known Good Die	34	52	71	71	68
UC36	23	—	—	—	—
QN48	34	—	—	—	—
QN68	—	49	—	—	—
UC81	—	52	—	—	—
CS81	—	52	60	60	60
VQ100	—	—	71	71	68

Note:

** When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

IGLOO PLUS

The low power FPGA with enhanced I/O capabilities

IGLOO PLUS products deliver unrivaled low power and I/O features in a feature-rich programmable device, offering up to 64 percent more I/Os than the award-winning IGLOO products and supporting independent Schmitt trigger inputs, hot-swapping and Flash*Freeze bus hold. Ranging from 30,000 to 125,000 gates, the 1.2 V to 1.5 V IGLOO PLUS devices have been optimized to meet the needs of I/O-intensive, power-conscious applications that require exceptional features.

- I/O-optimized FPGA
- Ultra low power in Flash*Freeze mode, as low as 5 µW
- Low power active capability
- Small footprint and low-cost packages
- Reprogrammable flash technology
- 1.2 V to 1.5 V single voltage operation
- Enhanced I/O features
- CCCs and PLLs
- Embedded SRAM NVM
- AES-protected ISP

IGLOO PLUS Devices

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
System Gates	30,000	60,000	125,000
Typical Equivalent Macrocells	256	512	1,024
VersaTiles (D-flip-flops)	792	1,584	3,120
Flash*Freeze Mode (typical, µW)	5	10	16
RAM (1,024 bits)	—	18	36
4,608-Bit Blocks	—	4	8
FlashROM Kbits (1,024 bits)	1	1	1
AES-Protected ISP	—	Yes	Yes
Integrated PLL in CCCs[1]	—	1	1
VersaNet Globals[2]	6	18	18
I/O Banks	4	4	4
Maximum User I/Os (packaged device)	120	157	212
Package Pins CS VQ	 CS201, CS289 VQ128	 CS201, CS289 VQ176	 CS281, CS289

Notes:
1. *AGLP060 in CS201 does not support the PLL.*
2. *Six chip (main) and twelve quadrant global networks are available for AGLP060 and AGLP125.*

I/Os Per Package

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
I/O Type	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O
CS201	120	157	—
CS281	—	—	212
CS289	120	157	212
VQ128	101	—	—
VQ176	—	137	—

Note:
** When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

ProASIC3/E

ProASIC3

The low power, low-cost FPGA solution

The ProASIC3 series of flash FPGAs offers a breakthrough in power, price, performance, density and features for today's most demanding high-volume applications. ProASIC3 devices support the ARM Cortex-M1 processor, offering the benefits of programmability and time-to-market at low cost. ProASIC3 devices are based on nonvolatile flash technology and support 30,000 to 3,000,000 gates and up to 620 high-performance I/Os. For automotive applications, selected ProASIC3 devices are qualified to the AEC-Q100 and are available with AEC T1 screening and PPAP documentation.

- Low power
- Single chip, single voltage
- Nonvolatile, reprogrammable
- Low cost
- Live at power-up
- Maximum design security
- Configuration memory error immune
- Clock management
- Advanced I/O standards
- User nonvolatile FlashROM
- Secure ISP
- High performance

ProASIC3/E Devices

ProASIC3/E Devices	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000	A3PE600	A3PE1500	A3PE3000
Cortex-M1 Devices				M1A3P250	M1A3P400	M1A3P600	M1A3P1000		M1A3PE1500	M1A3PE3000
System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	1,500,000	3,000,000
Typical Equivalent Macrocells	256	512	1,024	2,048	—	—	—	—	—	—
VersaTiles (D-flip-flops)	768	1,536	3,072	6,144	9,216	13,824	24,576	13,824	38,400	75,264
RAM (1,024 bits)	—	18	36	36	54	108	144	108	270	504
4,608-Bit Blocks	—	4	8	8	12	24	32	24	60	112
FlashROM Kbits (1,024 bits)	1	1	1	1	1	1	1	1	1	1
AES-Protected ISP[1]	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	—	1	1	1	1	1	1	6	6	6
VersaNet Globals	6	18	18	18	18	18	18	18	18	18
I/O Banks	2	2	2	4	4	4	4	8	8	8
Maximum User I/Os (packaged device)	81	96	133	157	194	235	300	270	444	620
Package Pins										
QFN	QN48 QN68 QN132	QN132	QN132[2]	QN132[2, 3]						
CS		CS121								
VQ	VQ100	VQ100[2]	VQ100[2]	VQ100[2]						
TQ		TQ144	TQ144							
PQ			PQ208	PQ208	PQ208	PQ208	PQ208	PQ208	PQ208	PQ208
FG		FG144[2]	FG144[2]	FG144[2] FG256[2, 3]	FG144 FG256 FG484	FG144 FG256 FG484	FG144[2] FG256[2] FG484[2]	FG256 FG484	FG484 FG676	FG324 FG484 FG896

Notes:

1. *AES is not available for Cortex-M1 ProASIC3 devices.*
2. *Available as automotive "T" grade*
3. *The M1A3P250 device does not support this package.*

I/Os Per Package

ProASIC3 Devices	A3P030	A3P060	A3P125	A3P250		A3P400		A3P600		A3P1000		A3PE600		A3PE1500		A3PE3000	
Cortex-M1 Devices				M1A3P250*		M1A3P400		M1A3P600		M1A3P1000				M1A3PE1500		M1A3PE3000	
I/O Type	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs
QN48	34	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
QN68	49	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
QN132	81	80	84	87	19	—	—	—	—	—	—	—	—	—	—	—	—
CS121	—	96	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VQ100	77	71	71	68	13	—	—	—	—	—	—	—	—	—	—	—	—
TQ144	—	91	100	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PQ208	—	—	133	151	34	151	34	154	35	154	35	147	65	147	65	147	65
FG144	—	96	97	97	24	97	25	97	25	97	25	—	—	—	—	—	—
FG256	—	—	—	157	38	178	38	177	43	177	44	165	79	—	—	—	—
FG324	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	221	110
FG484	—	—	—	—	—	194	38	235	60	300	74	270	135	280	139	341	168
FG676	—	—	—	—	—	—	—	—	—	—	—	—	—	444	222	—	—
FG896	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	620	310

Note:

** M1A3P250 does not support the FG256 and QN132 packages.*

ProASIC3 nano

The lowest-cost solution with enhanced I/O capabilities

Microsemi's innovative ProASIC3 nano devices bring a new level of value and flexibility to high-volume markets. When measured against the typical project metrics of performance, cost, flexibility and time-to-market, ProASIC3 nano devices provide an attractive alternative to ASICs and ASSPs in fast moving or highly competitive markets. Customer-driven total system cost reduction was a key design criterium for the ProASIC3 nano program. Reduced device cost, availability of known good die, a single-chip implementation and a broad selection of small footprint packages all contribute to lower total system costs.

- 1.5 V core for low power
- Known good die supported
- 350 MHz system performance
- Embedded SRAM NVM
- Configuration memory error immune
- Enhanced commercial temperature
- Enhanced I/O features
- ISP and security
- Reprogrammable flash technology
- Zero lead-time on selected devices
- CCCs and PLLs

ProASIC3 nano Devices

ProASIC3 nano Devices	A3PN010	A3PN020	A3PN060	A3PN125	A3PN250
System Gates	10,000	20,000	60,000	125,000	250,000
Typical Equivalent Macrocells	86	172	512	1,024	2,048
VersaTiles (D-flip-flops)	260	520	1,536	3,072	6,144
RAM[1] (1,024 bits)	–	–	18	36	36
4,608-Bit Blocks[1]	–	–	4	8	8
FlashROM Kbits (1,024 bits)	1	1	1	1	1
AES-Protected ISP[1]	–	–	Yes	Yes	Yes
Integrated PLL in CCCs[1]	–	–	1	1	1
VersaNet Globals	4	4	18	18	18
I/O Banks	2	3	2	2	4
Maximum User I/Os (packaged device)	34	49	71	71	68
Known Good Die User I/Os	34	52	71	71	68
Package Pin QN VQ	QN48	QN68	VQ100	VQ100	VQ100

Notes:

1. A3PN030 and smaller devices do not support this feature.

2. For higher densities and support of additional features, refer to the ProASIC3 and ProASIC3E datasheets and FPGA fabric user's guides.

I/Os Per Package

ProASIC3 nano Devices	A3PN010	A3PN020	A3PN060	A3PN125	A3PN250
Known Good Die	34	52	71	71	68
QN48	34	–	–	–	–
QN68	–	49	–	–	–
VQ100	–	–	71	71	68

ProASIC3L

Balancing low power, performance and low cost

ProASIC3L FPGAs feature 40 percent lower dynamic power and 90 percent lower static power than the previous generation ProASIC3 FPGAs and orders of magnitude lower power than SRAM competitors, combining dramatically reduced power consumption with up to 350 MHz operation. The ProASIC3L family also supports the free implementation of an FPGA-optimized 32-bit ARM Cortex-M1 processor, enabling system designers to select Microsemi's flash FPGA solution that best meets their speed and power design requirements, regardless of application or volume. Optimized software tools using power-driven layout (PDL) provide instant power reduction capabilities.

- Low power 1.2 V to 1.5 V core operation
- 700 Mbps DDR, LVDS capable I/Os
- Up to 350 MHz system performance
- Enhanced I/O features
- Embedded SRAM and NVM
- Configuration memory error immune
- ISP and security
- Flash*Freeze technology for lowest power
- Reprogrammable flash technology
- CCCs and PLLs

ProASIC3L Low Power Devices

ProASIC3L Devices	A3P250L	A3P600L	A3P1000L	A3PE3000L
Cortex-M1 Devices		M1A3P600L	M1A3P1000L	M1A3PE3000L
System Gates	250,000	600,000	1,000,000	3,000,000
VersaTiles (D-flip-flops)	6,144	13,824	24,576	75,264
RAM (1,024 bits)	36	108	144	504
4,608-Bit Blocks	8	24	32	112
FlashROM Kbits (1,024 bits)	1	1	1	1
AES-Protected ISP[1]	Yes	Yes	Yes	Yes
Integrated PLL in CCCs[2]	1	1	1	6
VersaNet Globals	18	18	18	18
I/O Banks	4	4	4	8
Maximum User I/Os (packaged device	157	235	300	620
Package Pins VQ PQ FG	 VQ100 PQ208 FG144, FG256	 PQ208 FG144, FG256, FG484	 PQ208 FG144, FG256, FG484	 PQ208 FG324, FG484, FG896

Notes:

1 AES is not available for Cortex-M1 ProASIC3L devices.

2 For the A3PE3000L, the PQ208 package has six CCCs and two PLLs.

I/Os Per Package

ProASIC3L Devices	A3P250L		A3P600L		A3P1000L		A3PE3000L	
Cortex-M1 Devices			M1A3P600L		M1A3P1000L		M1A3PE3000L	
I/O Type	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs
VQ100	68	13	–	–	–	–	–	–
PQ208	151	34	154	35	154	35	147	65
FG144	97	24	97	25	97	25	–	–
FG256	157	38	177	43	177	44	–	–
FG324	–	–	–	–	–	–	221	110
FG484	–	–	235	60	300	74	341	168
FG896	–	–	–	–	–	–	620	310

Military ProASIC3/EL

Low power FPGAs for military applications

Building on the successful heritage of the Military ProASIC^{PLUS} family, Military ProASIC3 FPGAs offer higher performance, greater density and more memory, while at the same time offering high reliability combined with compact single-chip logic integration, live at power-up operation and reprogrammability. Military ProASIC3/EL FPGAs have demonstrated immunity to configuration upsets caused by atmospheric neutrons.

- Supports single-voltage system operation
- 3,000,000 system gates
- Up to 504 Kbits of true dual-port SRAM
- Live-at-power-up level 0 support
- ISP protected using on-chip 128-bit advanced encryption
- Standard (AES) decryption via JTAG (IEEE 1532–compliant)

Military ProASIC3 Devices

Military ProASIC3 Devices	A3P250	A3PE600L	A3P1000	A3PE3000L
Cortex-M1 Devices[1]			M1A3P1000	M1A3PE3000L
System Gates	250,000	600,000	1,000,000	3,000,000
VersaTiles (D-flip-flops)	6,144	13,824	24,576	75,264
RAM (1,024 bits)	36	108	144	504
4,608-Bit Blocks	8	24	32	112
FlashROM (Kbits)	1	1	1	1
AES-Protected ISP[2]	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	1	6	1	6
VersaNet Globals	18	18	18	18
I/O Banks	4	8	4	8
Maximum User I/Os	68	270	154	620
Package Pins VQ PQ FG	100	 484	 208 144	 484, 896

Notes:

1. Refer to the ARM Cortex-M1 product brief for more information.

2. AES is not available for ARM-enabled ProASIC3/EL devices.

Military ProASIC^{PLUS}

Reprogrammable, nonvolatile military FPGAs

Military ProASIC^{PLUS} is the industry's first nonvolatile, reprogrammable FPGA with testing covering the full military temperature range (–55ºC to 125ºC), with available MIL-STD-883 Class B screening. The flash-based reprogrammable interconnect used in Microsemi's ProASIC^{PLUS} FPGAs has been proven to be immune to configuration changes caused by atmospheric neutrons, which plague SRAM-based FPGAs in high-reliability applications.

Military ProASIC^{PLUS} Devices

Military ProASIC^{PLUS} Devices	APA300	APA600	APA1000
Maximum System Gates	300,000	600,000	1,000,000
Tiles (registers)	8,192	21,504	56,320
RAM Kbits (1,024 bits)	72	126	198
RAM Blocks (256x9)	32	56	88
LVPECL	2	2	2
PLL	2	2	2
Global Networks	4	4	4
Maximum Clocks	32	56	88
Maximum User I/Os	290	454	712
JTAG ISP	Yes	Yes	Yes
PCI	Yes	Yes	Yes
Package Pins CQ CG	208, 352	208, 352 624	208, 352 624

I/O Table

SmartFusion					A2F060			A2F200				A2F500					
Fusion						*AFS090*			*AFS250*				*AFS600*			*AFS1500*	
Ext. Temp. Fusion													*AFS600*			*AFS1500*	
IGLOO/e			AGL030	AGL060			AGL125		AGL250		AGL400		AGL600	AGL1000	AGLE600		AGLE3000
IGLOO nano	AGLN010	AGLN020	AGLN030	AGLN060			AGLN125		AGLN250								
IGLOO PLUS			AGLP030	AGLP060			AGLP125										
ProASIC3/E			A3P030	A3P060			A3P125		A3P250		A3P400		A3P600	A3P1000	A3PE600	A3PE1500	A3PE3000
ProASIC3 nano	A3PN010	A3PN020	A3PN030	A3PN060			A3PN125		A3PN250								
ProASIC3L									A3P250L				A3P600L	A3P1000L			A3PE3000L
Military ProASIC3/EL									A3P250					A3P1000	A3PE600L		A3PE3000L
Military ProASIC^{PLUS}										APA300			APA600	APA1000			

Size (mm)	Name	Pitch (mm)															
3x3	UC36	0.40	23														
4x4	UC81	0.40		52	66												
5x5	CS81	0.50		52	66	60		60		60							
6x6	CS121	0.50				96											
6x6	QN48	0.40	34		34												
8x8	CS196	0.50						133		143/35		143/35					
8x8	QN68	0.40		49	49												
8x8	QN132	0.50			81	80		84		87/19							
8x8	CS201	0.50			120	157											
10x10	QN108	0.50					*37/9 (16)*										
10x10	QN180	0.50					*60/16 (20)*			*65/15 (24)*							
10x10	CS281	0.50						212					215/53	215/53			
11x11	CS288	0.50				112			135			135					
13x13	FG144	1.00				96		97		97/24		97/25	97/25	97/25			
14x14	CS289	0.80			120	157		212									
14x14	VQ100	0.50			77	71		71		68/13							
14x14	VQ128	0.40			101												
17x17	FG256	1.00				108	*75/22 (20)*		117	*114/37 (24)* 157/38		178/38	117	*119/58 (40)* 177/43	177/44	165/79	*119/58 (40)*	
19x19	FG324	1.00																221/110
20x20	TQ144	0.50				70 91		100										
20x20	VQ176	0.40				137												
23x23	FG484	1.00							161			194/38	204	*172/86 (40)* 235/60	300/74	270/135	*223/109(40)* 280/139	341/168
27x27	FG676	1.00															*252/126(40)* 444/222	
28x28	PQ208	0.50						133	113	*93/26 (24)* 151/34		151/34	113	*95/46 (40)* 154/35	154/35	147/65	147/65	147/65
31x31	FG896	1.00																620/310
32.5x32.5	CG624	1.27												440	440			
29.21x29.21	CQ208	0.50									158			158	158			
48x48	CQ352	0.50									248			248	248			

Notes: *# / # structure shows single-ended/double-ended I/Os. Fusion and Ext. Temp. Fusion I/O counts are in italics. Value in parentheses for Fusion is analog I/Os. SmartFusion values are total analog, MSS and FPGA I/Os. Please refer to the SoC Products Group's website at www.microsemi.com/soc and appropriate product datasheets for the latest device information and valid ordering codes.*

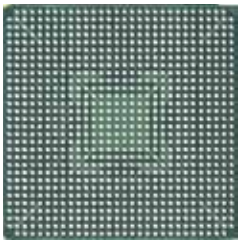
Go to www.microsemi.com/soc for information regarding previous generations of flash and antifuse FPGAs.

FPGA Packages

Key: **f** – family **bs** – package body size excluding leads **ps** – overall package dimensions including package leads **h** – package thickness **p** – pin pitch / ball pitch

FG896

f IGLOOe[1]
ProASIC3E[1]
ProASIC3L[1]
Military ProASIC3/EL[1]
ps 31x31 mm
h 2.23 mm
p 1.00 mm



FG676

f ProASIC3E[1]
Fusion[1]
ps 27x27 mm
h 2.23 mm
p 1.00 mm



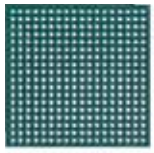
FG484

f SmartFusion
Fusion[1, 3]
IGLOO[1]
IGLOOe[1]
ProASIC3[1, 2]
ProASIC3E[1, 2]
ProASIC3L[1]
Military ProASIC3/EL[1]
ps 23x23 mm
h 2.23 mm
p 1.00 mm



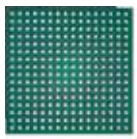
FG324

f ProASIC3E[1]
ProASIC3L[1]
ps 19x19 mm
h 1.63 mm
p 1.00 mm



FG256

f SmartFusion
Fusion[1, 3, 4]
IGLOO[1]
IGLOOe
ProASIC3[1, 2]
ProASIC3E[2]
ProASIC3L[1]
ps 17x17 mm
h 1.60 mm
p 1.00 mm



FG144

f IGLOO[1]
ProASIC3[1]
ProASIC3L[1]
Military ProASIC3/EL[1]
ps 13x13 mm
h 1.45 mm
p 1.00 mm



CS289

f IGLOO PLUS
ps 14x14 mm
h 1.20 mm
p 0.80 mm



CS288

f SmartFusion
ps 11x11 mm
h 1.05 mm
p 0.50 mm



CS281

f IGLOO[1]
IGLOO PLUS
ps 10x10 mm
h 1.05 mm
p 0.50 mm



CS201

f IGLOO PLUS
ps 8x8 mm
h 0.89 mm
p 0.50 mm



CS196

f IGLOO
ps 8x8 mm
h 1.11 mm
p 0.50 mm



CS121

f IGLOO
ProASIC3
ps 6x6 mm
h 0.90 mm
p 0.50 mm



CS81

f IGLOO
IGLOO nano
ps 5x5 mm
h 0.80 mm
p 0.50 mm



UC81

f IGLOO
IGLOO nano
ps 4x4 mm
h 0.80 mm
p 0.40 mm



UC36

f IGLOO nano
ps 3x3 mm
h 0.80 mm
p 0.40 mm



QN180

f Fusion
ps 10x10 mm
h 0.75 mm
p 0.50 mm



QN132

f IGLOO
ProASIC3
ps 8x8 mm
h 0.75 mm
p 0.50 mm



QN108

f Fusion
ps 8x8 mm
h 0.75 mm
p 0.50 mm



QN68

f IGLOO
IGLOO nano
ProASIC3
ProASIC3 nano
ps 8x8 mm
h 0.90 mm
p 0.40 mm



QN48

f IGLOO
IGLOO nano
ProASIC3
ProASIC3 nano
ps 6x6 mm
h 0.90 mm
p 0.40 mm



Notes:

1 Includes Cortex-M1 devices.
2 FG256 and FG484 are footprint-compatible for ProASIC3 and ProASIC3E.
3 Pigeon Point devices are only offered in FG484 and FG256.
4 MicroBlade devices are only offered in FG256.

PQ208

f SmartFusion
Fusion[1]
ProASIC3[1]
ProASIC3E[1]
ProASIC3L[1]
Military ProASIC3/EL[1]
bs 28x28 mm
ps 30.6x30.6 mm
h 3.40 mm
p 0.50 mm



TQ144

f ProASIC3
bs 20x20 mm
ps 22x22 mm
h 1.40 mm
p 0.50 mm



VQ176

f IGLOO PLUS
bs 20x20 mm
ps 22x22 mm
h 1.00 mm
p 0.40 mm



VQ128

f IGLOO PLUS
bs 14x14 mm
ps 16x16 mm
h 1.00 mm
p 0.40 mm



VQ100

f IGLOO[1]
IGLOO nano
ProASIC3[1]
ProASIC3 nano
ProASIC3L
Military ProASIC3/EL[1]
bs 14x14 mm
ps 16x16 mm
h 1.00 mm
p 0.50 mm



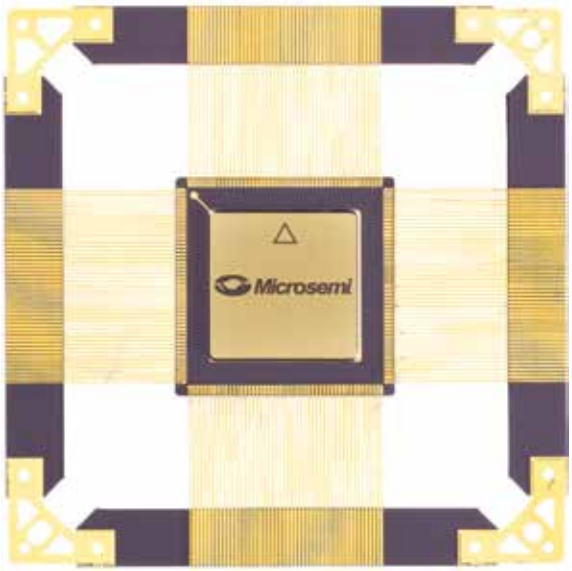
CQ352

f Military ProASIC[PLUS]
ps 48x48 mm
h 2.67 mm
p 0.50 mm



CQ208

f Military ProASIC[PLUS]
ps 29.21x29.21 mm
h 2.67 mm
p 0.50 mm



CG624

f Military ProASIC[PLUS]
ps 32.5x32.5 mm
h 4.94 mm
p 1.27 mm



Refer to the Package Mechanical Drawings document located at www.microsemi.com/soc/documents/PckgMechDrwngs.pdf for more information concerning package dimensions.

Axcelerator

First for speed and performance

The Axcelerator FPGA family is a single-chip, nonvolatile solution offering high performance and unprecedented design security at densities of up to 2 million equivalent system gates. Utilizing the AX architecture, Axcelerator devices have several system-level features, such as embedded SRAM (with embedded FIFO control logic), PLLs, segmentable clocks, chip-wide highway routing, and carry logic. Based upon 0.15 µm, seven-layers-of-metal CMOS antifuse process technology, 350 MHz system performance.

- 500+ MHz internal performance
- 500+ MHz embedded FIFOs
- PLL output up to 1 GHz and 8 PLLs per device
- 6 levels of logic at 156+ MHz
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V mixed-voltage operation
- Bank-selectable I/Os—8 banks per chip
- 8 global clocks per device
- 4.5 kbits variable-aspect RAM blocks with built-in FIFO control
- Secure programming technology is designed to prevent reverse engineering and design theft

Axcelerator Devices

Axcelerator Device	AX125	AX250	AX500	AX1000	AX2000
Capacity (in equivalent system gates)	125,000	250,000	500,000	1,000,000	2,000,000
Typical Gates	82,000	154,000	286,000	612,000	1,060,000
Register (R-cells)	672	1,408	2,688	6,048	10,752
Combinatorial (C-cells)	1,344	2,816	5,376	12,096	21,504
Maximum Flip-Flops	1,344	2,816	5,376	12,096	21,504
Number of Core RAM Blocks	4	12	16	36	64
Total Bits of Core RAM	18,432	55,296	73,728	165,888	294,912
Clocks (hardwired)	4	4	4	4	4
Clocks (routed)	4	4	4	4	4
PLLs	8	8	8	8	8
I/O Banks	8	8	8	8	8
Maximum User I/Os	168	248	336	516	684
Maximum LVDS Channels	84	124	168	258	342
Total I/O Registers	504	744	1,008	1,548	2,052
Speed Grades	Std., –1, –2	Std., –1, –2	Std., –1, –2	Std., –1, –2	Std., –1, –2
Temperature Grades	C, I	C, I, M	C, I, M	C, I, M	C, I, M

I/Os Per Package

Axcelerator Device	AX125	AX250	AX500	AX1000	AX2000
PQ		208	208		
BG				729	
FG	256, 324	256, 484	484, 676	484, 676, 896	896, 1152
CQ		208, 352	208, 352	352	256, 352
CG/LG				624	624

SX-A

Reducing the cost of performance

The SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. SX-A devices can be used to generate system-wide savings by integrating multiple functions into a single-chip solution. Providing a combination of performance, security, and low power, SX-A FPGAs decrease the premium for performance while providing a solution that is highly resistant to reverse engineering.

- 12,000 to 108,000 usable system gates
- 250 MHz system performance
- 350 MHz internal performance
- Hot-swap compliant I/Os
- Power-up and power-down friendly (no sequencing required for supply voltages)
- 66 MHz, 64-bit 3.3 V / 5.0 V PCI performance (supporting target, master and master/target)
- 2.5 V, 3.3 V, and 5.0 V mixed-voltage support
- 100% resource utilization with 100% pin locking

SX-A Devices

SX-A Device	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Typical Gates	8,000	16,000	32,000	72,000
System Gates	12,000	24,000	48,000	108,000
Logic Modules	768	1,452	2,880	6,036
Combinatorial Cells	512	924	1,800	4,024
Dedicated Flip-Flops	256	528	1,080	2,012
Maximum Flip-Flops	512 *	990	1,980	4,024
Maximum User I/Os	130	180	249	360
Global Clocks	3	3	3	3
Quadrant Clocks	0	0	0	4
Boundary Scan Testing	Yes	Yes	Yes	Yes
3.3 V / 5 V PCI	Yes	Yes	Yes	Yes
Input Set-Up (external)	0 ns	0 ns	0 ns	0 ns
Speed Grades	–F, Std., –1, –2	–F, Std., –1, –2	–F, Std., –1, –2	–F, Std., –1, –2
Temperature Grades	C, I, A, M	C, I, A, M	C, I, A, M, B	C, I, A, M, B

I/Os Per Package

SX-A Devices	A54SX08A	A54SX16A	A54SX32A	A54SX72A
PQ	208	208	208	208
VQ				
TQ	100, 144	100, 144	100, 144, 176	
BG			329	
FG	144	144, 256	144, 256, 484	256, 484
CQ			84, 208, 256	208, 256

MX

The price/performance leader at 5.0 V

Featuring very low power consumption and the industry's highest design security, MX FPGAs offer designers a reliable, single-chip ASIC alternative. MX devices provide high performance while shortening the system design and development cycle. Offering an efficient, flexible 5.0 V architecture, MX is an ideal high-volume platform for integrating your legacy PLDs into a single device. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and coprocessor functions.

- Single-chip ASIC alternative
- 3,000 to 54,000 system gates
- Up to 2.5 kbits configurable dual-port SRAM
- Fast wide-decode circuitry
- Up to 202 user-programmable I/O pins
- High performance mixed-voltage solution
- PCI compliant
- Contains embedded dual-port SRAM modules
- QML certification
- Ceramic devices available to DSCC SM

MX Devices

MX Devices	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
System Gates	3,000	6,000	14,000	24,000	36,000	54,000
SRAM Bits	—	—	—	—	—	2,560
Sequential	—	—	348	624	954	1,230
Combinatorial	295	547	336	608	912	1,184
Decode	—	—	—	—	24	24
Clock-to-Out	9.5 ns	9.5 ns	5.6 ns	6.1 ns	6.1 ns	6.3 ns
SRAM Modules (64x4 or 32x8)	—	—	—	—	—	10
Dedicated Flip-Flops	—	—	348	624	954	1,230
Clocks	1	1	2	2	2	6
Maximum Flip-Flops	147	273	516	928	1,410	1,822
User I/Os (maximum)	57	69	104	140	176	202
PCI	—	—	—	—	Yes	Yes
Boundary Scan Test (BST)	—	—	—	—	Yes	Yes
Speed Grades	–F, Std., –1, –2, –3	–F, Std., –1, –2, –3	–F, Std., –1, –2, –3	–F, Std., –1, –2, –3	–F, Std., –1, –2, –3	–F, Std., –1, –2, –3
Temperature Grades	C, I, M, A	C, I, M, A	C, I, M, A	C, I, M, A	C, I, M, A	C, I, M, A, B

I/Os Per Package

MX Devices	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PL	44, 68	44, 68, 84	84	84	84	
PQ	100	100	100, 160	100, 160, 208	160, 208	208, 240
VQ	80	80	100	100		
TQ			176	176	176	
CQ						208, 256
BG						272

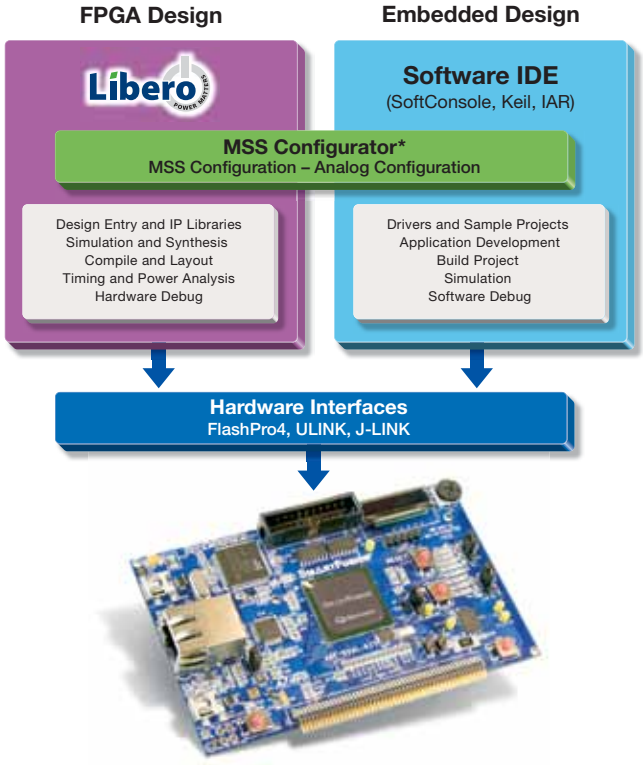
Design Environment for Microsemi Flash Devices

Microsemi's Libero® Integrated Design Environment (IDE) is a comprehensive software toolset for designing with all Microsemi FPGAs. Libero IDE includes industry-leading synthesis, simulation and debug tools from Synopsys® and Mentor Graphics,® as well as innovative timing and power optimization and analysis.

Microsemi's SmartDesign tool simplifies the use of Microsemi IP in user designs as well as offering a simple way to build on-chip processors with custom peripherals. Most Microsemi IP cores are now included by default in Libero IDE as either obfuscated or RTL versions, depending on the license selected.

For embedded designers, Microsemi offers FREE SoftConsole Eclipse-based IDE for use with ARM Cortex-M1, Cortex-M3 and Core8051s, as well as evaluation versions from Keil™ and IAR Systems®. Full versions are available from respective suppliers.

For SmartFusion cSoCs, the MSS configurator creates a bridge between the FPGA fabric and embedded designs, so device configuration can be easily shared among multiple developers. The MSS configurator allows the designer to choose peripherals, assign configuration settings and change I/O attributes. Most importantly, the memory map is automatically generated according to the user's selections, along with all the required firmware for the selected configuration. The memory map and firmware are imported into the software project, whether it is GNU, Keil or IAR.



FPGA Design Support

Libero IDE Licenses		Gold (FREE)	Platinum	Platinum Evaluation	Standalone
Device Support	All families	Up to 1,500,000 gates	All devices	All devices	All devices
Microsemi IP		Obfuscated	RTL	Obfuscated	RTL
Synthesis	Synplify® Pro AE	x	x	x	
Simulation	ModelSim® AE	x	x	x	
Debug	Identify® AE	x	x	x	
	Microsemi Debug	x	x	x	x
Program File		x	x		x

Embedded Design Support

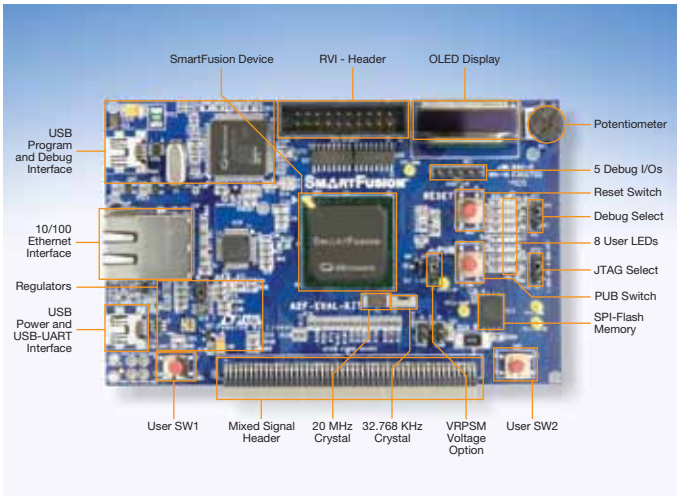
	Microsemi	Keil	IAR Systems
	SoftConsole	**Keil MDK**	**Embedded Workbench®**
Free Versions from Microsemi	Free with Libero IDE	32 K Code Limited	32 K Code Limited
Available from Vendor	N/A	Full version	Full version
Compiler	GNU GCC	RealView® C/C++	IAR ARM Compiler
Debugger	GDB Debug	µVision Debugger	C-SPY® Debugger
Instruction Set Simulator	No	µVision Simulator	Yes
Debug Hardware	FlashPro4	ULink®2 or ULINK-ME	J-Link™ or J-Link Lite

Platform Support

Tool	Libero IDE	SoftConsole	Keil	IAR	FlashPro
Windows® XP Professional	Now	Now	Now	Now	Now
Windows Vista Business and Windows 7	Now	Now	Now	Now	Now
RedHat Linux WS 5.0, 5.2	Now	N/A	N/A	N/A	N/A

** MSS configurator is specific to the SmartFusion design flow.*

SmartFusion Evaluation Kit

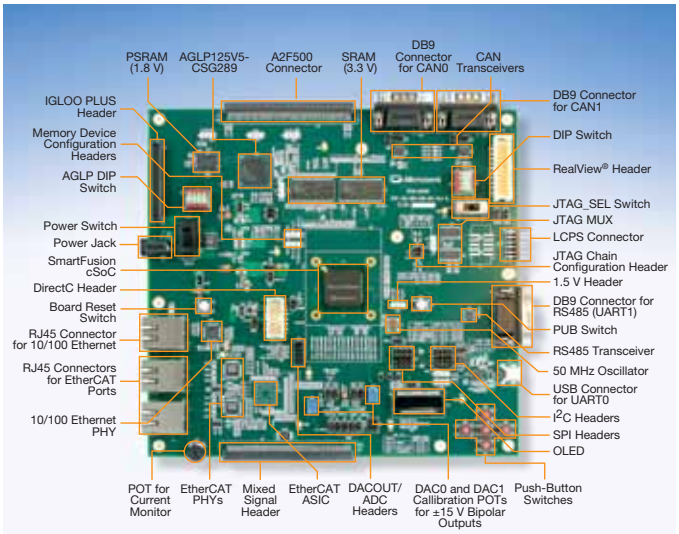


- **Supports SmartFusion cSoC evaluation, including ARM Cortex-M3, FPGA and programmable analog**
- **Free one-year Libero Integrated Design Environment (IDE) software and Gold license with SoftConsole for program and debug**
- **USB programming built into board**
- **Two USB cables**
- **User's guide, tutorial and design examples**
- **Printed circuit board (PCB) schematics, layout files and bill-of-materials (BOM)**

- **Board features**
  - Ethernet interface
  - USB port for power and HyperTerminal
  - USB port for programming and debug
  - J-Link header for debug
  - Mixed signal header
  - SPI flash – off-chip memory
  - Reset and 2 user switches, 8 LEDs
  - POT for voltage / current monitor
  - Temperature monitor
  - Organic light-emitting diode (OLED)

Ordering Code	Supported Device	Price
A2F-EVAL-KIT	A2F200M3F-FGG484	$ 99

SmartFusion Development Kit

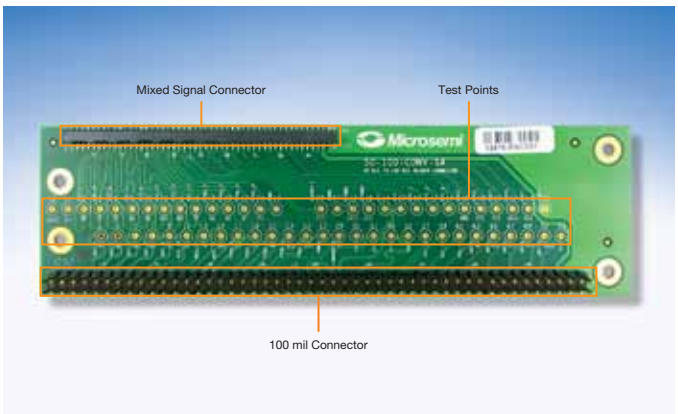


- **Supports SmartFusion development, including ARM Cortex-M3, FPGA and programmable analog**
- **Free one-year Libero IDE software and Gold license with SoftConsole for program and debug**
- **5 V power supply and international adapters**
- **Two USB cables and low cost programming stick**
- **User's guide, tutorial and design examples**
- **PCB schematics, layout files and BOM**

- **Board features**
  - Ethernet, EtherCAT, CAN, UART, I^2C and SPI interfaces
  - USB port for HyperTerminal
  - USB port for programming and debug
  - J-Link header for debug
  - Mixed signal and A2F500 digital expansion header
  - Extensive off-chip memory
  - Refer to www.microsemi.com/soc for a full list of features

Ordering Codes	Supported Devices	Price
A2F500-DEV-KIT	A2F500M3G-FGG484	$ 999

Mixed Signal Daughter Card

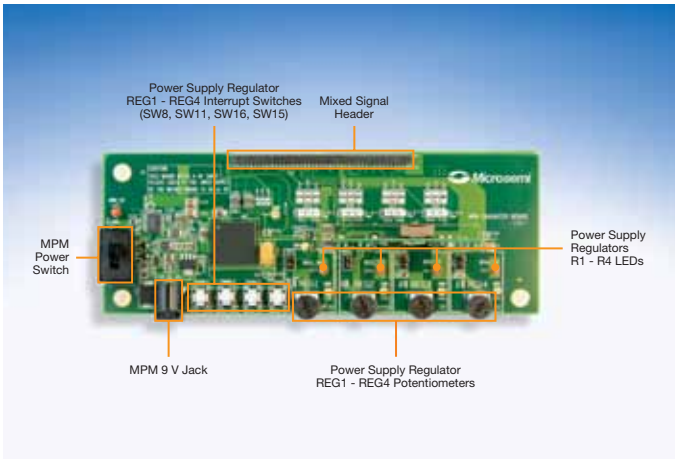


- **Supports debug access to the mixed signal header of the SmartFusion Evaluation Kit and SmartFusion Development Kit**
- **4 1/2" plastic standoffs and 4 plastic screws to match development kit height**
- **Sold standalone**

- **Board features**
  - Test points for signal probing
  - Mixed signal header for daughter card support
  - 100 Mil header for wire-wrapped or soldered signals

Ordering Code	Supported Device	Price
MIXED-SIGNAL-DC	No Microsemi device	$ 55

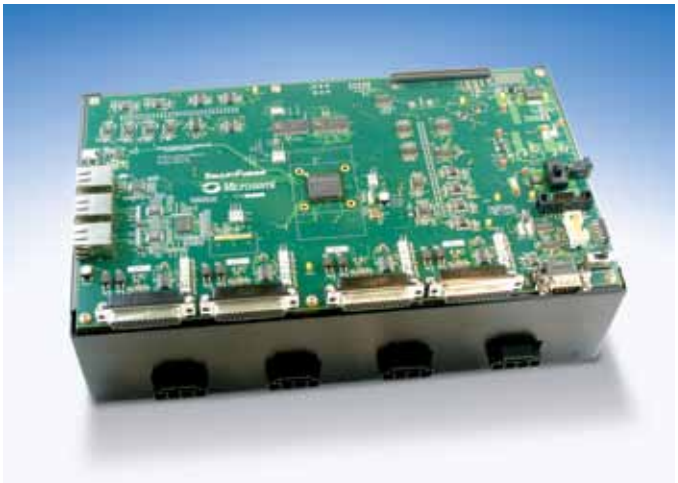
MPM Daughter Card



- **Supports power management design with the SmartFusion Evaluation Kit and SmartFusion Development Kit**
- **MPM design example implements configurable power management in SmartFusion cSoC**
- **Graphical configuration dialog**
- **In-system reconfigurable**
- **9 V power supply**
- **Board features**
  - 4 power supply regulators
  - 4 potentiometers to control regulators
  - 4 power supply regulator interrupt switches
  - 4 power supply regulator status LEDs
  - Mixed signal header connector connects to SmartFusion board

Ordering Code	Supported Device	Price
MPM-DC-KIT	No Microsemi device	$ 299

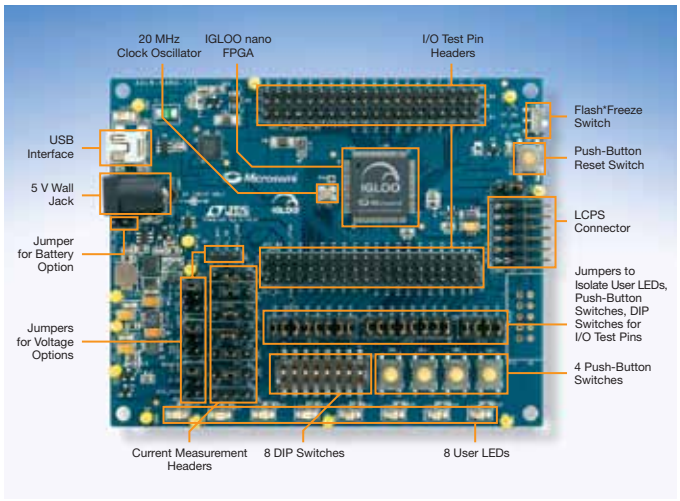
Motor Control Development Kit



- **Circuitry on board accommodates drivers for up to 4 PMSM motors (1 supplied with kit)**
- **One PMSM motor with Hall sensor and encoder included**
- **Reference design supporting multiple operation modes**
- **PC interface for defining velocity, torque and other parameters for up to four motors in real-time over an Ethernet connection**
- **18 V power supply**
- **Mains power supply with international adapter**
- **Cross over cable**
- **Schematics and design files available**
- **User's guide**
- **Five reference designs including C source code and RTL**
- **Commutation in trapezoidal mode using Hall effect sensor feedback**
- **Sinusoidal using Hall effect sensor feedback**
  - Commutation starts in trapezoidal mode and switches to sinusoidal when sufficient speed is achieved
- **Sinusoidal with Hall effect encoder feedback**
  - Commutation starts in trapezoidal mode and switches to sinusoidal mode on first edge of Hall sensor input using incremental encoder
- **Sensorless trapezoidal**
  - Uses back-EMF to generate six-step commutation feedback

Ordering Code	Description	Price
A2F-MOTOR-CONTROL-KIT	Motor control kit including reference designs and 1 motor	$ 2,499
A2F-MOTOR-CONTROL-DESIGNS	Motor control reference designs	$ 499
3-MOTORS	Additional 3 motors	$ 185

IGLOO nano Starter Kit



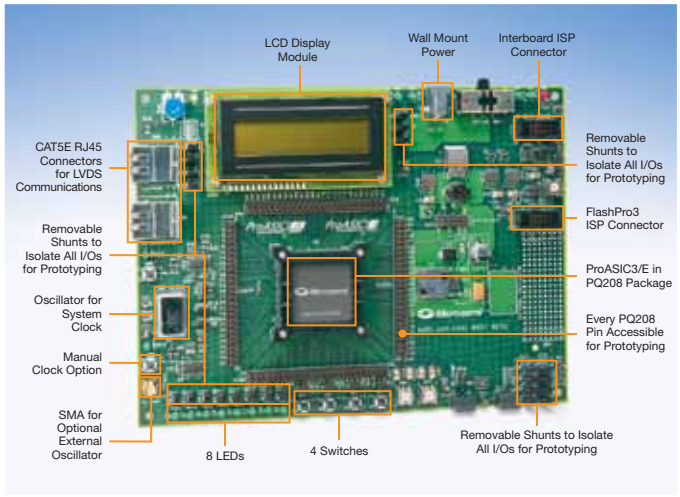
- **Supports basic IGLOO nano low power FPGA design, including Flash*Freeze mode**
- **Free one-year Libero IDE software and Gold license**
- **Low-cost programming stick (LCPS)**
- **Two USB cables**
- **Kit user's guide, Libero IDE tutorial and design examples**
- **PCB schematics, layout files and BOM**

- **Board features**
  - All I/Os available for external connections
  - Full current measurement capability of independent I/O banks and VCC
  - USB connection for USB-to-serial (RS232) interface for HyperTerminal or power
  - 20 MHz clock oscillator
  - LEDs and switches for simple inputs and outputs
  - Ability to switch VCORE from 1.2 V to 1.5 V
  - RoHS compliant

Ordering Code	Supported Device	Price
AGLN-NANO-KIT*	AGLN250V2-VQG100	$ 99

Note:
** Replaces -Z version of the nano Starter Kit.*

ProASIC3 Starter Kit

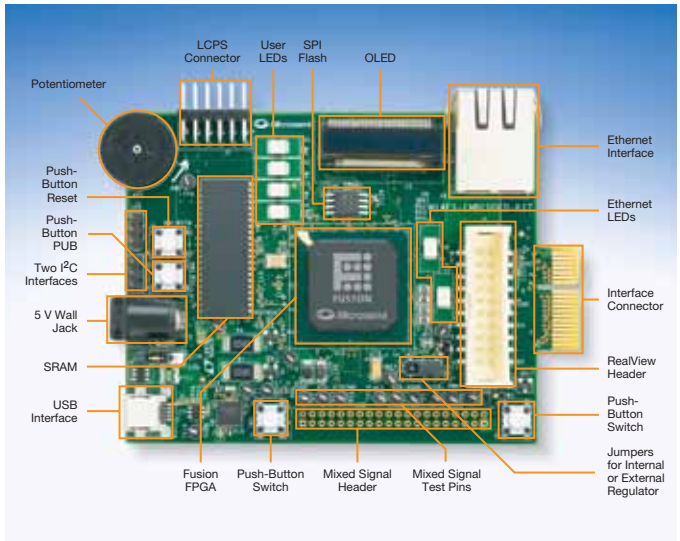


- **Supports basic ProASIC3 FPGA design and LVDS I/O usage**
- **Free one-year Libero IDE software and Gold license**
- **FlashPro3 or FlashPro4 Programmer**
- **9 V power supply and international adapters**
- **Kit user's guide, Libero IDE tutorial and design examples**
- **PCB schematics, layout files and BOM**

- **Board features**
  - Eight I/O banks with variety of voltage options
  - Oscillator for system clock or manual clock option
  - LEDs and switches for simple inputs and outputs
  - LCD display module
  - Two CAT5E RJ45 connectors for high-speed LVDS communications
  - All I/Os available for external connections
  - Not RoHS compliant

Ordering Codes	Supported Devices	Price
A3PE-PROTO-KIT	A3PE1500-PQ208	$ 665

Fusion Embedded Development Kit

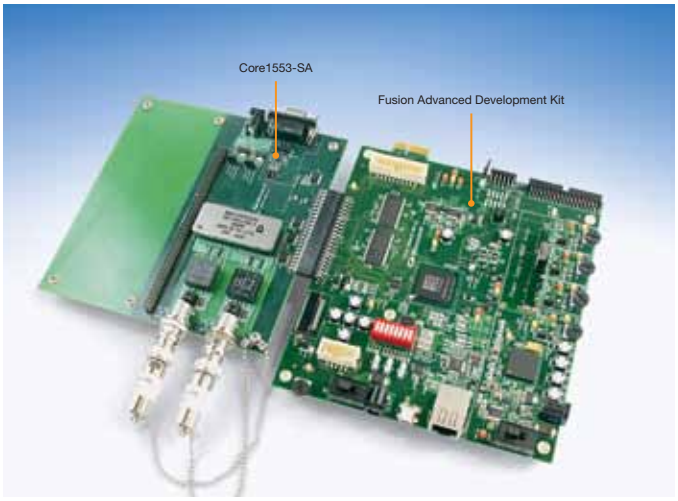


- **Supports royalty-free, industry-standard ARM Cortex-M1 or 8051s development**
- **Free one-year Libero IDE software and Gold license with SoftConsole for program and debug**
- **Low-cost programming stick (LCPS)**
- **5 V power supply and international adapters**
- **Two USB cables**
- **Kit user's guide, Libero IDE tutorial and design examples**
- **PCB schematics, layout files and BOM**

- **Board features**
  - 512 KB SRAM, 2 MB SPI flash memory provided on board
  - 10/100 Ethernet and I^2C interfaces
  - USB-to-UART connection for HyperTerminal on a PC
  - Built-in voltage, current and temperature monitor and voltage potentiometer
  - Mixed signal interface
  - Blue OLED 96x16 pixel display
  - Dynamic reconfigurable analog and flash memory
  - FlashPro3 and RealView debug interface
  - RoHS compliant

Ordering Code	Supported Device	Price
M1AFS-EMBEDDED-KIT	M1AFS1500-FGG484	$ 250

Core1553 Development Kit



- **Allows users to evaluate the functionality of Microsemi's Core1553BRM without having to create a complete MIL-STD-1553B compliant system**
- **Fusion Advanced Development Kit with two 9 V power supplies**
- **Core1553 daughter card**
- **User's guide, tutorial and design example**
- **PCB schematics, layout files and BOM**
- **Purchasing the kit gives the owner the right to the programming file of the demo, but not an evaluation of the IP. The IP evaluation or purchase is quoted separately.**

- **Board features**
  - MIL-STD-1553B transceiver, two transformers and two concentric twinax connectors included on the Core1553 daughter board
    - ~ *MIL-STD-1553B concentric twinax connectors are center pin signal high and cylindrical contact signal low*
    - ~ *Connectivity is MIL-C-49142 compliant*
    - ~ *Evaluate and develop medium speed on-board data communications bus solutions for MIL-STD-1553B / UK DEF-STAN 00-18 (Pt.2) / NATO STANAG 3838 AVS / Avionic Standards Coordinating Committee Air-Std 50/2*
  - CAN bus interface support
  - Connector to ARINC 429 Daughter Board (CORE429-SA)

Ordering Code	Description	Price
CORE1553-DEV-KIT	Core1553 Development Kit	$ 3,620
CORE1553-SA	Core1553 daughter card	$ 2,900
M1AFS-ADV-DEV-KIT-PWR	M1AFS-ADV-DEV-KIT with two 9 V power packs	$ 750

Hardware Summary

Microsemi offers hardware choices for terrestrial products. Most popular kits are listed in the table and shown in further detail in this section. Full details of these kits can also be found online with user's guides and accompanying tutorials.

Family	Ordering Code	Name	Device	Price	Power
SmartFusion	**A2F-EVAL-KIT***	SmartFusion Evaluation Kit	A2F200M3F-FGG484	$ 99	USB
SmartFusion	**A2F500-DEV-KIT**	SmartFusion Development Kit	A2F500M3G-FGG484	$ 999	5 V
SmartFusion	**MPM-DC-KIT**	MPM Daughter Card	none	$ 299	9 V
SmartFusion	**MIXED-SIGNAL-DC**	Mixed Signal Daughter Card	none	$ 55	N/A
Fusion	**M1AFS-EMBEDDED-KIT***	Fusion Embedded Development Kit	M1AFS1500-FGG484	$ 250	USB / 5 V
Fusion	**AFS-EVAL-KIT**	Fusion Starter Kit	AFS600-FG256	$ 500	9 V
Fusion	**M1AFS-ADV-DEV-KIT-PWR**	Fusion Advanced Development Kit	M1AFS1500-FGG484	$ 750	9 V
IGLOO	**AGLN-NANO-KIT***	IGLOO nano Starter Kit	AGLN250V2-ZVQG100	$ 99	USB
IGLOO	**AGL-ICICLE-KIT**	IGLOO Icicle Evaluation Kit	AGL125V2-QNG132	$ 150	USB
IGLOO	**AGLP-EVAL-KIT**	IGLOO PLUS Starter Kit	AGLP125V2-CSG289	$ 299	5 V
IGLOO	**M1AGL1000-DEV-KIT**	ARM Cortex-M1 IGLOO Development Kit	M1AGL1000V2-FGG484	$ 550	5 V
ProASIC3	**A3PE-PROTO-KIT***	ProASIC3 Starter Kit	A3PE1500-PQ208	$ 665	9 V
ProASIC3	**M1A3PL-DEV-KIT**	ARM Cortex-M1 ProASIC3L Development Kit	M1A3P1000L-FGG484	$ 550	5 V

**Most recommended Kit for each product family*

FlashPro4 In-System FPGA Programmer



- **Supports in-system programming**
- **Supports IEEE 1149 JTAG programming through STAPL**
- **Supports IEEE 1532**
- **Uses FlashPro software, available as part of Libero IDE or standalone**
- **Free software updates**
- **USB Connection to PC**
- **Operating systems**
  - Windows XP Professional (SP2 recommended)
  - Windows 2000 Professional (SP4 recommended)

Ordering Code	Price
FLASHPRO4	$ 49

Silicon Sculptor 3 FPGA Programmer



- **Programs all Microsemi packages, including PL, PQ, VQ, QN, BG, FG, and CS**
- **Universal Microsemi socket adapters**
- **Use with Silicon Sculptor software**
- **Security fuse can be programmed to secure the devices**
- **Includes self-test to test its own hardware**
- **Protection features**
  - Overcurrent shutdown
  - Power failure shutdown
  - ESD protection
  - ESD wrist straps with banana jacks (included as standard)
- **Operating systems**
  - Windows XP Professional (SP2 recommended)
  - Windows 2000 Professional (SP4 recommended)

Ordering Code	Price
SILICON-SCULPTOR 3	$ 4,330

For adapter modules, refer to www.microsemi.com/soc/products/hardware/program_debug/ss/modules.aspx

Programming Devices In-System Using a Microprocessor

Although the FlashPro3 programmer can perform in-system programming, it does require a specific header to be connected externally. For example, if your system already has external communication available through a microprocessor interface, you may prefer to have the processor perform the in-system programming. This can be done in two ways.

DirectC

DirectC v2.3 is a set of C code designed to support embedded microprocessor–based in-system programming for IGLOO, ProASIC3 and Fusion families. To use DirectC v2.3, you must make some minor modifications to the provided source code, add the necessary API and compile the source code and the API together to create a binary executable. The target system must contain a microprocessor with a minimum 256 bytes of RAM, a JTAG interface to the target device from the microprocessor and access to the programming data to be used for programming the FPGA. Access to programming data could be provided by a telecommunications link for most remote systems.

Download DirectC source files and the complete user's guide at: www.microsemi.com/soc/products/hardware/program_debug/directc/default.aspx

STAPL Player

The STAPL Player can be used to program third-generation flash devices such as IGLOO, ProASIC3 and Fusion, and interprets the contents of a STAPL file, which is generated by Libero IDE software tools. The file contains information about the programming of Microsemi flash-based devices, as well as the JTAG scan chain for a single device. The data format is a JEDEC standard known as the Standard Test and Programming Language (STAPL) format. For third-generation devices, note that the STAPL Player will not support serialization of the FlashROM, nor will it support Smart Erase enabled silicon. The STAPL Player reads the STAPL file and executes the file's programming instructions. Because all programming details are in the STAPL file, the STAPL Player itself is completely device-independent. In other words, the system does not need to implement any programming algorithm details; the STAPL file provides all of the details.

The key differences between the DirectC and the STAPL player methods are in the memory footprint in the microprocessor and amount of data to transmit. The DirectC option requires more code space on the processor, but as a result less data has to be transmitted to perform programming. On the other hand, the STAPL player communicates both the information to be programmed and the intelligence needed to perform programming. So the code footprint is smaller but the amount of data to transmit will be larger. One advantage of the STAPL player method is that if updates are required to the programming algorithm, the STAPL method does not require new code in the processor, but the DirectC would require new code for the processor.

Intellectual Property Cores

Microsemi IP Cores		Tiles	Obfuscated Core	RTL Core
Core10/100	10/100 Mbps Ethernet MAC with Host Controller (AHB/APB option available)	7,254	Free Libero Gold	Purchase
Core1553BBC	MIL-STD-1553B Bus Controller (BC)	2,331	Purchase	Purchase
Core1553BRM	MIL-STD-1553B Bus Monitor Only	3,016	Purchase	Purchase
Core1553BRM	MIL-STD-1553B Combined Remote Terminal (RT), Bus Controller, and Bus Monitor (BM)	6,787	Purchase	Purchase
Core1553BRT	MIL-STD-1553B Remote Terminal	1,612	Purchase	Purchase
Core429	ARINC 429 Bus Interface (1 receive channel)	740	Purchase	Purchase
Core429	ARINC 429 Bus Interface (1 transmit channel)	563	Purchase	Purchase
CorePCIF	PCI Specification 2.3 Bus Controller with FIFO Support (66/64 Target and Master)	3,808	Purchase	Purchase
CorePCIF	PCI Specification 2.3 Bus Controller with FIFO Support (33/32 Target)	996	Purchase	Purchase
Core16550	Universal Asynchronous Receiver/Transmitter with or without FIFO	979	Libero Gold	Libero Platinum
Core3DES	3DES Encryption and Decryption	1,413	Libero Gold	Libero Platinum
Core8051s	8-Bit Microprocessor, 100% ASM51 Compatible, Configurable Peripherals, AHB Bus Compliant	2,500	Libero Gold	Libero Platinum
CoreABC	Low-Gate-Count Controller for the APB	241	Libero Gold	Libero Platinum
CoreAES128	AES Encryption and Decryption	5,193	Libero Gold	Libero Platinum
CoreAHB	Multi-Master Advanced High Performance Bus (AHB)	1,300	Libero Gold	Libero Platinum
CoreAHB2APB	AHB to Advanced Peripheral Bus (APB) Bridge	250	Libero Gold	Libero Platinum
CoreAHBLite	Single-Master AHB	700	Libero Gold	Libero Platinum
CoreAHBNVM	On-Chip Flash Memory Controller with AHB Interface	396	Libero Gold	Libero Platinum
CoreAHBSRAM	On-Chip SRAM Memory Controller with AHB Interface	236	Libero Gold	Libero Platinum
CoreAI	Analog Interface Core (maximum configuration)	460	Libero Gold	Libero Platinum
CoreAPB	APB	125	Libero Gold	Libero Platinum
CoreCFI	Common Flash Interface—Typical Configuration	600	Libero Gold	Libero Platinum
CoreCORDIC	Coordinate Rotational Digital Computer Core (bit-serial architecture)	450	Libero Gold	Libero Platinum
CoreDDR	High Performance Double Data Rate (DDR) SDRAM Controller	1,748	Libero Gold	Libero Platinum
CoreDES	DES Encryption and Decryption	1,271	Libero Gold	Libero Platinum
CoreFMEE	Flash Memory Endurance Extender (typical configuration)	541	Libero Gold	Libero Platinum
CoreGPIO	General-Purpose Input/Output Controller with APB Interface	100	Libero Gold	Libero Platinum
CoreI2C	I^2C Master/Slave Interface	658	Libero Gold	Libero Platinum
CoreInterrupt	CoreMP7 Interrupt Controller	68	Libero Gold	Libero Platinum
CoreLPC	Intel Low Pin Count interface for Fusion/IGLOO/PA3 (SERIRQ disabled)	340	Libero Gold	Libero Platinum
CoreMemCtrl	Off-Chip Memory Controller with AHB Interface	100	Libero Gold	Libero Platinum
CorePWM	Pulse Width Modulation Core (typical configuration)	650	Libero Gold	Libero Platinum
CoreSDLC	Synchronous Data Link Controller	1,286	Libero Gold	Libero Platinum
CoreSDR	High Performance Single Data Rate (SDR) SDRAM Controller	1,350	Libero Gold	Libero Platinum
CoreSMBus	System Management Bus Controller (master/slave configuration)	1,078	Libero Gold	Libero Platinum
CoreSMBus	System Management Bus Controller (slave-only configuration)	733	Libero Gold	Libero Platinum
CoreSPI	Serial Peripheral Interface (Combined Mode)	330	Libero Gold	Libero Platinum
CoreTimer	16- or 32-Bit Timer with APB Interface	310	Libero Gold	Libero Platinum
CoreUART	Universal Asynchronous Receiver/Transmitter	337	Libero Gold	Libero Platinum
CoreUART_APB	Universal Asynchronous Receiver/Transmitter with APB Interface	300	Libero Gold	Libero Platinum
CoreWatchdog	Watchdog Timer with APB Interface	280	Libero Gold	Libero Platinum
Cortex-M1	High Performance 32-Bit FPGA-Optimized Processor (pre-placed design block)	4,300	Libero Gold	Libero Platinum
CoreFFT	Fast Fourier Transform Core Generator (1,024 points)	9,030	Web Only	Web Only
CoreFFT	Fast Fourier Transform Core Generator (256 points)	7,364	Web Only	Web Only
CoreFIR	Finite Impulse Response Core Generator (configuration 1)	583	Web Only	Web Only

Note: Additional Cores and configurations can be found on the website and in core handbooks.

www.microsemi.com/soc

You may be interested in:
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