

2-Bit Bidirectional Voltage-Level Translator with Automatic Direction Sensing

Check for Samples: [TXB0302](#)

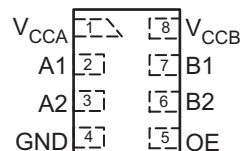
FEATURES

- **Fully Symmetric Supply Voltages.**
0.9 V to 3.6 V on A Port and 0.9 V to 3.6 V
- **V_{CC} Isolation Feature** — If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- **OE Input Circuit Referenced to V_{CCA}**
- **Low Power Consumption, 5-μA Max I_{CC}**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
 - 4000-V Human-Body Model (A114-B)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION

This 2-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 0.9 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 0.9 V to 3.6 V. This allows for low-voltage bidirectional translation between 1-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes. For the TXB0302, when the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver. The TXB0302 is designed so that the OE input circuit is supplied by V_{CCA}. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**DQM PACKAGE
(TOP VIEW)**



- Pull up resistors are not required on both sides for Logic I/O.
- If pull up or pull down resistors are needed, the resistor value must be over 20 kΩ.
- 20 kΩ is a safe recommended value, if the customer can accept higher V_{ol} or lower V_{oh}, smaller pull up or pull down resistor is allowed, the draft estimation is V_{ol} = V_{ccout} × 1.5k/(1.5k + R_{pu}) and V_{oh} = V_{ccout} × R_{dw}/(1.5k + R_{dw}).
- If pull up resistors are needed, please refer to the TXS0102 or contact TI.
- For detailed information, please refer to application note [SCEA043](#).

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	DQM – MicroQFN	TXB0302DQMR	77A

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](#).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](#).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TXB0302

SCES837B –MARCH 2012–REVISED OCTOBER 2012

www.ti.com



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
DQM	TXB0302	
1	VCCA	A-port supply voltage $0.9\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$
2	A1	Input/output 1. Referenced to V_{CCA} .
3	A2	Input/output 2. Referenced to V_{CCA} .
4	GND	Ground
5	OE	3-state output-mode enable. Pull OE (TXB0302) low to place all outputs in 3-state mode.
6	B2	Input/output 2. Referenced to V_{CCB} .
7	B1	Input/output 1. Referenced to V_{CCB} .
8	VCCB	B-port supply voltage $0.9\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}			–0.5	4.6	
V_I	Input voltage range	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state ⁽²⁾	A port	–0.5	$V_{CCA} + 0.5$	V
		B port	–0.5	$V_{CCB} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through VCCA, VCCB, or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE RATINGS⁽¹⁾⁽²⁾

THERMAL METRIC		TXB0302	UNIT
		DQM	
		8 PINS	
θ_{JA}	Package thermal impedance	259	°C/W

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.
(2) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			VCCA	VCCB	MIN	MAX	UNIT
VCCA	Supply voltage				0.9	3.6	V
VCCB					0.9	3.6	
V _{IH}	High-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	$V_{CCI}^{(2)} \times 0.65$	$V_{CCI}^{(2)}$	V
		OE	0.9 V to 3.6 V	0.9 V to 3.6 V	$V_{CCA} \times 0.65$	3.6	
V _{IL}	Low-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	0	$V_{CCI}^{(2)} \times 0.35$	V
		OE	0.9 V to 3.6 V	0.9 V to 3.6 V	0	$V_{CCA} \times 0.35$	
V _O	Voltage range applied to any output in the high-impedance or power-off state	A-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	V
		B-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	
Δt/Δv	Input transition rise or fall rate	A-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	ns/V
		B-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	
T _A	Operating free-air temperature				–40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.

(2) V_{CCI} is the supply voltage associated with the input port.

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VCCA	VCCB	T _A = 25°C			–40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OHA}	I _{OH} = –20 μA	0.9 V to 3.6 V				0.9 × VCCA			V
V _{OLA}	I _{OL} = 20 μA	0.9 V to 3.6 V					0.2		V
V _{OHB}	I _{OH} = –20 μA		0.9 V to 3.6 V			0.9 × VCCB			V
V _{OLB}	I _{OL} = 20 μA	0.9 V to 3.6 V					0.2		V
I _I	OE	V _I = V _{CCI} or GND	0.9 V to 3.6 V	0.9 V to 3.6 V		±1		±2	μA
I _{off}	A port	V _I or V _O = 0 to 3.6 V	0 V	0 V to 3.6 V		±1		±2	μA
	B port	V _I or V _O = 0 to 3.6 V	0.9 V to 3.6 V	0 V		±1		±2	
I _{OZ}	A or B port	OE = GND	0.9 V to 3.6 V	0.9 V to 3.6 V		±1		±2	μA
I _{CCA}	V _I = V _{CCI} or GND, I _O = 0	0.9 V to 3.6 V	0.9 V to 3.6 V					5	μA
I _{CCB}	V _I = V _{CCI} or GND, I _O = 0	0.9 V to 3.6 V	0.9 V to 3.6 V					5	μA
I _{CCA} + I _{CCB}	V _I = V _{CCI} or GND, I _O = 0	0.9 V to 3.6 V	0.9 V to 3.6 V					10	μA
I _{CCZA}	V _I = V _{CCI} or GND, I _O = 0, OE = GND	0.9 V to 3.6 V	0.9 V to 3.6 V					5	μA
I _{CCZB}	V _I = V _{CCI} or GND, I _O = 0, OE = GND	0.9 V to 3.6 V	0.9 V to 3.6 V					5	μA
C _I	OE	0.9 V to 3.6 V	0.9 V to 3.6 V		3				pF
C _{io}	A port	0.9 V to 3.6 V	0.9 V to 3.6 V		9				pF
	B port				12				

TIMING REQUIREMENTS

		VCCA	VCCB	MIN	MAX	UNIT
Data rate	C _L = 15 pF	0.9 to 3.6 V	0.9 to 3.6 V		40	Mbps
	C _L = 15 pF	1.2 to 3.6 V	1.2 to 3.6 V		100	Mbps
	C _L = 15 pF	1.8 to 3.6 V	1.8 to 3.6 V		140	Mbps
	C _L = 30 pF	0.9 to 3.6 V	0.9 to 3.6 V		40	Mbps
	C _L = 30 pF	1.2 to 3.6 V	1.2 to 3.6 V		90	Mbps
	C _L = 30 pF	1.8 to 3.6 V	1.8 to 3.6 V		120	Mbps
	C _L = 50 pF	1.2 to 3.6 V	1.2 to 3.6 V		70	Mbps
	C _L = 50 pF	1.8 to 3.6 V	1.8 to 3.6 V		100	Mbps

SWITCHING CHARACTERISTICS

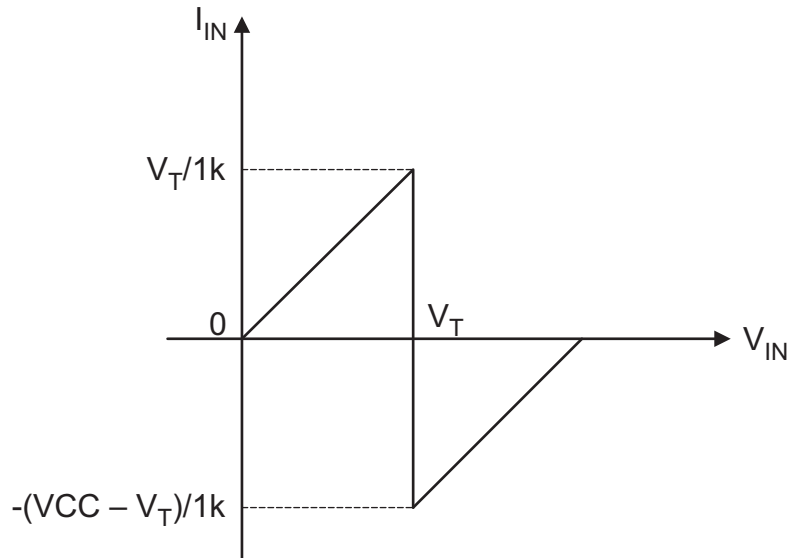
over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		VCCA	VCCB	MIN	TYP T _A = 25°C	MAX	UNIT
t _{pd}	A	B	C _L = 15	0.9-3.6	0.9-3.6		18.9	62.5	ns
	A	B	C _L = 15	1.2-3.6	1.2-3.6		7.5	15.5	
	A	B	C _L = 15	1.8-3.6	1.8-3.6		3.7	5.8	
	A	B	C _L = 30	0.9-3.6	0.9-3.6		19.5	64.5	
	A	B	C _L = 30	1.2-3.6	1.2-3.6		7.8	16.1	
	A	B	C _L = 30	1.8-3.6	1.8-3.6		3.8	6.1	
	A	B	C _L = 50	1.2-3.6	1.2-3.6		8	16.8	
	A	B	C _L = 50	1.8-3.6	1.8-3.6		4	6.5	ns
	B	A	C _L = 15	0.9-3.6	0.9-3.6		18.9	62.6	
	B	A	C _L = 15	1.2-3.6	1.2-3.6		7.5	15.4	
	B	A	C _L = 15	1.8-3.6	1.8-3.6		3.7	5.8	
	B	A	C _L = 30	0.9-3.6	0.9-3.6		19.5	64.5	
	B	A	C _L = 30	1.2-3.6	1.2-3.6		7.8	16.1	
	B	A	C _L = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	B	A	C _L = 50	1.2-3.6	1.2-3.6		8	16.9	
	B	A	C _L = 50	1.8-3.6	1.8-3.6		4	6.6	
t _{en}	OE	A	C _L = 15	0.9-3.6	0.9-3.6			504	ns
		B	C _L = 15	0.9-3.6	0.9-3.6			356	
t _{dis}	OE	A	C _L = 15	0.9-3.6	0.9-3.6			200	ns
		B	C _L = 15	0.9-3.6	0.9-3.6			200	ns
t _{FB} , t _{FB}	B-port rise and fall times		C _L = 15	0.9-3.6	0.9-3.6		2.95		ns
t _S , t _S	A-port rise and fall times		C _L = 15	0.9-3.6	0.9-3.6		3.1		ns
t _{SK(O)}	Channel-to-channel skew		C _L = 15	0.9-3.6	0.9-3.6			0.5	ns

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	VCCA, VCCB 0.9 V to 3.6 V	UNIT
			TYP	
C _{pdA}	A-port input, B-port output	C _L = 0, f = 10 MHz, t _r = t _f = 1 ns, OE = V _{CCA} (outputs enabled)	40	pF
	B-port input, A-port output		40	
C _{pdB}	A-port input, B-port output		40	pF
	B-port input, A-port output		40	
C _{pdA}	A-port input, B-port output	C _L = 0, f = 10 MHz, t _r = t _f = 1 ns, OE = GND (outputs disabled)	0.01	pF
	B-port input, A-port output		0.01	
C _{pdB}	A-port input, B-port output		0.01	pF
	B-port input, A-port output		0.01	



- (1) V_T is the input threshold voltage of the TXB0302 (typical $V_{CCI}/2$).
- (2) V_D is the supply voltage of the external driver.

Figure 2. Typical I_{IN} vs V_{IN} Curve

Power Up

There is no requirement for the power sequence. During operation, TXB0302 can work at both $V_{CCA} \leq V_{CCB}$ and $V_{CCA} \geq V_{CCB}$. During power-up sequencing, any power supply can be ramped up first. The TXB0302 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0$ V).

Enable and Disable

The TXB0302 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pullup or Pulldown Resistor on I/O Lines

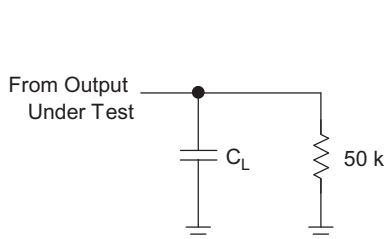
The TXB0302 is designed to drive capacitive loads of up to 50 pF. The output drivers of the TXB0302 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 20 k Ω to ensure that they do not contend with the output drivers of the TXB0302. but if the receiver is integrated with the smaller pull down or pull up resistor, below formula can be used for estimation to evaluate the V_{oh} and V_{ol} .

$$V_{ol} = V_{CCout} \times \frac{1.5k\Omega}{1.5k\Omega + R_{pu}} \quad (1)$$

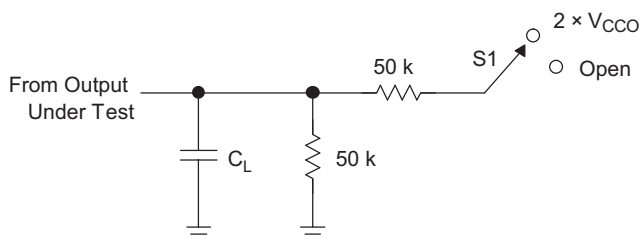
$$V_{oh} = V_{CCout} \times \frac{R_{pd}}{1.5k\Omega + R_{pd}} \quad (2)$$

For the same reason, the TXB0302 should not be used in applications such as I²C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

PARAMETER MEASUREMENT INFORMATION

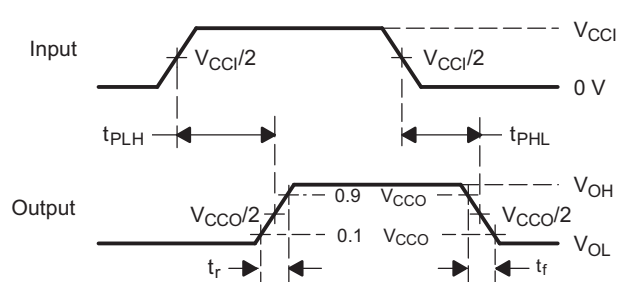


LOAD CIRCUIT FOR MAX DATA RATE,
PULSE DURATION PROPAGATION
DELAY OUTPUT RISE AND FALL TIME
MEASUREMENT

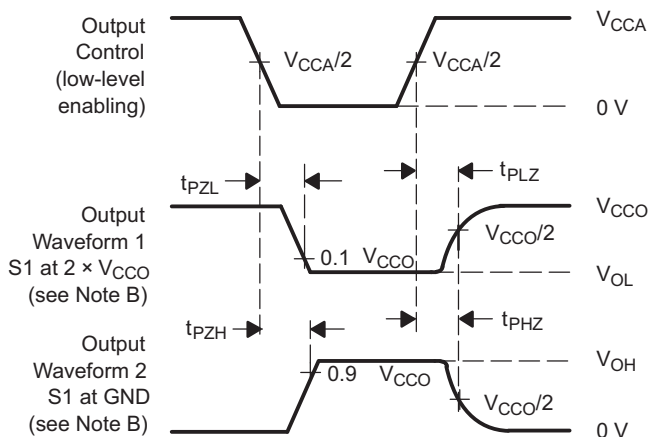


LOAD CIRCUIT FOR
ENABLE/DISABLE
TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ}	$2 \times V_{CCO}$
t_{PHZ}/t_{PHZ}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. V_{CCI} is the V_{CC} associated with the input port.
- F. V_{CCO} is the V_{CC} associated with the output port.
- G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuits and Voltage Waveforms

REVISION HISTORY**Changes from Original (March 2012) to Revision A** **Page**

- Added package pin out diagram notes. [1](#)

Changes from Revision A (May 2012) to Revision B **Page**

- Added Application Information Section [5](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0302DQMR	ACTIVE	X2SON	DQM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	77A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0302DQMR	X2SON	DQM	8	3000	180.0	9.5	1.4	2.0	0.5	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

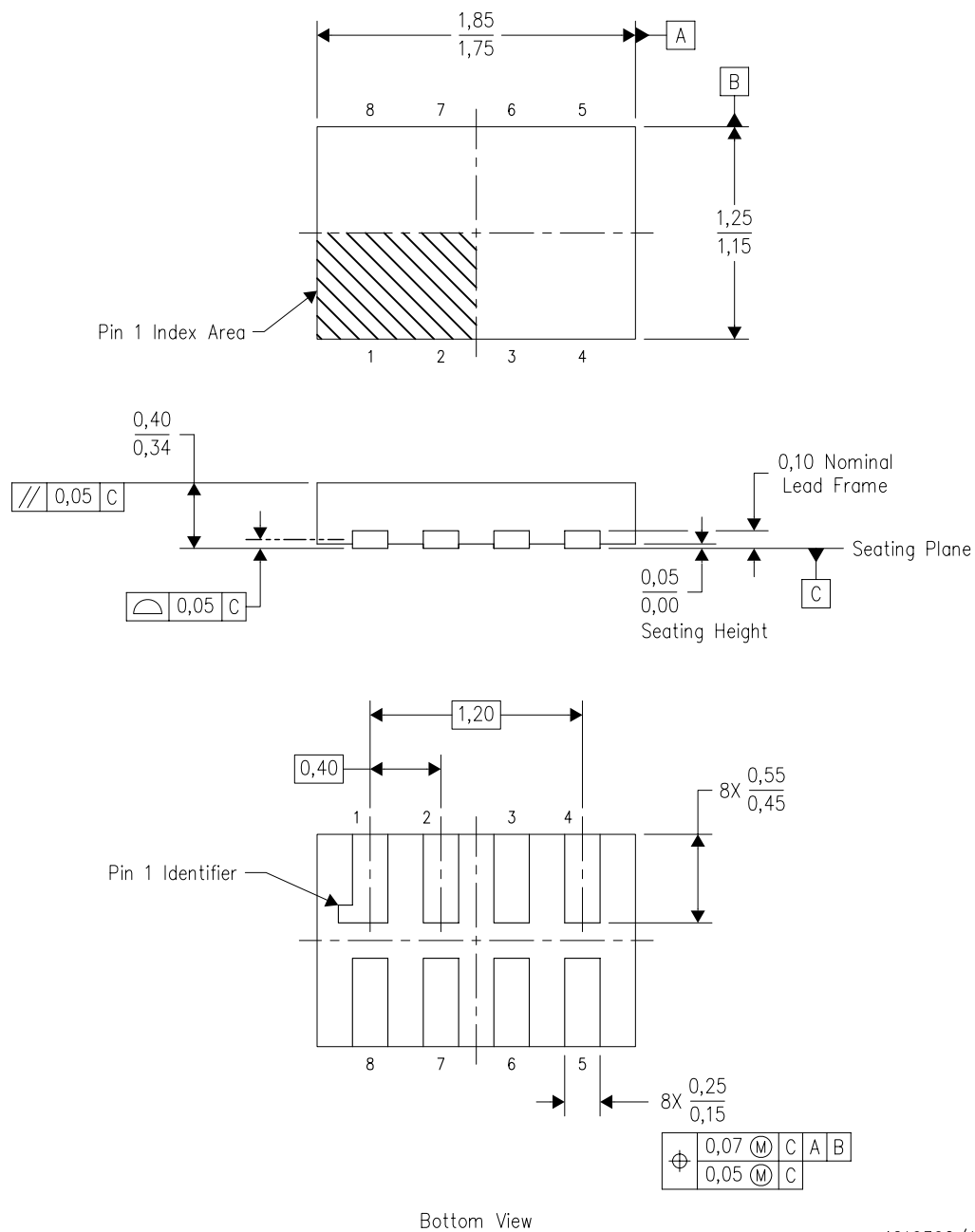


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0302DQMR	X2SON	DQM	8	3000	184.0	184.0	19.0

DQM (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



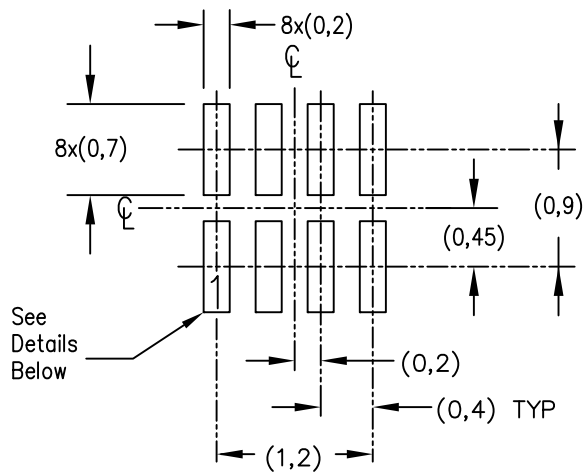
4210302/A 06/2009

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.

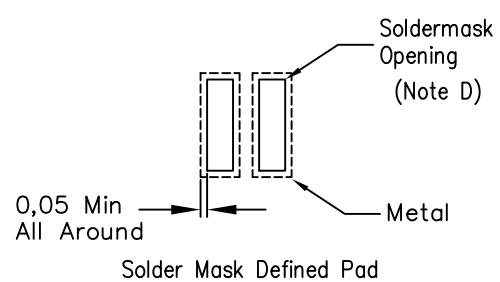
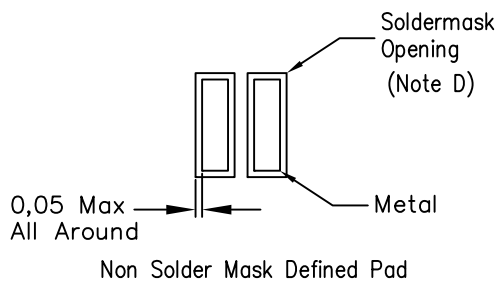
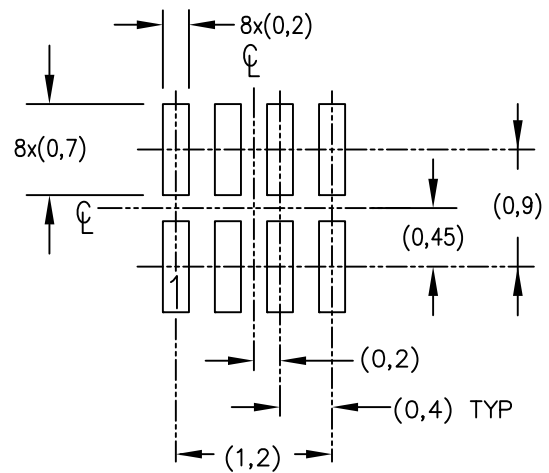
DQM (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout



Example Stencil Design
0.1mm Thick Stencil
(Note C)



Solder Mask Details

4218746/A 07/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - D. Customers should contact their board fabrication site for recommended solder mask tolerances.

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⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0302DQMR	X2SON	DQM	8	3000	180.0	9.5	1.4	2.0	0.5	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

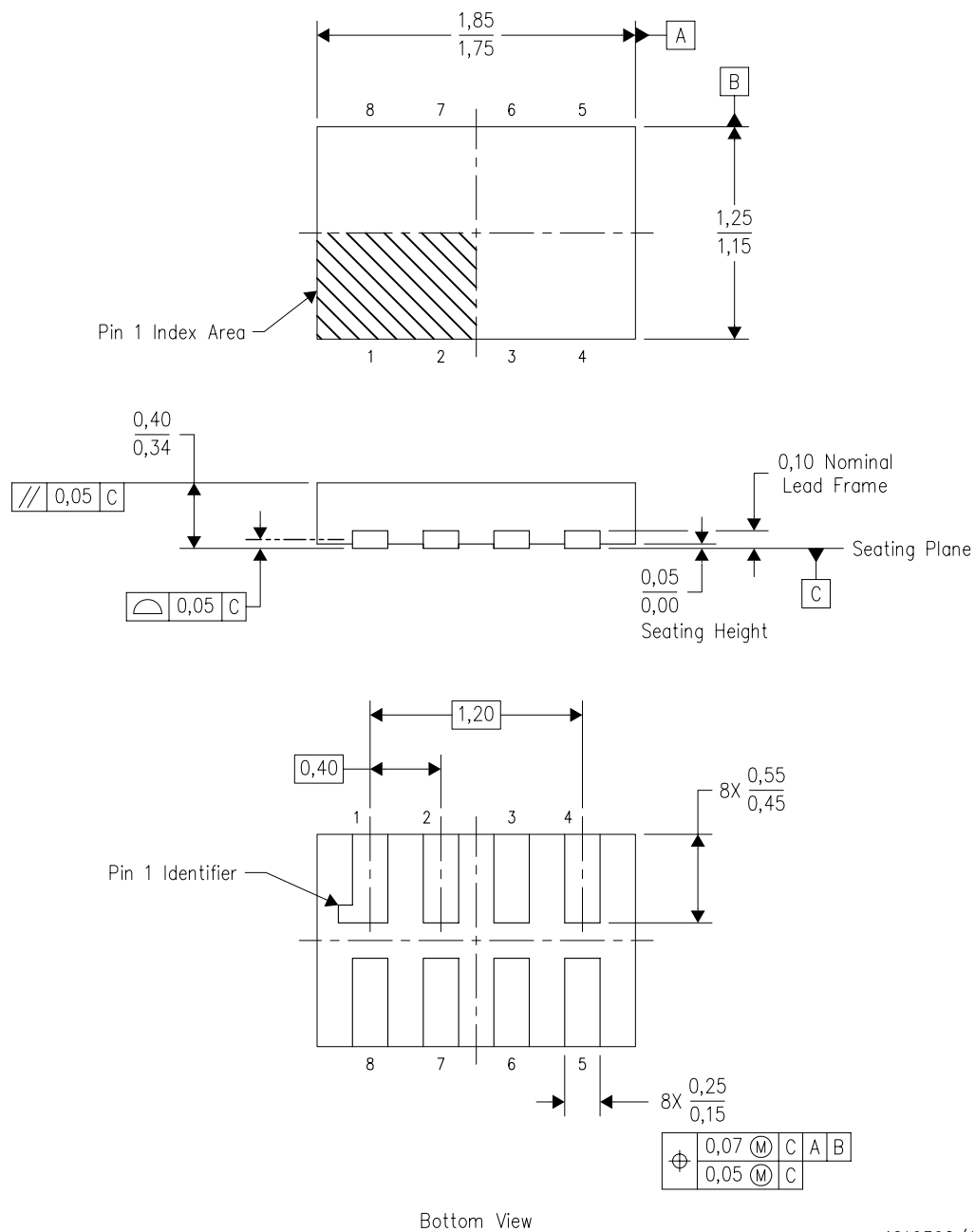


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0302DQMR	X2SON	DQM	8	3000	184.0	184.0	19.0

DQM (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



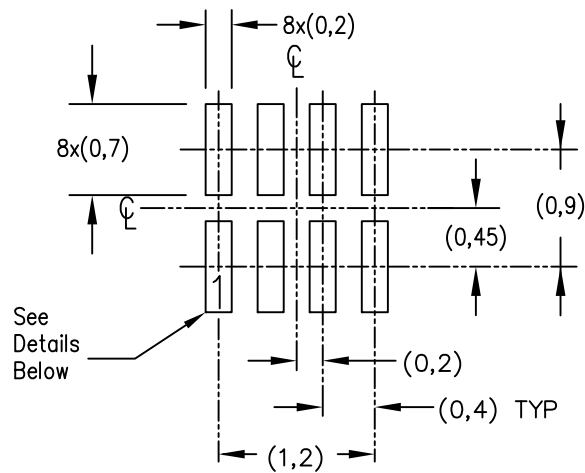
4210302/A 06/2009

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.

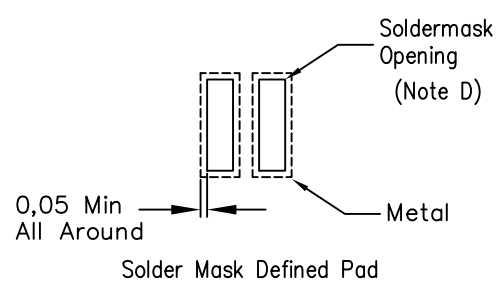
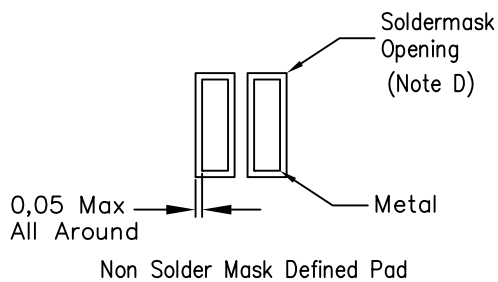
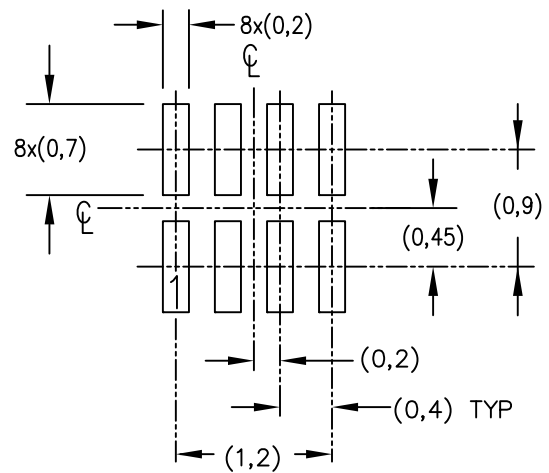
DQM (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout



Example Stencil Design
0.1mm Thick Stencil
(Note C)



Solder Mask Details

4218746/A 07/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - D. Customers should contact their board fabrication site for recommended solder mask tolerances.

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