

TUSB73x0 USB3.0 xHCI Controller Errata

This document serves to capture errata items on the TUSB7320 and TUSB7340 xHCI Host Controller devices.

Problem: *The ESD structure in the I/O cells used on WAKE# and CLKREQ# terminals may cause an oscillation when the signal de-asserts. Both of these open-drain signals rely on a pull-up resistor to return the signal to logic high after the signal de-asserts. It is at this time that the signal may start to oscillate if the ramp rate detector in the ESD structure detects a rise time that is too fast causing the signal to drive back low. This scenario is repeated indefinitely until power is removed from the device.*

WAKE# is an open drain, active low signal this is driven by the host controller to reactivate the PCI Express Link hierarchy's main power rails and reference clocks. Likewise CLKREQ# is also an open drain, active low signal that is driven low by the host controller to request that the PCI Express reference clock be available in order to allow the PCI Express interface to send/receive data.

The oscillation is caused by the TexFet ESD structure in the terminals I/O cell on both the TUSB7320 and TUSB7340 devices. If the rise time of the signal is too fast, this ESD structure will drive the signal back low. This scenario is repeated indefinitely until power is removed from the device.

Work Around: By slowing down the rise time the issue can be avoided. A target value for the rise time should be around 1 μ s to 2 μ s. Typically a 1.5-k Ω resistor is used as the pull-up on either WAKE# or CLKREQ#. By placing a 0.001- μ F capacitor on the WAKE# and/or CLKREQ# signal to ground, the rise time slows to around 1.5 μ s such that the ESD structure will not fire unexpectedly.

It may also be possible to tweak the pull-up resistor value based on the Wake circuit capacitance to achieve the desired rise time. This is board dependent and up to the user to define the appropriate pull-up value.

Problem: *Accesses to the PORTSC or PORTPMSC registers of a port that has been disabled via the PORT(x)_DIS bit at PCI configuration address 0xE0 may cause the controller to become unresponsive.*

Work Around: Customers should ensure that no access is attempted to the PORTSC or PORTPMSC registers of ports that have been disabled via the PORT(x)_DIS bits. The TI-provided driver for this device will not attempt to access disabled ports, but it is important that custom xHCI drivers and xHCI-aware BIOS implementations also do not attempt to access disabled ports.

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