TSW1200EVM: High-Speed LVDS Deserializer and Analysis System

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1 Introduction

The Texas Instruments TSW1200 High-Speed LVDS Deserializer and Analysis System provides a comprehensive set of hardware and user interface software to effectively evaluate the performance of a wide range of Texas Instruments (TI) high-speed, analog- to-digital converters (ADC), particularly those high-speed ADCs that employ an low-voltage differential signal (LVDS) format for the data converter's output data. With a high-quality, low-jitter clock and a high-quality input frequency provided to the evaluation module, the TSW1200 system can be used to demonstrate data sheet performance specifications.

The TSW1200 hardware has a high-speed connector that plugs into an evaluation module (EVM) for the ADC. Firmware for an FPGA on the TSW1200EVM has an interface to various LVDS data formats and FIFO memory sufficient to capture as much as 64K samples of data. A USB connection transfers the captured data to a personal computer for post-processing. The user Interface software controls the TSW1200 hardware and displays the FFT and important statistics related to the performance of the ADC.

2 Functionality

Many TI high-speed ADCs have LVDS outputs for the digitized data. These ADCs are generally available on an EVM that connects directly to the TSW1200EVM. The common connector between the ADC EVM and the TSW1200EVM is a Samtec high-speed connector suitable for differential pairs of pins separated by ground. A common pinout for the connector across a family of EVMs has been established. At present, the interface between the ADC EVM and the TSW1200EVM has defined connections for 14 pairs of LVDS plus two clock lines. The connector pinout has an additional 14 LVDS pairs for future product support. In most cases, if a TI ADC supports LVDS outputs, then the TSW1200 system can be used to capture data from the ADC. If the ADC supports a CMOS single-ended format, then the TSW1100 system is intended to interface to it.

The data format for the LVDS data bus can be in one of many formats, all supported by the TSW1200. For single-channel, high-speed ADCs, the data format is commonly parallel dual-data rate with one clock line. Dual-data rate means that both the rising and falling edges of the clock strobe data into the TSW1200. For multichannel ADCs, the data is commonly presented in a serialized format, where individual bits of the output data are presented on an LVDS line one bit at a time, at a higher data rate than the sample rate of the ADC.

The firmware in the FPGA on the TSW1200 is designed to accommodate both parallel DDR formats and serial LVDS formats, although not at the same time. The EEPROM on the TSW1200EVM is large enough to hold two distinct program files for the FPGA. One program bit file supports the parallel DDR format and the other bit file supports serial LVDS formats. The TSW1200 can be set to support the desired data format by simply setting two jumpers and pressing the PROGRAM button.

The parallel DDR FPGA program supports several types of data formats. One common format presents odd-numbered data bits on the bus on one clock edge and even-numbered data bits on the bus on the other clock edge. This format is commonly used for ADCs with sampling rates up to 250 MHz. For this bit-wise DDR format, the parallel data bus uses half as many LVDS pairs as there are bits in the sample. For example, a 16-bit ADC uses eight LVDS pairs for data plus an LVDS clock pair for bit-wise DDR. For higher sample rates up to 500 MHz, a sample-wise DDR format is often used. For sample-wise DDR, the data bus width has as many LVDS pairs as the bit resolution of the ADC. On one clock edge, a data sample from the ADC is registered; on the next clock edge, the next data sample from the ADC is registered.

The serial FPGA program also supports several data formats. For one-wire serial formats, the data is serialized onto a single LVDS pair at a rate that is 12 times the sample rate for an ADC with a 12-bit resolution. A one-wire serialization format also is used for 14-bit and 16-bit data at data rates 14 or 16 times the sample rate, respectively. For serial data formats, a DDR LVDS bit clock is used to strobe the serial data bits and to deserialize the data. An additional clock pair provided at the sample rate of the ADC identifies the sample-word boundaries in the serial data. For multichannel ADCs, a single-bit clock and a single sample-rate clock (frame clock) is used for all of the LVDS data channels. The other common serial data format is two-wire serialization. Two-wire serialization is similar to one-wire serialization except that a data channel uses two LVDS pairs to carry the serialized data at a rate that is half of what it is for one-wire serialization. Two-wire serialization commonly is used for sample rates up to 125 MHz, whereas one-wire serialization generally is used for sample rates up to 65 MHz.

The FPGA firmware for the TSW1200 generally consists of two major functions: the LVDS ADC interface and the FIFO capture. The LVDS ADC interface supports either the various parallel DDR interfaces or the various serial interfaces as previously described. The LVDS ADC interface code in the FPGA reformats the data into a standard single-ended parallel data word with sample clock. This parallel sample word plus clock is output continuously to header posts on the TSW1200 for capture by a logic analyzer. The parallel data word with sample clock also is presented to the FIFO capture logic. Note that for parallel DDR data formats, the header output posts are not enabled by default, as the data rate (up to a 500-MHz sample rate) is often too fast to be feasible for a single-ended CMOS output.

The TSW1200 FPGA has enough FIFO buffer to capture as much as a 65536-sample record length from the continuous sample data stream coming from the LVDS ADC interface. The TSW1200 FPGA design includes a UART function that can transfer data to and from a USB interface device on the TSW1200 board. The USB interface device on the TSW1200EVM connects to a personal computer (PC) running Windows™ over a standard USB cable. The operation of the FIFO capture logic is controlled by writes from the PC USB port to a register map defined within the FPGA. The user interface software on the PC selects by register operations such things as record length of data to capture, which channel of an ADC to capture from, and then the user interface software downloads the captured data from the TSW1200 for processing in the form of an FFT or time-domain display.

3 Hardware Configuration

In this section, the various portions of the TSW1200EVM hardware are described.

3.1 Power Connections

The TSW1200EVM hardware is designed to operate from a single-supply voltage of greater than 6 Vdc. For convenience, two options can supply power to the TSW1200EVM. A bench power supply can supply power to banana jack connections on the TSW1200EVM, or a laptop-style power module that is included with the TSW1200 hardware can supply power. Figure 1 shows the relative position of the power connections on the TSW1200EVM (revision B or C of the hardware).

CAUTION

TI recommends that the black banana jack J14 be connected to a bench ground even if the 6-V external power brick is connected to J7. Intermittent loss of the USB connection can sometimes be observed without a good ground from the TSW1200EVM to the bench ground reference.

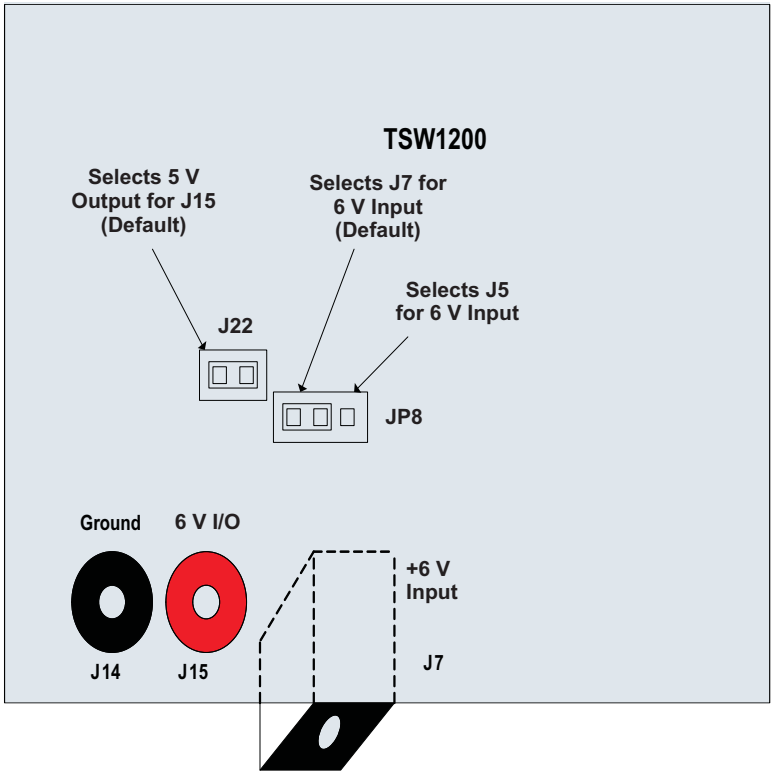


Figure 1. Position of Power Connections

Care must be taken in selection of the input power supply. One jumper selects whether the 6-V input power comes from the banana jack, or whether it comes from the external power module. Another jumper selects whether to connect the onboard regulated 5 V to the red banana jack for output. If the red banana jack is used to input 6 V from a bench power supply, the onboard regulated 5 V must not be connected to the red banana jack for output at the same time. Doing so causes the onboard 5-V regulator to fail over time.

3.2 Switches and Jumpers

3.2.1 Pushbuttons

Four pushbutton switches are mounted on the TSW1200EVM. Two pushbutton switches currently have defined functions; two of the switches are reserved for future use.

The PROGRAM pushbutton (SW3) causes the FPGA to reload its bit file from the FPGA EEPROM on the TSW1200EVM. The EEPROM currently is large enough to hold two FPGA bit files. When the FPGA loads a bit file, it loads the bit file indicated by the position of the jumpers J11 and J10. When power is first applied to the TSW1200EVM, the FPGA also loads its bit file from the EEPROM as determined by the jumpers J11 and J10. Therefore, pressing the PROGRAM pushbutton has the same effect as power-cycling the FPGA. All register settings in the FPGA and any data held in the FPGA are lost on loading the bit file, and the FPGA then is in its initial default configuration.

The RESET (SW4) pushbutton causes the FPGA to clear the FIFO storage, but does not clear any of the register settings in the FPGA. Any configuration of the FPGA done through register operations such as setting the UART baud rate will persist after pushing the RESET pushbutton. FPGA register settings only are cleared by pressing the PROGRAM pushbutton. For this reason, the RESET pushbutton has limited utility in this revision of the TSW1200EVM; this pushbutton may have more utility defined for it in future revisions of the FPGA firmware.

The PROM RESET (SW2) is reserved for future use, as is pushbutton SW5.

3.2.2 Jumpers

Jumpers J10 and J11 select the bit file to be programmed into the FPGA as indicated in Figure 2. The EEPROM is currently large enough to contain two complete programming files for the FPGA, with provision to later install a larger EEPROM with the capability to store four complete programming bit files for the FPGA.

Bit file CFG1 (jumper J10 set to LO and jumper J11 set to HI) is defined for use with ADC EVMs that employ a parallel LVDS DDR (dual-data rate) format. Bit file CFG2 is defined for use with ADC EVMs that employ a serialized data format, whether a one-wire serial format or a two-wire serial format. See Figure 3.

Simply moving the position of the jumpers J10 and J11 has no immediate effect. The FPGA does not load its programming bit file except on initial power up or until the PROGRAM pushbutton is pressed. To change the operation of the TSW1200EVM for use with a parallel DDR format or with a serial LVDS format, the jumpers J10 and J11 must be set to the desired position, and then the board must be power-cycled or have the PROGRAM button pushed.

Jumper JP8 selects whether the power supply to the TSW1200EVM is to be supplied by the external 6-V power module through power jack J7 or by an external 6-V bench power supply through the red banana jack J15.

A low drop-out linear power regulator on the TSW1200EVM generates a clean, low-noise 5-V supply from the 6-V power that is input to the TSW1200EVM. The jumper J22 can be used to connect this onboard regulated 5 V to the red banana jack J15 as an output. This option is a convenience for use with ADC EVMs that require a single 5-V supply input. In this way, the TSW1200EVM and ADC EVM combination can be powered completely from the laptop-style 6-V external power supply.

CAUTION

It is possible to select the red banana jack J15 as an input to be connected to a 6-V bench supply and at the same time install jumper J22 to connect the regulated 5 V to the red banana jack as an output. This, however, over time causes the 5-V regulator on the TSW1200 to fail.

Jumper J16 is used at the factory to program the small EEPROM for the USB port. The default position for this jumper is to be installed, and in normal operation, J16 is left installed.

Jumper J17 can be used to disable the 1.2-V power regulator for the FPGA core logic. The default position for this jumper is to be left uninstalled or open, and in normal operation, this jumper is left uninstalled.

Jumpers J1 and J12 form part of a JTAG chain through the FPGA and the FPGA EEPROM. A chain of JTAG devices form a loop, with the TDO from one JTAG device connected to the TDI of the next JTAG device. The normal setting of the JTAG jumpers is to connect the TDI of the JTAG connector to the TDI pin of the FPGA EEPROM through jumper J12 pins 2-4. Then, the TDO of the FPGA EEPROM connects to the TDI of the FPGA through jumper J12 pins 1-3 and jumper J1 pins 2-4. The TDO of the FPGA connects to the JTAG connector pin TDO through jumper J1 pins 1-2. If it desired to remove either the PFGA or the FPGA EEPROM from the JTAG chain, the jumpers J1 or J12 can be turned 90 degrees to connect pins 1-2 and 3-4. See the TSW1200EVM schematics and layout sections for illustration of this option.

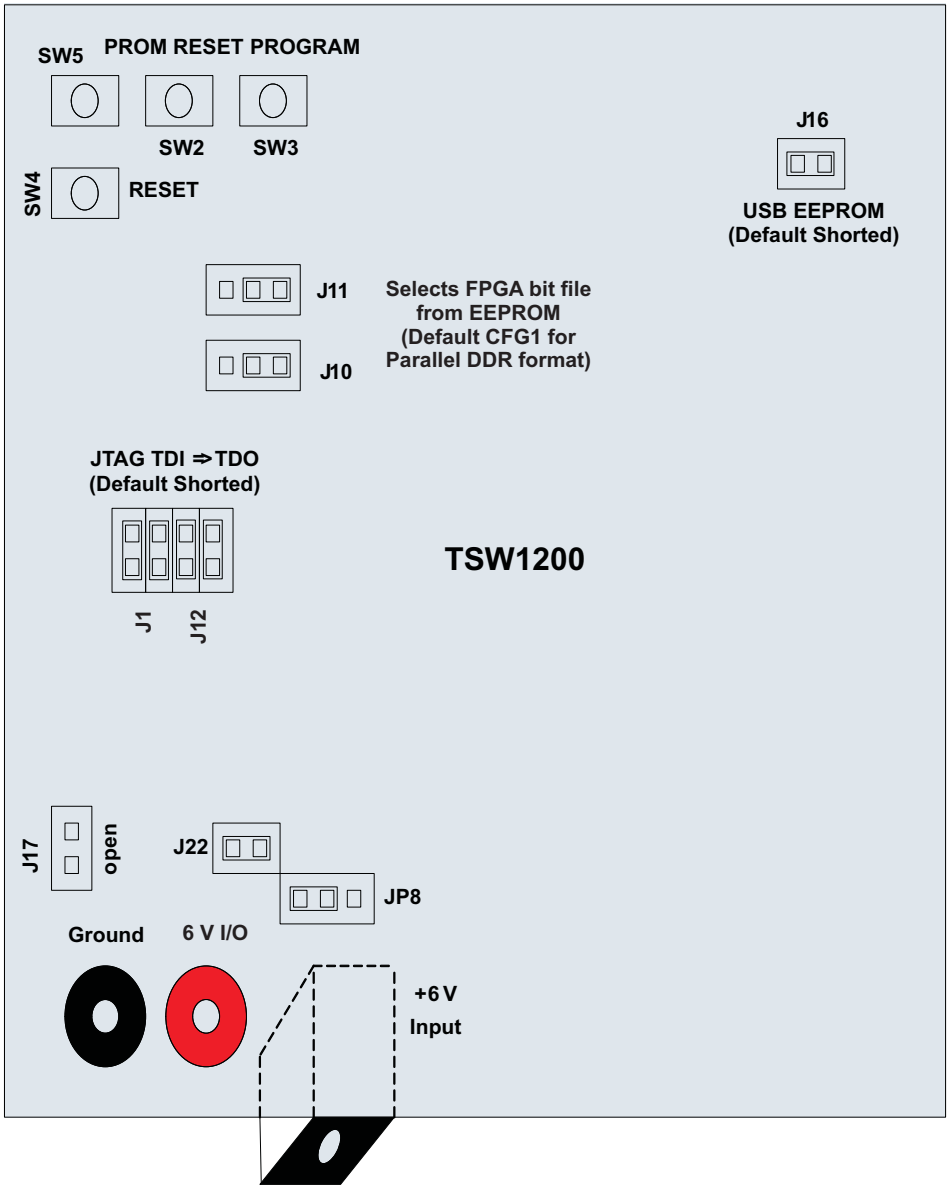


Figure 2. Position of Switches and Jumpers

J10	J11	PRGM LOAD
LO	LO	CFG2
LO	HI	CFG1
HI	LO	CFG4
HI	HI	CFG3

Figure 3. EEPROM Configuration Options

3.3 LEDs

Six LEDs are on the TSW1200EVM to indicate the presence of power and the state of the FPGA. See Figure 4. LED D16 illuminates to indicate the presence of a 6-V power supply to the board. On power up, the FPGA loads its programming bit file from the FPGA EEPROM. Once the programming bit file has completed loading, the LED D7 illuminates to indicate that the FPGA is operational.

Once the FPGA has loaded its bit file, it internally resets the clock circuitry that locks to a 200-MHz clock signal from a 200-MHz oscillator on the TSW1200 board. Once the internal reset is complete, LED D1 (labeled ADC on the TSW1200 silkscreen) illuminates to indicate that the TSW1200EVM is ready to use with an ADC EVM.

LED D4 flashes when the onboard 200-MHz oscillator is running. The 200-MHz oscillator clock is multiplied up to 250 MHz within the FPGA. The pattern of the flashing is of the form flash-flash-pause-pause. That is, the LED illuminates for a time, then turns off for the same time, then illuminates for the same time, then turns off 5 times. The internal time is derived from a division of the 250-MHz reference clock derived from the onboard oscillator.

LED D2 (labeled DCM on the TSW1200 silkscreen, which is an abbreviation for the digital clock manager block of logic in the FPGA) flashes when an LVDS clock from the ADC is present. The DCM clock flashes in the same flash-flash-pause-pause pattern, using the same clock division parameters as were used for the 250-MHz reference clock LED. In this manner, the DCM LED can be used to see that the clock from the ADC is present and approximately the right frequency by comparing it to the 250-MHz LED. That is, if the sample rate clock to the ADC is 250 MHz, then the DCM LED and the 250-MHz LED flash at the same rate. If the sample clock to the ADC is 125 MHz, then the DCM LED flashes at half the rate of LED D4. If the DCM LED is not flashing at all, then no clock is detected from the ADC. Common reasons for an ADC clock not to be detected are that the EVM is not powered on, or that the clock from the ADC is a CMOS clock instead of an LVDS clock due to an improper jumper setting.

LED D3 (labeled USB on the TSW1200EVM silkscreen) illuminates whenever the TSW1200 user interface software is accessing the FPGA by way of the USB connection. For longer FFT record lengths and lower UART baud rates, the USB LED illuminates longer than for shorter FFT record lengths or higher UART baud rates.

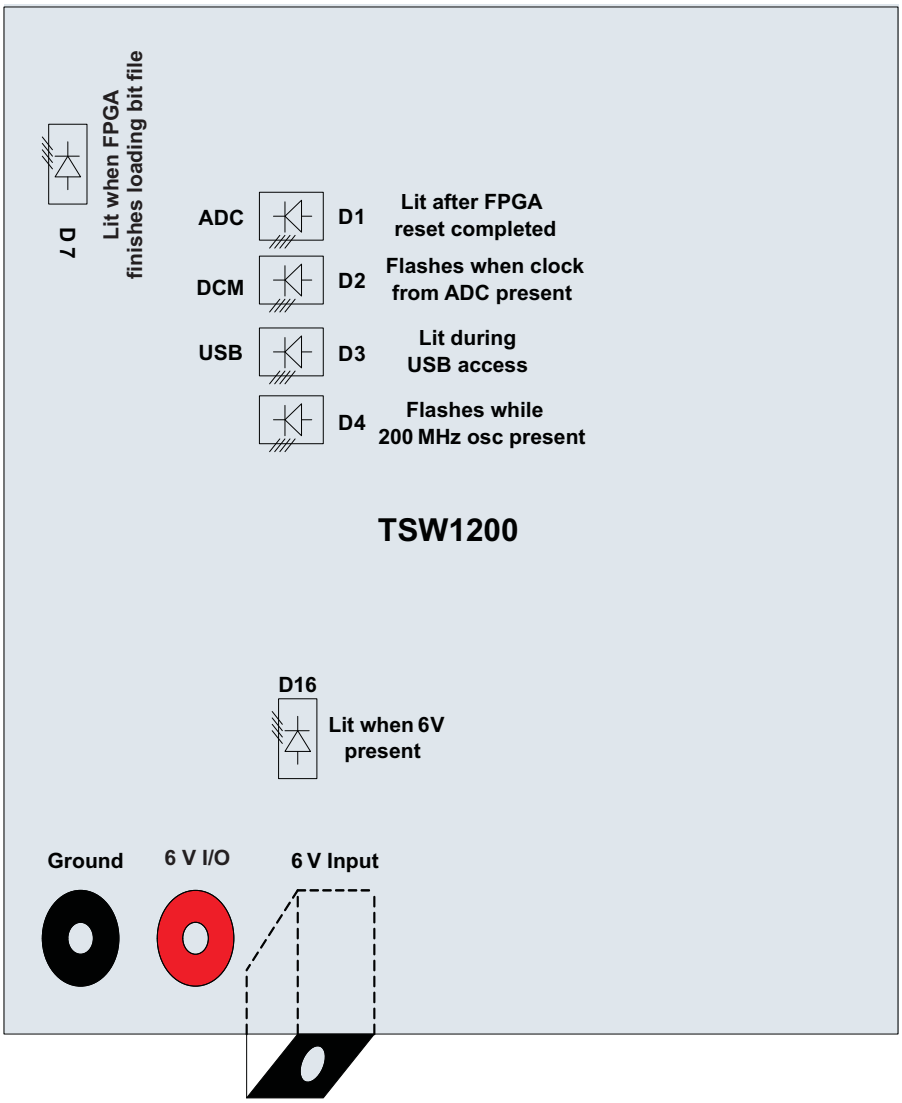


Figure 4. Position of LEDs

3.4 Input Connections

Figure 5 illustrates the position of the various input and output connections on the TSW1200EVM.

3.4.1 Samtec LVDS Connector

The connection between the TSW1200EVM and the ADC EVM to be tested is through a 120-pin Samtec connector. Fourteen LVDS data pairs plus two LVDS clock pairs have a defined position in the connector pinout that is common between the TSW1200EVM and many TI ADC EVMs. For the parallel LVDS DDR data format, the bit clock runs at the same rate as the sample clock to the ADC. For the serial LVDS data format, the bit clock runs at a higher multiple of the ADC sample clock and is used to strobe the serial data into the TSW1200EVM and then deserialize the data. For the serial LVDS data format, a second clock is provided, called the frame clock or FCLK, that runs at the sample rate and is used to delineate the

sample boundaries in the serial data stream. The frame clock line is unused in the parallel LVDS DDR format. In addition, 14 extra LVDS pairs are defined in the connector and routed to the TSW1200EVM FPGA for future expansion for larger parallel bus widths needed for faster data converters. The data direction for the LVDS data pairs is always defined as the ADC EVM driving the signal through the connector to the TSW1200EVM FPGA, with integrated 100-Ω termination in the FPGA.

For one-channel parallel DDR bit-wise data formats, eight of the LVDS data pairs are used to support up to 16-bit-resolution ADCs at up to 250-MHz sampling rates. For one-channel parallel DDR sample-wise data formats, 14 of the LVDS data pairs are used to support up to 14-bit-resolution ADCs at up to 500-MHz sampling rates. For two-channel parallel DDR bit-wise data formats, 14 of the LVDS data pairs are used to support two channels of 14-bit resolution at up to 250-MHz sampling rate.

For serial data formats, eight of the LVDS data pairs support up to eight channels of one-wire serial ADCs at up to 65-MHz sampling rate or four channels of two-wire serial ADCs at up to 125-MHz sampling rates. All other LVDS pairs are ignored for this release.

Five extra CMOS single-ended signals are defined in the Samtec connector that are sourced from the FPGA through the connector to the ADC EVM. These signals are optionally defined to allow the FPGA (under control of the TSW1200 user interface software) control the SPI serial programming of the ADC for those ADC EVMs that support this feature. For those ADC EVMs that support this feature, the SPI signals SEN (SPI Enable), SCLK (SPI Clk), and SDATA (SPI Data) are sourced by the TSW1200EVM FPGA to allow the TSW1200 user Interface to configure the operational mode of the ADC under evaluation. There SPI signals are by default not connected on the ADC EVM until a 0-Ω resistor is installed on the EVM to enable control of the SPI port from the TSW1200 user Interface software. Two additional signals, SPI Reset and SPI Power Down, are defined for possible future use.

The Samtec connectors snap together with no screws or other mechanism to hold the TSW1200EVM and the ADC EVM together. The TSW1200EVM comes with standoff posts for setting the TSW1200EVM flat on a bench or table. The ADC EVM has shorter standoff posts so that the TSW1200EVM and ADC EVM will lay flat on a bench or table and stay snapped together during use.

3.4.2 JTAG Connector

The TSW1200EVM includes an industry-standard JTAG connector that loops the JTAG ports of the FPGA and the FPGA EEPROM. Jumpers on the TSW1200EVM allow for either the FPGA or the FPGA EEPROM to be removed from the JTAG chain. The most frequent use for the JTAG connector is to program the TSW1200EVM FPGA. An FPGA programming pod can be purchased inexpensively from Xilinx™ to program the FPGA or the FPGA EEPROM.

The FPGA programming pod can be used to load a programming bit file directly into the FPGA for debug and development. However, once the FPGA is power-cycled or programmed by the PROGRAM pushbutton, this loaded FPGA bit file will be lost and the FPGA will revert to the bit file that is stored in the FPGA EEPROM. The FPGA programming pod also can be used to store a new FPGA programming bit file in the FPGA EEPROM so that the TSW1200 can be upgraded as new revisions of FPGA firmware become available.

The part number of the Xilinx Platform Cable USB programming pod that can be used to program or upgrade the TSW1200EVM is **DLC9G**. The programming pod operates from a USB port of a PC and connects directly with the TSW1200 JTAG connector through a ribbon cable supplied with the programming pod.

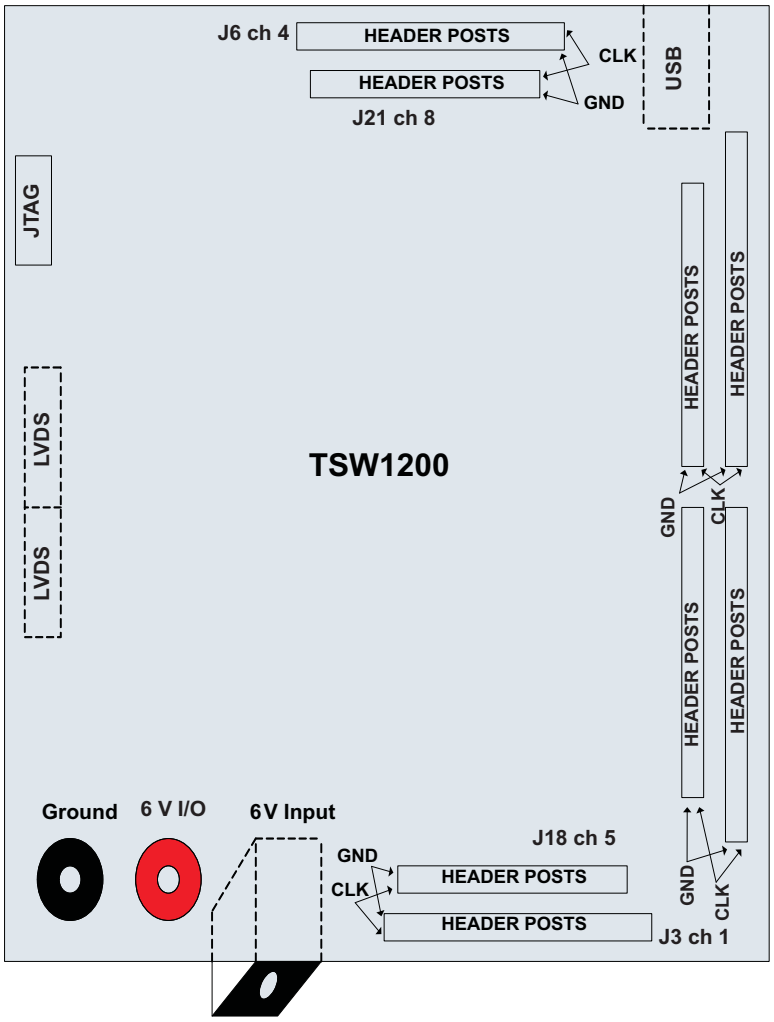


Figure 5. Position of Input, Output, and USB Connections

3.5 Output Connections

Two ways are available to output the parallel clock and sample data from the TSW1200EVM. The ADC sample data can be presented as a continuous stream of CMOS single-ended data on output header posts, or a set record length of ADC parallel data samples can be captured in the TSW1200EVM FIFOs and output to a PC through the USB serial port. The data capture by the FIFOs and TSW1200 user interface is the most convenient way to capture data from an ADC, but sometimes the continuous stream of data is desirable. For example, an application may require a larger capture depth for an FFT on a million continuous data samples or more. For this, the output header posts are available so that a logic analyzer can be used to capture ADC data in real time.

The pinout of the output data headers is shown in Figure 6. In all cases, the output header is a standard two-row header of square 0.025-inch posts on 0.1-inch centers. One of the two rows of posts are connected to ground down the whole row of posts, whereas the other row of posts are signal. The sample-rate clock is presented on the first post, and after skipping one no-connect post (or three posts for Channel 1) the parallel data bus is presented from the least-significant bit (bit D0) through the most-significant bit. Two of the channels allow for as much as 16-bit data resolution whereas the other six channels provide for up to 14-bit data.

By default, the output headers are not enabled for parallel DDR data formats due to the potential high sample rates of up to 500 MHz.

For the current release, four of the header posts are enabled for serial data formats. For up to four-channel ADCs, the parallel deserialized sample data is presented on the corresponding output header. For eight-channel serial data formats, the TSW1200 user interface software selects whether to output the lower four channels of data on the output headers for Channels 1 through 4 or whether to output the data for Channels 5 through 8 on the output headers for Channels 1 through 4. Output headers for Channels 5 through 8 are unused for this release.

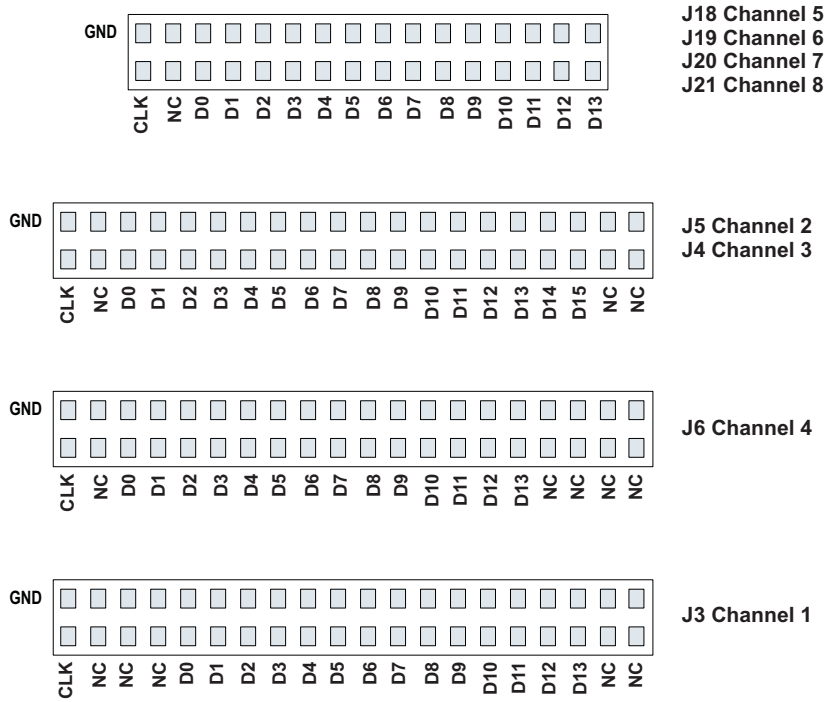


Figure 6. Pinout of Header Posts for Parallel Output Data

3.6 USB I/O Connection

Control of the TSW1200EVM is through a USB connection to a PC running Windows operating system.

For the computer, the drivers needed to access the USB port are included on the TSW1200 Installation CD and are installed during the installation process. The USB is accessed as a virtual communication port (VCP) and shows up in the Hardware Device Manager as TSW1200 under COM ports and as TSW1200 EVM under Multi-Port Serial Adapters. See Figure 8. On the TSW1200EVM, the USB port acts as a bridge to UART control of the FPGA. Control of the FPGA is managed by reads and writes to a register map of control registers defined in the design of the FPGA. Normally, register writes from the TSW1200 user interface software sets up the mode of operation of the FPGA. These register writes define such things as the depth of FIFO to use for data capture or from which channel of an ADC to capture data. Then, a single register access triggers the filling of the capture FIFOs. Immediately after the capture FIFOs have captured the desired amount of data, the FIFO data is streamed back up the USB connection to the TSW1200 user interface software. The UART data rate between the FPGA and the USB port can be set to 115K, 230K, or 460K baud. A UART baud rate of 920K is not recommended for reliable data transfer. On first connection of the USB port to a computer, the Microsoft Found New Hardware Wizard appears. Follow the dialog box prompts as covered in the Software Installation section of this User's Guide.

4 Software Installation

4.1 Installation CD

A software installation CD is included with the TSW1200 kit. This Installation CD includes all that is necessary to install the TSW1200 user interface software on a computer that is running the Microsoft Vista or Microsoft XP operating system. Included on the installation CD is this user's guide, a setup program to install the user interface software, and a suite of MATLAB™ routines that can be used to interface to the TSW1200EVM hardware. All drivers necessary for the USB connection and the user interface software are included.

The user interface software is installed in two parts, which is done automatically once the setup program is run. The actual user interface software is installed first along with the run-time engine that underlies the user interface. Then, Virtual Com Port (VCP) is installed for the USB connection to the hardware.

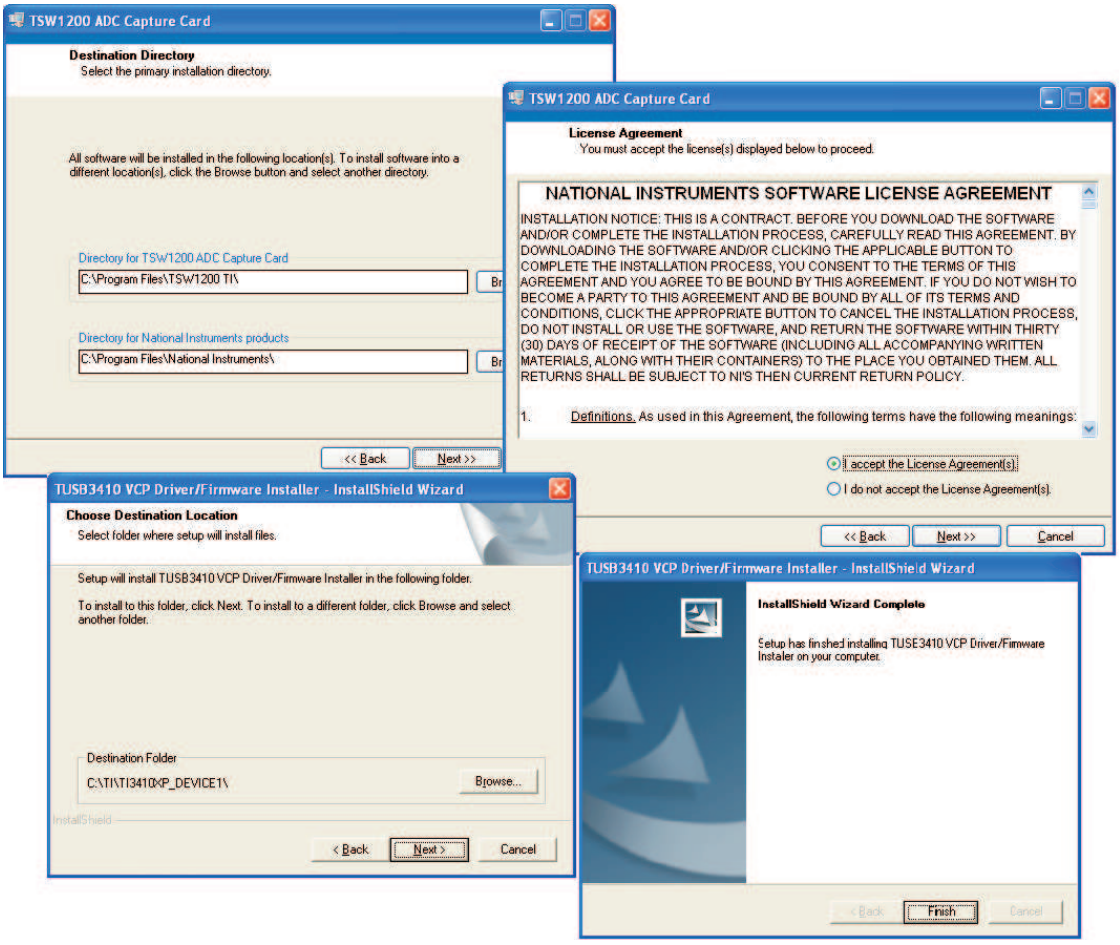


Figure 7. TSW1200 User Interface Installation

If the TSW1200 user interface software is being installed on a machine that has an older version, TI recommends that you first remove the old TSW1200 installation, using the Microsoft Add/Remove Programs function in the Control Panel. The TUSB3410 VCP (Virtual Com Port) can be left installed, but during the installation of the new TSW1200 user interface software, a dialog box appears to warn that the previous TUSB3410 is about to be uninstalled. Click cancel for this uninstall to leave the old installation of the TUSB3410 VCP in place.

If the installation program encounters an older revision of the TSW1200 user interface software that was not removed with Add/Remove Programs, it removes the older version, and the Setup.exe must be executed again to install the newer version. If an existing TUSB3410 Virtual Com Port is on the machine, the Installation program may remove this also unless the removal is canceled when the dialog box appears.

To install the TSW1200 user interface software, run the setup.exe file that is contained on the installation CD. Figure 7 shows the more important dialog boxes that appear during the installation process. Folders are created for the TSW1200 user interface and for the USB Virtual Com Port software. The default folder names can be accepted in the dialog box as shown in Figure 7, or a folder name and directory path can be entered into the dialog box. A license agreement is required for the National Instruments LabVIEW™ runtime engine that is used by the TSW1200 user interface software. It is unnecessary for the target computer to have LabVIEW installed; the TSW1200 user interface software comes with the runtime engine and is completely self-contained.

4.2 USB Port and Drivers

When the Virtual Com Port is installed and the USB cable has connected the TSW1200EVM to the PC, the TSW1200 can be located in the Hardware Device Manager as shown in Figure 8. The TSW1200 appears as TSW1200 as a COM port. Each time the USB cable is connected, it is possible that a different communication port is assigned. The TSW1200 user interface software locates the TSW1200 com port and opens communications with the TSW1200EVM. If the TSW1200 software is unable to find the port for the TSW1200EVM, it displays an error message that the TSW1200 is not found. Usually, this is an indication that the user interface software was opened before the USB cable was plugged in or that power is not supplied to the TSW1200EVM. In this case, ensure that power is applied to the TSW1200EVM and that the USB cable is plugged in. Then close and re-open the TSW1200 user interface software.

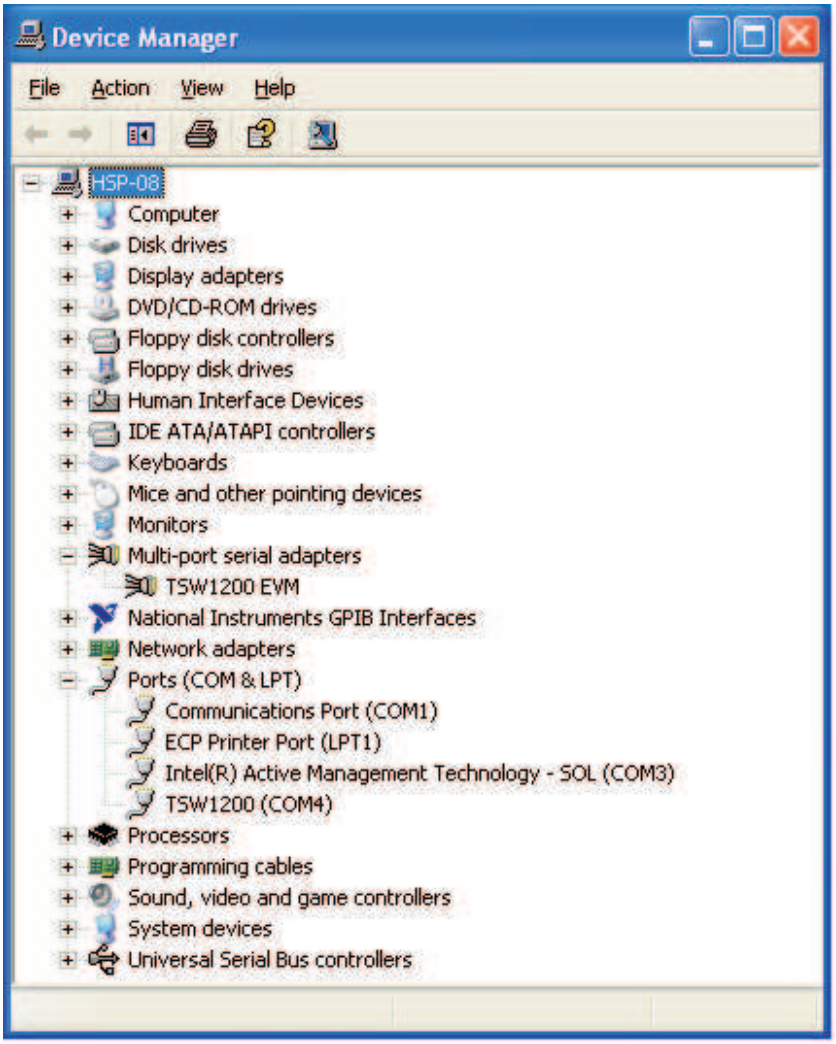


Figure 8. Hardware Device Manager

When the USB cable connects the TSW1200 to the PC for the first time, the Microsoft Found New

Hardware Wizard appears along with a series of pop-up windows. Select the default settings as shown in Figure 9. If the warning dialog box appears and indicates that the software has not passed Microsoft Logo Testing, select Continue Anyway. The Found New Hardware Wizard usually appears twice, once to install the com port and once to install the TSW1200 under Multi-Port Serial Adapters. The response to the dialog box prompts is the same in both cases.

When the TSW1200EVM USB cable is unplugged and plugged in again to a different USB port on the computer, the Found New Hardware Wizard may appear again, depending on whether that USB port is controlled by a different USB controller in the computer and depending on the registry configuration for the PC. If the Found New Hardware Wizard does appear again when the USB cable is reconnected, follow the same responses to the dialog boxes as when the TSW1200 was first installed.

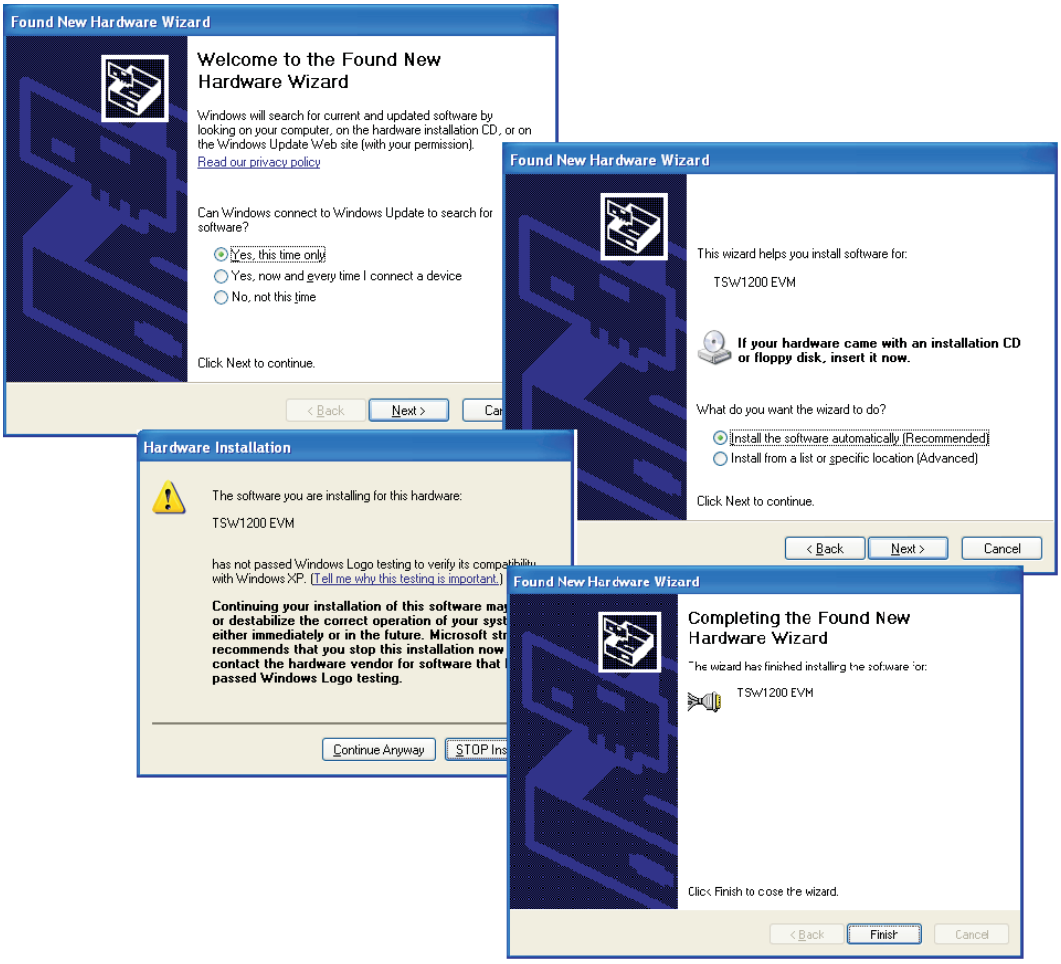


Figure 9. Found New Hardware Windows

4.3 Device ini Files

Included in the installation for the TSW1200 user interface software is a subdirectory of ini files for each category of ADC that is supported by the TSW1200EVM. TI strongly recommends that these files are not edited except at the factory. These files contain necessary information for the user interface software to properly configure the TSW1200EVM FPGA registers for proper operation with the desired ADC EVM. Some of the entries within the ini file are obvious, such as defining the bit resolution for a device to be 11, 12, 14, or 16 bits. Other entries in the ini file define for the FPGA which LVDS pairs within the Samtec

connector define the data bus, and correct operation may not be possible if these entries are edited. The use of ini files allows for new device types to be supported by the TSW1200EVM as they become available without having to modify, re-release, or re-install the TSW1200 user interface software. New device types may be supported at a later date simply by adding a new ini file to the proper subdirectory, using a script that TI will make available at that time.

5 User Interface

When the TSW1200 user interface software is started, the initial setup screen of Figure 10 appears. The status pane in the lower left reports on the firmware selection of the TSW1200EVM, the revision of the firmware, and the revision of the user interface software. Many of the TSW1200 software controls are available from this setup screen, such as ADC device selection. However, a test must be selected before the TSW1200 software is ready for data capture from the TSW1200EVM. The tests available for this revision of the TSW1200 software are a logic-analyzer-style Time Domain test and a single-tone FFT test. At any time, this setup screen can be chosen from the test pulldown menu.

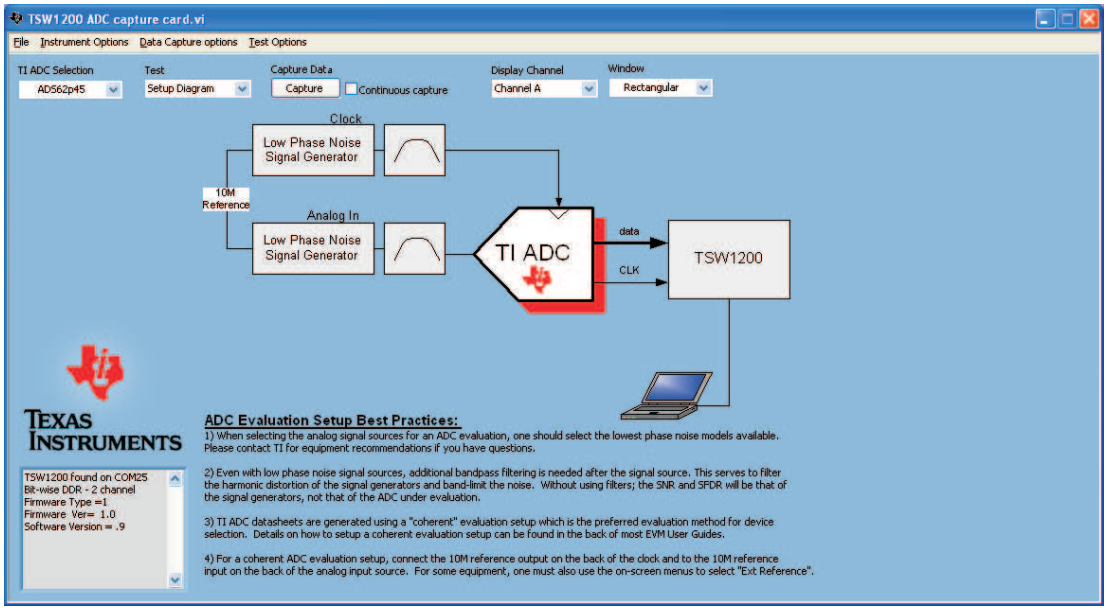


Figure 10. User Interface Initial Setup Screen

5.1 Toolbar

The toolbar contains options and settings that are independent of the device selected for test or the test to be performed, such as configuration options and save/recall operations. The operations available under the toolbar are grouped in categories of File, Instrument Options, Data Capture Options, and Test Options

5.1.1 File Options

Instrument Options contains all of the options for saving or importing test results and saving or recalling the setup of the TSW1200 User Interface software.

The Save Capture operation can save the results that are displayed in the test window for export or archival purposes. If the Single Tone FFT test is active, then the FFT plot is be saved, along with the performance statistics and setup information. If the Time Domain test is active, then the Time Domain plot is saved along with the time domain statistics. The saved data plot can be saved in jpeg, png, or bmp format.

The captured data from the ADC under test also can be saved to a file, or previously saved data can be imported back into the TSW1200 software and re-displayed in the Single-tone FFT or Time Domain windows. Data can be saved in the format of binary, comma separated format, or both.

5.1.2 Instrument Options

The Instrument Options menu tab contains two options: Reinitialize Instrument and Read ADC EVM Setup Procedure.

The Reinitialize Instrument option causes the TSW1200 software to reset itself to initial conditions and to read the firmware settings from the TSW1200EVM again. The firmware and software revisions then are displayed in the status window. This command is useful for cases where the jumper settings on the TSW1200EVM may have changed since the TSW1200 software was opened, or in cases where the USB connection to the PC has been dropped and the COM port must be reopened.

The Read ADC EVM Setup Procedure command causes the TSW1200 software to read a comment string from the ini file for the ADC that is currently selected and then display that comment string in the status pane. This comment string generally contains necessary setup information pertaining to the ADC EVM, such as possibly requiring a non-default data format or required jumper setting for the EVM to communicate properly with the TSW1200EVM.

5.1.3 Data Capture Options

The Data Capture menu tab contains two options: Capture Options and UART Baud Rate.

Capture Options allows for continuous capture that can be checked or unchecked. Continuous capture causes the capture button to continuously capture, process, and display test data. Once the results are displayed, the capture process automatically begins again at the desired capture interval The default capture interval is zero, which means that the next capture is started once the current results are displayed. The capture interval can be set in seconds to make the continuous capture less frequent.

The UART baud rate can be set to one of four data rates. This controls the data rate of unloading the FIFO capture from the TSW1200EVM FPGA to the USB port. The UART baud rate is the limiting factor for the time it takes to capture long record lengths of data. The UART data rate is commonly set to 460800, as 921600 is not recommended for reliable data transfer.

5.1.4 Test Options

The Test Options menu tab allows for setting the parameter options for the Single Tone FFT test and the Time Domain test. Later revisions of the TSW1200 software will allow for setting test parameters for a Dual Tone FFT test and the ACPR test.

For a Single Tone FFT test, the RMS line may be enabled or disabled. When enabled, a horizontal marker is displayed over the FFT plot to indicate the RMS average of the noise floor of the FFT plot. The RMS average is computed over all of the FFT bins except the bin containing the input frequency. More precisely, the RMS line = SINAD + FFT Record Length Process Gain where FFT Record Process Gain = 10log(number of points/2).

SNR, SFDR, and SINAD can be expressed in either dBc or dBFS as selected by the dBFS selection under the Single Tone FFT options.

By default, the noise calculations for SNR and SINAD do not include the five FFT bins around the expected input frequency or the first five FFT bins at DC. The rest of the FFT bins out to the Nyquist frequency are included in the calculation of the total noise. Vertical marker cursors are present in the FFT display that indicate the beginning and the end of the bandwidth of interest for noise calculations. Because these vertical markers are located at the extreme left-most and right-most positions on the FFT display, these vertical markers often are not noticeable. It is possible to compute the total noise power over a narrower range than the default DC through Nyquist band of frequencies. An integration band for the noise calculations can be set in two ways. First, the mouse can be used to click on one of the vertical cursors and drag it to a new desired location. Second, the Cursor Band Location window under the Single Tone FFT Test Option in the tool bar can be used to set a new frequency band of integration for the calculation of the total noise power.

Also excluded from calculation of the SNR is the power in the first five harmonics of the input frequency. These first five harmonics are included in calculation of SINAD (signal to noise and distortion) and thus this is the principal difference between SNR and SINAD. (SINAD is sometimes called SNDR, signal to noise and distortion ratio.) The number of harmonics to exclude from SNR can be set to a value other than the default 5 in the Number of Harmonics window in the Single Tone FFT Test Option in the toolbar.

5.2 Status Window

The lower left portion of the TSW1200 user interface software window under the TI logo is reserved for reporting status, warnings, errors, and informational output. When the TSW1200 software is first run, it queries the TSW1200EVM and displays the revision of the FPGA firmware and the type of ADC interface the TSW1200EVM is expecting to see based on jumper settings J10 and J11. At any time, this initial information can be displayed again by selecting the Reinitialize Instrument option in the Instrument Options tab of the toolbar.

During operation of the TS1200 software, warnings may appear in the status window if selections made from the drop-down menus of the interface are incompatible with the hardware selections or settings. If an ADC selection is made that is not supported by the TSW1200EVM jumper settings of J10 and J11, then a message in the status window prompts the user for a different device selection or to set the jumpers to the proper position on the hardware. If a sample rate is entered that is faster than that supported by a particular ADC data sheet, then a warning is displayed in the status window.

5.3 Device Specific Selections

Drop-down menus that are specific to a particular ADC device selection are located along the top of the display under the toolbar.

The first selection a user makes is to select a type of ADC device from the device selection drop-down menu. Each ADC that has an ini file installed in the proper directory automatically has an entry in the device selection drop-down menu.

Once an ADC device part number is selected, the ADC Channel can be selected in the Channel selection drop-down menu. The proper number of channel selections are made available based on the ADC device selection.

The format for display of the captured data is chosen in the Test Selection drop-down menu. Single Tone FFT displays the power spectrum of the captured data with calculated AC performance statistics. Time Domain displays the raw captured data in the format of a logic analyzer display and output level over time.

In the Window Display drop-down menu, the user chooses a windowing function to be applied to the captured data. Rectangular Window applies a unity gain to all data points of the captured data. A Hanning Window, Hamming Window, or Blackman-Harris Window function can be applied to the captured data for situations where the sample rate and the input frequency are not or cannot be set precisely to capture an integer number of cycles of the input frequency (sometimes called coherent frequency).

The Capture button initiates a data capture once all other selections are made. The data capture can be a single capture and display, or a continuous repeating capture.

5.4 Single Tone FET

The Single Tone FFT test is shown in Figure 11. The larger central pane displays the FFT power spectrum, whereas the calculated statistics are grouped into categories on the right of the screen. Settings and inputs relevant to the test are entered in drop-down menus or text input boxes on the left portion of the window.

5.4.1 Parameter Controls

The sampling rate is entered in the ADC Sampling Rate text box, also called the Sampling Frequency FS. The number is entered in Hertz (Hz), although the letter M may be appended to represent the sampling rate in MHz. For example, 125M = 125 MHz or 125,000,000 Hz.

The expected input frequency is entered in the ADC Input Frequency input box, also known as FC. If the Auto Calculation of Coherent Input Frequency mode is enabled, then this input frequency is adjusted up or down slightly away from the input frequency automatically. If coherent input frequency is required, the signal generator used to source the input frequency must be set to this exact calculated coherent frequency. The coherent frequency calculation takes the sampling frequency, the input frequency as entered by the user, and the FFT record length and adjusts the input frequency so that the captured data starts and ends on the same place of the sine wave of the input frequency. This avoids an artifact of the

FFT calculation from presenting a *smeared* power spectrum due to the fact that the FFT presumes the sample of the input is part of a continuous input signal. If the input and sampling frequency is not coherent, and the sampled data is appended end to end to form a continuous input signal, then there is an apparent phase discontinuity at the beginning and the end of the sampled data. Making the sampling and input frequencies coherent avoids this apparent discontinuity. If the input frequency cannot be made coherent, then the windowing functions other than Rectangular can be used to process out this effect to some degree.

The FFT record length can be set in the FFT Record Length (NS) input text box. The TSW1200EVM supports FFT record lengths of as much as 65536 samples, or as little as 4096 samples.

5.4.2 FFT Power Spectrum

The FFT power spectrum of the captured data is displayed in the major center portion of the window. The TSW1200 software automatically scales the horizontal axis from DC through the Nyquist frequency, although the scale of the horizontal axis can be changed simply by highlighting the text and typing in a new value. For example, the display in Figure 11 can be used to zoom in on the input frequency by highlighting the 0MHz and typing 25M, and then highlighting the 62.5M and typing in 35M. This causes the portion of the power spectrum from 25 MHz through 35 MHz to fill the power spectrum display.

The vertical scale of the power spectrum is automatically scaled to display the noise floor of the FFT result up through 0 dBFS. The vertical scale can also be manually adjusted by highlighting the limits of the vertical scale and typing in new limits.

By default, the first few harmonics of the input frequency are marked in the display, as well as an additional marker that can be placed by dragging the marker to any place in the power spectrum, such as a noise spur that is not already marked as a harmonic. By default this additional marker initially goes to the highest spur that is not identified as a harmonic.

Display properties can be edited by using the mouse to right-click in the power spectrum display. Visible properties such as the graph palette or plot legend can be edited, and auto-scale of the vertical and horizontal axises can be enabled or not.

5.4.3 Single FFT Statistics

For the Single FFT test, a number of calculated statistics and AC performance measurements are displayed to the right of the power spectrum display, grouped into several categories.

AC

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) or input frequency to the noise floor power (P_N), excluding the power at DC and the first five harmonics. SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

$$SNR = 10Log\ 10\ \frac{P_S}{P_N} \quad (1)$$

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding DC.

$$SINAD = 10Log\ 10\ \frac{P_S}{P_N + P_D} \quad (2)$$

Spurious-Free Dynamic Range (SFDR) – SFDR is ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

SFDR w/o 2,3 – Spurious-Free Dynamic Range without the second or third harmonic. Commonly the largest spectral components after the fundamental are the second and third harmonics of the input frequency, and commonly the input frequency can contain significant power in the second and third harmonics. SFDR w/o 2,3 reports the SFDR with these two harmonics ignored.

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power in the first five harmonics (P_D). THD is typically given in data sheets in units of dBc (dB to carrier).

$$THD = 10Log\ 10\ \frac{P_S}{P_D} \quad (3)$$

Effective Number of Bits (ENOB) – The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (4)$$

Time Domain
Several of the statistics of the Time Domain test are repeated here, particularly the minimum and maximum sample values in the FFT record length, as well as the mean and standard deviation of the sample values

Signal
The frequency of the expected input signal is reported, as well as the power level of the signal in either dBc or dBFS. The amplitude of the input frequency for typical data sheet measurements is commonly set externally to be about 1 dB below Full Scale, or –1 dBFS.

Distortion
The power values for the second, third, fourth, and fifth harmonics of the input frequency and the user-selectable marker are displayed in either dBFS or dBc.

Test setup
Input parameters relevant to the test are repeated, particularly FFT record length, sample rate, and the end points of the bandwidth of integration for noise calculations. The lower end point for the bandwidth of integration is normally not zero because the first few FFT bins are not included to remove any DC biasing component of the signal.

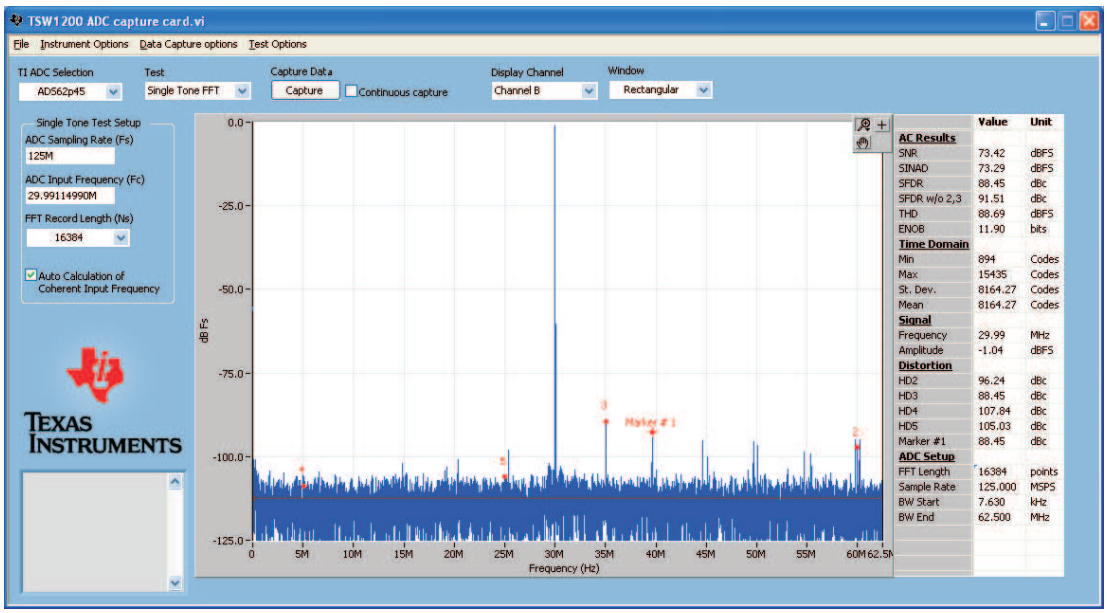


Figure 11. User Interface Single FFT format

5.5 Time Domain

The Time Domain test is shown in Figure 12. The larger central pane displays the raw sampled data whereas the calculated statistics are grouped into categories on the right of the screen. Settings and inputs relevant to the test are entered in drop-down menus or text input boxes on the left portion of the window.

5.5.1 Input Parameters

The sampling rate is entered in the ADC Sampling Rate text box, also called the Sampling Frequency FS. If this number was entered in the Single FFT test then it is carried over to this test.

The expected input frequency is entered in the ADC Input Frequency input box, although the auto-calculation of coherent frequency does not occur in this test. If auto-calculation of coherent frequency is required, it must be entered in the Single Tone FFT test and then the Time Domain test must be selected. When done in this order, the coherent input frequency is carried over to the Time Domain test.

The FFT record length can be set in the FFT Record Length (NS) input text box. The TSW1200EVM supports FFT record lengths of as much as 65536 samples, or as little as 4096 samples.

The Overlay Unwrap Waveform check box allows a calculated normalized waveform to be overlaid over the sample data. If the sample and input frequencies are coherent, the sampled data is normalized into a calculated representation of a single period of a sine wave. Errors in the sampled data for any reason become immediately apparent as spikes on the unwrapped waveform.

5.5.2 Results

The captured sample data is displayed in two formats in the Time Domain results window. In the upper half of the window, the arithmetic value of the sample is represented on the vertical scale. In the lower half of the window the individual bits of the data are displayed as if it were captured by a logic analyzer. If Unwrap Waveform is enabled, the normalized calculation of one period of a sine wave is overlaid over the time domain data in the upper half of the display.

The Time Domain display automatically scales the horizontal display to represent the full data capture to the amount specified by the FFT Record Length. The horizontal scale may be manually adjusted by highlighting the minimum and maximum sample limits and typing in new scale limits.

The Time Domain display automatically scales the vertical display according the bit resolution of the selected ADC. For example, for a 14-bit ADC such as the ADS62P45, the vertical scale is represented as values from 0 through 16000. The logic-analyzer-style display shows 16 bits of data, of which only 14 bits are shown to toggle for a 14-bit ADC. The vertical scale can also be adjusted manually by highlighting limits of the scale and typing in new limits.

5.5.3 Time Domain Statistics

For the Time Domain test, sample statistics are displayed on the right of the display. The minimum and maximum sample values are displayed, as is the median sample and the mean, standard deviation, and RMS value of the samples.

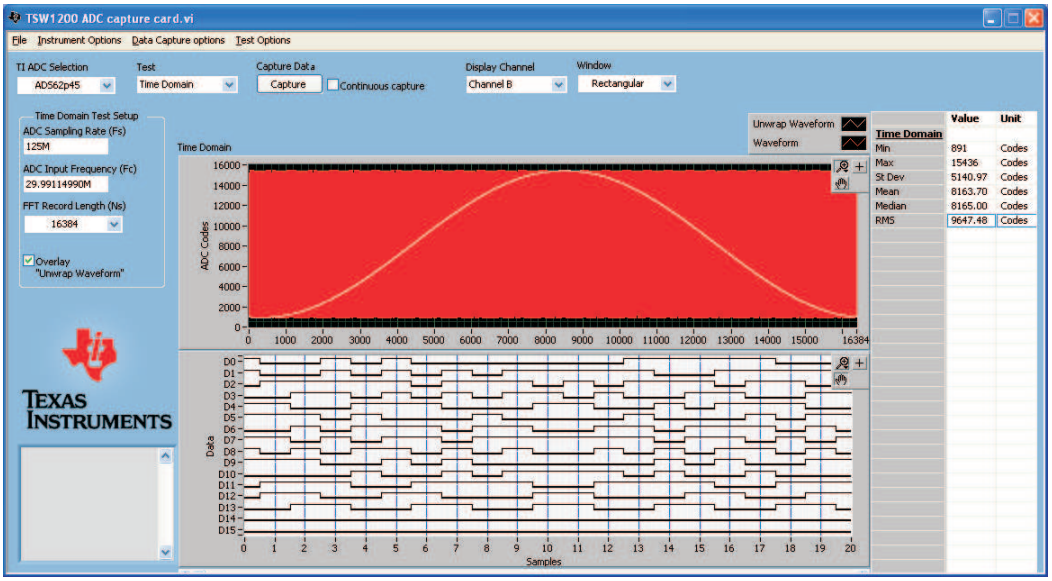


Figure 12. User Interface Time Domain Format

5.6 Future Revisions

Two additional test windows are expected to be supported by a future revision of the TSW1200 user interface software: two-tone FFT and ACPR. The two-Tone FFT allows for the specification of two input frequencies, and the Inter-Modulation Distortion (IMD) components of 2×F1 – F2 and 2×F2 – F1 are identified and displayed. Adjacent Channel Power Ratio (ACPR) is used for more complex input frequencies than for just single or two tones. For ACPR, an input bandwidth for a complex signal is defined, and then the ACPR takes the place of SNR by presenting the ratio of the power in the defined signal bandwidth to the total power outside of that bandwidth.

6 MATLAB™ Interface

The standard TSW1200 user interface software that is installed with the Installation CD uses a supplied National Instruments LabVIEW™ run-time engine. This user interface uses drivers to open a com port to a USB port to communicate with the TSW1200EVM. This communication takes the form of a register-mapped series of register writes and reads of the TSW1200 hardware. It is possible to communicate with the TSW1200 hardware with other software than the supplied TSW1200 user interface as long as this other software can open a com port to the USB channel and can perform the register reads and writes to the TSW1200 hardware. One common request for another user interface is MATLAB, as the user might then want to use their own MATLAB routines to process the data record captured by the TSW1200EVM FIFOs.

Included on the Installation CD for the TSW1200EVM is a directory of files for an alternative MATLAB interface to the TSW1200EVM. This MATLAB code is a functional starting point for communicating with the TSW1200 hardware and capturing data from a number of TI ADCs. This MATLAB code can be integrated into a larger portion of MATLAB code of the customer's own design, or the supplied MATLAB code can be taken as a starting point for a new development. Currently, the supplied MATLAB code supports data capture from several families of TI data converters: the ADS5481 through ADS5485, the ADS6129 and ADS6149, and the ADS62P41 through ADS62P45 and ADS62P21 through ADS62P25.

To use the MATLAB interface, TI recommends that users install the TSW1200 user interface software using the setup.exe command on the Installation CD. This installs the USB drivers that are needed for the VCP (Virtual Com Port) so that the PC recognizes the TSW1200 hardware when the USB cable is plugged in. The MATLAB interface then is able to open the com port to the TSW1200EVM.

7 Schematics and Bill of Materials

7.1 Schematics

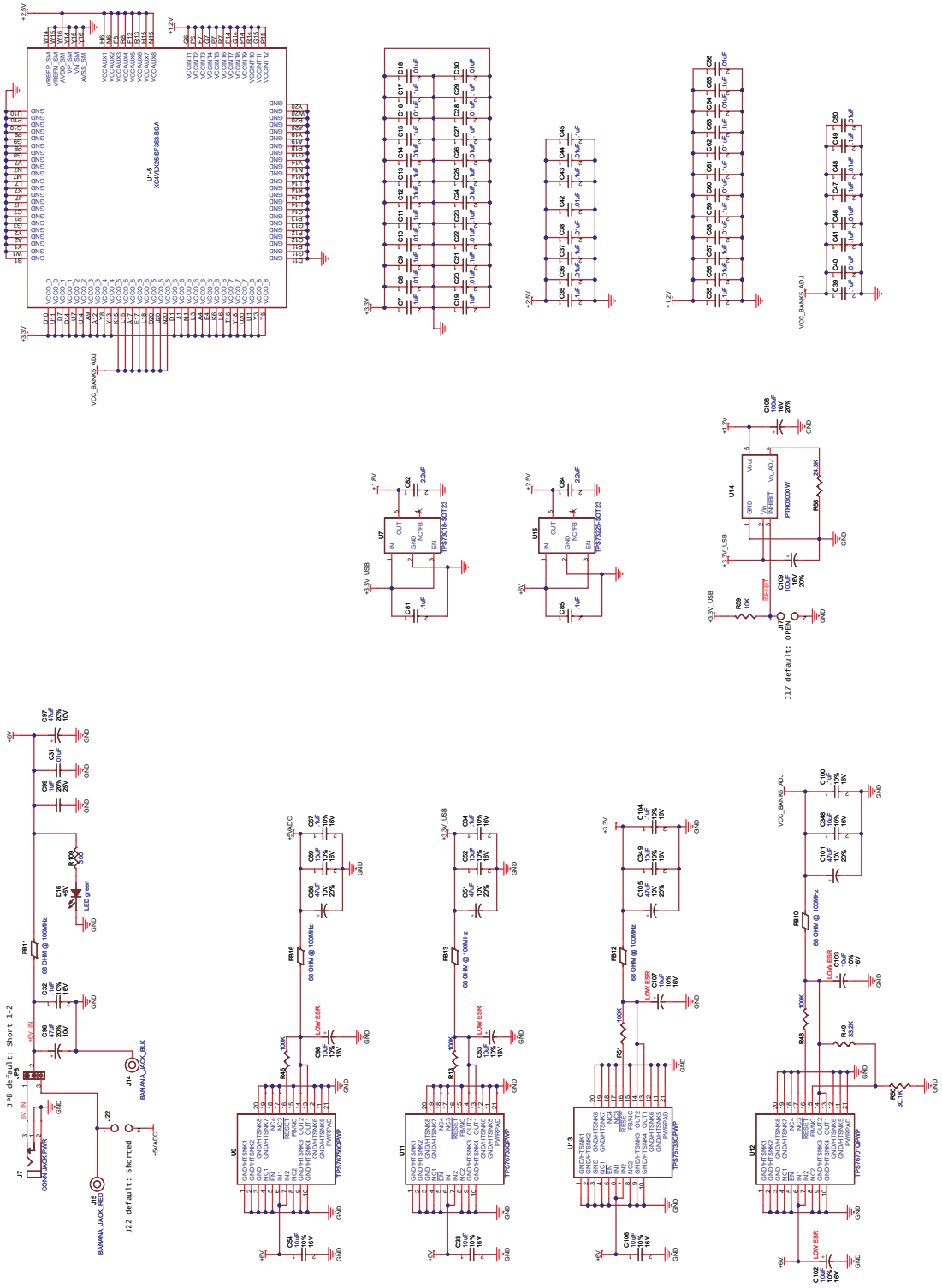


Figure 13. Schematic Diagram Page 1

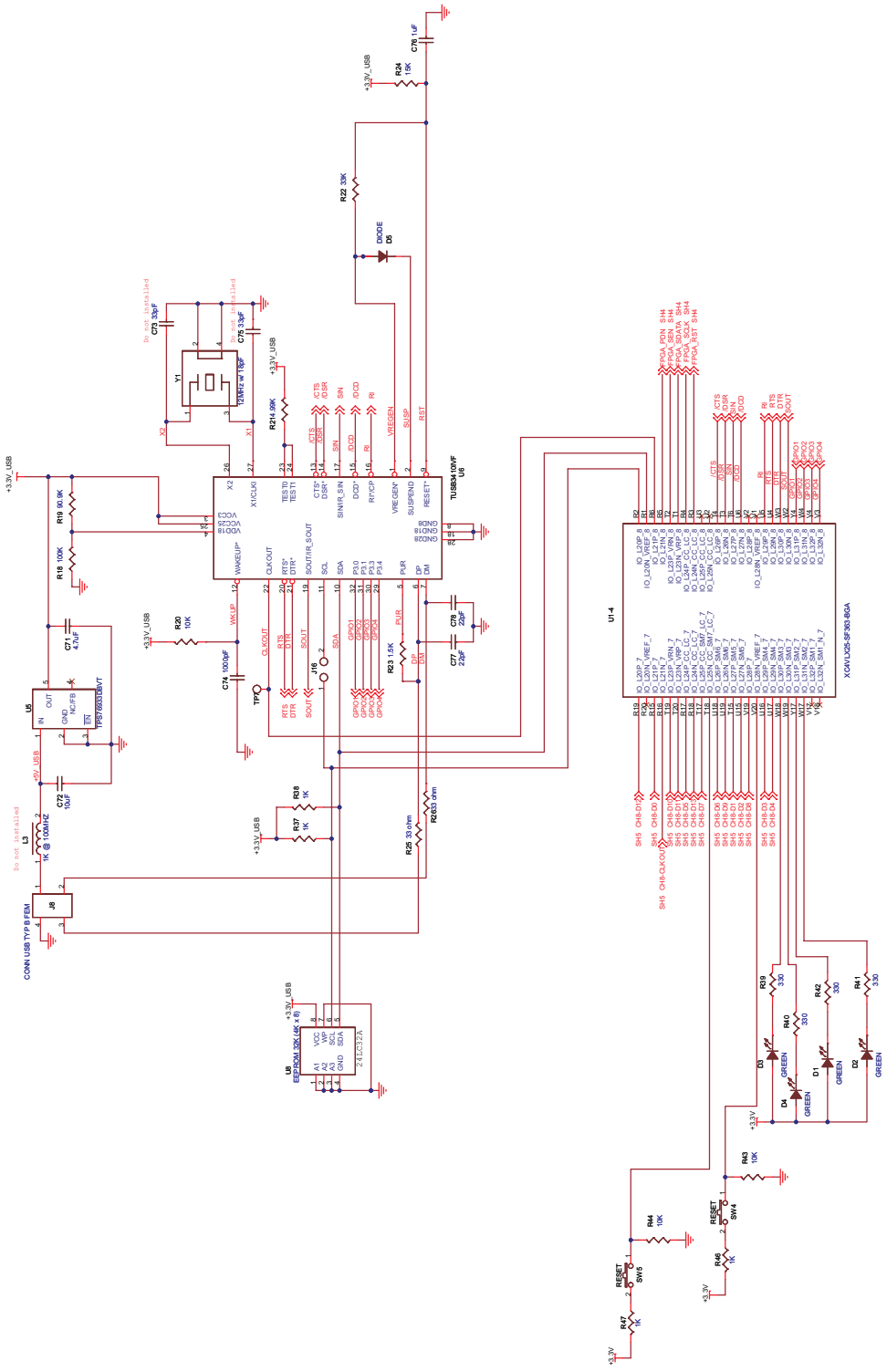


Figure 14. Schematic Diagram Page 2

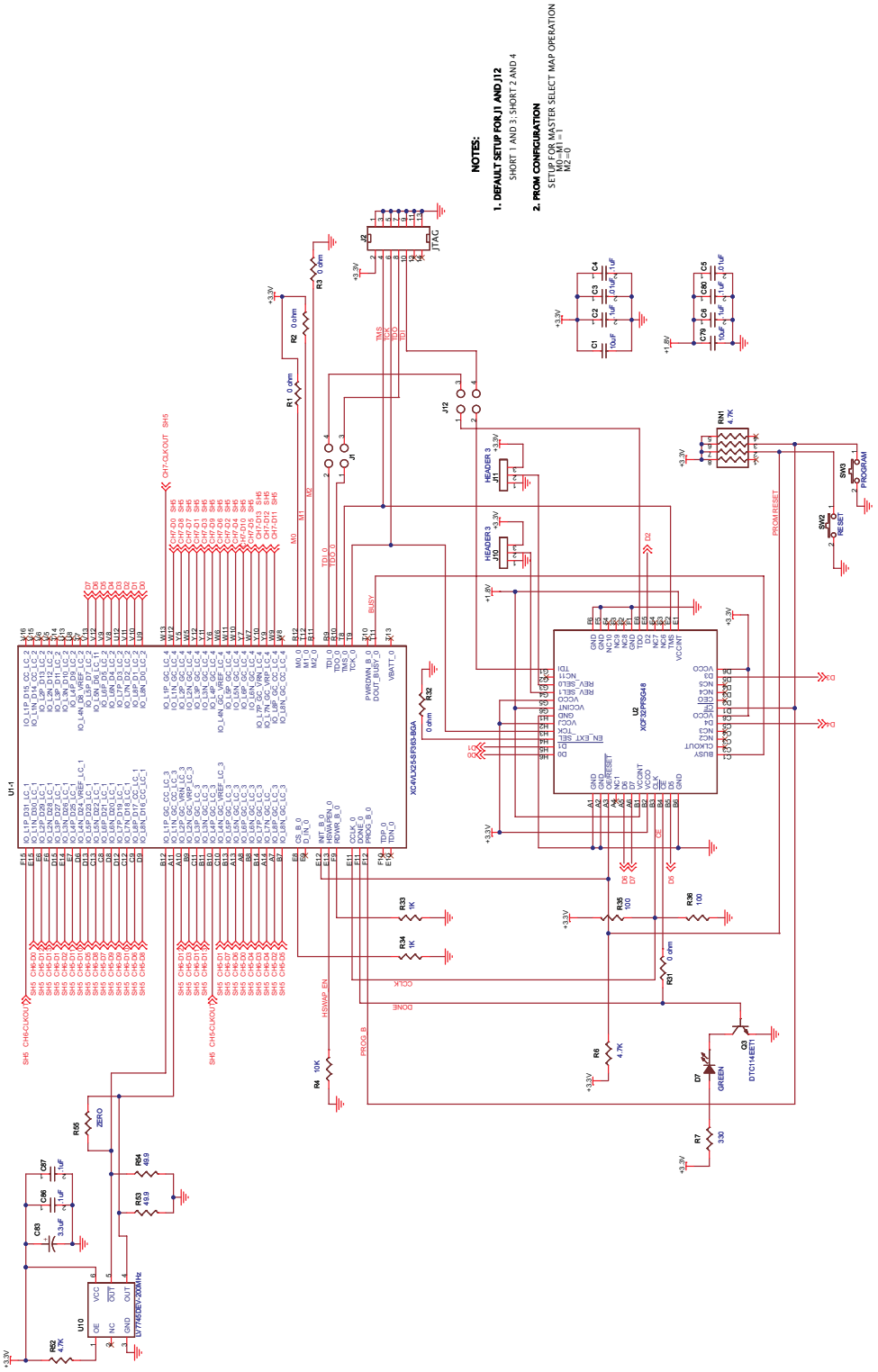


Figure 15. Schematic Diagram Page 3

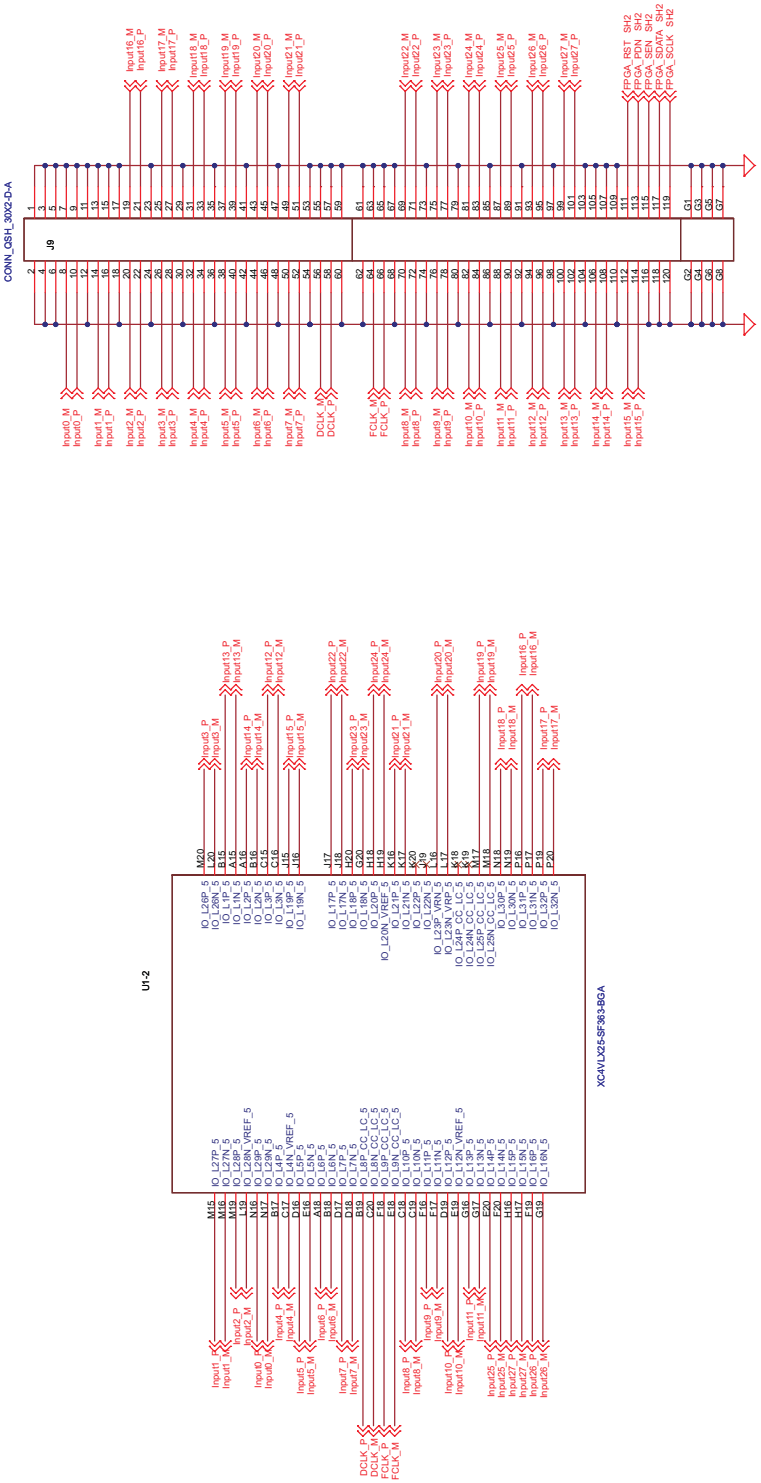


Figure 16. Schematic Diagram Page 4

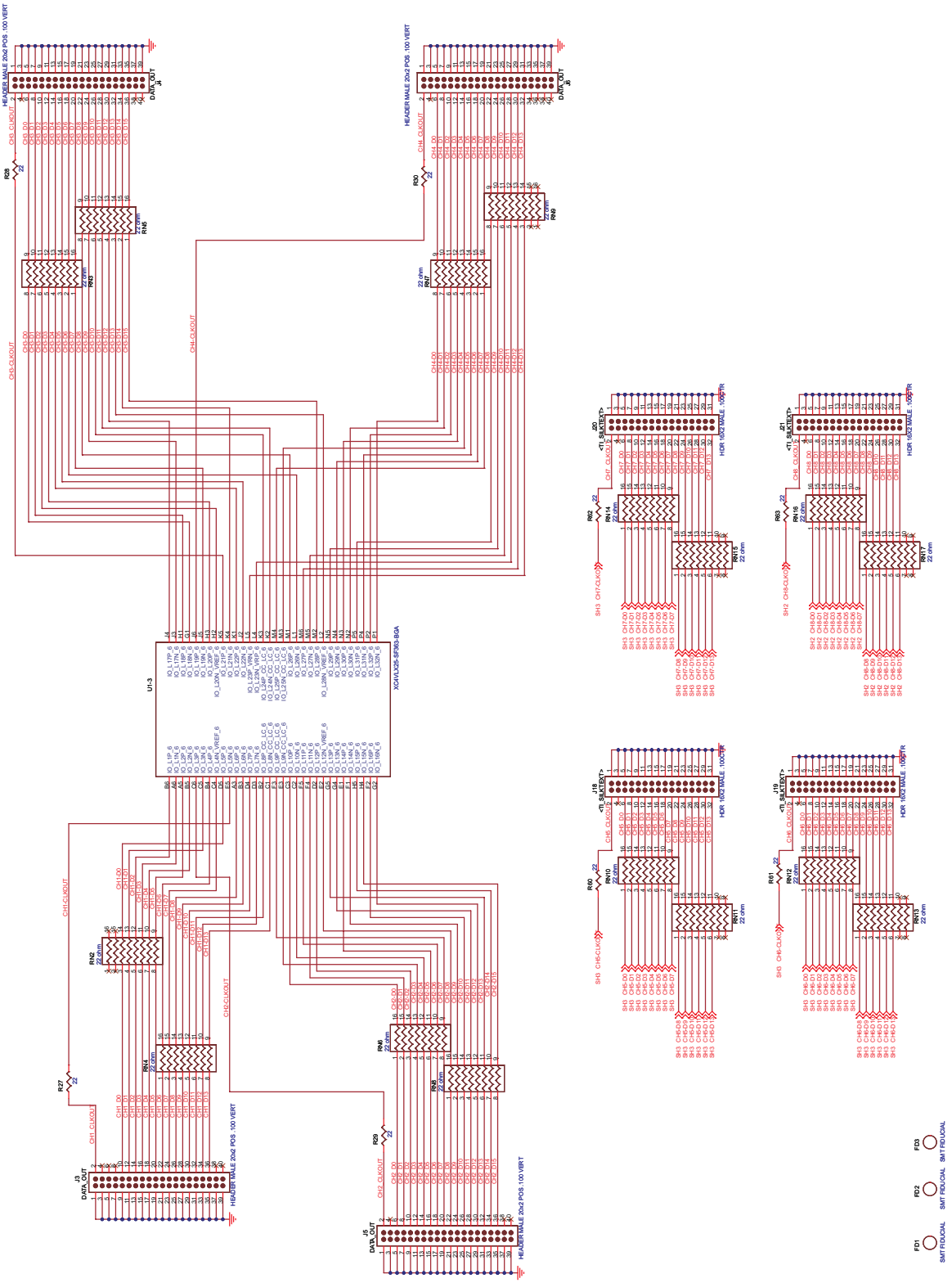


Figure 17. Schematic Diagram Page 5

7.2 Bill of Materials

Table 1. Bill of Materials

QTY	Reference	Not Installed	Part	Foot Print	Part Number	Manufacturer	Tol	Volt	Wat
3	C1,C72,C79		10 µF	603	ECJ-1VB0J106M	Panasonic	20%	6.3V	
4	C2,C4,C6,C80		0.1 µF	603	GRM188R71H104KA93D	Murata	5%	50V	
2	C3,C5		0.01 µF	603	C0603C103K5RACTU	Kemet	10%	50V	
26	C7,C9,C11,C13, C15,C17,C19,C 21,C23,C25,C2 7,C29,C35,C37, C39,C41,C43,C 45,C47,C49,C5 5,C57,C59,C61, C63,C65		0.1 µF	201	ECJ-ZEBFJ104K	Panasonic	5%	50V	
26	C8,C10,C12,C1 4,C16,C18,C20, C22,C24,C26,C 28,C30,C36,C3 8,C40,C42,C44, C46,C48,C50,C 56,C58,C60,C6 2,C64,C66		0.01 µF	201	ECJ-ZEB1A103K	Panasonic	5%	50V	
1	C31		0.01 µF	402	ECJ-0EB1E103K	Panasonic	10%	25V	
1	C32		0.1 µF	402	ECJ-0EB1C104K	Panasonic	10%	16V	
11	C33,C52,C53,C 89,C98,C102,C 103,C106,C107, C348,C349		10uF	1206	Panasonic ECJ-3YB1C106K		10%	16V	
4	C34,C67,C100, C104		0.1 µF	402	Panasonic ECJ-0EB1C104K		10%	16V	
5	C51,C88,C96,C 101,C105		47 µF	tant_b	Kemet T494B476M010AS		20%	10V	
1	C54		10 µF	1206	ECJ-3YB1C106K	Panasonic	10%	16V	
1	C71		4.7 µF	603	GRM188F51A475ZE20D	Murata	0.6	10V	
0	C73,C75	Not Installed	33 pF	603	GRM1885C2A330JA01D	Murata	5%	100V	
1	C74		1000 pF	603	ECJ-1VB1H102K	Panasonic	10%	50V	
1	C76		1 µF	603	ECJ-1VB1A105K	Panasonic	10%	10V	
2	C77,C78		22 pF	603	GRM1885C2A220JA01D	Murata	5%	100V	
2	C81,C85		0.1 µF	603	ECJ-1VB1H104K	Panasonic	10%	50V	
2	C82,C84		2.2 µF	603	ECJ-1VB1A225K	Panasonic	10%	10V	
1	C83		3.3 µF	TANT_B	TAJB335K016R	AVX	10%	16V	
2	C86,C87		0.1 µF	603	GRM188R71H104KA93D	Murata	10%	50V	
1	C97		47 µF	tant_b	T494B476M010AS	Kemet	20%	10V	
1	C99		1 µF	603	ECJ-1V41E105M	Panasonic	20%	25V	
2	C108,C109		100 µF	smd_cap_elec_TCE	EEE-TG1C101P	Panasonic	20%	16V	
5	D1–D4, D7		Green	diode_0805	DC1112H-TR	Stanley			
1	D5		Diode	SOT23_DIODE	BAS21TA	Zetec Inc.			
1	D16		LED green	LED_0805	LNJ306G5UUX	Panasonic			
5	FB10–FB13, FB16		68 Ω at 100 MHz	1206	EXC-ML32A680U	Panasonic			
1	JP8		Header 3 POS 0.1 CTR	JUMPER3	HTSW-103-07-F-S	Samtec	Short pins 1-2 with shunt connector DigiKey # S9000-ND		
2	J1,J12		Header 2X2	hdr2X2_100ctr_alt	90131-0122	Molex	Short pins with shunt connector DigiKey # S9000-ND (as shown on silkscreen)		
1	J2		CONN 7x2	CON_2X7_2mm_M	87831-1420	Molex			
4	J3–6		Header male 20x2 POS 0.100 VERT	CON20X2_100ctr_M_tsw1100_mate	HTSW-120-07-L-D	Samtec			
1	J7		CONN JACK PWR	PWRJACK	RAPC722	Switchcraft			
1	J8		CONN USB TYP B FEM	conn_usb_typb_fem	897-43-004-90-000	Milmax			
1	J9		CONN_QSH_30X2-D-A	conn_QSH_30X2-D-A	QSH-060-01-F-D-A	Samtec			
2	J10, J11		Header 3	jumper3	22-28-4030	Molex	Short pins 1-2 with shunt connector DigiKey # S9000-ND		

Table 1. Bill of Materials (continued)

QTY	Reference	Not Installed	Part	Foot Print	Part Number	Manufacturer	Tol	Volt	Wat
1	J14		BANANA_JACK_BLK	banana_jack	ST-351B BLK	Alectron Connectors			
1	J15		BANANA_JACK_RED	banana_jack	ST-351B RED	Alectron Connectors			
2	J16,J22		Header 2	JUMPER2	22-28-4020	Molex	Short pins with shunt connector DigiKey # S9000-ND		
1	J17		Header 2	JUMPER2	22-28-4020	Molex			
4	J18–J21		HDR 16X2 MALE 0.100CTR	CON16X2_100ctr_M_alt	TSW-116-07-L-D	SAMTEC			
0	L3	Not Installed	1K at 100 MHz	smd_0805	BLM21AG102SN1D	Murata			
1	Q3		DTC114EET1	sc75	DTC114EET1	On Semi			
1	RN1		4.7K	RNET4_8_0603	EXB-V8V472JV	Panasonic	5%		
16	RN2–RN17		22 Ω	rnet8_16_0603	742C163220JTR	CTS	5%		0.063W
5	R1–R3,R31,R32		0 Ω	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
5	R4,R20,R43,R44,R59		10K	603	ERJ-3EKF1002V	Panasonic	1%		1/10W
1	R6		4.7K	603	ERJ-3GEYJ472V	Panasonic	5%		1/10W
5	R7,R39, R40–R42		330	603	RC0603FR-07330RL	Yageo			
3	R13,R48,R51		100K	603	ERJ-3EKF1003V	Panasonic	1%		1/10W
1	R18		100K	603	ERJ-3EKF1003V	Panasonic	1%		1/10W
1	R19		90.9K	603	ERJ-3EKF9092V	Panasonic	1%		1/10W
1	R21		4.99K	603	ERJ-3EKF4991V	Panasonic	1%		1/10W
1	R22		33K	603	RC0603FR-0733KL	Yageo	1%		1/10W
1	R23		1.5K	603	ERJ-3EKF1501V	Panasonic	1%		1/10W
1	R24		15K	603	ERJ-3EKF1502V	Panasonic	1%		1/10W
2	R25,R26		33 Ω	603	RC0603FR-0733RL	Yageo	1%		1/10W
8	R27–R30, R60–R63		22	603	RC0603FR-0722RL	Yageo	1%		1/10W
6	R33,R34,R37,R38,R46,R47		1K	603	ERJ-3EKF1001V	Panasonic	1%		1/10W
2	R35,R36		100	603	ERJ-3EKF1000V	Panasonic	1%		1/10W
1	R45		100K	603	ERJ-3EKF1003V	Panasonic	1%		1/10W
1	R49		33.2K	603	ERJ-3EKF3322V	Panasonic	1%		1/10W
1	R50		30.1K	603	ERJ-3EKF3012V	Panasonic	1%		1/10W
1	R52		4.7K	603	ERA-V15J472V	Panasonic	5%		1/16W
2	R53,R54		49.9	603	ERJ-3EKF49R9V	Panasonic	1%		1/10W
0	R55	Not Installed	Zero	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
1	R58		24.3K	603	ERJ-3EKF2432V	Panasonic	1%		1/10W
1	R109		300	603	ERJ-3EKF3000V	Panasonic			
1	SW2		Reset	SW_RESET_PTS635	PTS635SL43	ITT Industries/C&K Div			
3	SW3,SW4,SW5		Program	SW_RESET_PTS635	PTS635SL43	ITT Industries/C&K Div			
1	TP7		T POINT R	testpoint	5002	Keystone			
1	U1		XC4VLX25-SF363-BGA	MBGA_PT8MM_363	XC4VLX25-SF363-BGA -11C	Xilinx			TI Provide
1	U2		XCF32P/FSG48	MBGA_FS48_PT8MM	XCF32PFSG48	Xilinx			TI Provide
1	U5		TPS76933DBVT	dbv5	TPS76933DBVT	TI			TI Provide
1	U6A		TUSB3410IVF	pqfp32	TUSB3410IVF	TI			TI Provide
1	U7		TPS73018-SOT23	DBV5	TPS73018DBVT	TI			TI Provide
1	U8		EEPROM 32K (4K x 8)	DIP8_3	24LC32A-I/P	Microchip			
1	XU8		Socket, dip 8	DIP8_3	ED58083-ND	DigiKey			
1	U9		TPS76750QPWP	HTSSOP_20_260x177_26_pwrpad	TPS76750QPWP	TI			TI Provide
1	U10		LV7745DEV-200MHz	SMD_XTAL_7X5MM_6PIN	LV7745DEV-200MHz	Pletronics			
2	U11,U13		TPS76733QPWP	HTSSOP_20_260x177_26_pwrpad	TPS76733QPWP	TI			TI Provide

Table 1. Bill of Materials (continued)

QTY	Reference	Not Installed	Part	Foot Print	Part Number	Manufacturer	Tol	Volt	Wat
1	U12		TPS76701QPWP	HTSSOP_20_260x177_26_pwr pad	TPS76701QPWP	TI			TI Provide
1	U14		PTH03000W	SMD_PWRMOD_EUT5	PTH03000WAS	TI			TI Provide
1	U15		TPS73225-SOT23	DBV5	TPS73225DBVT	TI			TI Provide
1	Y1		12MHz w/ 18pF	smd_xtal_AMB3B	ABM3B-12.000MHZ-10-1-U-T	Abracon			
4			Screw 4-40 X 3/8"		PMS 440 0038 PH	Building Fasteners	PCB legs		
4			Standoff RD 4-40 THR 0.875" ALUM		1846	Keystone			

8 Circuit Board Layout and Layer Stackup

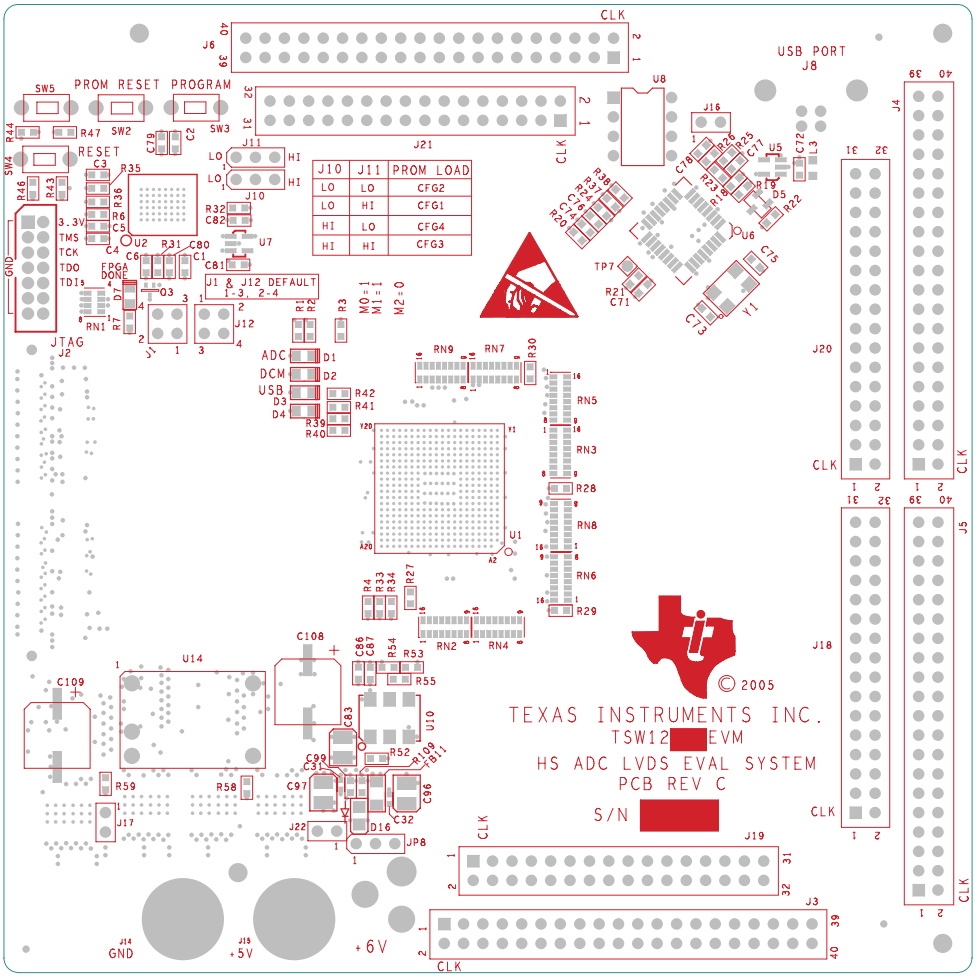


Figure 18. TSW1200C Layout Top Layer

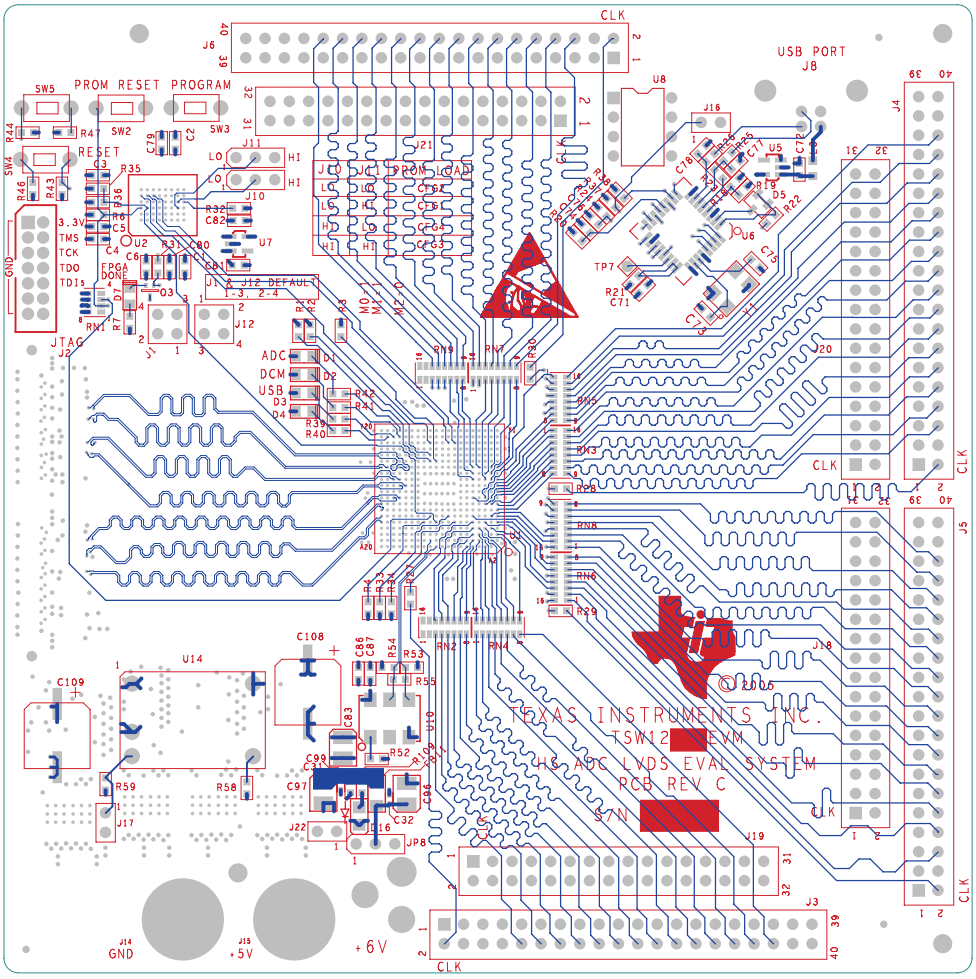


Figure 19. TSW1200C Layout Layer Two

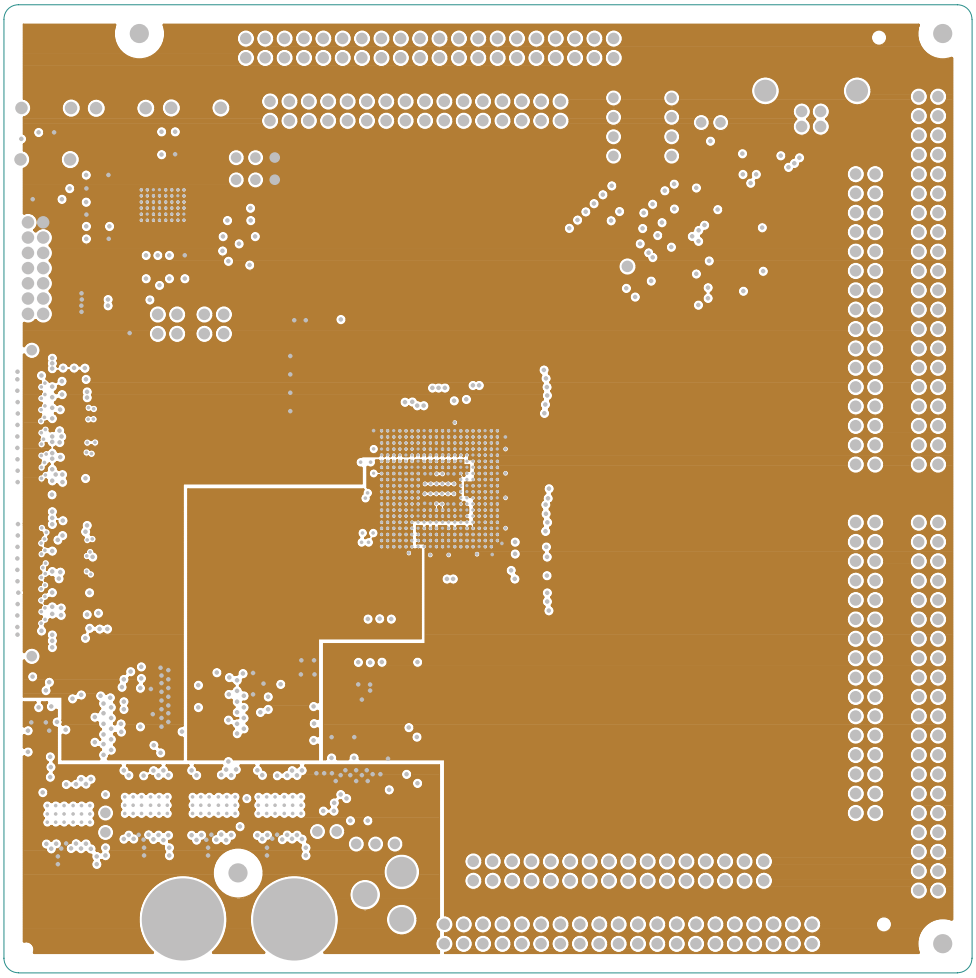


Figure 20. TSW1200C Layout Power Plane

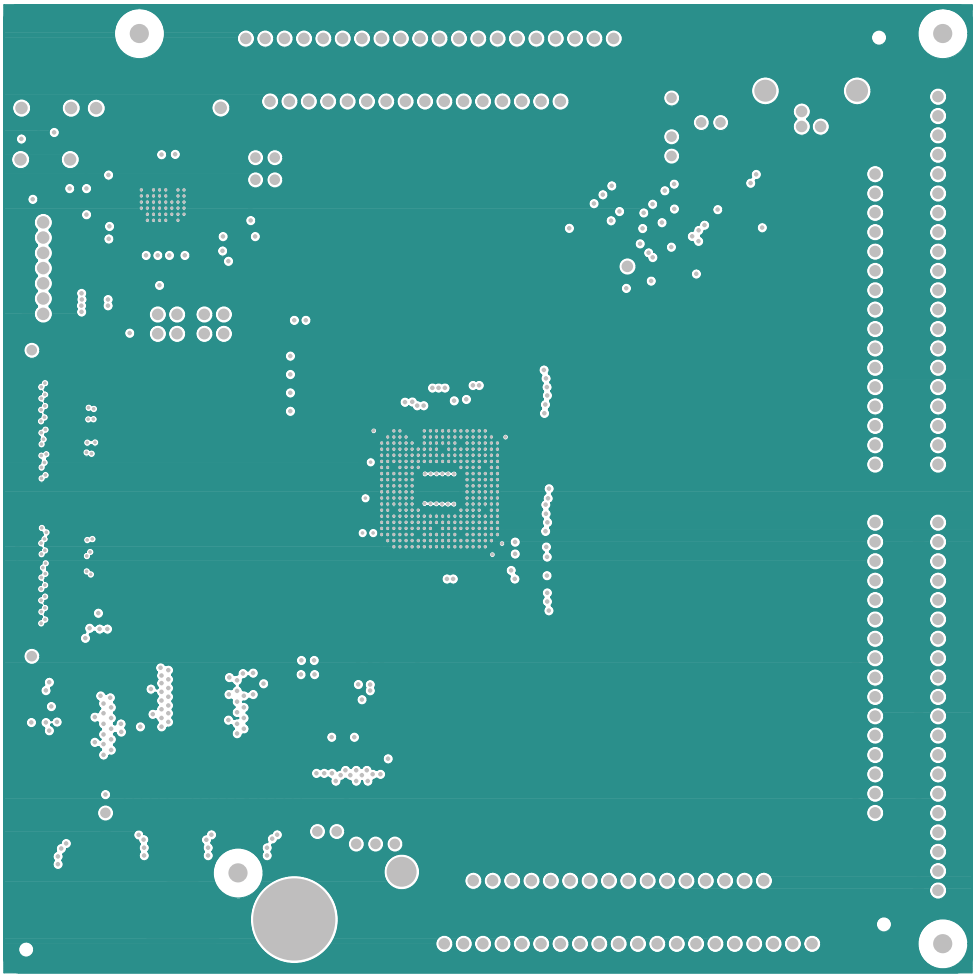


Figure 21. TSW1200C Layout Ground Plane

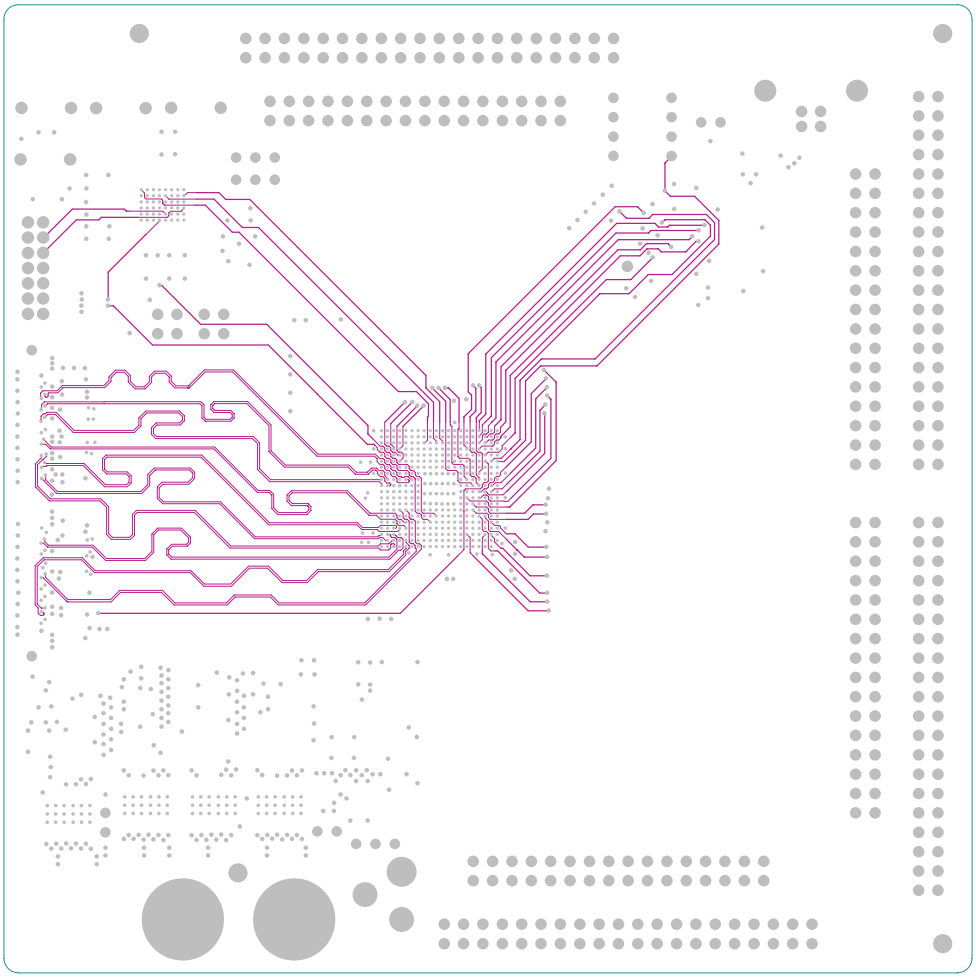


Figure 22. TSW1200C Layout Layer 5

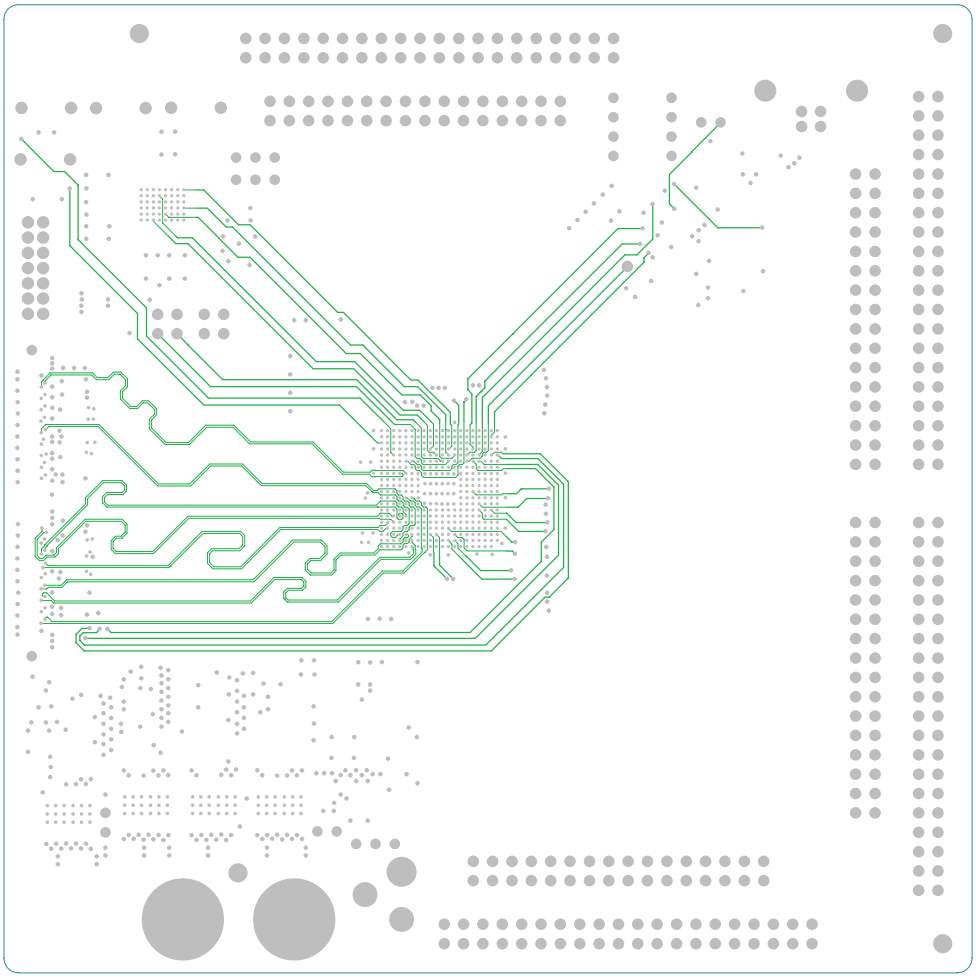


Figure 23. TSW1200C Layer 6

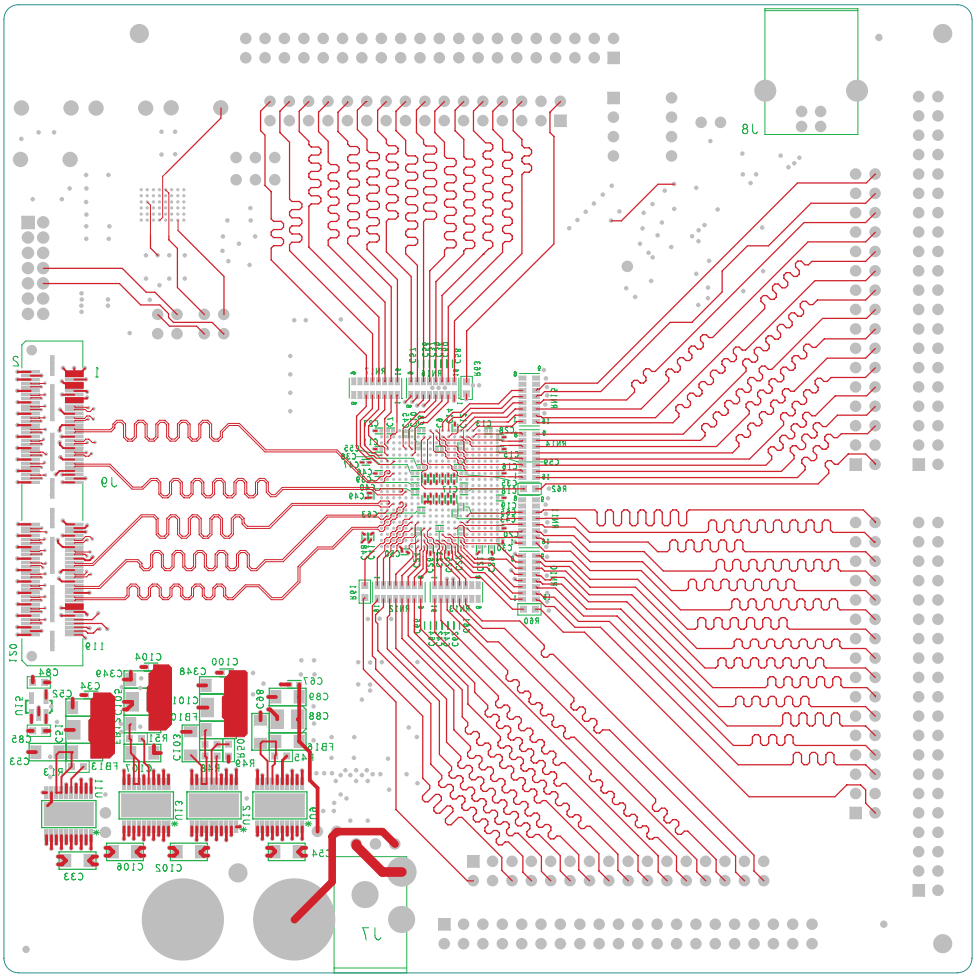
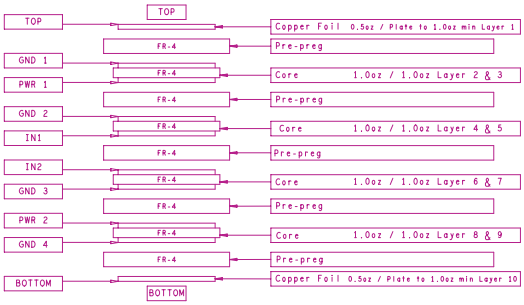
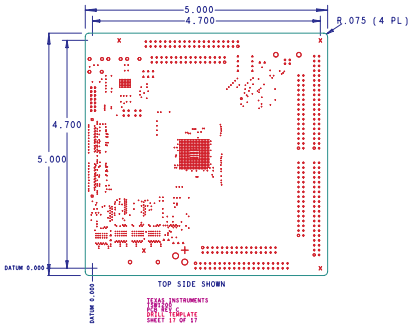


Figure 24. TSW1200C Bottom Layer



UNLESS OTHERWISE SPECIFIED, ALL NOTES ARE APPLICABLE.
NOTES PRECEDED BY AN UNMARKED '☐' ARE NOT APPLICABLE.

1. APPLICATION DESIGN, MANUFACTURING AND INSPECTION DOCUMENTS.
   IPC-2221A & IPC-2222 / DESIGN STANDARD FOR RIGID PRINTED CIRCUIT BOARDS AND RIGID PRINTED BOARD ASSEMBLIES.
   IPC-6012B / QUALIFICATION AND PERFORMANCE SPECIFICATION FOR RIGID PRINTED BOARD.
   IPC-A-600G / ACCEPTABILITY OF PRINTED BOARDS.
2. HOLE SIZE APPLY AFTER PLATING. TOLERANCE TO BE +/-.003.
3. REGISTRATION TOLERANCE: ARTWORK +/-.002
   ALL HOLE CENTERS +/-.005 FROM DIMENSION DATUM.
4. MINIMUM COPPER WALL THICKNESS SHALL BE .001 INCH.
   FOR ALL PLATED THROUGH HOLES, BREAKOUT NOT ALLOWED.
5. PROCESS AND MATERIAL MUST CONFORM TO UL 796. MATERIAL MUST MEET OR EXCEED UL FLAMMABILITY RATING 94V-0.
   MATERIAL: ☐ SINGLE SIDED, ☐ DOUBLE SIDED, ☒ MULTI-LAYER
   COPPER THICKNESS: .062 +/- .006
   BOARD THICKNESS: .062 +/-.006
   NUMBER OF FINISHED LAYERS: 10
6. ☒ MANUFACTURE'S UL MARKING, FLAMMABILITY RATING, ☒ LOGO AND DATE CODE TO BE PLACED IN COPPER ON BOTTOM SIDE OF THE BOARD.
7. SOLDERMASK: LPI, COLOR = GREEN
8. SILKSCREEN ☐ TOP SIDE ☒ BOTH SIDES, USING ☐ YELLOW ☒ WHITE NPI LEADFREE.
   REGISTRATION TOLERANCE TO BE +/-.005.
9. P.C. BOARD TO BE FREE OF DIRT, OIL, FINGER PRINTS, ETC.
10. BOARD WARPAGE: WARP AND TWIST SHALL NOT EXCEED .007 INCH PER INCH MEASURED AT ANY LOCATION OR DIRECTION ON THE BOARD.
11. BOARD MUST BE 100% ELECTRICALLY TESTED TO ENSURE NO SHORTS OR OPEN CIRCUITS.
12. GOLD PLATING (FULL BODY): 5-15 uIN OVER 100-200 NICKEL.
    IMMERSION GOLD.
13. PADS MAY BE TEAR-DROPPED TO MEET THE ANNUAL RING REQUIREMENTS.
14. FILL VIAS UNDER BGA'S (U1, U2) WITH CONDUCTIVE EPOXY.
15. 5 MIL DIFFERENTIAL PAIRS ON LAYER 1, 5, 6, AND 10 ARE TO BE 100 OHM IMPEDANCE.
16. GROUND ETCH EXTENDED TO BOARD EDGE IS INTENTIONAL; DO NOT PULL BACK.



DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	SIZE	PLATED	QTY
·	8.0	PLATED	412
·	10.0	PLATED	87
·	10.0	PLATED	81
·	12.0	PLATED	435
·	13.0	PLATED	1
*	35.0	PLATED	14
⊕	35.0	PLATED	8
*	35.0	PLATED	292
*	36.0	PLATED	23
⊕	40.0	PLATED	1
⊙	55.0	PLATED	8
○	94.0	PLATED	2
○	120.0	PLATED	2
+	140.0	PLATED	1
⊙	250.0	PLATED	2
⊕	40.0	NON-PLATED	2
x	125.0	NON-PLATED	4

Figure 25. Circuit Board Stackup

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -0.3 V to 7 V and the output voltage range of -0.3 V to 3.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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