



TSM6866D

20V Dual N-Channel MOSFET w/ESD Protected

TSSOP-8



Pin assignment:

1. Drain
2. Source 1
3. Source 1
4. Gate 1
5. Gate 2
6. Source 2
7. Source 2
8. Drain

$V_{DS} = 20V$

$R_{DS(on)}, V_{GS} @ 4.5V, I_{DS} @ 6.5A = 28m\Omega$

$R_{DS(on)}, V_{GS} @ 2.5V, I_{DS} @ 5.5A = 40m\Omega$

Features

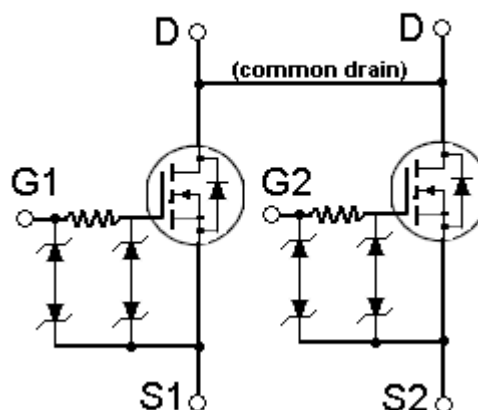
- ✧ Advanced trench process technology
- ✧ High density cell design for ultra low on-resistance
- ✧ Excellent thermal and electrical capabilities
- ✧ Specially designed for Li-ion battery packs.
- ✧ Battery switch application

Ordering Information

Part No.	Packing	Package
TSM6968DCA	Tape & Reel 3,000/per reel	TSSOP-8

Block Diagram

Dual N-channel



Absolute Maximum Rating ($T_a = 25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	20V	V
Gate-Source Voltage		V _{GS}	± 12	V
Continuous Drain Current, V _{GS} @4.5V.		I _D	6.5	A
Pulsed Drain Current, V _{GS} @4.5V		I _{DM}	30	A
Maximum Power Dissipation	Ta = 25 °C	P _D	1.5	W
	Ta = 70 °C		0.96	
Operating Junction Temperature		T _J	+150	°C
Operating Junction and Storage Temperature Range		T _J , T _{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Foot (Drain) Thermal Resistance	$R_{\theta JF}$	35	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta JA}$	83	$^\circ C/W$

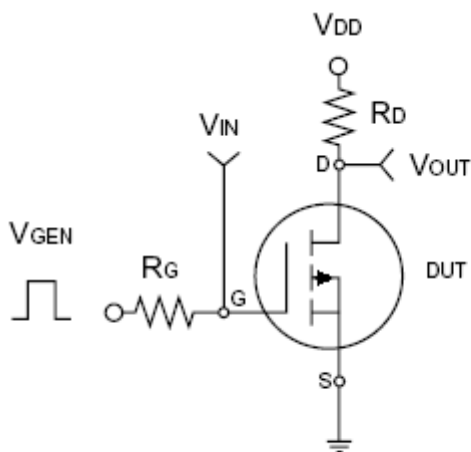
Note: Surface mounted on FR4 board $t \leq 10sec$.

Electrical Characteristics

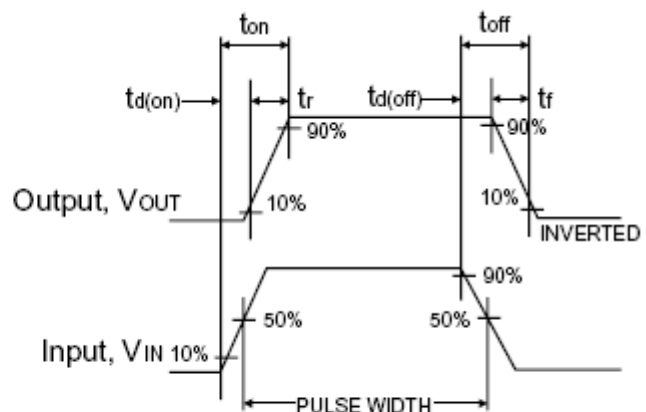
Rate $I_D = 6.5A$, ($T_a = 25^\circ C$ unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	20	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 4.5V, I_D = 6.5A$	$R_{DS(ON)}$	--	22	28	mΩ
Drain-Source On-State Resistance	$V_{GS} = 2.5V, I_D = 5.5A$	$R_{DS(ON)}$	--	30	40	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	0.5	1.0	--	V
Zero Gate Voltage Drain Current	$V_{DS} = 20V, V_{GS} = 0V$	I_{DSS}	--	--	10	μA
Gate Body Leakage	$V_{GS} = \pm 4.5V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Gate Body Leakage	$V_{GS} = \pm 12V, V_{DS} = 0V$	I_{GSS}	--	--	± 10	mA
On-State Drain Current	$V_{GS} = 4.5V, V_{DS} \geq 5V$	$I_{D(ON)}$	30	--	--	A
Forward Transconductance	$V_{DS} = 10V, I_D = 6.5A$	g_{fs}	--	40	--	S
Dynamic						
Total Gate Charge	$V_{DS} = 10V, I_D = 6.5A,$ $V_{GS} = 4.5V$	Q_g	--	12	--	nC
Gate-Source Charge		Q_{gs}	--	2	--	
Gate-Drain Charge		Q_{gd}	--	3.5	--	
Turn-On Delay Time	$V_{DD} = 10V, R_L = 10\Omega,$ $I_D = 1A, V_{GEN} = 4.5V,$ $R_G = 6\Omega$	$t_{d(on)}$	--	75	100	nS
Turn-On Rise Time		t_r	--	125	150	
Turn-Off Delay Time		$t_{d(off)}$	--	600	720	
Turn-Off Fall Time		t_f	--	300	360	
Input Capacitance	$V_{DS} = 10V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	870	--	pF
Output Capacitance		C_{oss}	--	320	--	
Reverse Transfer Capacitance		C_{rss}	--	240	--	
Source-Drain Diode						
Max. Diode Forward Current		I_S	--	--	1.0	A
Diode Forward Voltage	$I_S = 1.0A, V_{GS} = 0V$	V_{SD}	--	0.7	1.2	V

Note : pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

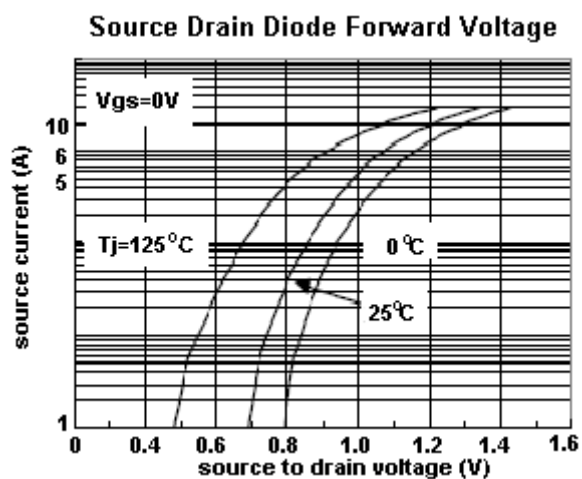
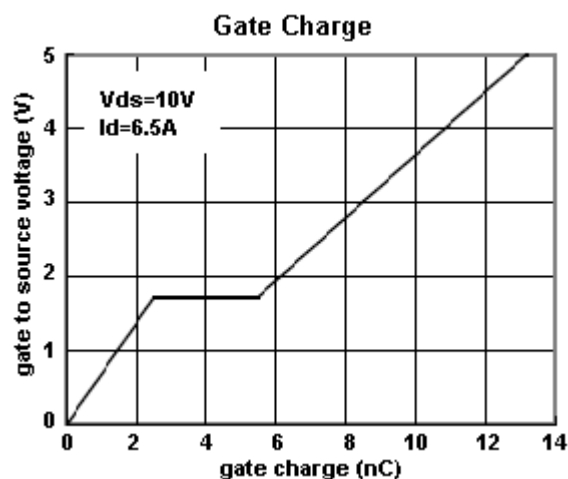
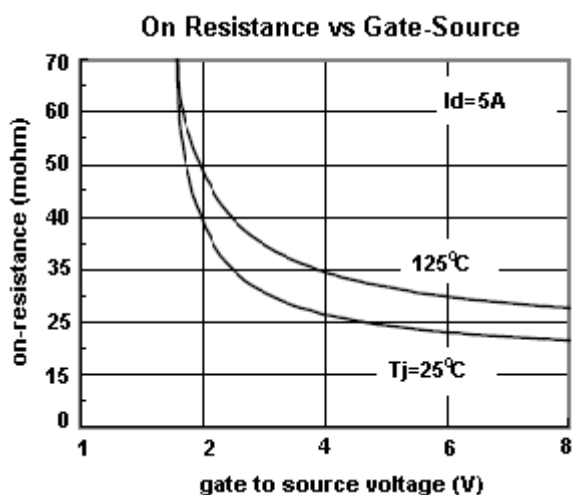
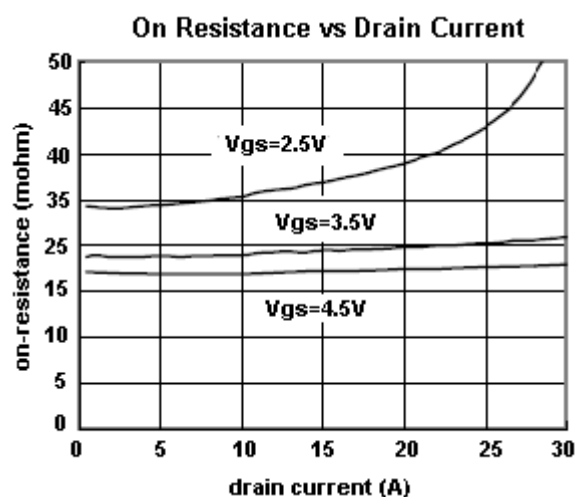
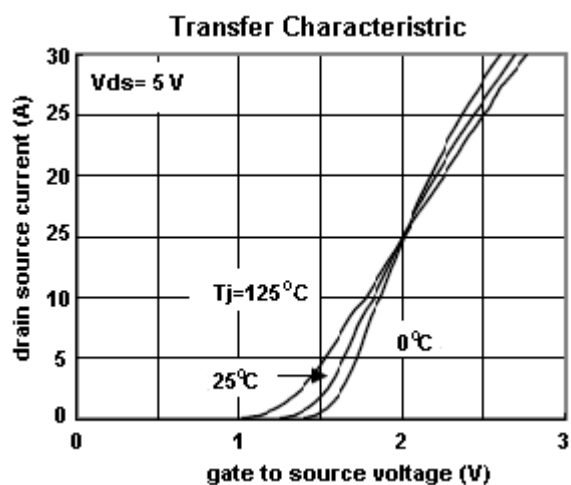
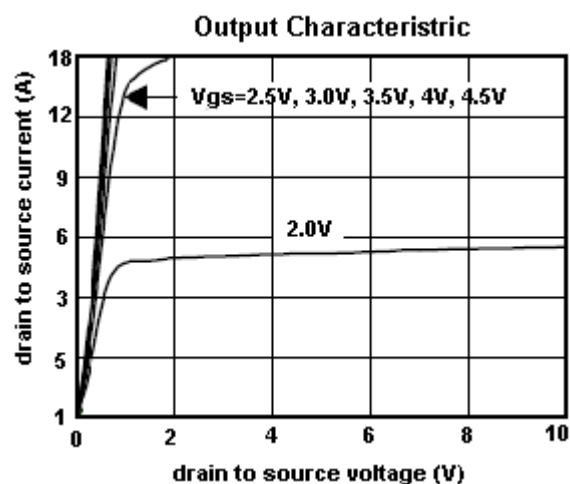


Switching Test Circuit

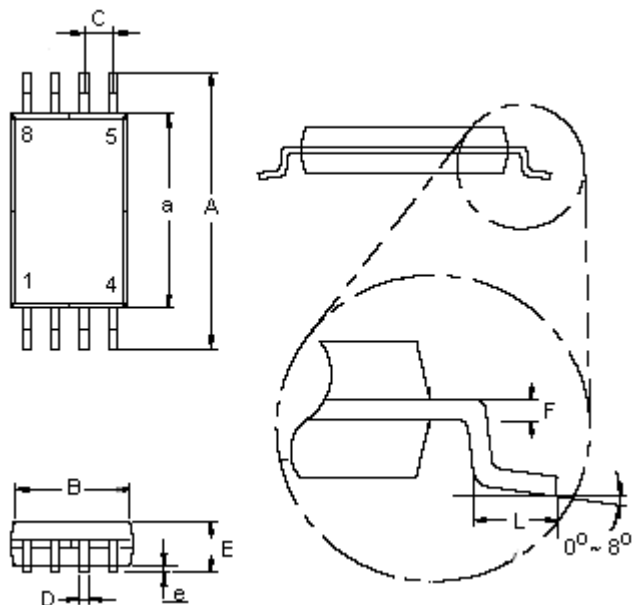


Switchin Waveforms

Typical Characteristics Curve ($T_a = 25^\circ\text{C}$ unless otherwise noted)



TSSOP-8 Mechanical Drawing



TSSOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.20	6.60	0.244	0.260
a	4.30	4.50	0.170	0.177
B	2.90	3.10	0.114	0.122
C	0.65 (typ)		0.025 (typ)	
D	0.25	0.30	0.010	0.019
E	1.05	1.20	0.041	0.049
e	0.05	0.15	0.002	0.009
F	0.127		0.005	
L	0.50	0.70	0.020	0.028