

SBAS191F – FEBRUARY 2001 – REVISED APRIL 2004

PDA ANALOG INTERFACE CIRCUIT

FEATURES

- 4-WIRE TOUCH SCREEN INTERFACE AND 4-BY-4 KEYPAD INTERFACE
- RATIOMETRIC CONVERSION
- SINGLE 2.7V TO 3.6V SUPPLY
- SERIAL INTERFACE
- INTERNAL DETECTION OF SCREEN TOUCH AND KEYPAD
- PROGRAMMABLE 8-, 10-, OR 12-BIT RESOLUTION
- PROGRAMMABLE SAMPLING RATES
- DIRECT BATTERY MEASUREMENT (0.5V to 6V)
- ON-CHIP TEMPERATURE MEASUREMENT
- TOUCH-PRESSURE MEASUREMENT
- FULL POWER-DOWN CONTROL
- TSSOP-28 AND QFN-32 PACKAGES

APPLICATIONS

- PERSONAL DIGITAL ASSISTANTS
- CELLULAR PHONES
- MP3 PLAYERS

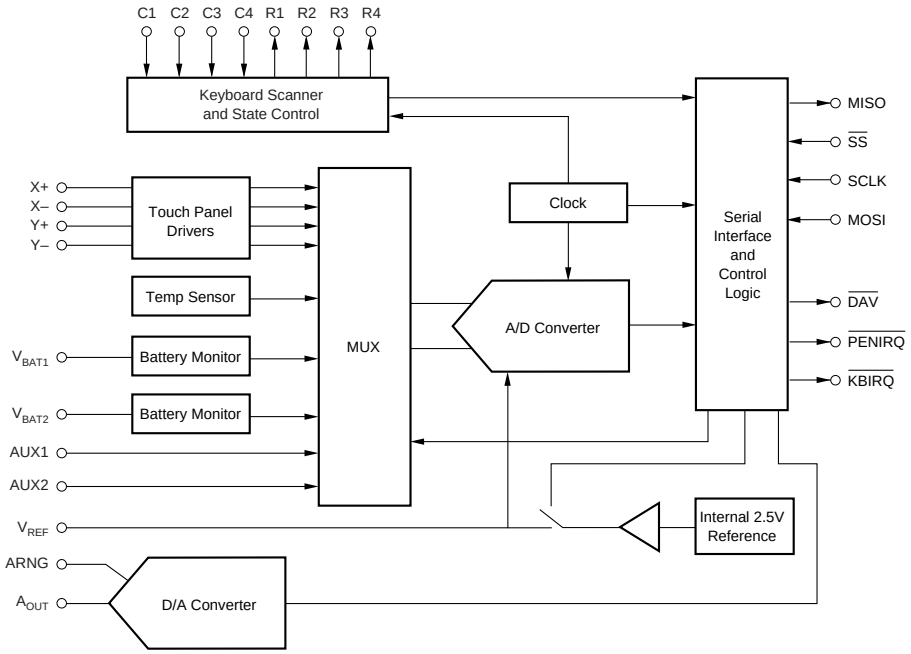
DESCRIPTION

The TSC2200 is a complete PDA analog interface circuit. It contains a complete 12-bit, Analog-to-Digital (A/D) resistive touch screen converter including drivers, the control to measure touch pressure, keyboard controller, and an 8-bit Digital-to-Analog (D/A) converter output for LCD contrast control. The TSC2200 interfaces to the host controller through a standard SPI™ serial interface. The TSC2200 offers programmable resolution and sampling rates from 8- to 12-bits and up to 125kHz to accommodate different screen sizes.

The TSC2200 also offers two battery-measurement inputs capable of reading battery voltages up to 6V, while operating at only 2.7V. It also has an on-chip temperature sensor capable of reading 0.3°C resolution. The TSC2200 is available in a TSSOP-28 and a QFN-32 package.

SPI is a registered trademark of Motorola.

US Patent No. 624639.



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ABSOLUTE MAXIMUM RATINGS(1)

V_{DD} to GND	–0.3V to +6.0V
V_{BAT} Input Voltage to GND	–0.3V to +6.0V
Analog Input Voltage to GND (except V_{BAT})	–0.3V to V_{DD} + 0.3V
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature (T_J Max)	+150°C
TSSOP Package	
Power Dissipation	(T_J Max – T_A)/θ_{JA}
θ_{JA} Thermal Impedance	90°C/W
Lead Temperature, Soldering	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT	INTEGRAL LINEARITY ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TSC2200	±2	TSSOP-28	PW	–40°C to +85°C	TSC2200I	TSC2200IPW	Rails, 50
"	"	"	"	"	"	TSC2200IPWR	Tape and Reel, 2000
TSC2200	±2	QFN-32	RHB	–40°C to +85°C	TSC2200I	TSC2200IRHB	Tubes, 72
"	"	"	"	"	"	TSC2200IRHBR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

TIMING CHARACTERISTICS(1)(2)

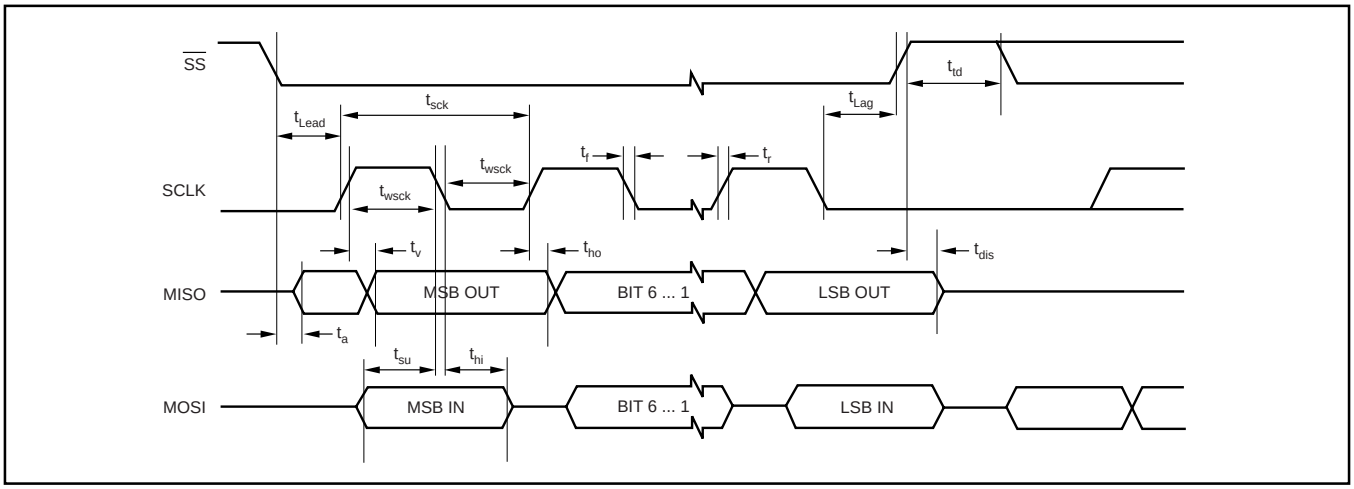
At –40°C to +85°C, +V_{DD} = +2.7V, V_{REF} = +2.5V, unless otherwise noted.

PARAMETER	CONDITIONS	TSC2200 MIN	TSC2200 TYP	TSC2200 MAX	UNITS
SCLK Period	t_{sck}	30			ns
Enable Lead Time	t_{Lead}	15			ns
Enable Lag Time	t_{Lag}	15			ns
Sequential Transfer Delay	t_{td}	30			ns
Data Setup Time	t_{su}	10			ns
Data Hold Time (inputs)	t_{hi}	10			ns
Data Hold Time (outputs)	t_{ho}	0			ns
Slave Access Time	t_a			15	ns
Slave D_{OUT} Disable Time	t_{dis}			15	ns
Data Valid	t_v			10	ns
Rise Time	t_r			30	ns
Fall Time	t_f			30	ns

NOTES: (1) All input signals are specified with t_r = t_f = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. (2) See timing diagram below.

TIMING DIAGRAM

All specifications typical at –40°C to +85°C, +V_{DD} = +2.7V.



ELECTRICAL CHARACTERISTICS

At –40°C to +85°C, $+V_{DD}$ = +2.7V, internal V_{REF} = +2.5V, conversion clock = 2MHz, and 12-bit mode, unless otherwise noted.

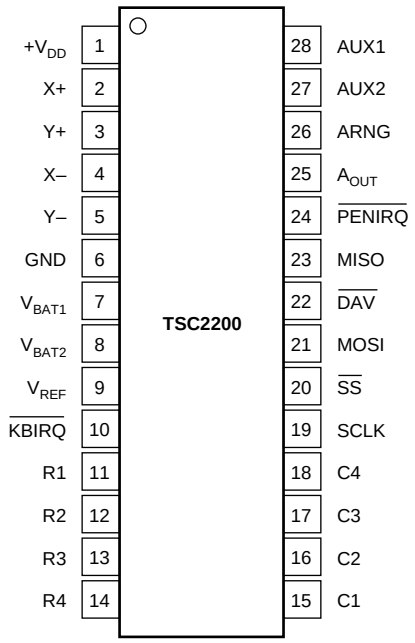
PARAMETER	CONDITIONS	TSC2200IPW			TSC2200IRHB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
AUXILIARY ANALOG INPUT								
Input Voltage Range		0		$+V_{REF}$	*		*	V
Input Capacitance			25			*		pF
Input Leakage Current			±1			*		µA
BATTERY MONITOR INPUT								
Input Voltage Range		0.5		6.0	*		*	V
Input Capacitance			25			*		pF
Input Leakage Current			±1			*		µA
Accuracy		–3		+3	*		*	%
TEMPERATURE MEASUREMENT								
Temperature Range		–40		+85	*		*	°C
Temperature Resolution			0.3			*		°C
Accuracy			±2			*		°C
A/D CONVERTER								
Resolution	Programmable: 8-, 10-, or 12-Bits			12			*	Bits
No Missing Codes	12-Bit Resolution	11			*			Bits
Integral Linearity				±2			±3	LSB
Offset Error				±6			*	LSB
Gain Error	Excluding Reference Error			±6			*	LSB
Noise			30			*		µVrms
Power-Supply Rejection			80			*		dB
D/A CONVERTER								
Output Current Range	Set by Resistor from ARNG to GND	650			500			µA
Resolution				8			*	Bits
Integral Linearity			±2			*		LSB
VOLTAGE REFERENCE								
Voltage Range	Internal 2.5V	2.45	2.5	2.55	*	*	*	V
	Internal 1.25V	1.225	1.25	1.275	*	*	1.285	V
Reference Drift			20			*		ppm/°C
External Reference Input Range		1.0		V_{DD}	*		*	V
Current Drain			20			*		µA
DIGITAL INPUT/OUTPUT								
Internal Clock Frequency			8			*		MHz
Logic Family			CMOS			*		
Logic Levels: V_{IH}	I_{IH} = +5µA	$0.7V_{DD}$			*			V
V_{IL}	I_{IL} = +5µA	–0.3		$0.3V_{DD}$	*		*	V
V_{OH}	I_{OH} = 2 TTL Loads	$0.8V_{DD}$			*			V
V_{OL}	I_{OL} = 2 TTL Loads			0.4			*	V
POWER-SUPPLY REQUIREMENTS								
Power-Supply Voltage, $+V_{DD}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current	See Note (1)		1.25	2.3		*	2.5	mA
	See Note (2)		500			*		µA
	Power-Down			3			*	µA
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as TSC2200IPW.

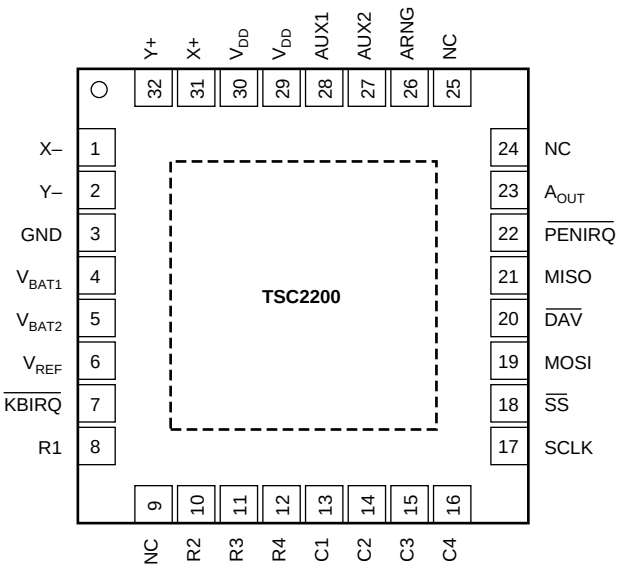
NOTES: (1) AUX1 conversion, no averaging, no REF power down, 50µs conversion. (2) AUX1 conversion, no averaging, external reference, 50µs conversion.

PIN CONFIGURATION

Top View **TSSOP**



Top View **QFN**



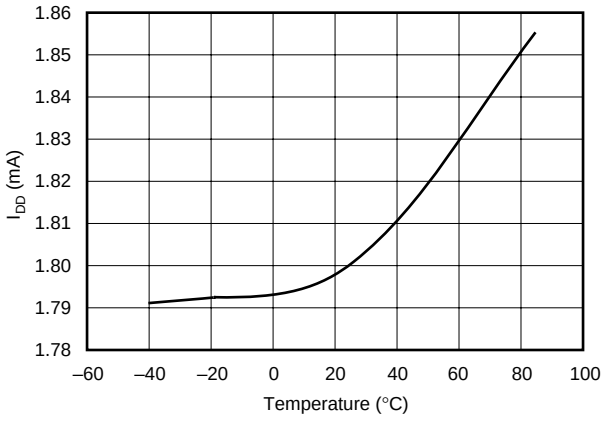
PIN DESCRIPTION

PIN			
TSSOP	QFN	NAME	DESCRIPTION
1	29, 30	V_{DD}	Power Supply
2	31	X+	X+ Position Input
3	32	Y+	Y+ Position Input
4	1	X–	X– Position Input
5	2	Y–	Y– Position Input
6	3	GND	Ground
7	4	V_{BAT1}	Battery Monitor Input 1
8	5	V_{BAT2}	Battery Monitor Input 2
9	6	V_{REF}	Voltage Reference Input/Output
10	7	$\overline{KBIRQ}$	Keyboard Interrupt (active LOW)
11	8	R1	Row 1
12	10	R2	Row 2
13	11	R3	Row 3
14	12	R4	Row 4
15	13	C1	Column 1
16	14	C2	Column 2
17	15	C3	Column 3
18	16	C4	Column 4
19	17	SCLK	Serial Clock Input
20	18	$\overline{SS}$	Slave Select Input (active LOW). Data will not be clocked in to MOSI unless $\overline{SS}$ is LOW. When $\overline{SS}$ is HIGH, MISO is high impedance.
21	19	MOSI	Serial Data Input. Data is clocked in at SCLK falling edge.
22	20	$\overline{DAV}$	Data Available (active LOW)
23	21	MISO	Serial Data Output. Data is clocked out at SCLK falling edge. High impedance when $\overline{SS}$ is HIGH.
24	22	$\overline{PENIRQ}$	Pen Interrupt
25	23	A_{OUT}	Analog Output Current from D/A Converter
26	26	ARNG	D/A Converter Analog Output Range Set
27	27	AUX2	Auxiliary A/D Converter Input 2
28	28	AUX1	Auxiliary A/D Converter Input 1
—	9, 24, 25	NC	No Connection

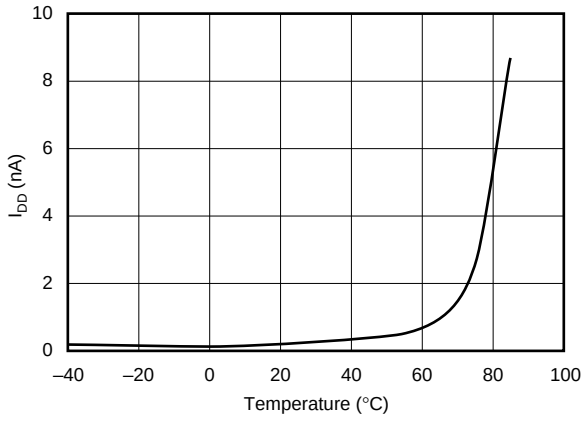
TYPICAL CHARACTERISTICS

At T_A = +25°C, $+V_{DD}$ = +2.7V, conversion clock = 2MHz, 12-bit mode, and V_{REF} = +2.5V, unless otherwise noted.

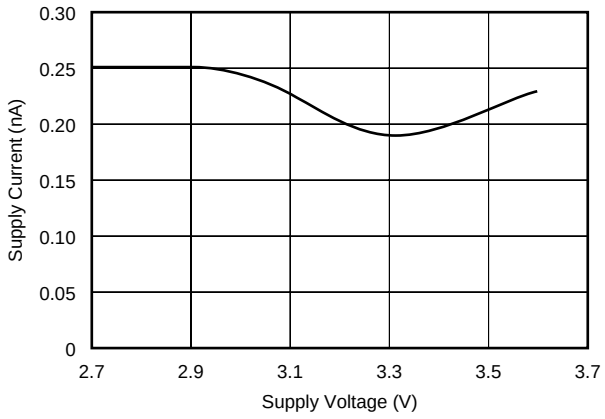
CONVERSION SUPPLY CURRENT vs TEMPERATURE



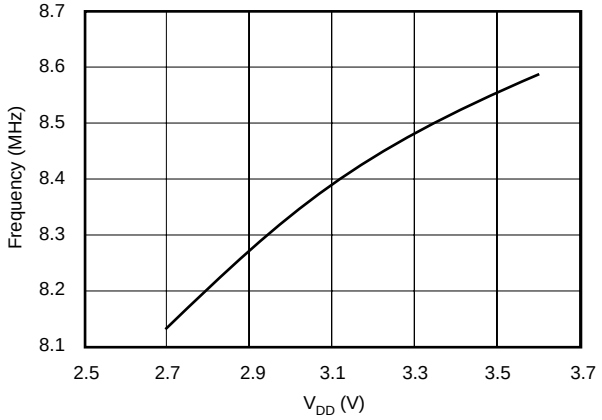
POWER-DOWN SUPPLY CURRENT vs TEMPERATURE



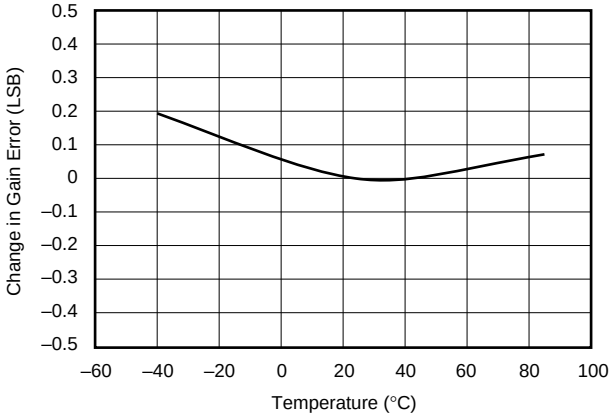
POWER-DOWN SUPPLY CURRENT vs SUPPLY VOLTAGE



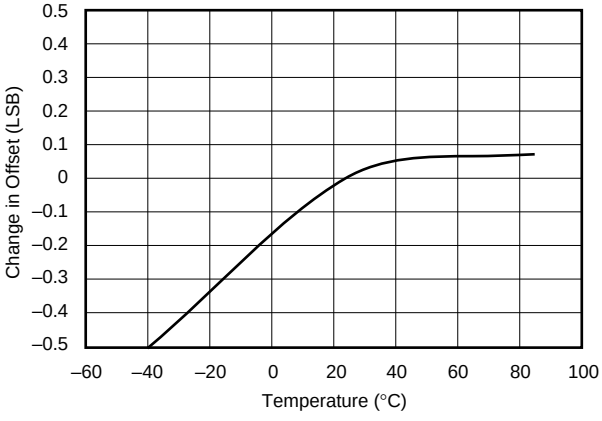
INTERNAL OSCILLATOR FREQUENCY vs V_{DD}



CHANGE IN GAIN ERROR vs TEMPERATURE



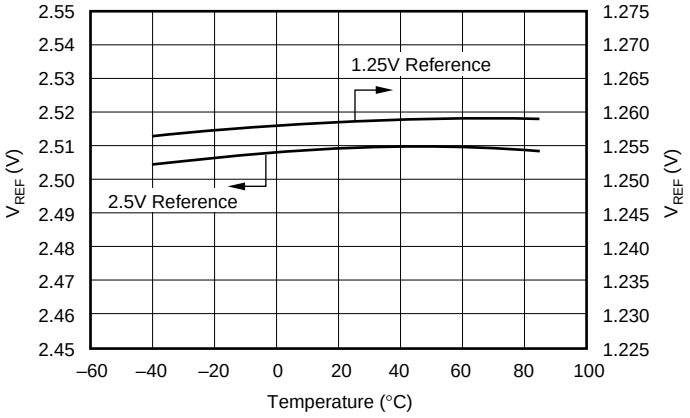
CHANGE IN OFFSET ERROR vs TEMPERATURE



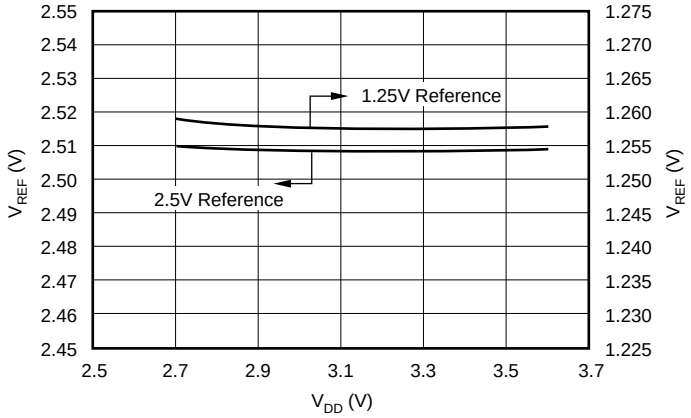
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_{DD}$ = +2.7V, conversion clock = 2MHz, 12-bit mode, and V_{REF} = +2.5V, unless otherwise noted.

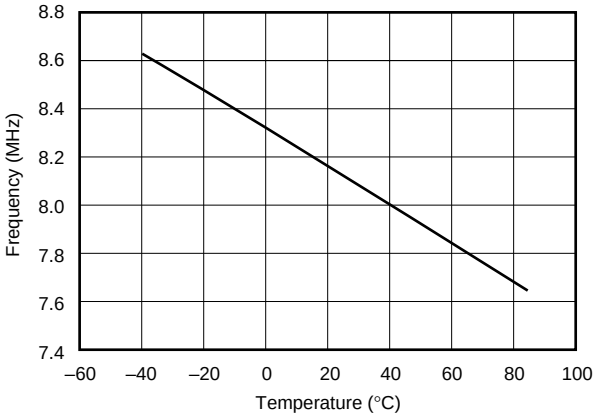
INTERNAL REFERENCE vs TEMPERATURE



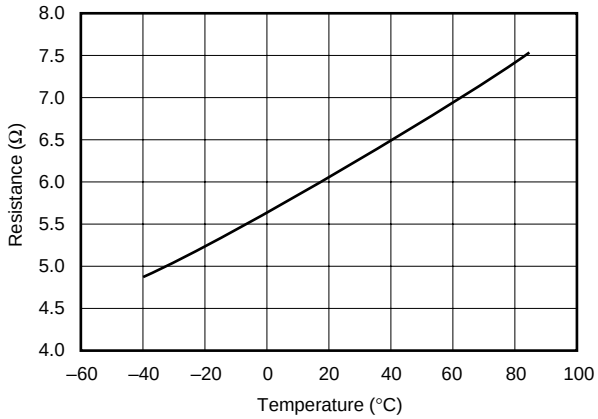
INTERNAL REFERENCE vs V_{DD}



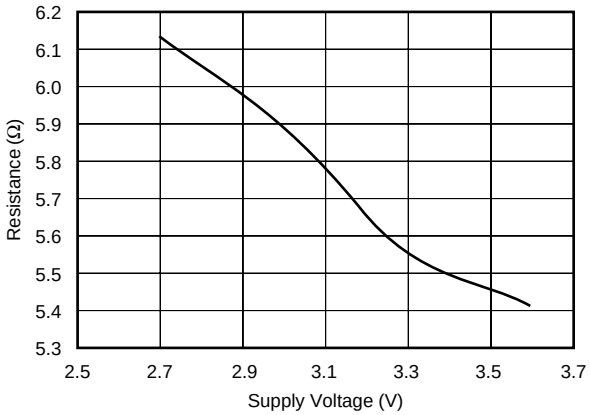
INTERNAL OSCILLATOR FREQUENCY vs TEMPERATURE



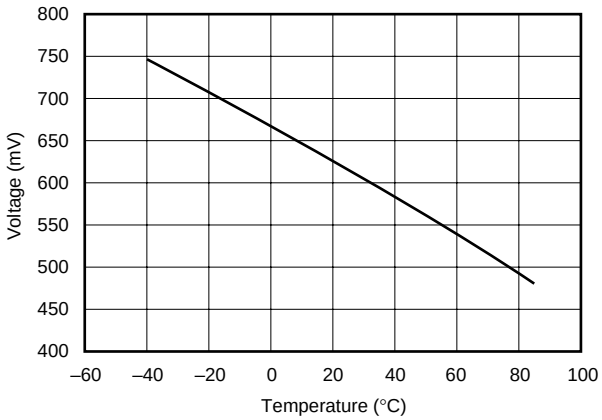
TOUCH SCREEN DRIVER ON-RESISTANCE vs TEMPERATURE



SWITCH-ON RESISTANCE vs V_{DD}



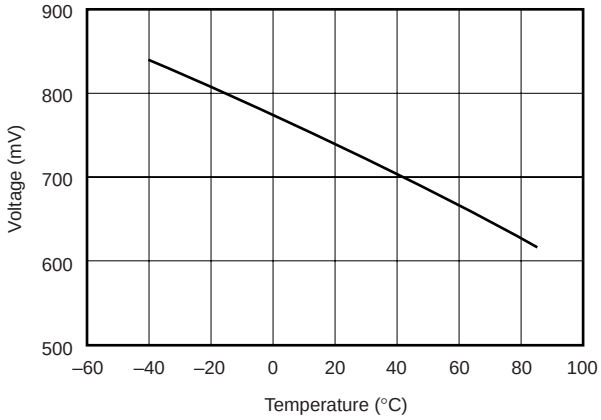
TEMP1 DIODE VOLTAGE vs TEMPERATURE



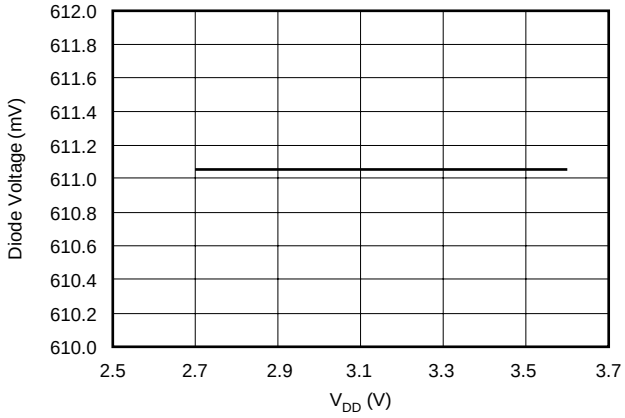
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_{DD}$ = +2.7V, conversion clock = 2MHz, 12-bit mode, and V_{REF} = +2.5V, unless otherwise noted.

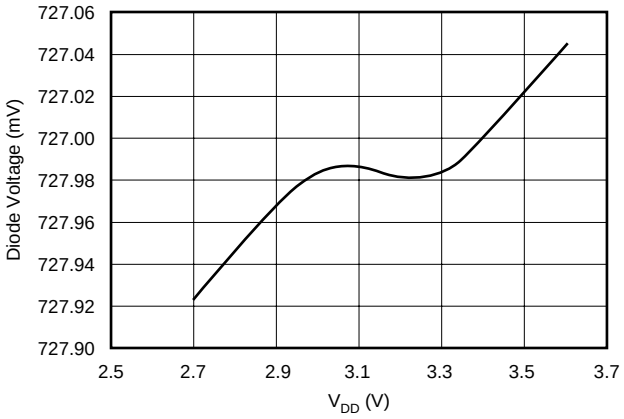
TEMP2 DIODE VOLTAGE vs TEMPERATURE



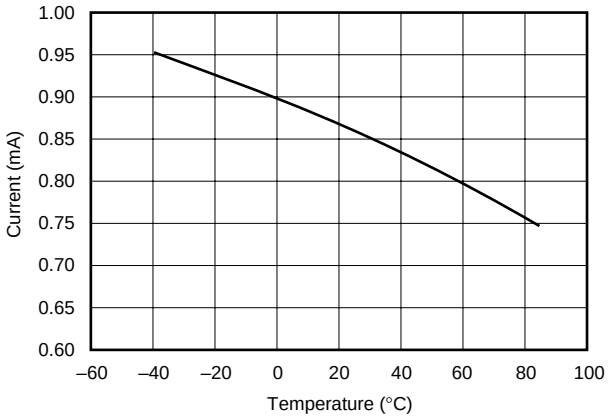
TEMP1 DIODE VOLTAGE vs SUPPLY VOLTAGE



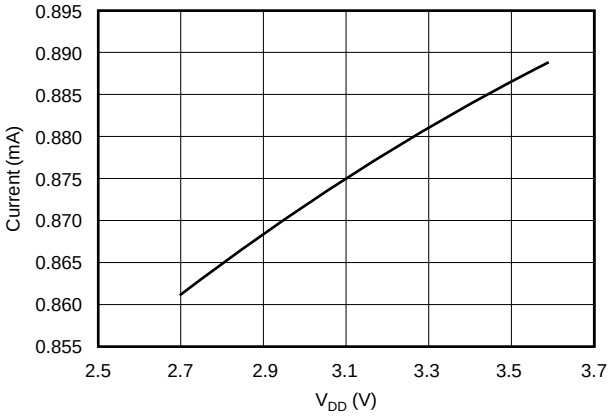
TEMP2 DIODE VOLTAGE vs SUPPLY VOLTAGE



DAC OUTPUT CURRENT vs TEMPERATURE



DAC MAX CURRENT vs V_{DD}



OVERVIEW

The TSC2200 is an analog interface circuit for human interface devices. A register-based architecture eases integration with microprocessor-based systems through a standard SPI bus. All peripheral functions are controlled through the registers and onboard state machines.

The TSC2200 consists of the following blocks (refer to the block diagram on the front page):

- Touch Screen Interface
- Keypad Interface
- Battery Monitors
- Auxiliary Inputs
- Temperature Monitor
- Current Output D/A Converter

Communication to the TSC2200 is via a standard SPI serial interface. This interface requires that the Slave Select signal be driven LOW to communicate with the TSC2200. Data is then shifted into or out of the TSC2200 under control of the host microprocessor, which also provides the serial data clock.

Control of the TSC2200 and its functions is accomplished by writing to different registers in the TSC2200. A simple command protocol is used to address the 16-bit registers. Registers control the operation of the A/D converter, D/A converter, and keypad scanner.

The result of measurements made will be placed in the TSC2200's memory map and may be read by the host at any time. Three signals are available from the TSC2200 to indicate that data is available for the host to read. The $\overline{DAV}$ output indicates that an A/D conversion has completed and that data is available. The $\overline{KBIRQ}$ output indicates that a key on the keypad has been pressed. The $\overline{PENIRQ}$ output indicates that a touch has been detected on the touch screen. A typical application of the TSC2200 is shown in Figure 1.

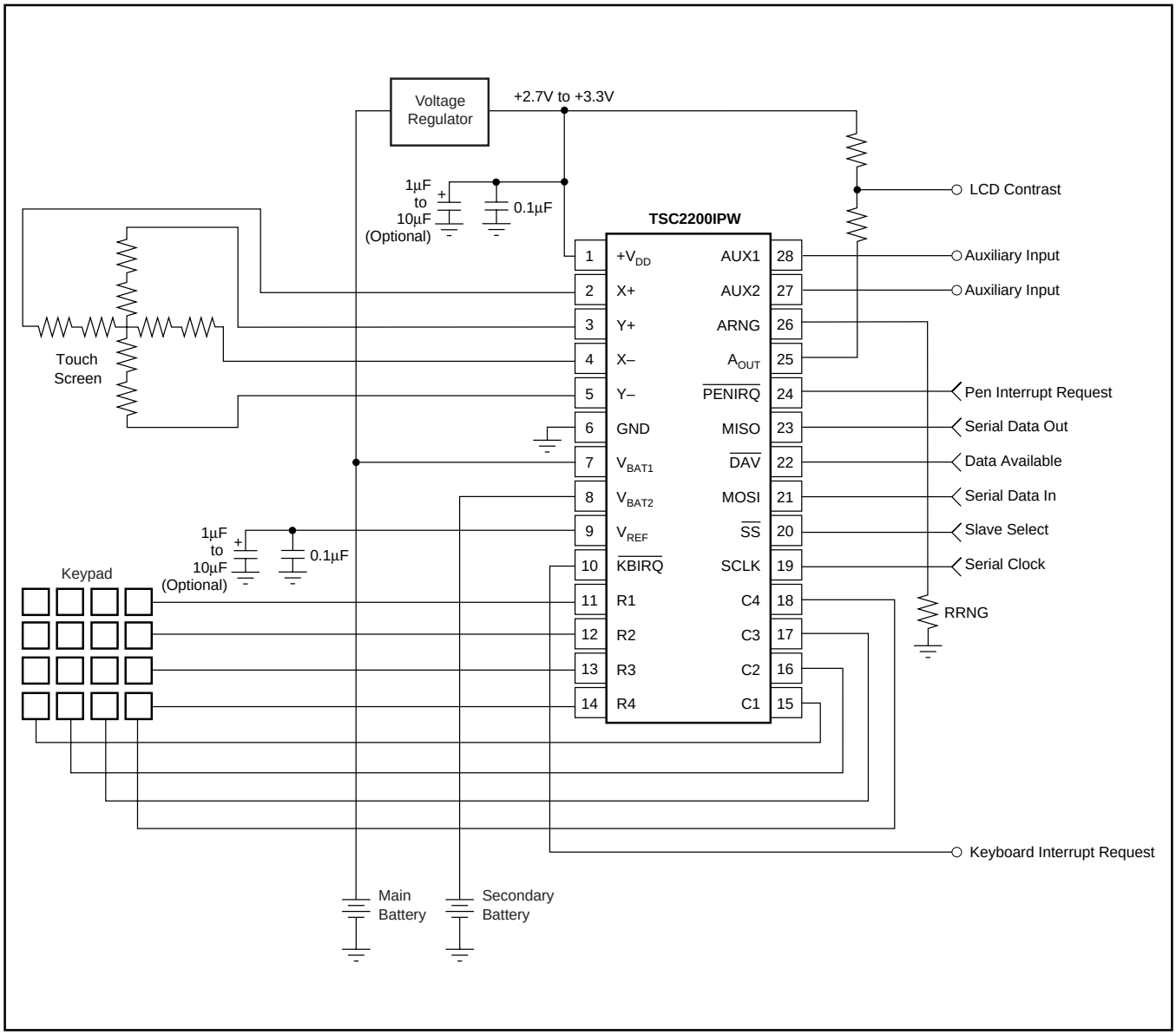


FIGURE 1. Typical Circuit Configuration.

OPERATION—TOUCH SCREEN

A resistive touch screen works by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where a screen is touched by an input stylus, pen, or finger. The change in the resistance ratio marks the location on the touch screen.

The TSC2200 supports the resistive 4-wire configurations (see Figure 1). The circuit determines location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure.

THE 4-WIRE TOUCH SCREEN COORDINATE PAIR MEASUREMENT

A 4-wire touch screen is constructed as shown in Figure 2. It consists of two transparent resistive layers separated by insulating spacers.

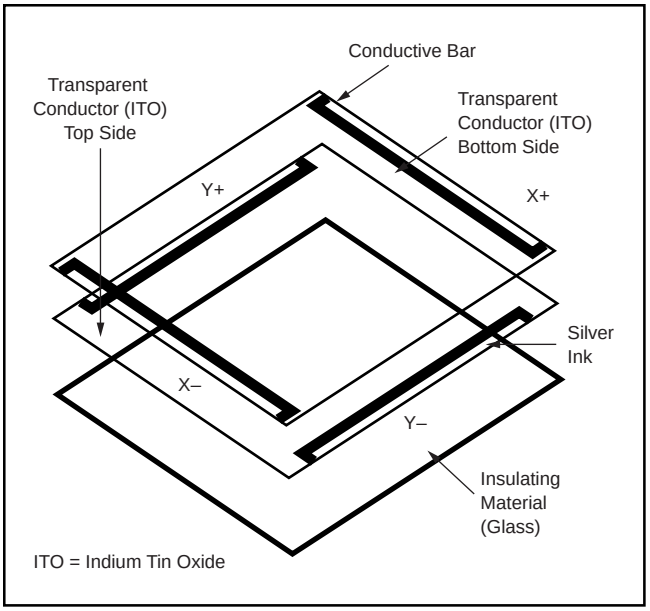


FIGURE 2. 4-Wire Touch Screen Construction.

The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The A/D converter converts the voltage measured at the point the panel is touched. A measurement of the Y-position of the pointing device is made by connecting the X+ input to a data converter chip, turning on the Y+ and Y– drivers, and digitizing the voltage seen at the X+ input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead does not affect the conversion due to the high input impedance of the A/D converter.

Voltage is then applied to the other axis, and the A/D converter converts the voltage representing the X-position on the screen. This provides the X- and Y-coordinates to the associated processor.

Measuring touch pressure (Z) can also be done with the TSC2200. To determine pen or finger touch, the pressure of the "touch" needs to be determined. Generally, it is not necessary to have very high performance for this test, therefore, the 8-bit resolution mode is recommended (however, calculations will be shown with the 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2200 supports two methods. The first method requires knowing the X-plate resistance, measurement of the X-position, and two additional cross panel measurements (Z_2 and Z_1) of the touch screen, as seen in Figure 3. Using Equation 1 will calculate the touch resistance:

$$R_{TOUCH} = R_{X\text{-}Plate} \bullet \frac{X\text{-}Position}{4096} \left(\frac{Z_2}{Z_1} - 1 \right) \quad (1)$$

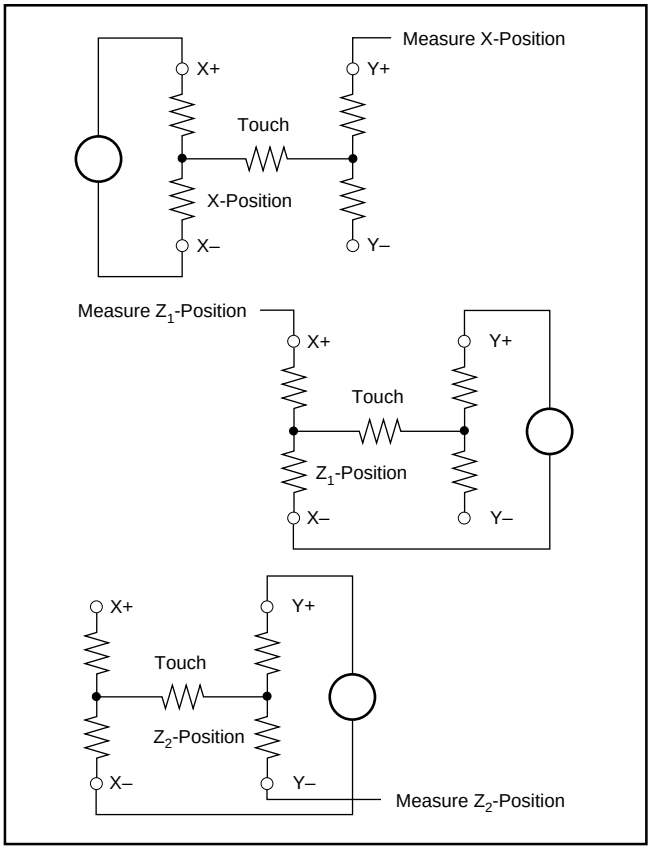


FIGURE 3. Pressure Measurement.

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-position and Y-position, and Z_1. Using Equation 2 will also calculate the touch resistance:

$$R_{TOUCH} = R_{X\text{-}Plate} \bullet \frac{X\text{-}Position}{4096} \left(\frac{4096}{Z_1} - 1 \right) - R_{Y\text{-}Plate} \bullet \left(1 - \frac{Y\text{-}Position}{4096} \right) \quad (2)$$

When the touch panel is pressed or touched, and the drivers to the panel are turned on, the voltage across the touch panel will often overshoot and then slowly settle (decay) down to a stable DC value. This is due to mechanical bouncing which is caused by vibration of the top layer sheet of the touch panel when the panel is pressed. This settling time must be accounted for, or else the converted value will be in error. Therefore, a delay must be introduced between the time the driver for a particular measurement is turned on, and the time measurement is made.

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen; i.e., noise generated by the LCD panel or back-light circuitry. The value of these capacitors will provide a low-pass filter to reduce the noise, but will cause an additional settling time requirement when the panel is touched.

Several solutions to this problem are available in the TSC2200. A programmable delay time is available that sets the delay between turning the drivers on and making a conversion. This is referred to as the Panel Voltage Stabilization time, and is used in some of the modes available in the TSC2200. In other modes, the TSC2200 can be commanded to turn on the drivers only without performing a conversion. Time can then be allowed before a conversion is started.

The TSC2200 touch screen interface can measure position (X and Y) and pressure (Z). Determination of these coordinates is possible under three different modes of the A/D converter: conversion controlled by the TSC2200, initiated by detection of a touch; conversion controlled by the TSC2200, initiated by the host responding to the $\overline{\text{PENIRQ}}$ signal; or conversion completely controlled by the host processor.

A/D CONVERTER

The analog inputs of the TSC2200 are shown in Figure 4. The analog inputs (X, Y, and Z touch panel coordinates, battery voltage monitors, chip temperature, and auxiliary inputs) are provided via a multiplexer to the Successive Approximation Register (SAR) A/D converter. The A/D converter architecture is based on capacitive redistribution architecture that inherently includes a sample-and-hold function.

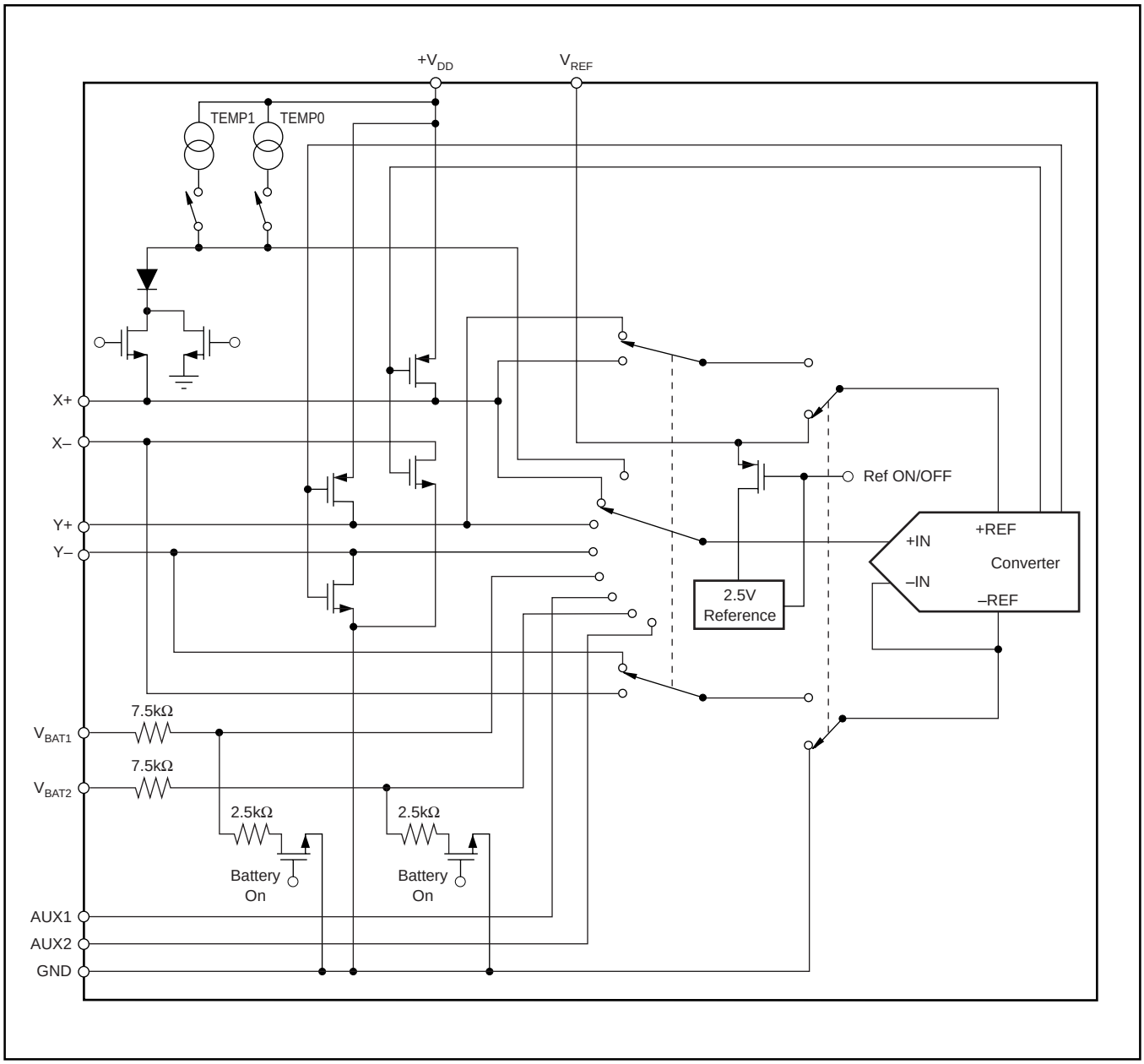


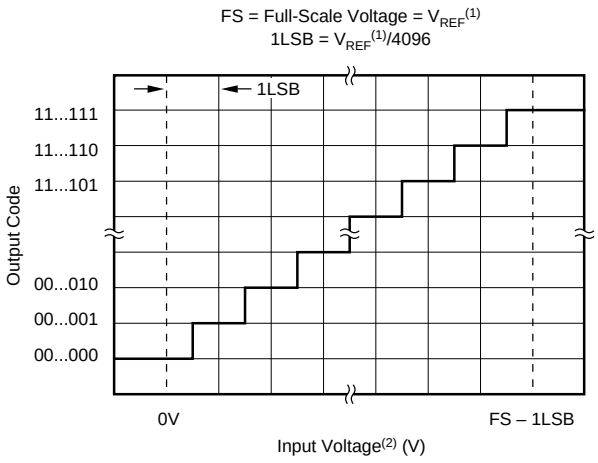
FIGURE 4. Simplified Diagram of the Analog Input Section.

A unique configuration of low on-resistance switches allows an unselected A/D converter input channel to provide power and an accompanying pin to provide ground for driving the touch panel. By maintaining a differential input to the converter and a differential reference input architecture, it is possible to negate errors caused by the driver switch on-resistances.

The A/D converter is controlled by an A/D Converter Control Register. Several modes of operation are possible, depending upon the bits set in the control register. Channel selection, scan operation, averaging, resolution, and conversion rate may all be programmed through this register. These modes are outlined in the sections below for each type of analog input. The results of conversions made are stored in the appropriate result register.

Data Format

The TSC2200 output data is in Straight Binary format, as shown in Figure 5. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



NOTES: (1) Reference voltage at converter: +REF – (–REF). See Figure 4.
(2) Input voltage at converter, after multiplexer: +IN – (–IN). See Figure 4.

FIGURE 5. Ideal Input Voltages and Output Codes.

Reference

The TSC2200 has an internal voltage reference that can be set to 1.25V or 2.5V, through the Reference Control Register.

The internal reference voltage is only used in the single-ended mode for battery monitoring, temperature measurement, and for utilizing the auxiliary inputs. Optimal touch screen performance is achieved when using a ratiometric conversion, thus all touch screen measurements are done automatically in the differential mode. An external reference can also be applied to the V_{REF} pin, and the internal reference can be turned off.

Variable Resolution

The TSC2200 provides three different resolutions for the A/D converter: 8-, 10-, or 12-bits. Lower resolutions are often practical for measurements such as touch pressure. Performing the conversions at lower resolutions reduces the amount of time it takes for the A/D converter to complete its conversion process, which lowers power consumption.

Conversion Clock and Conversion Time

The TSC2200 contains an internal 8MHz clock, which is used to drive the state machines inside the device that perform the many functions of the part. This clock is divided down to provide a clock to run the A/D converter. The division ratio for this clock is set in the A/D Converter Control Register. The ability to change the conversion clock rate allows the user to choose the optimal value for resolution, speed, and power. If the 8MHz clock is used directly, the A/D converter is limited to 8-bit resolution; using higher resolutions at this speed will not result in accurate conversions. Using a 4MHz conversion clock is suitable for 10-bit resolution; 12-bit resolution requires that the conversion clock run at 1MHz or 2MHz.

Regardless of the conversion clock speed, the internal clock will run nominally at 8MHz. The conversion time of the TSC2200 is dependent upon several functions. Although the conversion clock speed plays an important role in the time it takes for a conversion to complete, a certain number of internal clock cycles is needed for proper sampling of the signal. Moreover, additional times, such as the Panel Voltage Stabilization time, can add significantly to the time it takes to perform a conversion. Conversion time can vary depending upon the mode in which the TSC2200 is used. Throughout this data sheet, internal and conversion clock cycles will be used to describe the times that many functions take. In considering the total system design, these times must be taken into account by the user.

Touch Detect

The pen interrupt ($\overline{\text{PENIRQ}}$) output function is detailed in Figure 6. While in the power-down mode, the Y– driver is ON and connected to GND and the $\overline{\text{PENIRQ}}$ output is connected to the X+ input. When the panel is touched, the X+ input is

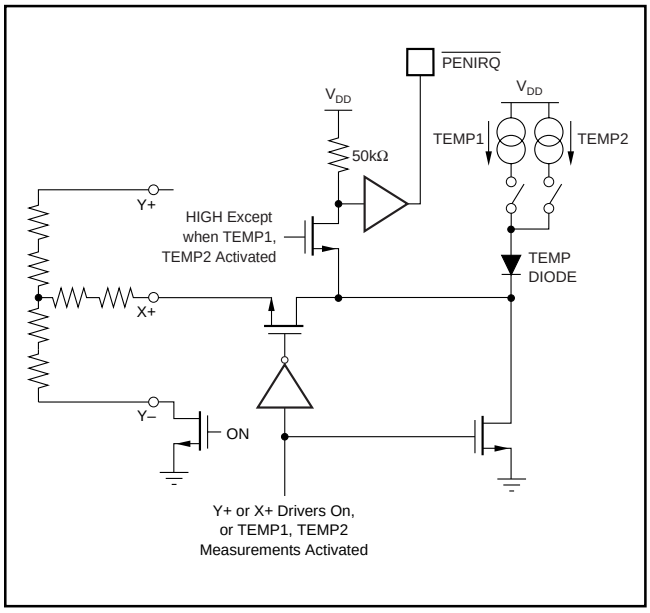


FIGURE 6. $\overline{\text{PENIRQ}}$ Functional Block Diagram.

pulled to ground through the touch screen and $\overline{\text{PENIRQ}}$ output goes LOW due to the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycles for the X- and Y-positions, the X+ input will be disconnected from the $\overline{\text{PENIRQ}}$ pull-down transistor to eliminate any leakage current from the pull-up resistor to flow through the touch screen, thus causing no errors.

In modes where the TSC2200 needs to detect if the screen is still touched (for example, when doing a $\overline{\text{PENIRQ}}$-initiated X, Y, and Z conversion), the TSC2200 must reset the drivers so that the 50kΩ resistor is connected again. Due to the high value of this pull-up resistor, any capacitance on the touch screen inputs will cause a long delay time, and may prevent the detection from occurring correctly. To prevent this, the TSC2200 has a circuit that allows any screen capacitance to be “precharged”, so that the pull-up resistor does not have to be the only source for the charging current. The time allowed for this precharge, as well as the time needed to sense if the screen is still touched, can be set in the Configuration Control register.

This illustrates the need to use the minimum capacitor values possible on the touch screen inputs. These capacitors may be needed to reduce noise, but too large a value will increase the needed precharge and sense times, as well as panel voltage stabilization time.

DIGITAL INTERFACE

The TSC2200 communicates through a standard SPI bus. The SPI allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master generates the synchronizing clock and initiates transmissions. The SPI slave devices depend on a master to start and synchronize transmissions.

A transmission begins when initiated by a master SPI. The byte from the master SPI begins shifting in on the slave MOSI pin under the control of the master serial clock. As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

The idle state of the serial clock for the TSC2200 is LOW, which corresponds to a clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The TSC2200 interface is designed so that with a clock phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI pin and the slave begins driving its MISO pin on the first serial clock edge. The $\overline{\text{SS}}$ pin should idle HIGH between transmissions. The TSC2200 will only interpret command words that are transmitted after the falling edge of $\overline{\text{SS}}$.

TSC2200 COMMUNICATION PROTOCOL

The TSC2200 is entirely controlled by registers. Reading and writing these registers is accomplished by the use of a 16-bit command, which is sent prior to the data for that register. The command is constructed as shown in Table I.

The command word begins with an R/$\overline{\text{W}}$ bit, which specifies the direction of data flow on the serial bus. The following four bits specify the page of memory this command is directed to, as shown in Table II. The next six bits specify the register address on that page of memory to which the data is directed. The last five bits are reserved for future use.

PG3	PG2	PG1	PG0	PAGE ADDRESSED
0	0	0	0	0
0	0	0	1	1
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

TABLE II. Page Addressing.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
R/$\overline{\text{W}}$	PG3	PG2	PG1	PG0	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	X	X	X	X	X

TABLE I. TSC2200 Command Word.

To read all the first page of memory, for example, the host processor must send the TSC2200 the command 8000_H—this specifies a read operation beginning at Page 0, Address 0. The processor can then start clocking data out of the TSC2200. The TSC2200 will automatically increment its address pointer to the end of the page; if the host processor continues clocking data out past the end of a page, the TSC2200 will simply send back the value $FFFF_H$.

Likewise, writing to Page 1 of memory would consist of the processor writing the command 0800_H, which would specify a write operation, with PG0 set to 1, and all the ADDR bits set to 0. This would result in the address pointer pointing at the first location in memory on Page 1. See the TSC2200 Memory Map section for details of register locations. Figure 7 shows an example of a complete data transaction between the host processor and the TSC2200.

TSC2200 MEMORY MAP

The TSC2200 has several 16-bit registers that allow control of the device as well as provide a location for results from the TSC2200 to be stored until read by the host microprocessor. These registers are separated into two pages of memory in the TSC2200: a Data page (Page 0) and a Control page (Page 1). The memory map is shown in Table III.

PAGE 0: DATA REGISTERS		PAGE 1: CONTROL REGISTERS	
ADDR	REGISTER	ADDR	REGISTER
00	X	00	ADC
01	Y	01	KEY
02	Z_1	02	DACCTL
03	Z_2	03	REF
04	KPDATA	04	RESET
05	BAT1	05	CONFIG
06	BAT2	06	Reserved
07	AUX1	07	Reserved
08	AUX2	08	Reserved
09	TEMP1	09	Reserved
0A	TEMP2	0A	Reserved
0B	DAC	0B	Reserved
0C	Reserved	0C	Reserved
0D	Reserved	0D	Reserved
0E	Reserved	0E	Reserved
0F	Reserved	0F	Reserved
10	ZERO	10	KPMASK
11	Reserved	11	Reserved
12	Reserved	12	Reserved
13	Reserved	13	Reserved
14	Reserved	14	Reserved
15	Reserved	15	Reserved
16	Reserved	16	Reserved
17	Reserved	17	Reserved
18	Reserved	18	Reserved
19	Reserved	19	Reserved
1A	Reserved	1A	Reserved
1B	Reserved	1B	Reserved
1C	Reserved	1C	Reserved
1D	Reserved	1D	Reserved
1E	Reserved	1E	Reserved
1F	Reserved	1F	Reserved

TABLE III. TSC2200 Memory Map.

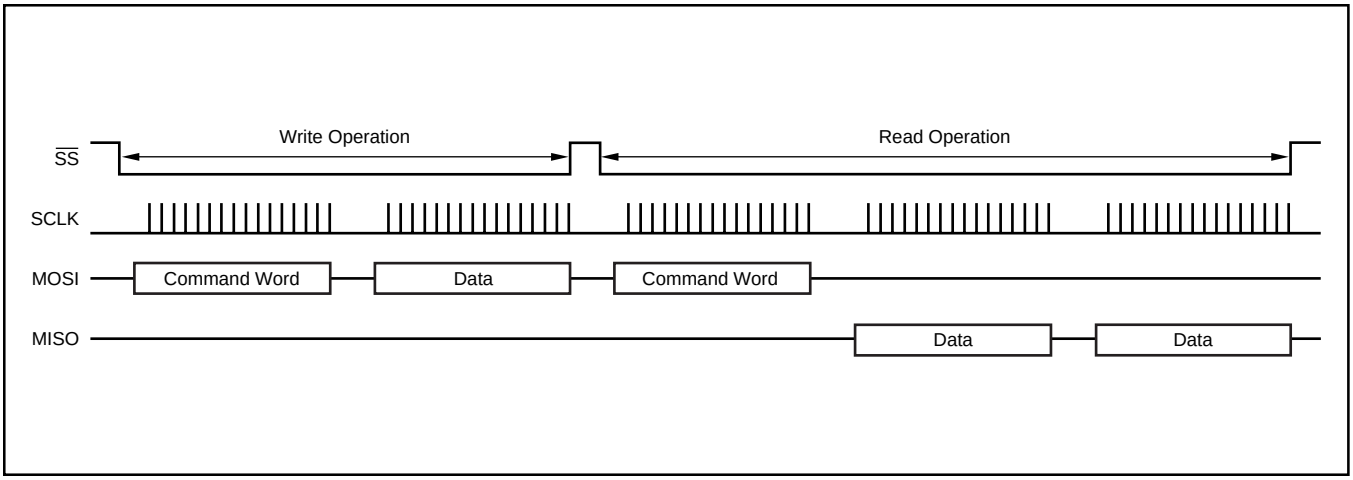


FIGURE 7. Write and Read Operation of TSC2200 Interface.

TSC2200 CONTROL REGISTERS

This section will describe each of the registers that were shown in the memory map of Table III. The registers are grouped according to the function they control. Note that in the TSC2200, bits in control registers may refer to slightly different functions depending upon if you are reading the register or writing to it. A summary of all registers and bit locations is shown in Table IV.

PAGE	ADDR (HEX)	REGISTER NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	RESET VALUE (HEX)
0	00	X	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	01	Y	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	02	Z_1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	03	Z_2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	04	KPDATA	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0	0000
0	05	BAT1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	06	BAT2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	07	AUX1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	08	AUX2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	09	TEMP1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	0A	TEMP2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
0	0B	DAC	X	X	X	X	X	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0	007F
0	0C	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	0D	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	0E	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	0F	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	10	ZERO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
0	11	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	12	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	13	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	14	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	15	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	16	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	17	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	18	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	19	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1A	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1B	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1C	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1D	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1E	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
0	1F	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	00	ADC	PSM	STS	AD3	AD2	AD1	AD0	RS1	RS0	AV1	AV0	CL1	CL0	PV2	PV1	PV0	x	4000
1	01	KEY	STC	SCS	DB2	DB1	DB0	X	X	X	X	X	X	X	X	X	X	X	4000
1	02	DACCTL	DPD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8000
1	03	REF	X	X	X	X	X	X	X	X	X	X	X	INT	DL1	DL0	PND	RFV	0002
1	04	RESET	1	0	1	1	1	0	1	1	X	X	X	X	X	X	X	X	FFFF
1	05	CONFIG	1	1	1	1	1	1	1	1	1	DAVB	PR2	PR1	PR0	SN2	SN1	SN0	FFC0
1	06	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	07	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	08	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	09	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0A	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0B	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0C	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0D	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0E	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	0F	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	10	KPMASK	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	0000
1	11	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	12	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	13	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	14	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	15	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	16	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	17	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	18	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	19	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1A	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1B	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1C	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1D	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1E	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
1	1F	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF

NOTE: X = Don't Care.

TABLE IV. Register Summary for TSC2200.

TSC2200 A/D CONVERTER CONTROL REGISTER (PAGE 1, ADDRESS 00_H)

The A/D converter in the TSC2200 is shared between all the different functions. A control register determines which input is selected, as well as other options. The result of the conversion is placed in one of the result registers in Page 0 of memory, depending upon the function selected.

The A/D Converter Control Register controls several aspects of the A/D converter. The register is formatted as shown in Table VI.

Bit 15: PSM—Pen Status/Control Mode. Reading this bit allows the host to determine if the screen is touched. Writing to this bit determines the mode used to read coordinates: host controlled, or under control of the TSC2200 responding to a screen touch. When reading, the PENSTS bit indicates if the pen is down or not. When writing to this register, this bit determines if the TSC2200 controls the reading of coordinates, or if the coordinate conversions are host-controlled. The default state is host-controlled conversions (0).

PSM		
READ/WRITE	**VALUE**	**DESCRIPTION**
Read	0	No Screen Touch Detected
Read	1	Screen Touch Detected
Write	0	Conversions Controlled by Host
Write	1	Conversions Controlled by TSC2200

TABLE V. PSM Bit Operation.

Bit 14: STS—A/D Converter Status. When reading, this bit indicates if the converter is busy, or if conversions are complete and data is available. Writing a 0 to this bit will cause touch screen scans to continue until either the pen is lifted or the process is stopped. Continuous scans or conversions can be stopped by writing a 1 to this bit. This will immediately halt a conversion (even if the pen is still down) and cause the A/D converter to power down. The default state is continuous conversions, but if this bit is read after a reset or power-up, it will read 1.

STS		
READ/WRITE	**VALUE**	**DESCRIPTION**
Read	0	Converter is Busy
Read	1	Conversions are Complete, Data is Available
Write	0	Normal Operation
Write	1	Stop Conversion and Power Down

TABLE VII. STS Bit Operation.

Bits [13:10]: AD3–AD0—A/D Converter Function Select. These bits control which input is to be converted, and what mode the converter is placed in. These bits are the same whether reading or writing. A complete listing of how these bits are used is shown in Table VIII.

Bits[9:8]: RS1, RS0—Resolution Control. The A/D converter resolution is specified with these bits. A description of these bits is shown in Table IX. These bits are the same whether reading or writing.

RS1	RS0	FUNCTION
0	0	12-Bit Resolution. Power up and reset default.
0	1	8-Bit Resolution
1	0	10-Bit Resolution
1	1	12-Bit Resolution

TABLE IX. A/D Converter Resolution Control.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
PSM	STS	AD3	AD2	AD1	AD0	RS1	RS0	AV1	AV0	CL1	CL0	PV2	PV1	PV0	X

TABLE VI. A/D Converter Control Register.

A/D3	A/D2	A/D1	A/D0	FUNCTION
0	0	0	0	Invalid. No registers will be updated. This is the default state after a reset.
0	0	0	1	Touch screen scan function: X and Y coordinates converted and the results returned to the X and Y data registers. Scan continues until either the pen is lifted or a stop bit is sent.
0	0	1	0	Touch screen scan function: X, Y, Z_1, and Z_2 coordinates converted and the results returned to the X, Y, Z_1, and Z_2 data registers. Scan continues until either the pen is lifted or a stop bit is sent.
0	0	1	1	Touch screen scan function: X coordinate converted and the results returned to the X data register.
0	1	0	0	Touch screen scan function: Y coordinate converted and the results returned to the Y data register.
0	1	0	1	Touch screen scan function: Z_1 and Z_2 coordinates converted and the results returned to the Z_1 and Z_2 data registers.
0	1	1	0	Battery Input 1 converted and the results returned to the BAT1 data register.
0	1	1	1	Battery Input 2 converted and the results returned to the BAT2 data register.
1	0	0	0	Auxiliary Input 1 converted and the results returned to the AUX1 data register.
1	0	0	1	Auxiliary Input 2 converted and the results returned to the AUX2 data register.
1	0	1	0	A temperature measurement is made and the results returned to the temperature measurement 1 data register.
1	0	1	1	Port scan function: Battery Input 1, Battery Input 2, Auxiliary Input 1, and Auxiliary Input measurements are made and the results returned to the appropriate data registers.
1	1	0	0	A differential temperature measurement is made and the results returned to the temperature measurement 2 data register.
1	1	0	1	Turn on X+, X– drivers.
1	1	1	0	Turn on Y+, Y– drivers.
1	1	1	1	Turn on Y+, X– drivers.

TABLE VIII. A/D Converter Function Select.

Bits[7:6]: AV1, AV0—Converter Averaging Control. These two bits allow you to specify the number of averages the converter will perform, as shown in Table X. Note that when averaging is used, the STS bit and the $\overline{DAV}$ output will indicate that the converter is busy until all conversions necessary for the averaging are complete. The default state for these bits is 00, selecting no averaging. These bits are the same whether reading or writing.

AV1	AV0	FUNCTION
0	0	None
0	1	4 Data Averages
1	0	8 Data Averages
1	1	16 Data Averages

TABLE X. A/D Conversion Averaging Control.

Bits[5:4]: CL1, CL0—Conversion Clock Control. These two bits specify the internal clock rate which the A/D converter uses when performing a single conversion, as shown in Table XI. These bits are the same whether reading or writing.

CL1	CL0	FUNCTION
0	0	8MHz Internal Clock Rate—8-Bit Resolution Only
0	1	4MHz Internal Clock Rate—10-Bit Resolution Only
1	0	2MHz Internal Clock Rate
1	1	1MHz Internal Clock Rate

TABLE XI. A/D Converter Clock Control.

Bits [3:1]: PV2 – PV0—Panel Voltage Stabilization Time control. These bits allow you to specify a delay time from the time a pen touch is detected to the time a conversion is started. This allows you to select the appropriate settling time for the touch panel used. Table XII shows the settings of these bits. The default state is 000, indicating a 0ms stabilization time. These bits are the same whether reading or writing.

Bit 0: This bit is not used, and is a "don't care" when writing. It will always read as a zero.

PV2	PV1	PV0	FUNCTION
0	0	0	0µs Stabilization Time
0	0	1	100µs Stabilization Time
0	1	0	500µs Stabilization Time
0	1	1	1ms Stabilization Time
1	0	0	5ms Stabilization Time
1	0	1	10ms Stabilization Time
1	1	0	50ms Stabilization Time
1	1	1	100ms Stabilization Time

TABLE XII. Panel Voltage Stabilization Time Control.

D/A CONVERTER CONTROL REGISTER (PAGE 1, ADDRESS 02_H)

The single bit in this register controls the power down control of the onboard D/A converter. This register is formatted as shown in Table XIII.

Bit 15: DPD—D/A Converter Power Down. This bit controls whether the D/A converter is powered up and operational, or powered down. If the D/A converter is powered down, the A_{OUT} pin will neither sink nor source current.

DPD	
VALUE	DESCRIPTION
0	D/A Converter is Powered and Operational
1	D/A Converter is Powered Down

TABLE XIV. DPD Bit Operation.

REFERENCE REGISTER (PAGE 1, ADDRESS 03_H)

The TSC2200 has a register to control the operation of the internal reference. This register is formatted as shown in Table XV.

Bit 4: $\overline{INT}$—Internal Reference Mode. If this bit is written to a 1, the TSC2200 will use its internal reference; if this bit is a zero, the part will assume an external reference is being supplied. The default state for this bit is to select an external reference (0). This bit is the same whether reading or writing.

$\overline{INT}$	
VALUE	DESCRIPTION
0	External Reference Selected
1	Internal Reference Selected

TABLE XVI. $\overline{INT}$ Bit Operation.

Bits [3:2]: DL1, DL0—Reference Power-Up Delay. When the internal reference is powered up, a finite amount of time is required for the reference to settle. If measurements are made before the reference has settled, these measurements will be in error. These bits allow for a delay time for measurements to be made after the reference powers up, thereby assuring that the reference has settled. Longer delays will be necessary depending upon the capacitance present at the REF pin (see Typical Characteristics).

See Table XVII for the delays. The default state for these bits is 00, selecting a 0µs delay. These bits are the same whether reading or writing.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
DPD	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

TABLE XIII. D/A Converter Control Register.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
X	X	X	X	X	X	X	X	X	X	X	INT	DL1	DL0	PDN	RFV

TABLE XV. Reference Register.

DL1	DL0	DELAY TIME
0	0	0µs
0	1	100µs
1	0	500µs
1	1	1000µs

TABLE XVII. Reference Power-Up Delay Settings.

Bit 1: PDN—Reference Power Down. If a 1 is written to this bit, the internal reference will be powered down between conversions. If this bit is a zero, the internal reference will be powered at all times. The default state is to power down the internal reference, so this bit will be a 1. This bit is the same whether reading or writing.

PDN	
VALUE	**DESCRIPTION**
0	Internal Reference is Powered at All Times
1	Internal Reference is Powered Down Between Conversions

TABLE XVIII. PDN Bit Operation.

Note that the PDN bit, in concert with the $\overline{INT}$ bit, creates a few possibilities for reference behavior. These are detailed in Table XIX.

INT	PDN	REFERENCE BEHAVIOR
0	0	External Reference Used, Internal Reference Powered Down
0	1	External Reference Used, Interenal Reference Powered Down
1	0	Internal Reference Used, Always Powered Up
1	1	Internal Reference Used, Will Power Up During Conversions and Then Power Down

TABLE XIX. Reference Behavior Possibilities.

Bit 0: RFV—Reference Voltage control. This bit selects the internal reference voltage, either 1.25V or 2.5V. The default value is 1.25V. This bit is the same whether reading or writing.

RFV	
VALUE	**DESCRIPTION**
0	1.25V Reference Voltage
1	2.5V Reference Voltage

TABLE XX. RFV Bit Operation.

TSC2200 CONFIGURATION CONTROL REGISTER (PAGE 1, ADDRESS 05_H)

This control register controls the configuration of the precharge and sense times for the touch detect circuit. The register is formatted as shown in Table XXI.

Bit 6: DAVB = Data Available. This bit mirrors the operation of the $\overline{DAV}$ pin. When any conversion is complete, the $\overline{DAV}$ pin and this bit will be a logic 0 (LOW). It will stay LOW until the register(s) updated by the conversion have been read. When all updated data has been read by the host, the $\overline{DAV}$ pin and this bit will return to a logic 1 (HIGH).

DAVB	
VALUE	**DESCRIPTION**
0	Data from A/D conversion is available. This will stay at 0 until the host has read all updated registers.
1	No new data is available.

TABLE XXII. PDN Bit Operation.

Bits [5:3]: PRE[2:0]—Precharge Time Selection. These bits set the amount of time allowed for precharging any pin capacitance on the touch screen prior to sensing if a screen touch is happening.

PRE[2:0]			
PRE2	**PRE1**	**PRE0**	**TIME**
0	0	0	20µs
0	0	1	84µs
0	1	0	276µs
0	1	1	340µs
1	0	0	1.044ms
1	0	1	1.108ms
1	1	0	1.300ms
1	1	1	1.364ms

TABLE XXIII. Precharge Times.

Bits [2:0]: SNS[2:0]—Sense Time Selection. These bits set the amount of time the TSC2200 will wait to sense a screen touch between coordinate axis conversions in $\overline{PENIRQ}$-controlled mode.

SNS[2:0]			
SNS2	**SNS1**	**SNS0**	**TIME**
0	0	0	32µs
0	0	1	96µs
0	1	0	544µs
0	1	1	608µs
1	0	0	2.080ms
1	0	1	2.144ms
1	1	0	2.592ms
1	1	1	2.656ms

TABLE XXIV. Sense Times.

TSC2200 KEYPAD REGISTERS

The Keypad scanner hardware in the TSC2200 is controlled by two registers: the Keypad Control register and the Keypad Mask register. The Keypad Control register controls general keypad functions such as scanning and de-bouncing, whereas the Keypad Mask register allows certain keys to be masked from being detected at all.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
X	X	X	X	X	X	X	X	X	X	PRE2	PRE1	PRE0	SNS2	SNS1	SNS0

TABLE XXI. Configuration Control Register.

KEYPAD CONTROL REGISTER (PAGE 1, ADDRESS 01_H)

The Keypad Control register is formatted as shown in Table XXV.

Bit 15: STC = Keyboard Status. This bit reflects the operation of the $\overline{KBIRQ}$ pin, with inverted logic. This bit will go HIGH when a key is pressed and de-bounced. The default value for this bit is zero.

STC	
VALUE	**DESCRIPTION**
0	No Keys Are Pressed
1	Keys Pressed and De-Bounced

TABLE XXVI. STC Bit Operation.

Bit 14: SCS = Keyboard Scan Status. When reading, this bit indicates if the scanner or de-bouncer is busy or if scans are complete and data is available. Writing a zero to this bit will cause keyboard scans to continue until either the key is lifted or the process is stopped. Continuous scans can be stopped by writing a 1 to this bit. This will immediately halt a conversion (even if a key is still down). The default value for this bit when read is 1.

SCS		
READ/WRITE	**VALUE**	**DESCRIPTION**
Read	0	Scanner or De-Bouncer Busy
Read	1	Scans are Complete, Data is Available
Write	0	Normal Operation
Write	1	Stop Scans

TABLE XXVII. SCS Bit Operation.

Bits [13:11]: KBDB2-KBDB0 = Keyboard De-Bounce Control. These bits set the length of the de-bounce time for the keypad, as shown in Table XXVIII. The default setting is a 2ms de-bounce time (000).

KBDB2	KBDB1	KBDB0	FUNCTION
0	0	0	De-Bounce: 2ms
0	0	1	De-Bounce: 10ms
0	1	0	De-Bounce: 20ms
0	1	1	De-Bounce: 50ms
1	0	0	De-Bounce: 60ms
1	0	1	De-Bounce: 80ms
1	1	0	De-Bounce: 100ms
1	1	1	De-Bounce: 120ms

TABLE XXVIII. Keypad De-Bounce Control.

KEYPAD MASK REGISTER (PAGE 1, ADDRESS 10_H)

The Keypad Mask register is formatted as shown in Table XXIX. This is the same format as used in the Keypad Data register (Page 0, Address 04_H). Each bit in these registers represents one key on the keypad. In the Mask register, if a bit is set (1), then that key will not be detected in keyboard scans. Pressing that key on the keypad will also not cause a $\overline{KBIRQ}$, if the bit is set. If the bit is cleared (0), the corresponding key will be detected. A 16-key keypad is mapped into the Keypad Mask (and Keypad Data) register, as shown in Table XXX. The default value for this register is 0000_H, detecting all key presses.

	C1	C2	C3	C4
R1	K0	K1	K2	K3
R2	K4	K5	K6	K7
R3	K8	K9	K10	K11
R4	K12	K13	K14	K15

TABLE XXX. Keypad to Key Bit Mapping.

The result of a keypad scan will appear in the Keypad Data register. Each bit will be set in this register, corresponding to the key(s) actually pressed. For example, if only KEY1 was pressed on a particular scan, the data in the register would read as 0002_H; however, if keys 6, 8, and 13 were all pressed simultaneously on that scan, the data would read as 2140_H.

Multiple keys may be pressed simultaneously, and will generally be decoded correctly by the keypad scan circuitry. However, keys that land on three corners of a rectangle may cause a false reading of a key on the fourth corner of the rectangle. For example, if 0, 3, and 11 were pressed simultaneously, the KEY0, KEY3, and KEY11 bits will be set, but the KEY8 bit will also be set. Thus, when considering using multiple-key combinations in an application, try to avoid combinations that put three keys on the corners of a rectangle.

RESET REGISTER (PAGE 1, ADDRESS 04_H)

The TSC2200 has a special register, the RESET register, which allows a software reset of the device. Writing the code $BBXX_H$, as shown in Table XXXI, to this register will cause the TSC2200 to reset all its registers to their default, power-up values.

Writing any other values to this register will do nothing. Reading this register or any reserved register will result in reading back all 1's, or $FFFF_H$.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
STC	SCS	DB2	DB1	DB0	X	X	X	X	X	X	X	X	X	X	X

TABLE XXV. Keypad Control Register.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

TABLE XXIX. Keypad Mask Register.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
1	0	1	1	1	0	1	1	X	X	X	X	X	X	X	X

TABLE XXXI. Reset Register.

TSC2200 DATA REGISTERS

The data registers of the TSC2200 hold data results from conversions or keypad scans, or the value of the D/A converter output current. All of these registers default to 0000_H upon reset, except the D/A converter register, which is set to 0080_H, representing the midscale output of the D/A converter.

X, Y, Z_1, Z_2, BAT1, BAT2, AUX1, AUX2, TEMP1, AND TEMP2 REGISTERS

The results of all A/D conversions are placed in the appropriate data register (see Tables III and VIII). The data format of the result word, R, of these registers is right-justified, as shown in Table XXXII.

KEYPAD DATA REGISTER (PAGE 0, ADDRESS 04_H)

The Keypad Data register (Page 0, Address 04_H) is formatted as shown in Table XXXIII.

This is the same format as used in the Keypad Mask register (Page 1, Address 10_H). Each bit in these registers represents one key on the keypad. A 16-key keypad is mapped into the Keypad Data register, see Table XXIX.

D/A CONVERTER DATA REGISTER (PAGE 0, ADDRESS $0B_H$)

The data to be written to the D/A converter is written into the D/A converter data register, which is formatted as shown in Table XXXIV.

ZERO REGISTER (PAGE 0, ADDRESS 10_H)

This is a reserved data register, but instead of reading all 1's ($FFFF_H$), when read will return all 0's (0000_H).

OPERATION—TOUCH SCREEN MEASUREMENTS

As noted previously in the discussion of the A/D converter, several operating modes can be used, which allow great flexibility for the host processor. These different modes will now be examined.

Conversion Controlled by TSC2200 Initiated at Touch Detect

In this mode, the TSC2200 will detect when the touch panel is touched and cause the $\overline{\text{PENIRQ}}$ line to go LOW. At the same time, the TSC2200 will start up its internal clock. It will then turn on the Y-drivers, and after a programmed Panel Voltage Stabilization time, power up the A/D converter and convert the Y-coordinate. If averaging is selected, several conversions may take place; when data averaging is complete, the Y-coordinate result will be stored in the Y-register.

If the screen is still touched at this time, the X-drivers will be enabled, and the process will repeat, but instead measuring the X-coordinate and storing the result in the X-register.

If only X- and Y-coordinates are to be measured, then the conversion process is complete. See Figure 8 for a flowchart for this process. The time it takes to go through this process depends upon the selected resolution, internal conversion clock rate, averaging selected, panel voltage stabilization time, and precharge and sense times.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	R11 MSB	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0 LSB

TABLE XXXII. Result Data Format.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0

TABLE XXXIII. Keypad Data Register.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
X	X	X	X	X	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0

TABLE XXXIV. D/A Converter Register.

The time needed to get a complete X/Y-coordinate reading can be calculated by:

(3)

$$t_{COORDINATE} = 2.5\mu s + 2(t_{PVS} + t_{PRE} + t_{SNS}) + 2N_{AVG}\left(N_{BITS} \bullet \frac{1}{f_{CONV}} + 4.4\mu s\right)$$

where,

$t_{COORDINATE}$ = Time to Complete X/Y-Coordinate Reading

t_{PVS} = Panel Voltage Stabilization time (see Table XII)

t_{PRE} = Precharge time (see Table XXII)

t_{SNS} = Sense time (see Table XXIII)

N_{AVG} = Number of Averages (see Table X); for no averaging, N_{AVG} = 1

N_{BITS} = Number of Bits of Resolution (see Table IX)

f_{CONV} = A/D Converter Clock Frequency (see Table XI)

If the pressure of the touch is also to be measured, the process will continue in the same way, but measuring the Z_1 and Z_2 values, and placing them in the Z_1 and Z_2 registers (see Figure 9). As before, this process time depends upon the settings described above. The time for a complete X, Y, Z_1, and Z_2 coordinate reading is given by:

(4)

$$t_{COORDINATE} = 4.75\mu s + 3(t_{PVS} + t_{PRE} + t_{SNS}) + 4N_{AVG}\left(N_{BITS} \bullet \frac{1}{f_{CONV}} + 4.4\mu s\right)$$

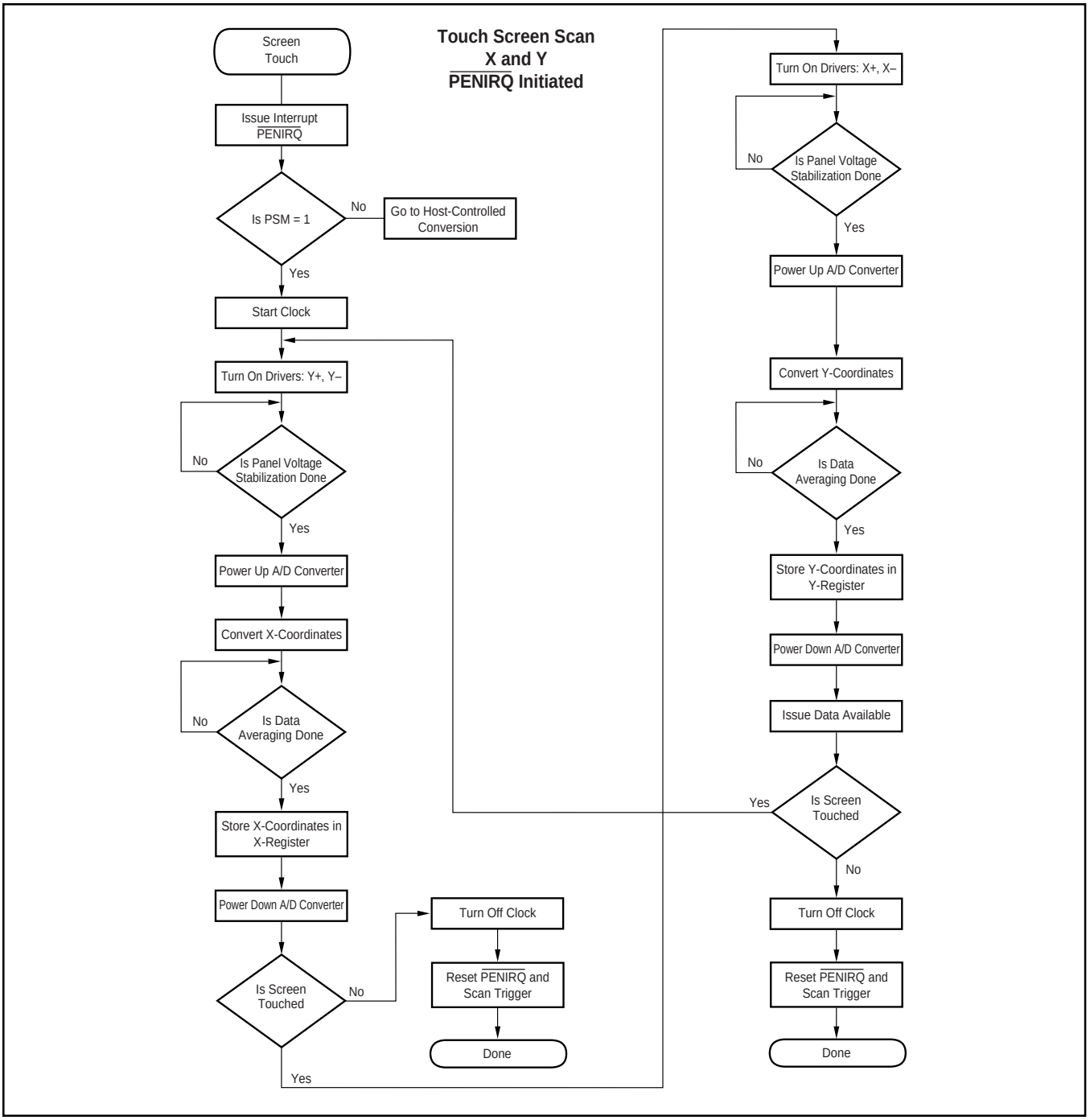


FIGURE 8. X- and Y-Coordinate Touch Screen Scan, Initiated by Touch.

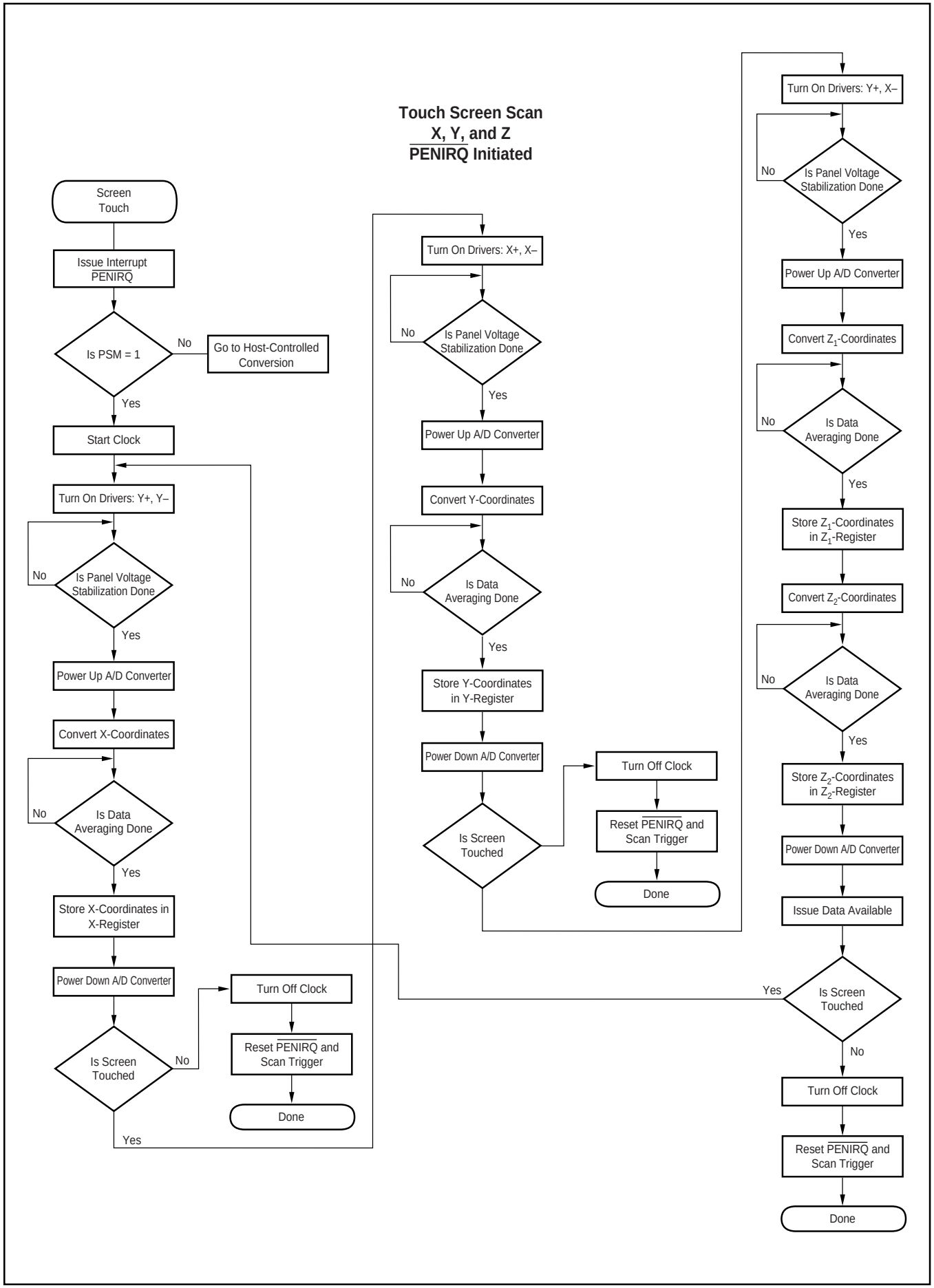


FIGURE 9. X- Y- and Z-Coordinate Touch Screen Scan, Initiated by Touch.

Conversion Controlled by TSC2200 Initiated By Host Responding to $\overline{\text{PENIRQ}}$

In this mode, the TSC2200 will detect when the touch panel is touched and cause the $\overline{\text{PENIRQ}}$ line to go LOW. The host will recognize the interrupt request, and then write to the A/D Converter Control register to select one of the touch screen scan functions. The conversion process then proceeds as described above, and as outlined in Figures 10 through 14.

The main difference between this mode and the previous mode is that the host, not the TSC2200, decides when the touch screen scan begins.

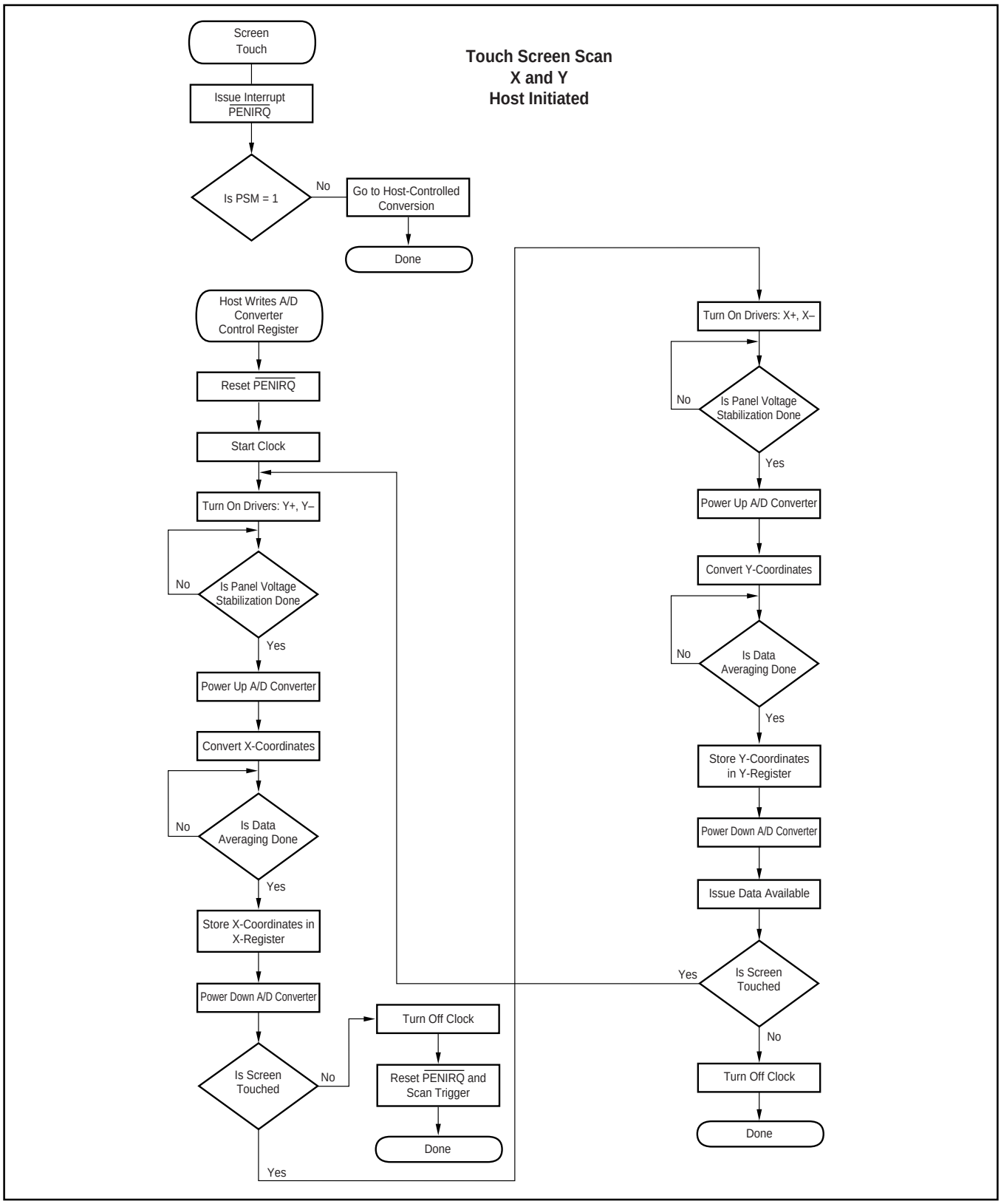


FIGURE 10. X- and Y-Coordinate Touch Screen Scan, Initiated by Host.

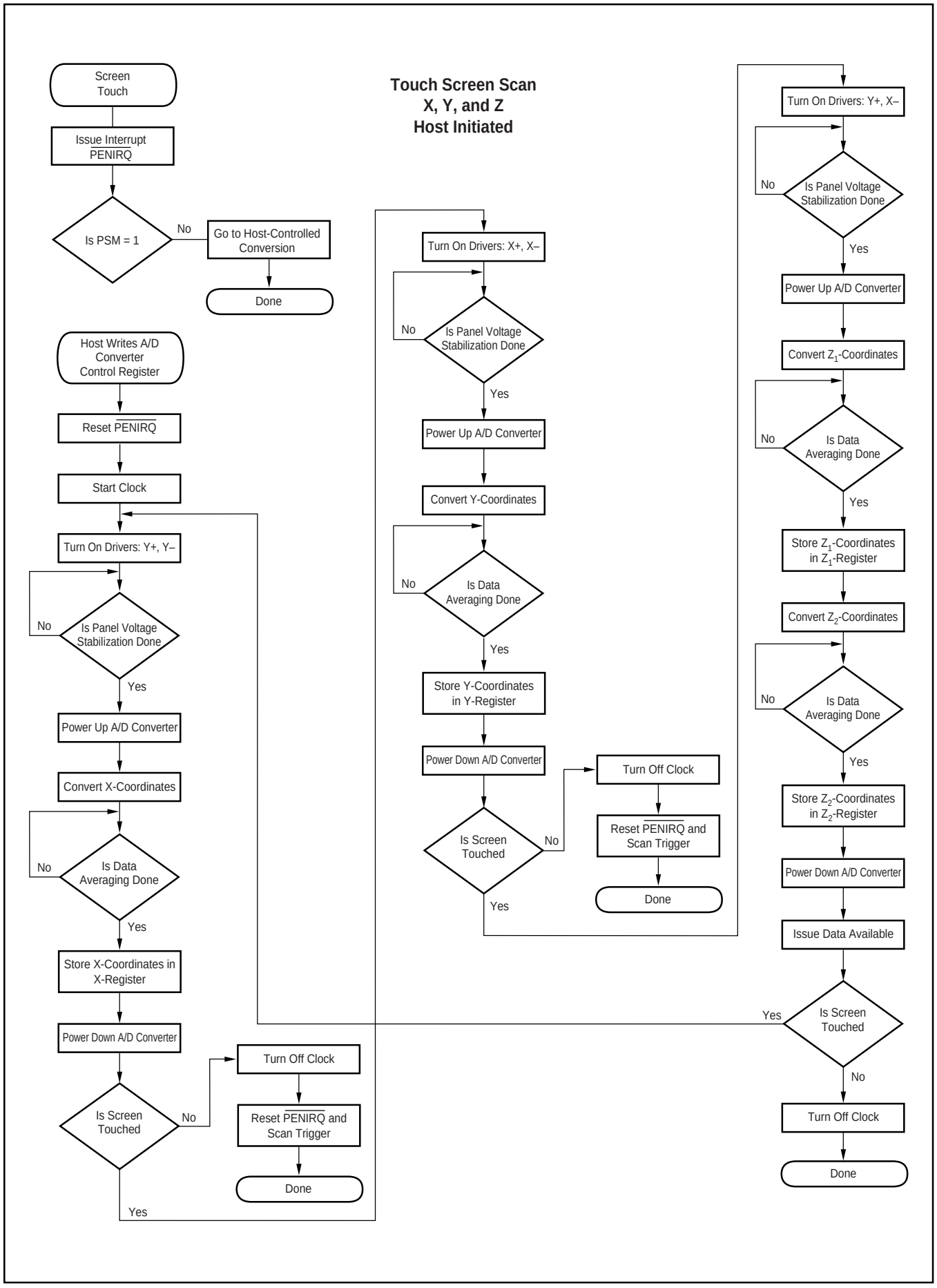


FIGURE 11. X-, Y-, and Z-Coordinate Touch Screen Scan, Initiated by Host.

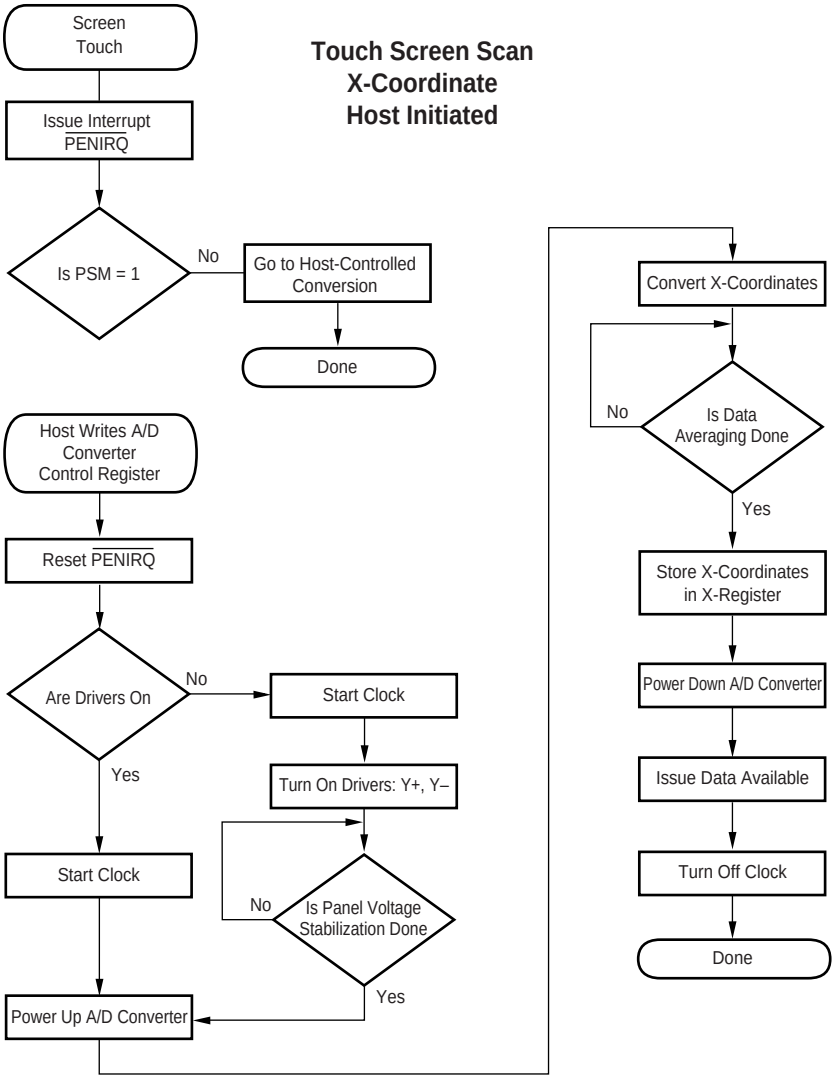


FIGURE 12. X-Coordinate Reading Initiated by Host.

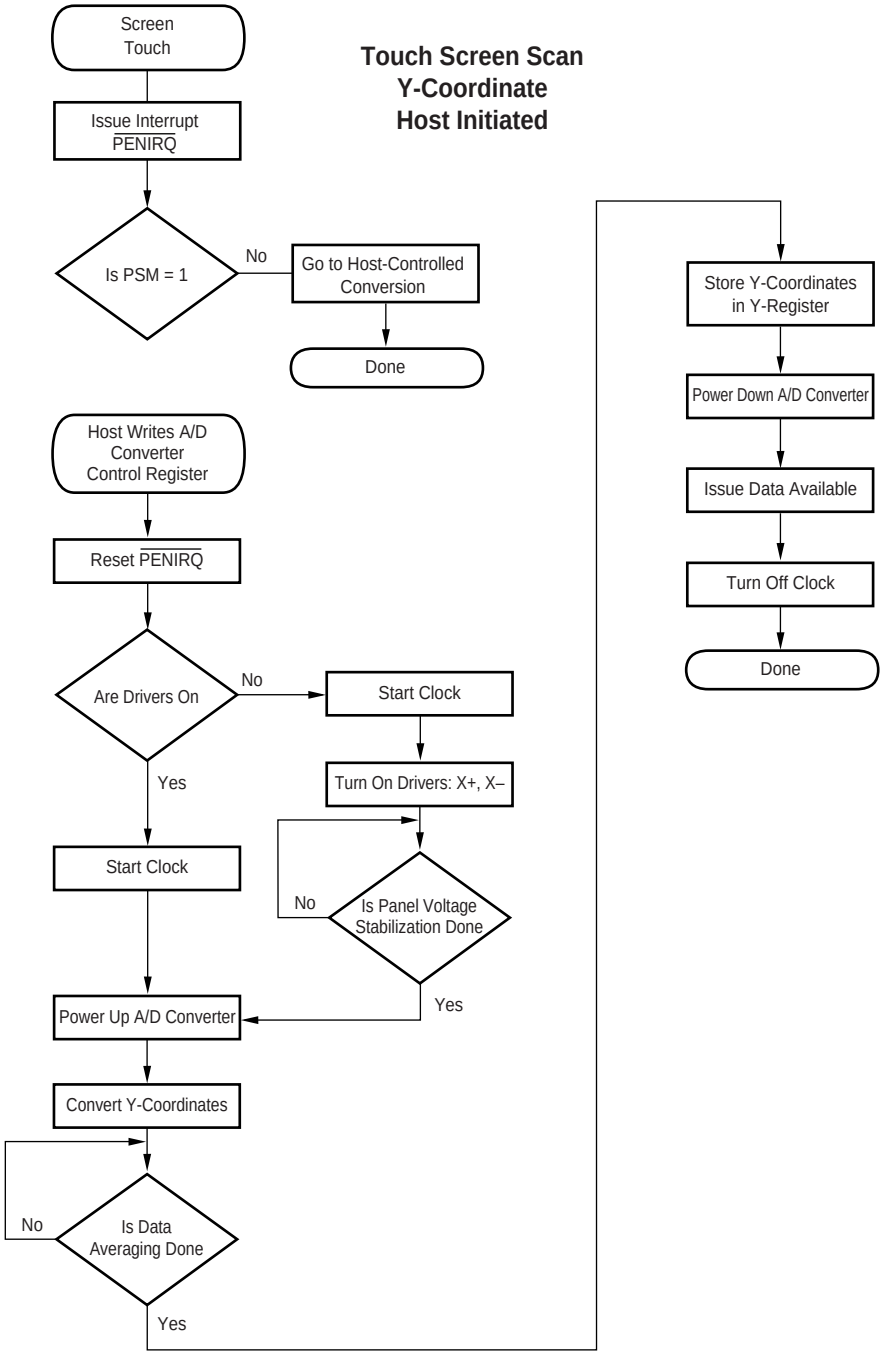


FIGURE 13. Y-Coordinate Reading Initiated by Host.

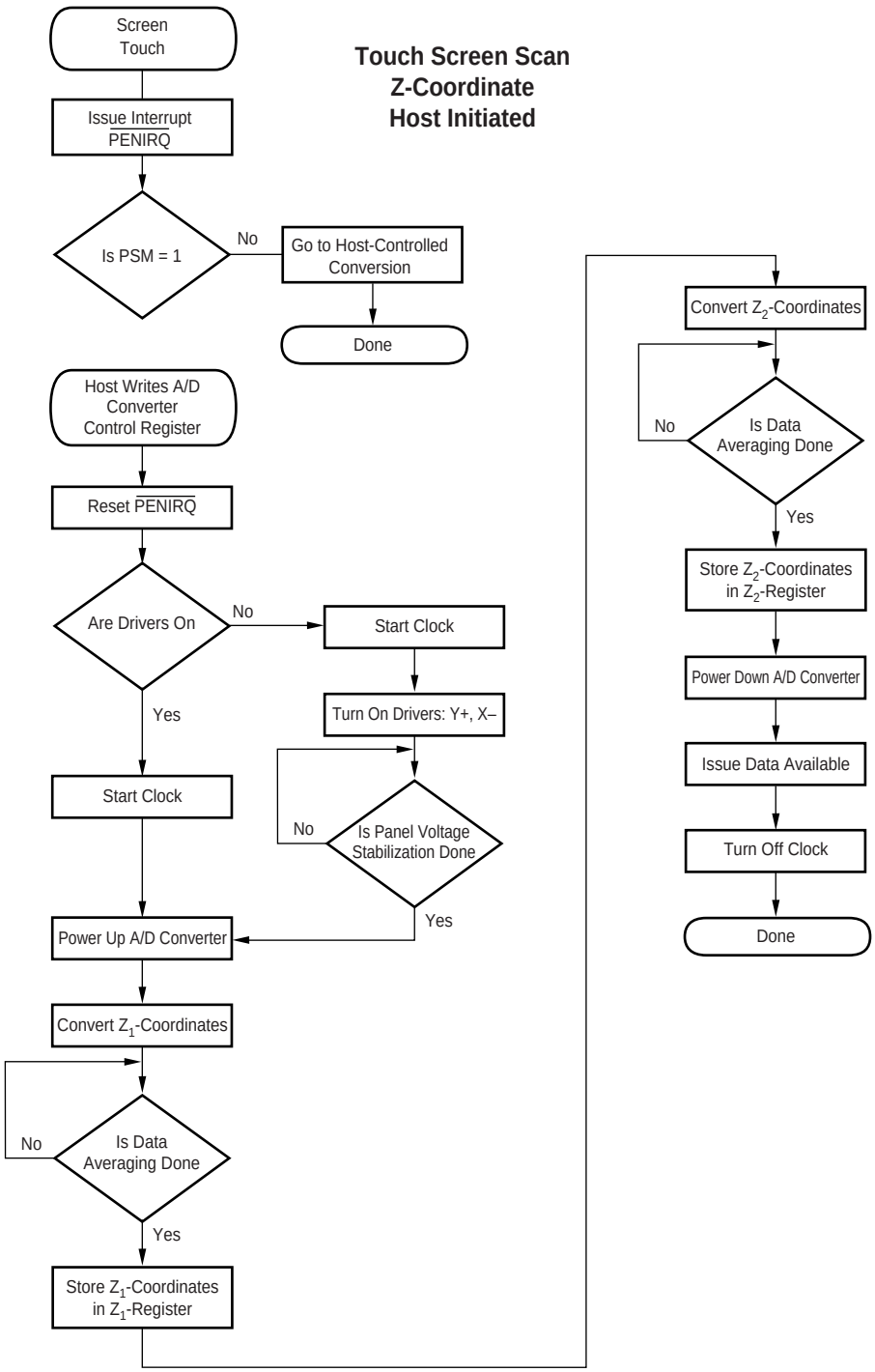


FIGURE 14. Z-Coordinate Reading Initiated by Host.

Conversion Controlled by the Host

In this mode, the TSC2200 will detect when the touch panel is touched and cause the $\overline{\text{PENIRQ}}$ line to go LOW. The host will recognize the interrupt request. Instead of starting a sequence in the TSC2200 which then reads each coordinate in turn, the host now must control all aspects of the conversion. Generally, upon receiving the interrupt request, the host will turn on the Y-drivers. After waiting for the settling time, the host will then address the TSC2200 again, this time requesting an X-coordinate conversion.

The process is then repeated for Y- and Z-coordinates. The processes are outlined in Figures 15 through 17.

The time needed to convert any single coordinate under host control (not including the time needed to send the command over the SPI bus) is given by:

(5)

$$t_{COORDINATE} = 2.125\mu s + t_{PVS} + N_{AVG}\left(N_{BITS} \bullet \frac{1}{f_{CONV}} + 4.4\mu s\right)$$

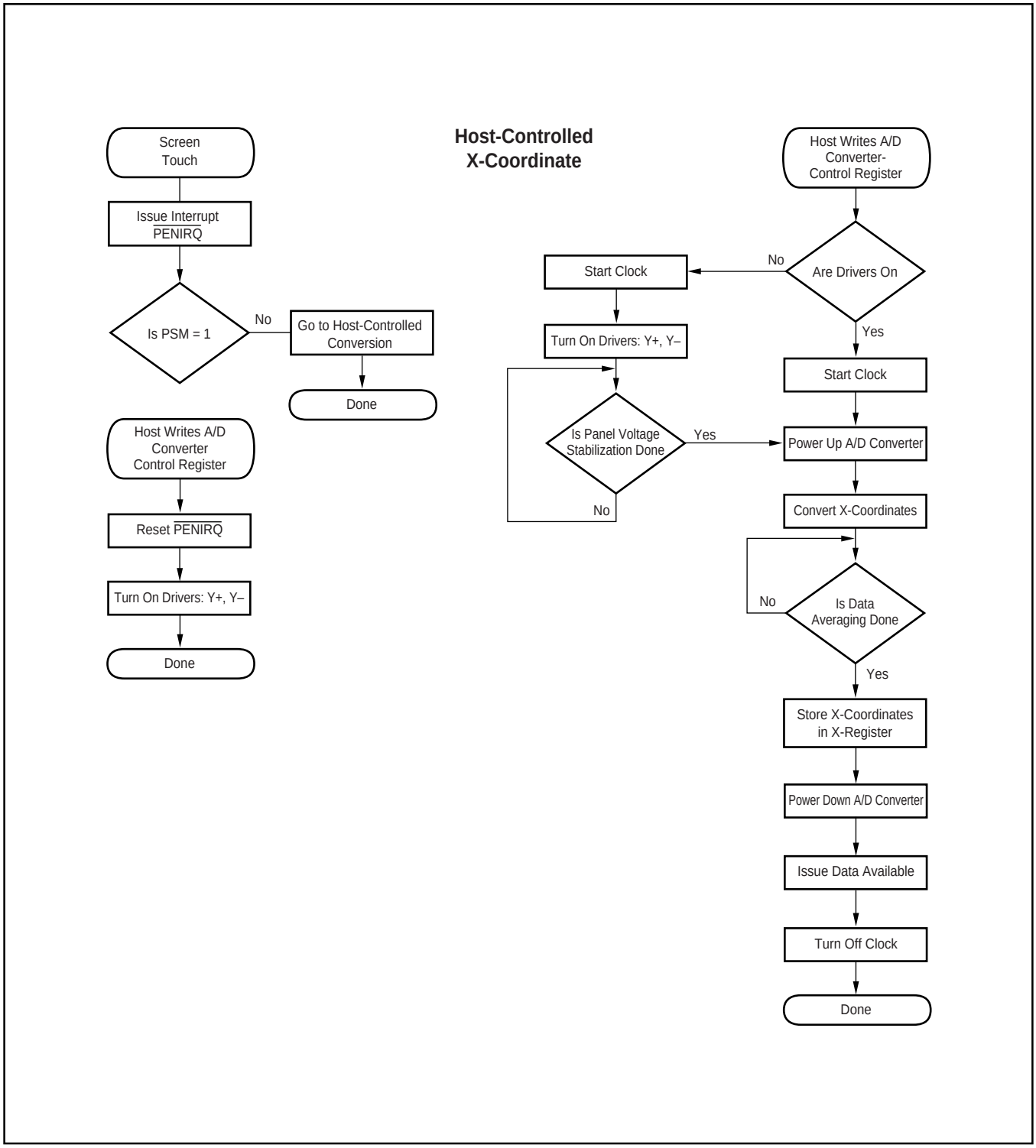


FIGURE 15. X-Coordinate Reading Controlled by Host.

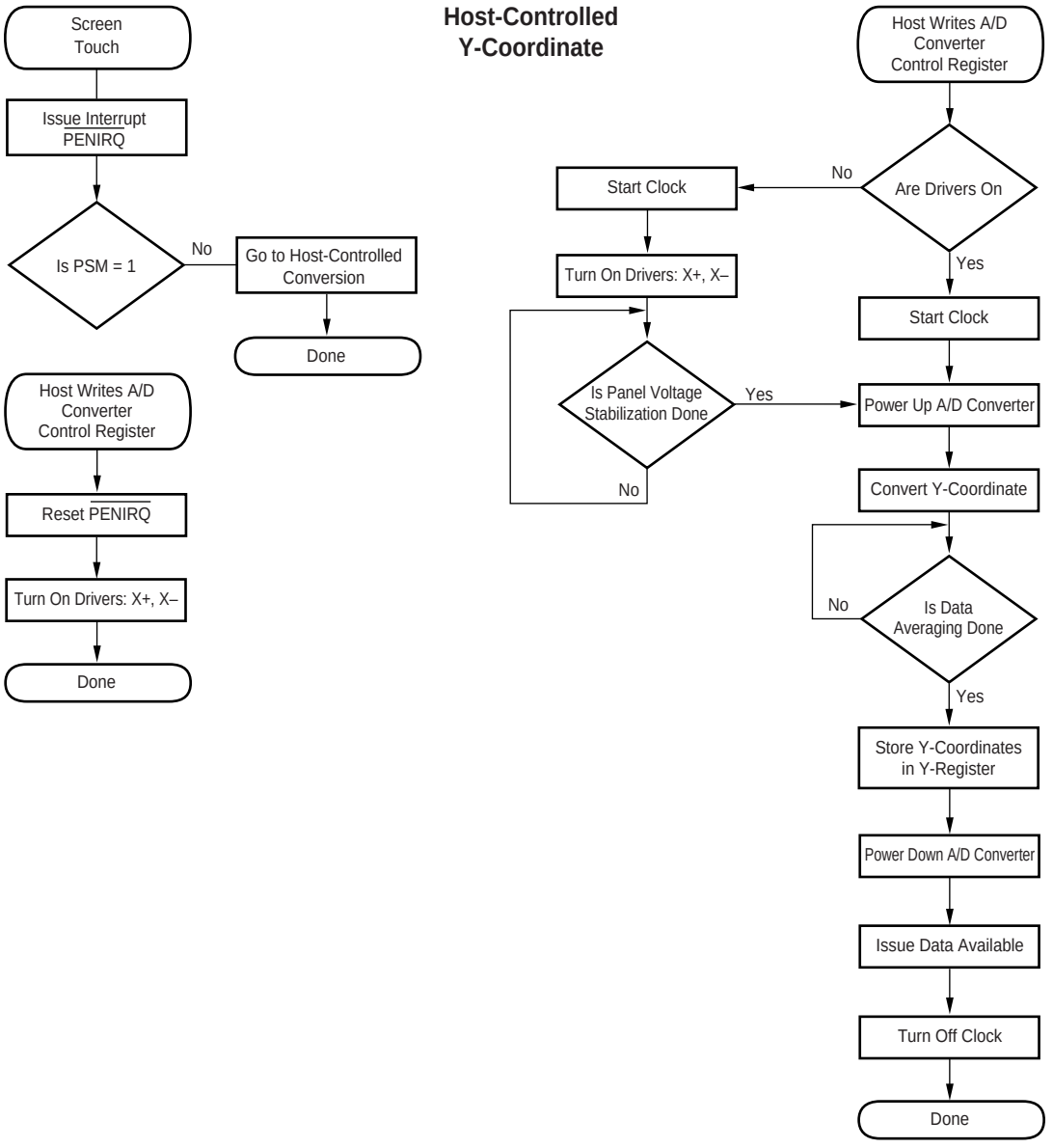


FIGURE 16. Y-Coordinate Reading Controlled by Host.

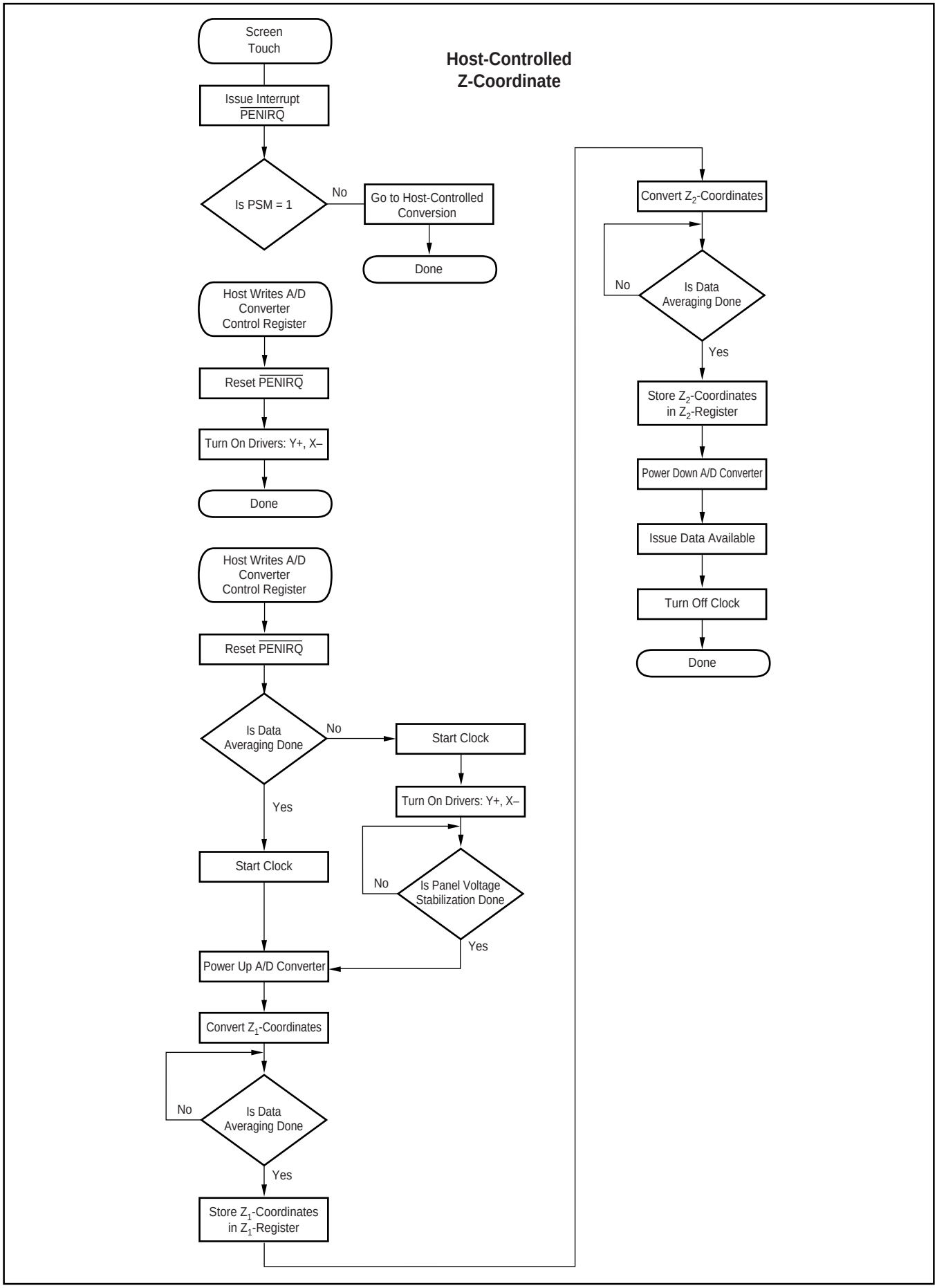


FIGURE 17. Z-Coordinate Reading Controlled by Host.

OPERATION—TEMPERATURE MEASUREMENT

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the TSC2200 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the 25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes.

The TSC2200 offers two modes of temperature measurement. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. A diode, shown in Figure 18, is used during this measurement cycle. This voltage is typically 600mV at +25°C with a 20μA current through it. The absolute value of this diode voltage can vary by a few millivolts; the temperature coefficient (TC) of this voltage is very consistent at –2.1mV/°C. During the final test of the end product, the diode voltage would be stored at a known room temperature, in system memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB. This measurement of what is referred to as Temperature 1 is illustrated in Figure 19.

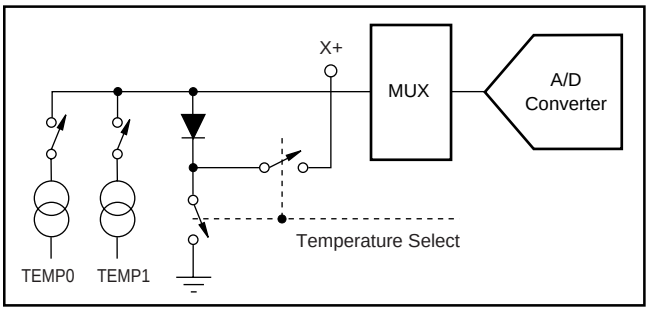


FIGURE 18. Functional Block Diagram of Temperature Measurement Mode.

The second mode does not require a test temperature calibration, but uses a two-measurement (differential) method to eliminate the need for absolute temperature calibration and for achieving 2°C/LSB accuracy. This mode requires a second conversion with a 91 times larger current. The voltage difference between the first (TEMP1) and second (TEMP2) conversion, using 91 times the bias current, will be represented by kT/q • ln (N), where N is the current ratio = 91, k = Boltzmann's constant ($1.38054 \bullet 10^{-23}$ electrons volts/degrees Kelvin), q = the electron charge ($1.602189 \bullet 10^{-19}$ °C), and T = the temperature in degrees Kelvin. This method can provide much improved absolute temperature measurement, but less resolution of 2°C/LSB. The resultant equation for solving for °K is:

$$°K = \frac{q \bullet \Delta V}{k \bullet \ln(N)} \qquad (6)$$

where,

$$\Delta V = V(I_{91}) - V(I_1) \quad (\text{in mV})$$

$$\therefore °K = 2.573 \Delta V °K/mV$$

$$°C = 2.573 \bullet \Delta V(mV) - 273°K$$

Figure 20 shows the Temperature 2 measurement.

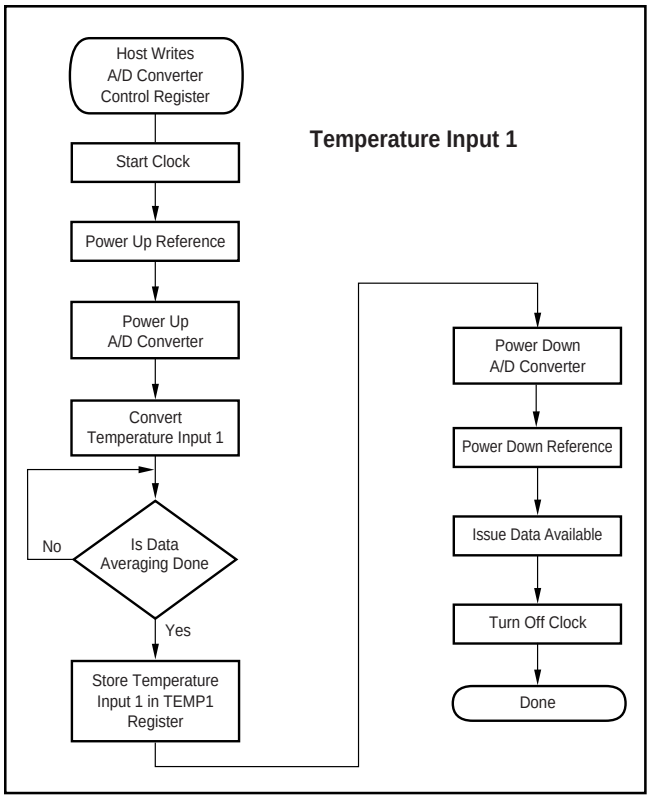


FIGURE 19. Single Temperature Measurement Mode.

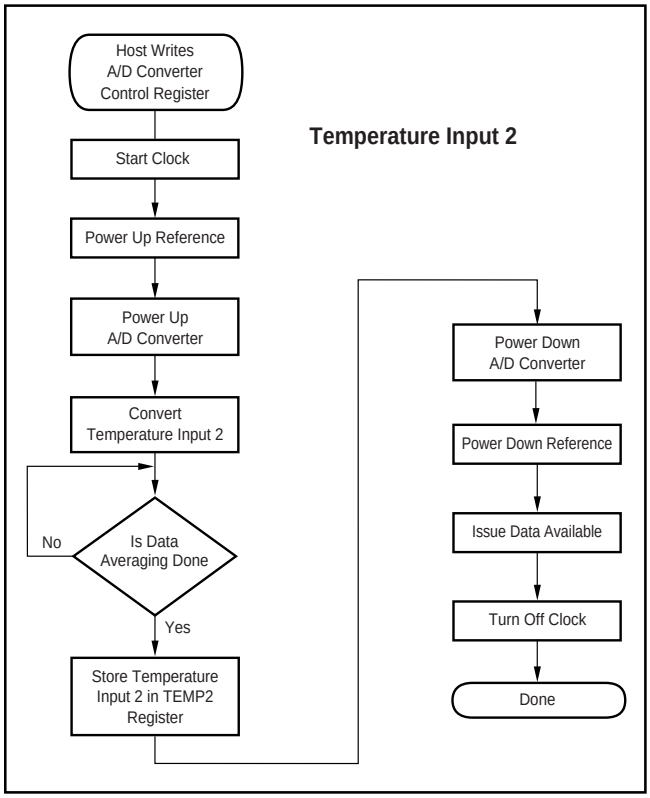


FIGURE 20. Additional Temperature Measurement for Differential Temperature Reading.

OPERATION—BATTERY MEASUREMENT

An added feature of the TSC2200 is the ability to monitor the battery voltage on the other side of a voltage regulator (DC/DC converter), as shown in Figure 21. The battery voltage can vary from 0.5V to 6V while maintaining the voltage to the TSC2200 at 2.7V, 3.3V, etc. The input voltage (V_{BAT1} or V_{BAT2}) is divided down by 4 so that a 6.0V battery voltage is represented as 1.5V to the A/D converter. This simplifies the multiplexer and control logic. In order to minimize the power consumption, the divider is only ON during the sampling of the battery input.

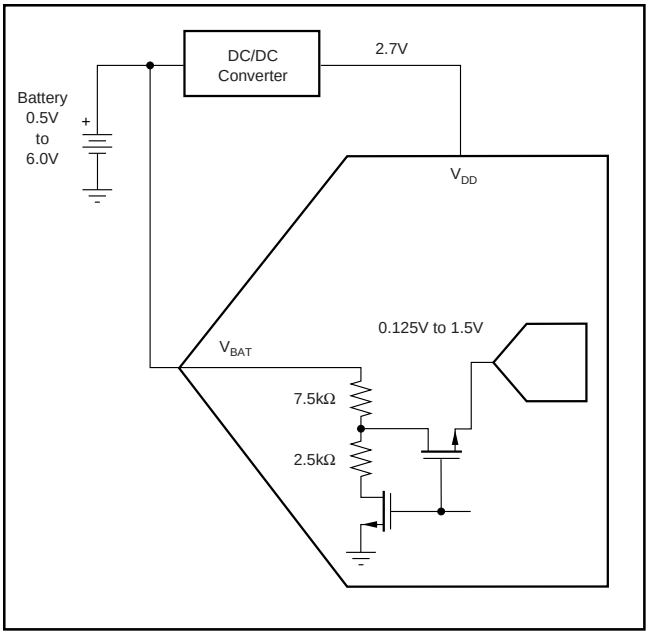


FIGURE 21. Battery Measurement Functional Block Diagram.

Flowcharts that detail the process of making a battery input reading are shown in Figures 22 and 23.

The time needed to make temperature, auxiliary, or battery measurements is given by:

(7)

$$t_{READING} = 2.625\mu s + t_{REF} + N_{AVG}\left(N_{BITS} \bullet \frac{1}{f_{CONV}} + 4.4\mu s\right)$$

where t_{REF} is the reference delay time as given in Table XVII.

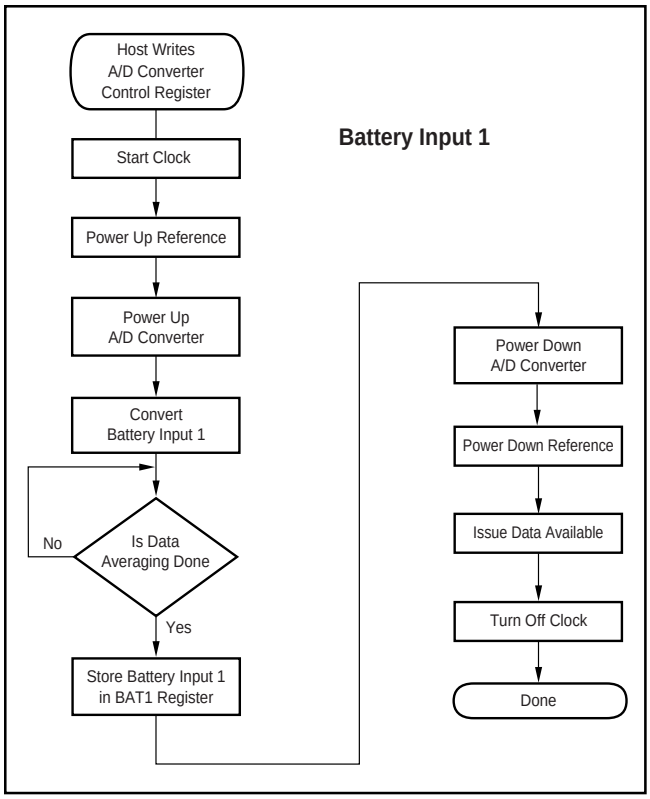


FIGURE 22. V_{BAT1} Measurement Process.

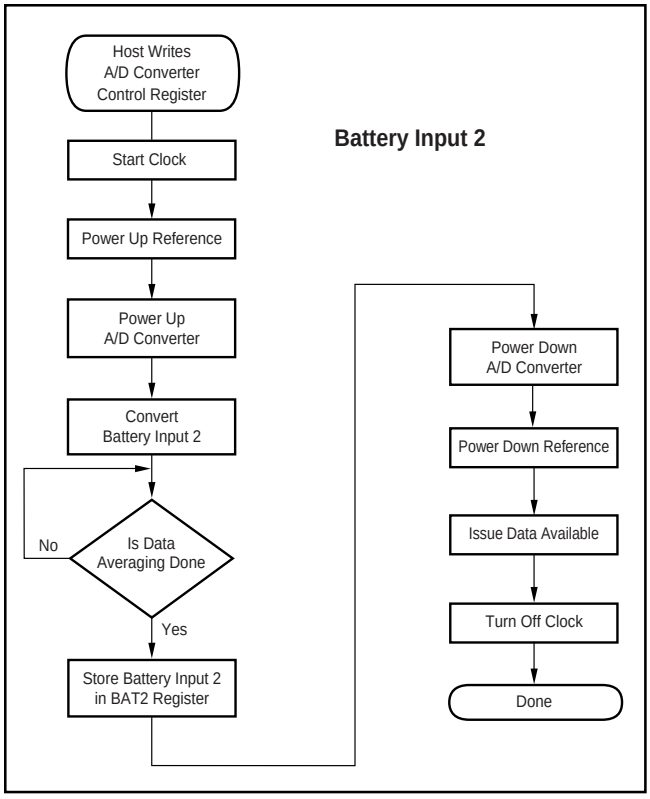


FIGURE 23. V_{BAT2} Measurement Process.

OPERATION—AUXILIARY MEASUREMENT

The two auxiliary voltage inputs can be measured in much the same way as the battery inputs, as shown in Figures 24 and 25. Applications might include external temperature sensing, ambient light monitoring for controlling the backlight, or sensing the current drawn from the battery.

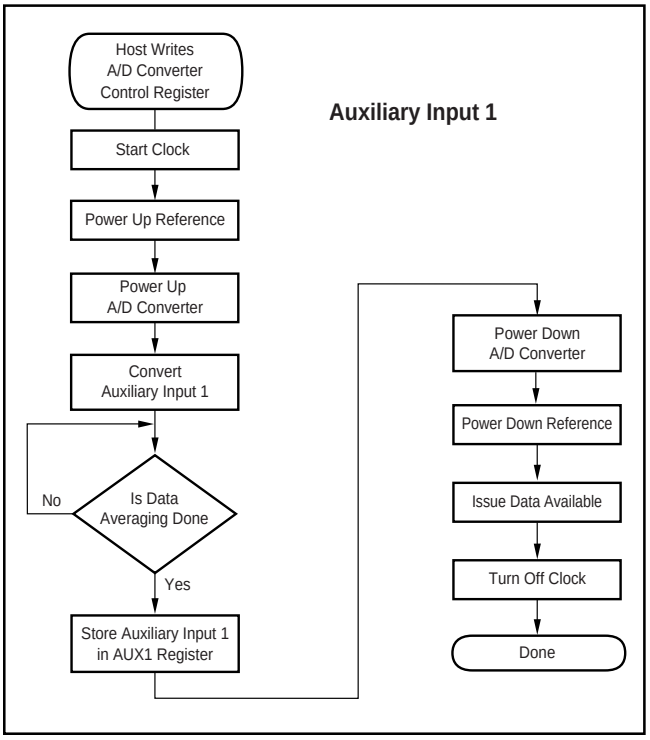


FIGURE 24. AUX1 Measurement Process.

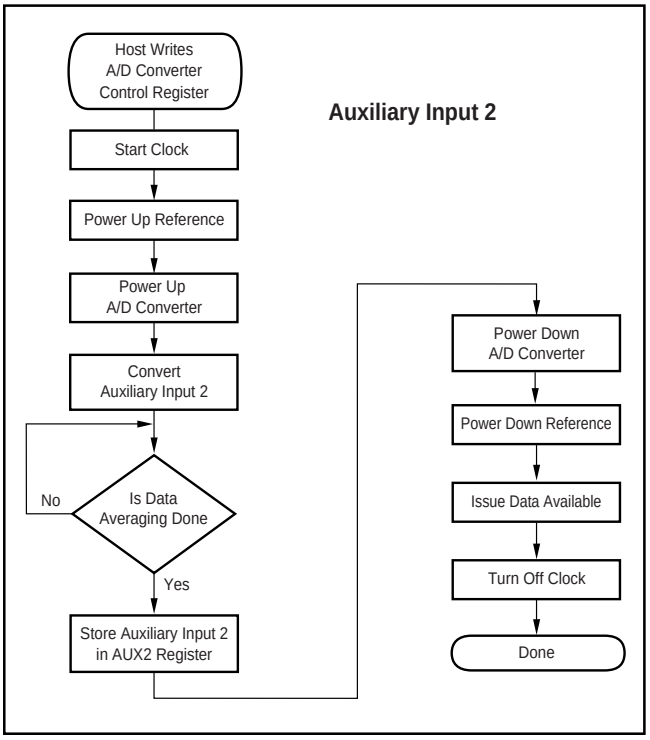


FIGURE 25. AUX2 Measurement Process.

OPERATION—PORT SCAN

If making measurements of all the analog inputs (except the touch screen) is desired on a periodic basis, the Port Scan mode can be used. This mode causes the TSC2200 to sample and convert both battery inputs and both auxiliary inputs. At the end of this cycle, the battery and auxiliary result registers will contain the latest values. Thus, with one write to the TSC2200, the host can cause four different measurements to be made.

The flowchart for this process is shown in Figure 26. The time needed to make a complete port scan is given by:

$$t_{READING} = 7.5\mu s + t_{REF} + 4N_{AVG}\left(N_{BITS} \bullet \frac{1}{f_{CONV}} + 4.4\mu s\right) \quad (8)$$

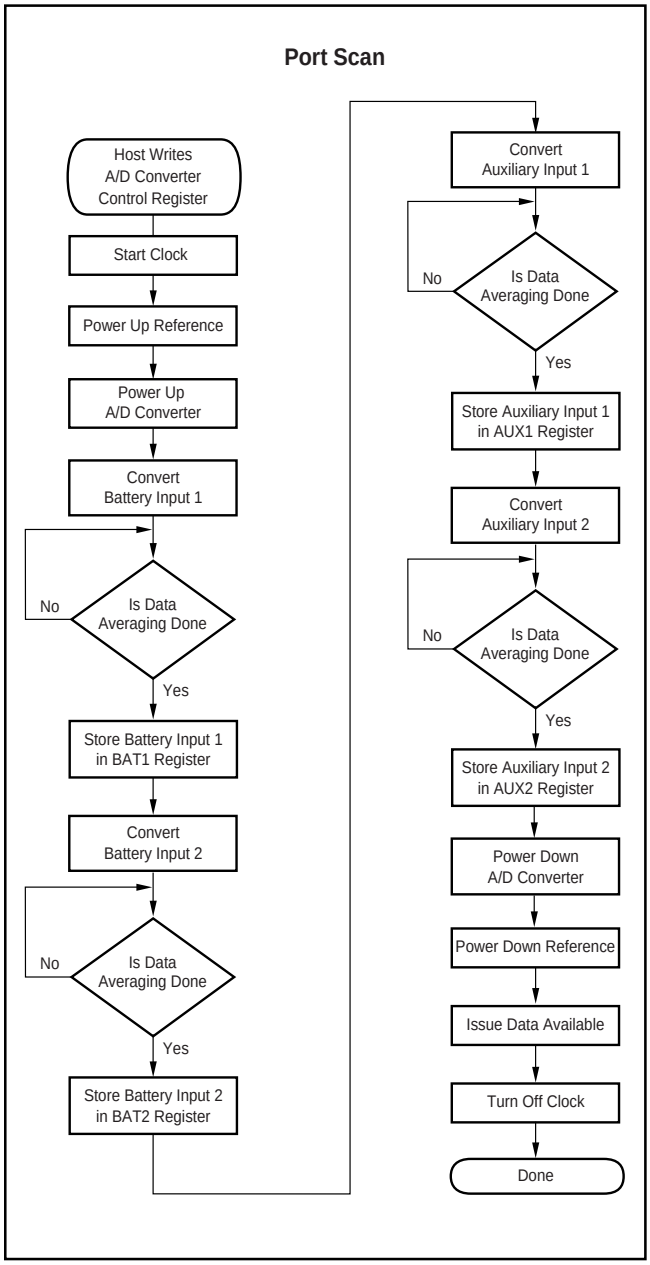


FIGURE 26. Port Scan Mode.

OPERATION—D/A CONVERTER

The TSC2200 has an onboard 8-bit D/A converter, configured as shown in Figure 27. This configuration yields a current sink (A_{OUT}) controlled by the value of a resistor connected between the ARNG pin and ground. The D/A converter has a control register that controls whether or not the converter is powered up. The 8-bit data is written to the D/A converter through the D/A converter data register.

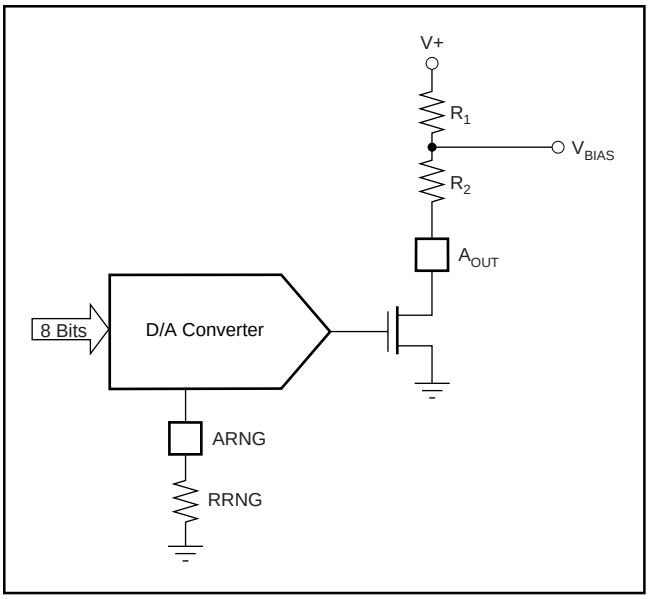


FIGURE 27. D/A Converter Configuration.

This circuit is designed for flexibility in the output voltage at the V_{BIAS} point shown in Figure 27 to accommodate the widely varying requirements for LCD contrast control bias. V+ can be a higher voltage than the supply voltage for the TSC2200. The only restriction is that the voltage on the A_{OUT} pin can never go above the absolute maximum ratings for the device, and should stay above 1.5V for linear operation.

The D/A converter has an output sink range that is limited to 1mA. This range can be adjusted by changing the value of RRNG shown in Figure 27. As this D/A converter is not designed to be a precision device, the actual output current range can vary as much as ±20%. Furthermore, the current output will change due to variations in temperature; the D/A converter has a temperature coefficient of approximately –2µA/°C. To set the full-scale current, RRNG can be determined from the graph shown in Figure 28.

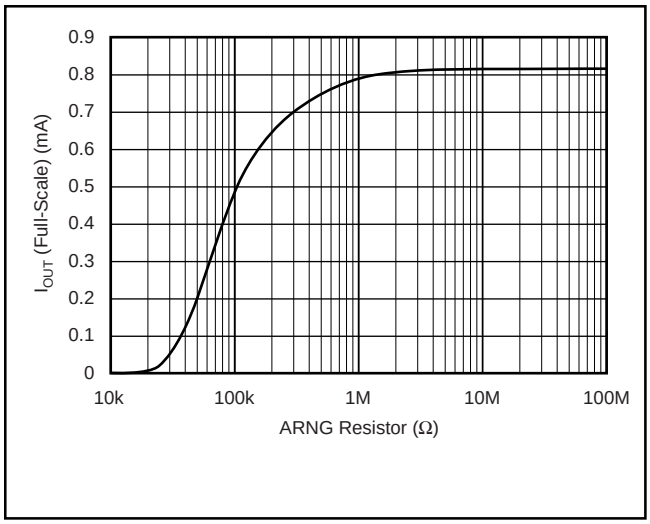


FIGURE 28. D/A Converter Output Current Range versus RRNG Resistor Value.

For example, consider an LCD that has a contrast control voltage V_{BIAS} that can range from 2V to 4V, which draws 400µA when used, and an available +5V supply. Note that this is higher than the TSC2200 supply voltage, but it is within the absolute maximum ratings.

The maximum V_{BIAS} voltage is 4V, and this occurs when the D/A converter current is 0, so only the 400µA load current I_{LOAD} will be flowing from 5V to V_{BIAS}. This means 1V will be dropped across R_1, so R_1 = 1V/400µA = 2.5kΩ.

The minimum V_{BIAS} is 2V, which occurs when the D/A converter current is at its full scale value, I_{MAX}. In this case, 5V – 2V = 3V will be dropped across R_1, so the current through R_1 will be 3V/2.5K = 1.2mA. This current is I_{MAX} + I_{LOAD} = I_{MAX} + 400uA, so I_{MAX} must be set to 800µA. Looking at Figure 28, this means that RRNG should be around 1MΩ.

Since the voltage at the A_{OUT} pin should not go below 1.5V, this limits the voltage at the bottom of R_2 to be 1.5V minimum; this occurs when the D/A converter is providing its maximum current, I_{MAX}. In this case, I_{MAX} + I_{LOAD} flows through R_1, and I_{MAX} flows through R_2. Thus,

$$R_2 I_{MAX} + R_1(I_{MAX} + I_{LOAD}) = 5V - 1.5V = 3.5V \quad (8)$$

We already have found R_1 = 2.5kΩ, I_{MAX} = 800µA, I_{LOAD} = 400µA, so we can solve this for R_2 and find that it should be 625Ω.

In the previous example, when the D/A converter current is zero, the voltage on the A_{OUT} pin will rise above the TSC2200 supply voltage. This is not a problem, however, since V+ was within the absolute maximum ratings of the TSC2200, so no special precautions are necessary. Many LCD displays require voltages much higher than the absolute maximum ratings of the TSC2200. In this case, the addition of an NPN transistor, as shown in Figure 29, will protect the A_{OUT} pin from damage.

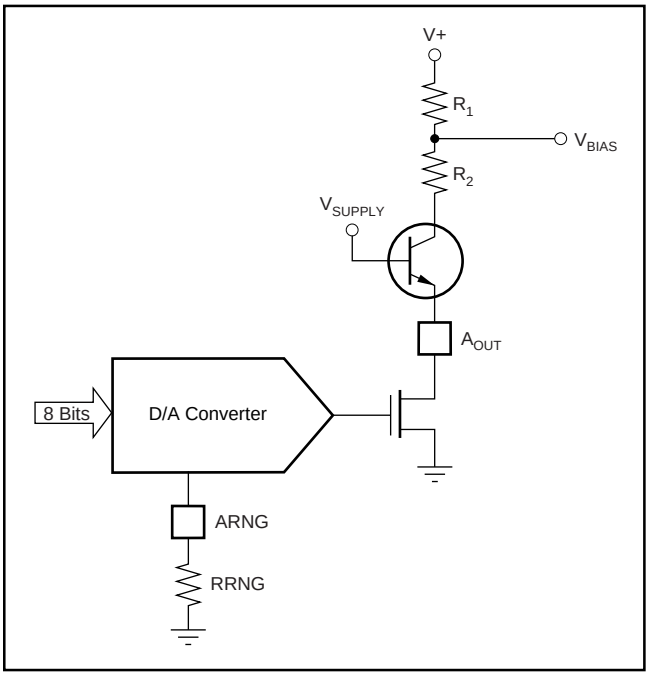


FIGURE 29. D/A Converter Circuit when Using V+ Higher than V_{SUPPLY}.

OPERATION—KEYPAD INTERFACE

The TSC2200 contains a keypad interface that is suitable for use with matrix keypads up to 4-by-4 keys. A control register, the Keypad Control Register, is used to set the scan rate for the keypad and de-bounce times. There is also a Keypad Mask register which allows certain keys to be masked from being read or causing the TSC2200 to detect a key press. The results of keyboard scans are placed in the Keypad Data register.

When a key press is detected, the TSC2200 automatically scans the keypad and de-bounces the key press. It will then drive the $\overline{\text{KBIRQ}}$ LOW. All keys pressed at the time of the scan will then be reflected in the Keypad Data Register. This mode is shown in Figure 30.

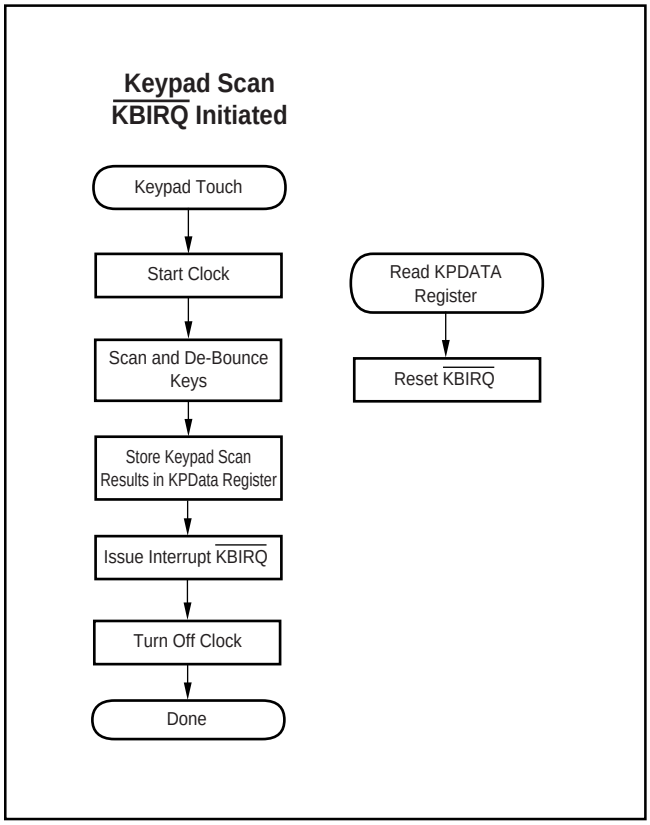


FIGURE 30. Keypad Scan Initiated by Keypress.

LAYOUT

The following layout suggestions should provide optimum performance from the TSC2200. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly “clean” power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter’s power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the TSC2200 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an ‘n-bit’ SAR converter, there are n ‘windows’ in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the SCL input.

With this in mind, power to the TSC2200 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. A 1µF to 10µF capacitor may also be needed if the impedance of the connection between $+V_{DD}$ and the power supply is HIGH.

A bypass capacitor is generally not needed because the reference is buffered by an internal op amp. If an external reference voltage originates from an op amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The TSC2200 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery-connection point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch screen applications (e.g., applications that require a back-lit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause “flickering” of the converted data. Several things can be done to reduce this error, such as utilizing a touch screen with a bottom-side metal layer connected to ground. This will couple the majority of noise to ground. Additionally, filtering capacitors, from Y+, Y–, X+, and X– to ground, can also help. Note, however, that the use of these capacitors will increase screen settling time and require longer panel voltage stabilization times, as well as increased precharge and sense times for the $\overline{\text{PENIRQ}}$ circuitry of the TSC2200.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSC2200IPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSC2200I	Samples
TSC2200IPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSC2200I	Samples
TSC2200IPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSC2200I	Samples
TSC2200IRHB	ACTIVE	VQFN	RHB	32	73	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TSC 2200I	Samples
TSC2200IRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TSC 2200I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

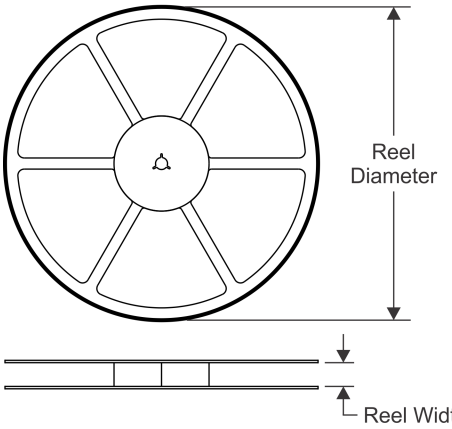
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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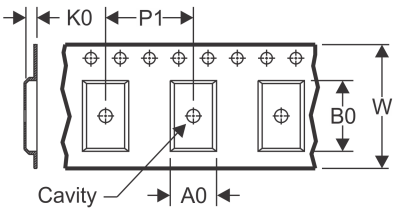
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

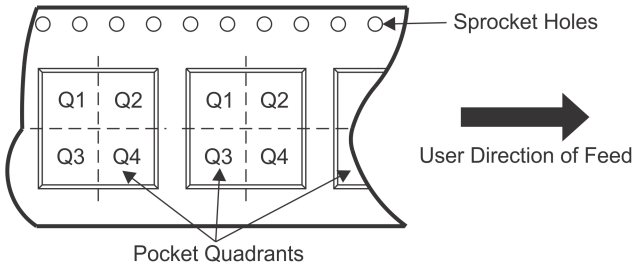


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

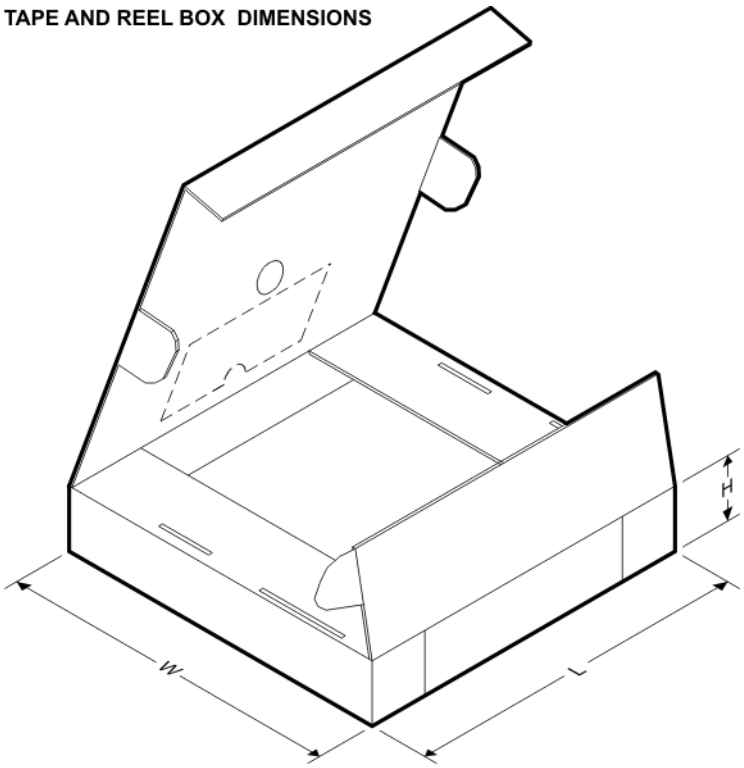
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2200IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TSC2200IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2200IPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
TSC2200IRHBR	VQFN	RHB	32	3000	350.0	350.0	43.0

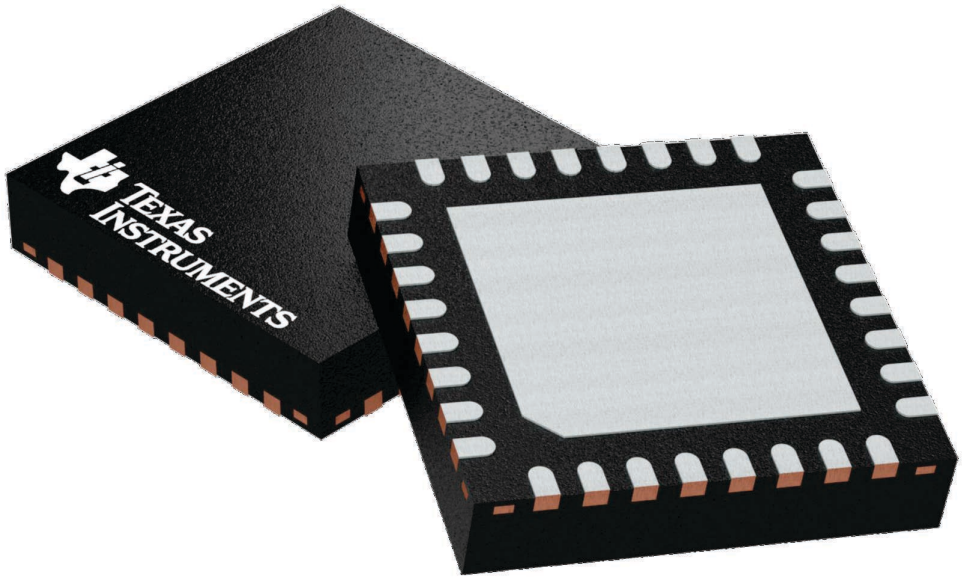
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

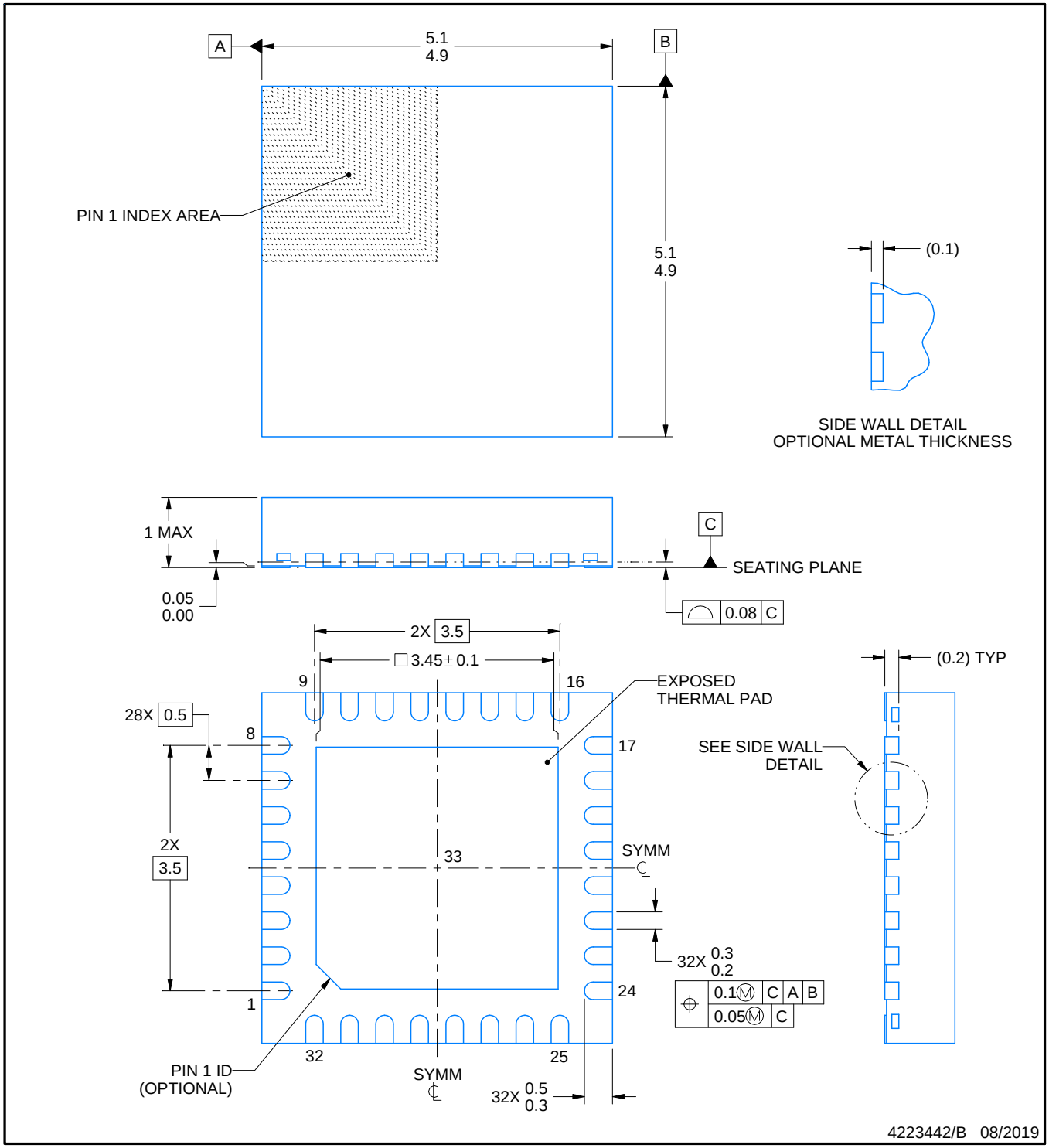
4224745/A

RHB0032E

PACKAGE OUTLINE

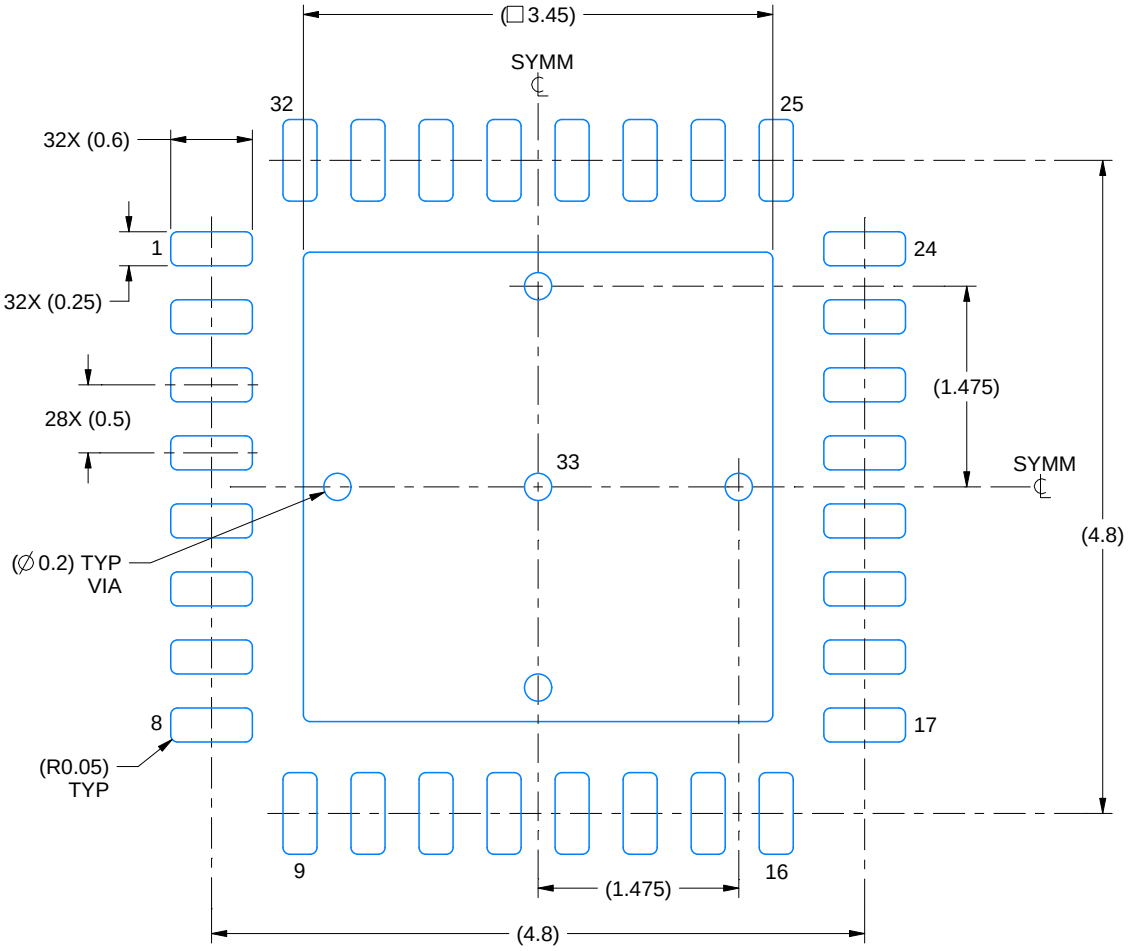
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

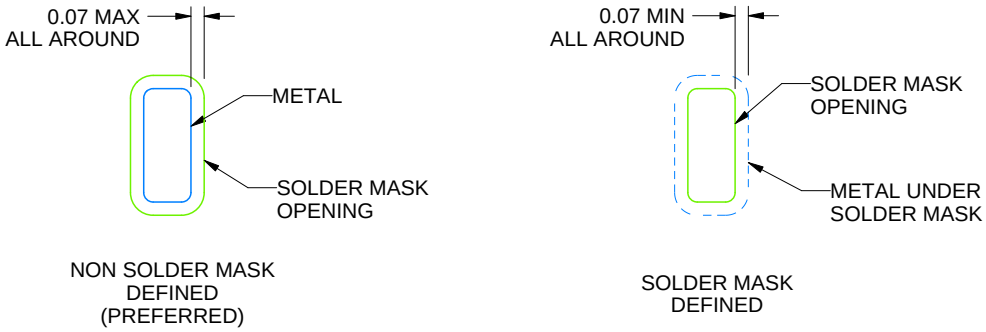


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

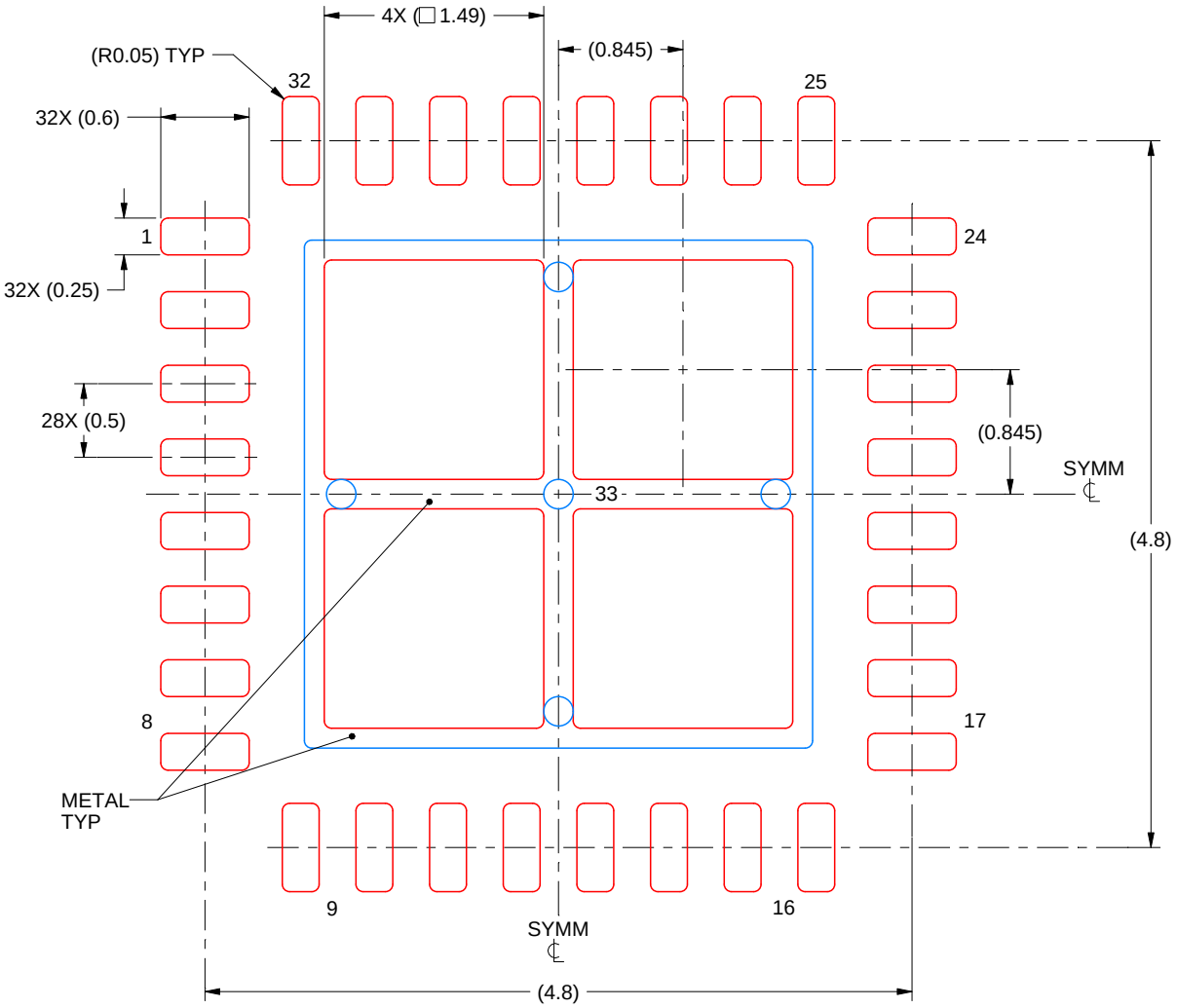


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

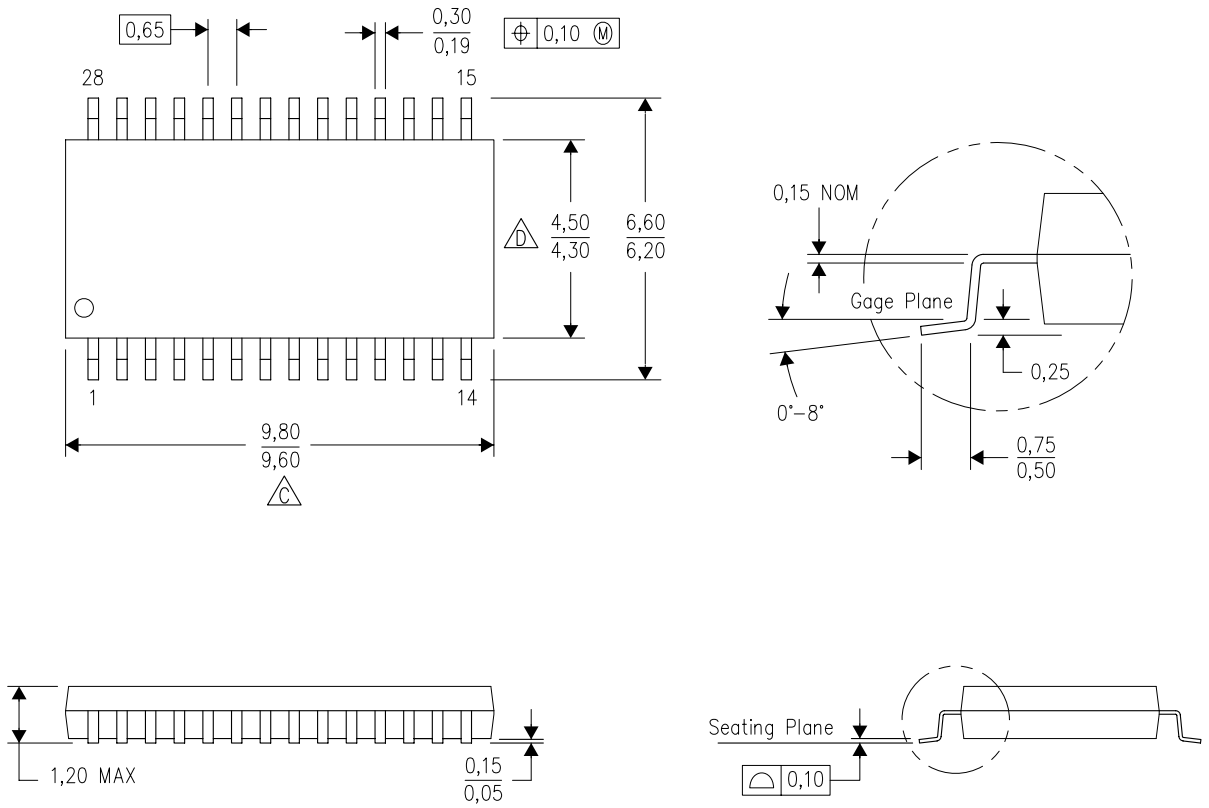
EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

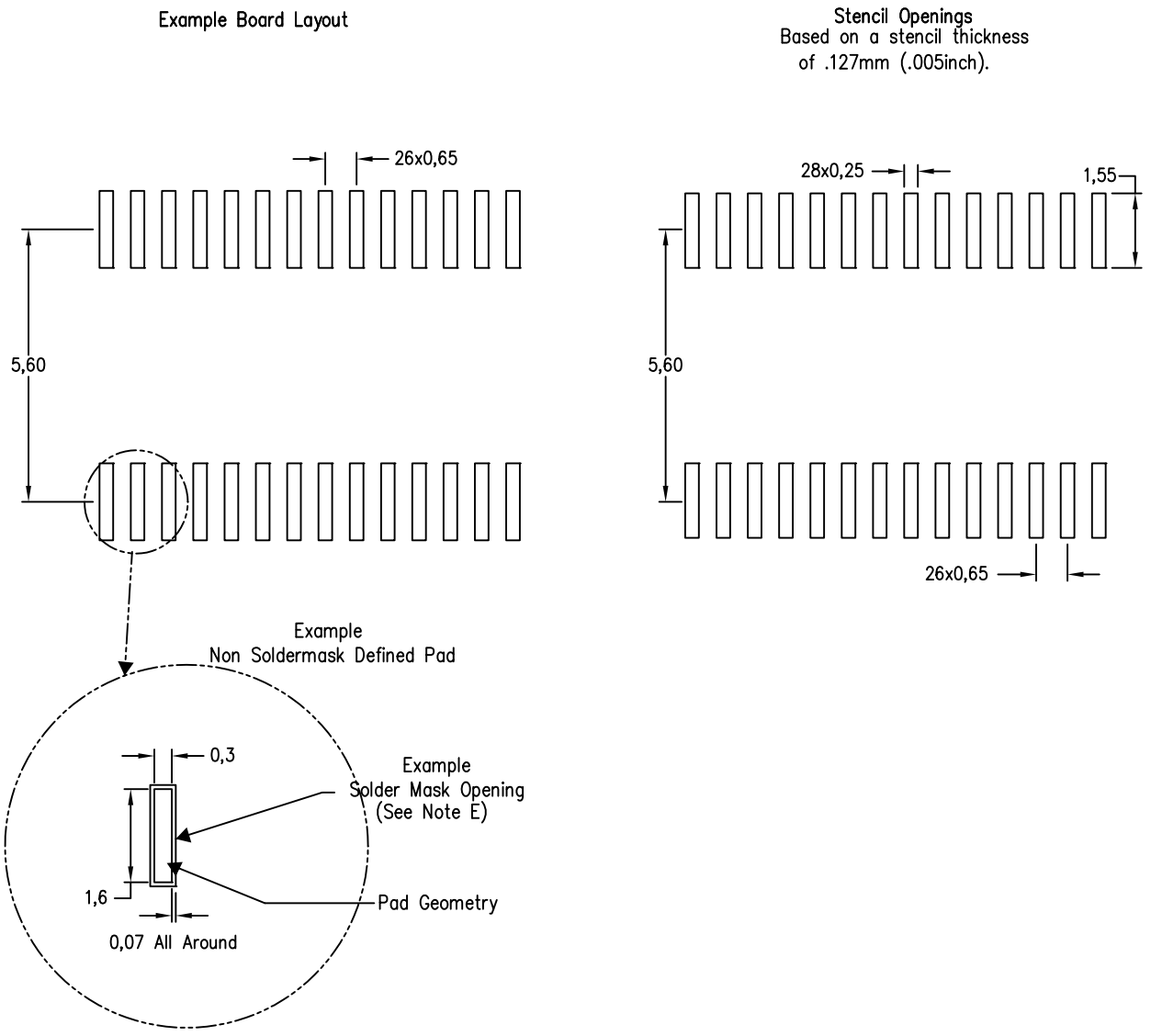
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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