PROGRAMMABLE TOUCH SCREEN CONTROLLER WITH INTEGRATED STEREO AUDIO DAC AND HEADPHONE AMPLIFIER

FEATURES

- **4-Wire Touch Screen Interface**
- **Integrated Touch Screen Processor With Fully Automated Modes of Operation**
- **Programmable Converter Resolution, Speed, and Averaging**
- **Programmable Autonomous Timing Control**
- **Direct Battery Measurement**
- **On-Chip Temperature Measurement**
- **Stereo Audio Playback Up to 48 ksps**
- **97-dB Stereo Audio Playback**
- **Integrated PLL for Audio Clock Generation**
- **Programmable Digital Audio Effects Processing**
- **Stereo Headphone Amplifier**
- **SPI™ Serial Interface**
- **Glueless Interface With OMAP™ and Xscale™ Processors**
- **Full Power-Down Control**
- **Low Power: 11-mW Stereo Audio Playback**
- **32-Pin TSSOP Package**

APPLICATIONS

- **Personal Digital Assistants**
- **Smart Cellular Phones**
- **MP3 Players**

DESCRIPTION

The TSC2102 is a highly integrated combination resistive touch screen controller with on-chip processor and audio DAC. The touch screen portion of the TSC2102 contains a 12-bit 4-wire resistive touch screen converter complete with drivers, and interfaces to the host controller through a standard SPI™ serial interface. The on-chip processor provides extensive features specifically designed to reduce host processor and bus overhead, with capabilities that include fully automated operating modes, programmable conversion resolution up to 12 bits, programmable sampling rates up to 125 kHz, programmable conversion averaging, and programmable on-chip timing generation.

The TSC2102 also features a high-performance audio DAC with 16, 20, 24, or 32-bit stereo playback functionality at up to 48 ksps. The stereo output drivers on the TSC2102 can be programmed for headphone drive or line-level drive, and support capless as well as ac-coupled output configurations. The digital audio data format is programmable to work with popular audio standard protocols (I2S, DSP, left/right justified) in master or slave mode, and also includes an on-chip PLL for flexible clock generation capability.

The TSC2102 offers two battery measurement inputs capable of reading battery voltages up to 6 V, while operating at only 2.7 V. It also has an on-chip temperature sensor capable of reading 0.3°C resolution. The TSC2102 is available in a 32-lead TSSOP.

US Patent No. 624639

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

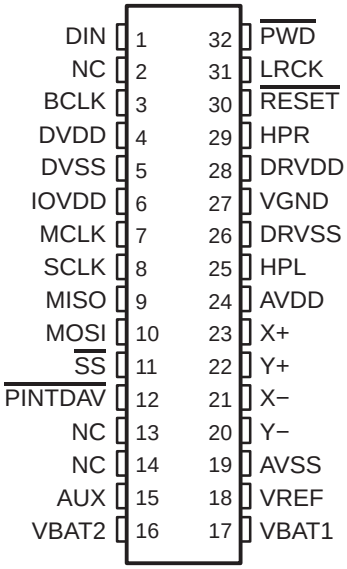
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA
TSC2102IDA	TSSOP-32	360	−40°C to +85°C	TSC2102IDA	Rails
				TSC2102IDAR	Tape and Reel

PIN ASSIGNMENTS

(TOP VIEW) **TSSOP**



Terminal Functions

PIN	NAME	INPUT/ OUTPUT	DESCRIPTION	PIN	NAME	INPUT/ OUTPUT	DESCRIPTION
1	DIN	I	Digital audio data input	17	VBAT1	I	Battery monitor input 1
2	NC		No connection	18	VREF	I/O	Reference voltage
3	BCLK	I/O	Audio bit clock to be consistent with pin 31 word-clock	19	AVSS	I	Analog ground
4	DVDD	I	Digital core supply	20	Y−	I/O	Y− position input and driver
5	DVSS	I	Digital core and IO ground	21	X−	I/O	X− position input and driver
6	IOVDD	I	IO supply	22	Y+	I/O	Y+ position input and driver
7	MCLK	I	Master clock	23	X+	I/O	X+ position input and driver
8	SCLK	I	SPI serial clock input	24	AVDD	I	Analog power supply
9	MISO	O	SPI serial data output	25	HPL	O	Left channel audio output
10	MOSI	I	SPI serial data input	26	DRVSS	I	Speaker ground
11	$\overline{SS}$	I	SPI slave select input	27	VGND	O	Virtual ground for audio output
12	$\overline{PINTDAV}$	O	Pen interrupt/data available output	28	DRVDD	I	Speaker and PLL supply
13	NC		No connection	29	HPR	O	Right channel audio output
14	NC		No connection	30	$\overline{RESET}$	I	Device reset
15	AUX	I	Auxiliary input	31	LRCK	I/O	Audio DAC word-clock
16	VBAT2	I	Battery monitor input 2	32	$\overline{PWD}$	I	Hardware power down

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNITS
AVDD to AVSS		−0.3 V to 3.9 V
DRVDD to DRVSS		−0.3 V to 3.9 V
IOVDD to DVSS		−0.3 V to 3.9 V
DVDD to DVSS		−0.3 V to 2.5 V
Digital input voltage to GND		−0.3 V to IOVDD + 0.3 V
Operating temperature range		−40°C to 85°C
Storage temperature range		−65°C to 105°C
Junction temperature (T_J Max)		105°C
TSSOP package	Power dissipation	$(T_J$ Max − $T_A)/\theta_{JA}$
	θ_{JA} Thermal impedance	60°C/W
Lead temperature	Soldering vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At +25°C, AVDD,DRVDD,IOVDD = 3.3 V, DVDD = 1.8 V, Int. V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TOUCH SCREEN					
AUXILIARY ANALOG INPUT					
Input voltage range	AUX input selected as input by touch-screen ADC	0		+VREF	V
Input capacitance			25		pF
Input leakage current			±1		µA
BATTERY MONITOR INPUTS					
Input voltage range		0.5		6.0	V
Input leakage current	Battery conversion not selected		±1		µA
TOUCH SCREEN A/D CONVERTER					
Resolution	Programmable: 8-, 10-,12-bits			12	Bits
No missing codes	12-bit resolution		11		Bits
Integral nonlinearity		−5		5	LSB
Offset error		−6		6	LSB
Gain error	Gain error is calculated with the effect of internal reference variation removed.	−6		6	LSB
Noise			50		µVrms
STEREO AUDIO CODEC					
DAC INTERPOLATION FILTER					
Pass band		20		0.45Fs	Hz
Pass band ripple			±0.06		dB
Transition band		0.45Fs		0.5501Fs	Hz
Stop band		0.5501Fs		7.455Fs	Hz
Stop band attenuation			65		dB
Filter group delay			21/Fs		Sec
De−emphasis error			±0.1		dB

ELECTRICAL CHARACTERISTICS (continued)

At +25°C, AVDD,DRVDD,IOVDD = 3.3 V, DVDD = 1.8 V, Int. V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC LINE OUTPUT (16−Ω driver bypassed)	1020-Hz sine wave input, Fs = 48 ksps, Load = 10 kΩ, 10 pF				
Full scale output voltage (0 dB)			0.707		Vrms
Output common mode			1.35		V
SNR	Measured as idle channel noise, A-weighted	85	97		dBA
THD	0-dB FS input, 0-dB gain		−97		dB
PSRR	1 kHz, 100mVpp on AVDD(1)		55		dB
DAC HEADPHONE OUTPUT	Load = 16 Ω, 10 pF				
SNR	Measured as idle channel noise, A-weighted	85	96		dBA
THD	−1 dBFS input, 0-dB gain		−65	−55	dB
PSRR	1 kHz, 100 mVpp on AVDD(1)		50		dB
Mute attenuation			90		dB
Maximum output power	Per channel		25		mW
Digital volume control		−63.5		0	dB
Digital volume control step size			0.5		dB
Channel separation	Between HPR and HPL		90		dB
VOLTAGE REFERENCE					
Voltage range	VREF output programmed as 2.5 V	2.3	2.5	2.7	V
	VREF output programmed as 1.25 V	1.15	1.25	1.35	
Voltage range	External reference	1.2		2.55	V
Reference drift	Internal VREF = 2.5 V		50		ppm/°C
Current drain	Extra current drawn when the internal reference is turned on.		500		µA
DIGITAL INPUT / OUTPUT					
Internal clock frequency			8		MHz
Logic family			CMOS		
Logic level: V_{IH}	I_{IH} = +5 µA	0.7xIOVDD			V
V_{IL}	I_{IL} = +5 µA	−0.3		0.3xIOVDD	V
V_{OH}	I_{OH} = 2 TTL loads	0.8xIOVDD			V
V_{OL}	I_{OL} = 2 TTL loads			0.1xIOVDD	V
Capacitive load			10		pF

ELECTRICAL CHARACTERISTICS (continued)

At +25°C, AVDD,DRVDD,IOVDD = 3.3 V, DVDD = 1.8 V, Int. V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted (continued)

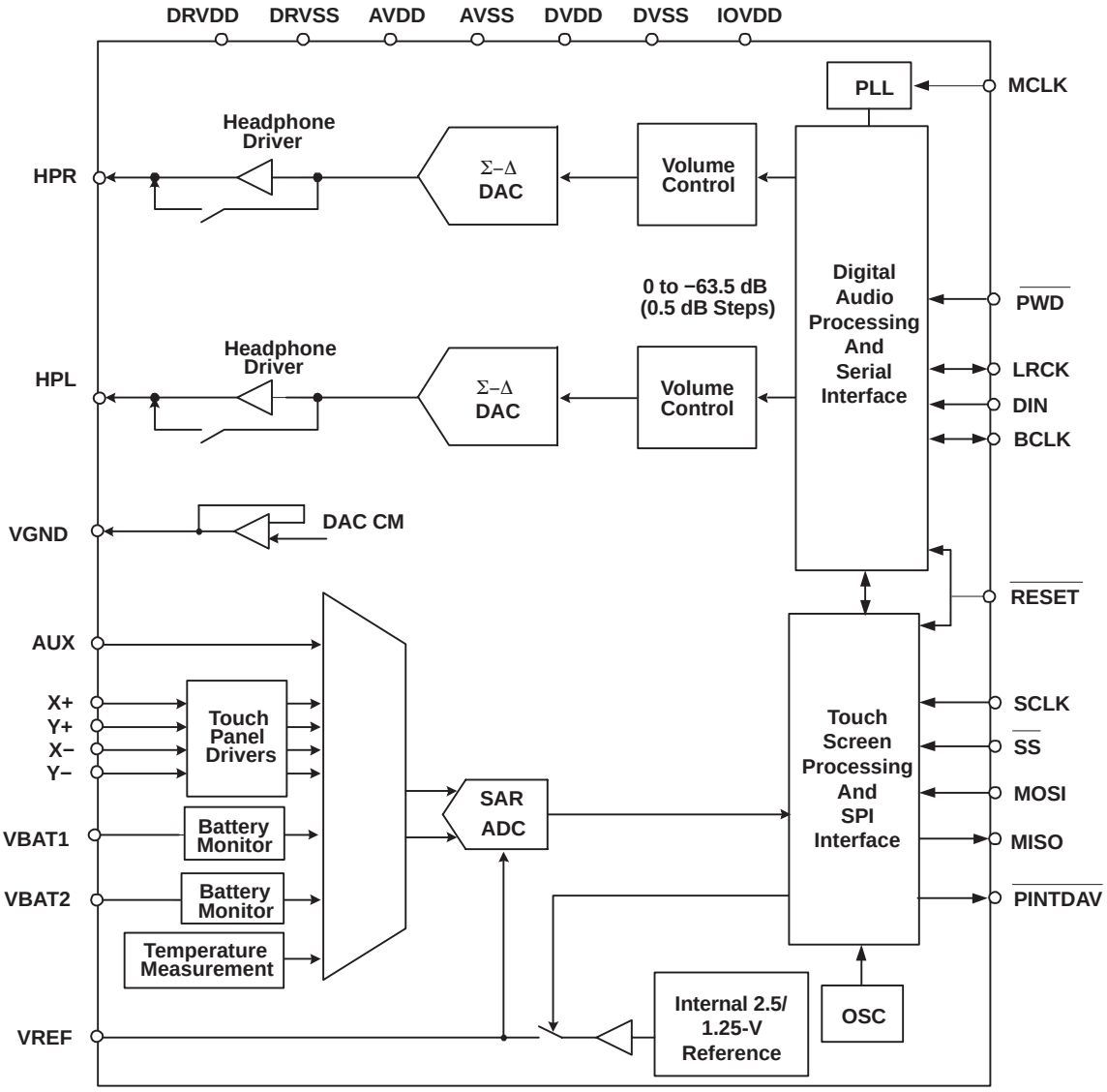
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS					
Power supply voltage					
AVDD		2.7		3.6	V
DRVDD		2.7		3.6	V
IOVDD		2.7		3.6	V
DVDD		1.525		1.95	V
Touch-screen ADC quiescent current	IAVDD, host controlled AUX conversion at 10 ksps with external reference		45		µA
	IDVDD, host controlled AUX conversion at 10 ksps		65		
Analog supply current – Audio play back only	IAVDD + IDRVDD, headphone driver bypassed, VGND off, PLL off, no signal		2.1		mA
	IAVDD + IDRVDD, headphone driver and VGND on, PLL off, no signal		7.1		
Digital supply current – Audio play back only	48 ksps, PLL off, no signal		2.2		mA
PLL current	IDRVDD		1		mA
	IDVDD		0.8		
Total current	Hardware power down. All digital inputs at 0 V or IOVDD.		5		µA

(1) DAC PSRR measurement is calculated as:

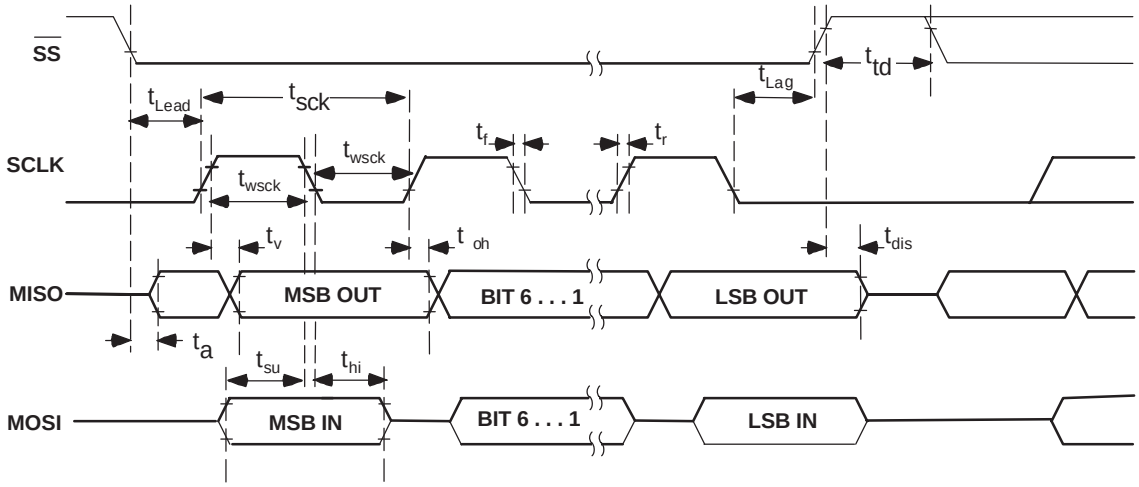
$$PSRR = 20 \log_{10}\left(\frac{VSIG_{sup}}{V_{HPR/L}}\right)$$

where $VSIG_{sup}$ is the ac signal applied on AVDD, which is 100 mV_{PP} at 1 kHz, and $V_{HPR/L}$ is the peak-to-peak ac signal seen on HPR and HPL outputs.

FUNCTIONAL BLOCK DIAGRAM



SPI TIMING DIAGRAM



TYPICAL TIMING REQUIREMENTS

All specifications at 25°C, IOVDD = 3.3 V, DVDD = 1.8 V(1)

PARAMETER		MIN	MAX	UNITS
t_{wsck}	SCLK pulse width	18		ns
t_{Lead}	Enable lead time	15		ns
t_{Lag}	Enable lag time	15		ns
t_{td}	Sequential transfer delay	15		ns
t_a	Slave MISO access time		15	ns
t_{dis}	Slave MISO disable time		15	ns
t_{su}	MOSI data setup time	6		ns
t_{hi}	MOSI data hold time	6		ns
t_{ho}	MISO data hold time	4		ns
t_v	MISO data valid time		13	ns
t_r	Rise time		4	ns
t_f	Fall time		4	ns

(1) These parameters are based on characterization and are not tested in production.

AUDIO INTERFACE TIMING DIAGRAMS

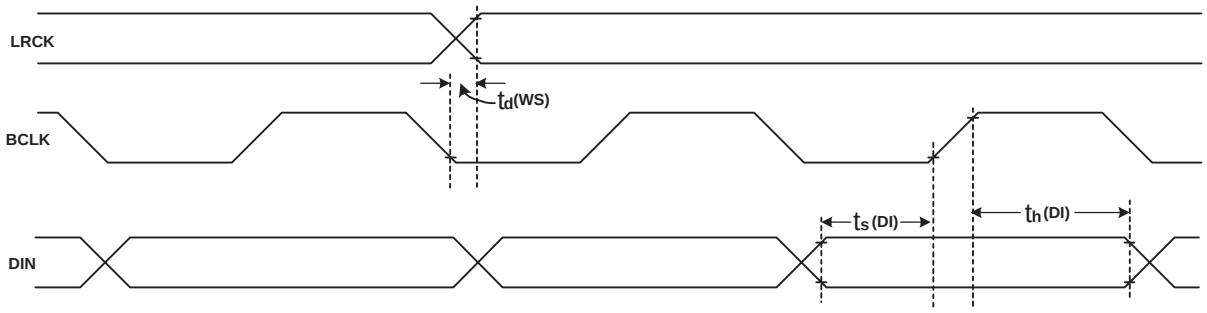


Figure 1. I2S/LJF/RJF Timing in Master Mode

TYPICAL TIMING REQUIREMENTS

All specifications at 25°C, IOVDD = 3.3 V, DVDD = 1.8 V(1)

PARAMETER		MIN	MAX	UNITS
t_d (WS)	LRCK delay		15	ns
t_s(DI)	DIN setup	6		ns
t_h(DI)	DIN hold	6		ns
t_r	Rise time		6	ns
t_f	Fall time		6	ns

(1) These parameters are based on characterization and are not tested in production.

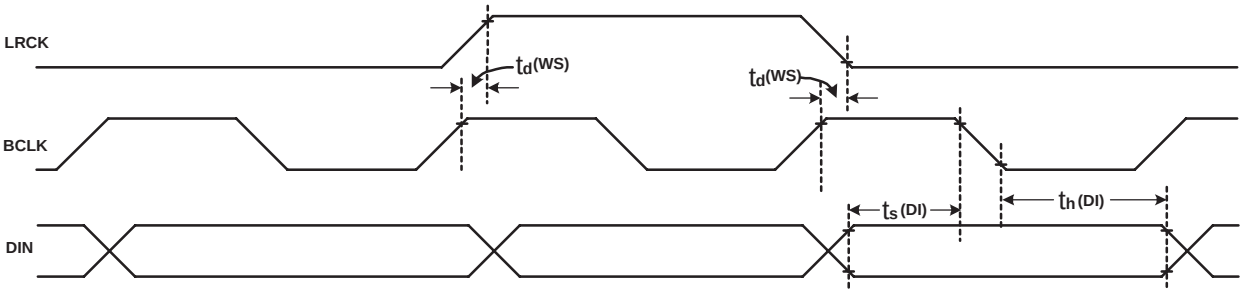


Figure 2. DSP Timing in Master Mode

TYPICAL TIMING REQUIREMENTS

All specifications at 25°C, IOVDD = 3.3 V, DVDD = 1.8 V(1)

PARAMETER		MIN	MAX	UNITS
t_d (WS)	LRCK delay		15	ns
t_s(DI)	DIN setup	6		ns
t_h(DI)	DIN hold	6		ns
t_r	Rise time		6	ns
t_f	Fall time		6	ns

(1) These parameters are based on characterization and are not tested in production.

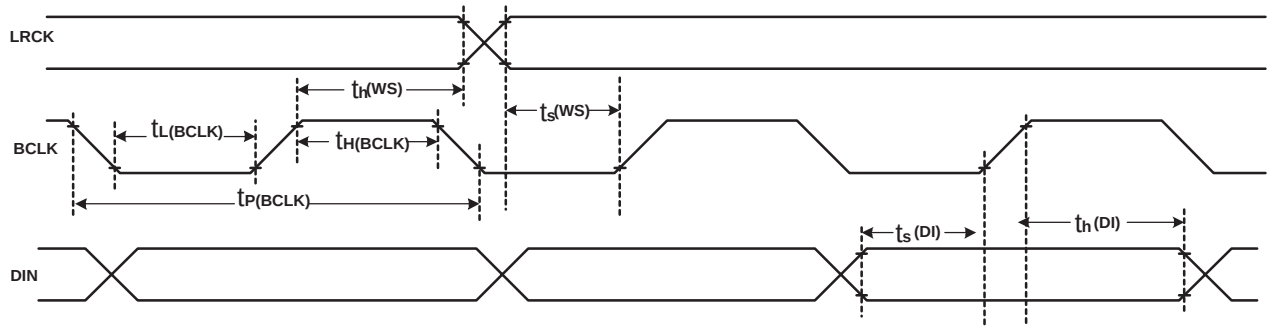


Figure 3. I2S/LJF/RJF Timing in Slave Mode

TYPICAL TIMING REQUIREMENTS

All specifications at 25°C, IOVDD = 3.3 V, DVDD = 1.8 V(1)

PARAMETER		MIN	MAX	UNITS
t_H (BCLK)	BCLK high period	35		ns
t_L (BCLK)	BCLK low period	35		ns
t_P (BCLK)	BCLK period	85		ns
t_S(WS)	LRCK setup	6		ns
t_h(WS)	LRCK hold	6		ns
t_S(DI)	DIN setup	6		ns
t_h(DI)	DIN hold	6		ns
t_r	Rise time		4	ns
t_f	Fall time		4	ns

(1) These parameters are based on characterization and are not tested in production.

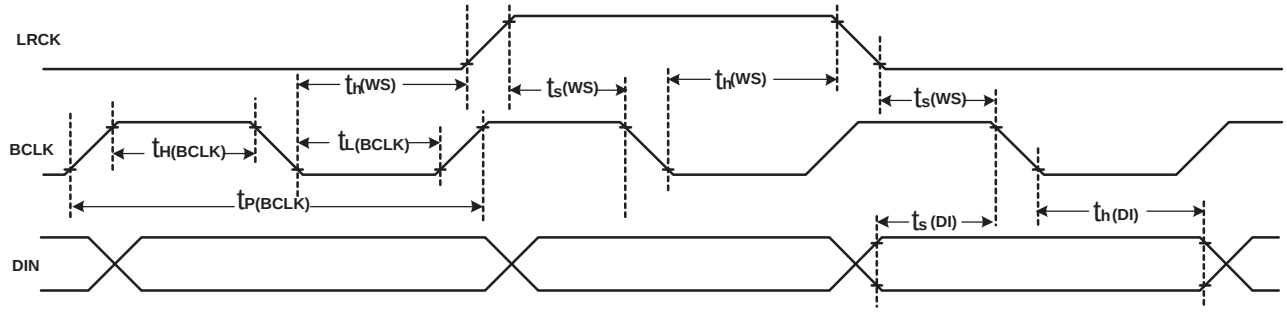


Figure 4. DSP Timing in Slave Mode

TYPICAL TIMING REQUIREMENTS

All specifications at 25°C, IOVDD = 3.3 V, DVDD = 1.8 V(1)

PARAMETER		MIN	MAX	UNITS
t_H (BCLK)	BCLK high period	35		ns
t_L (BCLK)	BCLK low period	35		ns
t_P (BCLK)	BCLK period	85		ns
t_S(WS)	LRCK setup	6		ns
t_h(WS)	LRCK hold	6		ns
t_S(DI)	DIN setup	6		ns
t_h(DI)	DIN hold	6		ns
t_r	Rise time		4	ns
t_f	Fall time		4	ns

(1) These parameters are based on characterization and are not tested in production.

TYPICAL CHARACTERISTICS

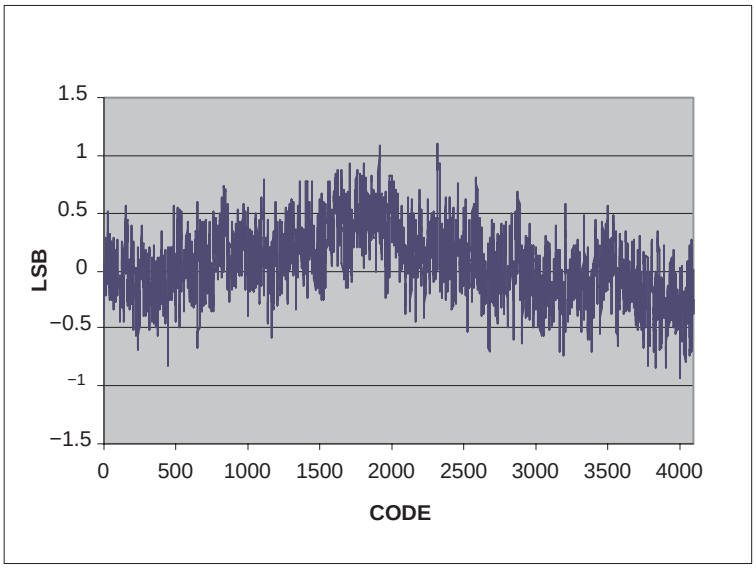


Figure 5. SAR INL (T_A = 25°C, Internal Ref = 2.5 V, 12 bit, AVDD = 3.3 V)

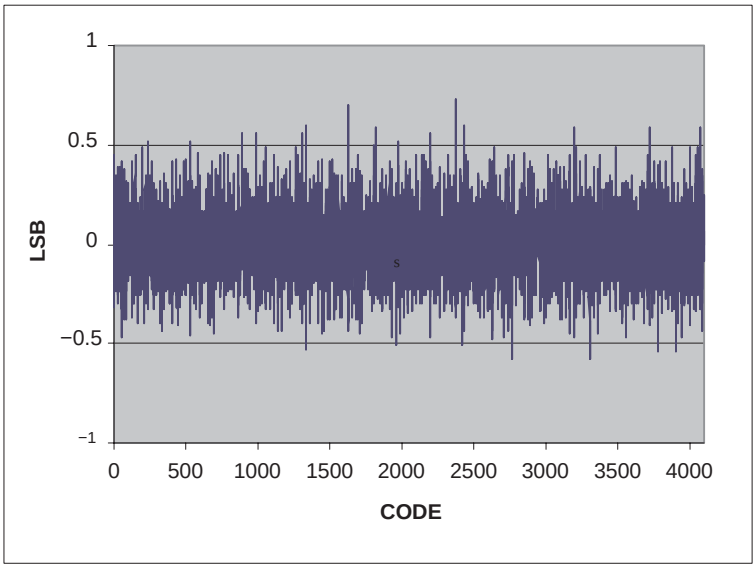


Figure 6. SAR DNL (T_A = 25°C, Internal Ref = 2.5 V, AVDD = 3.3 V)

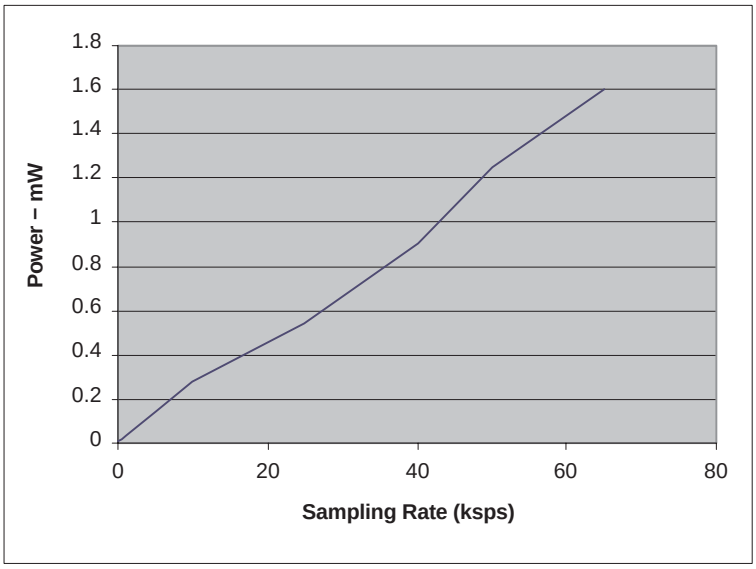


Figure 7. Touch Screen Power Consumption With Speed (T_A = 25°C, External Ref, Host Controlled AUX Conversion, AVDD = 3.3 V)

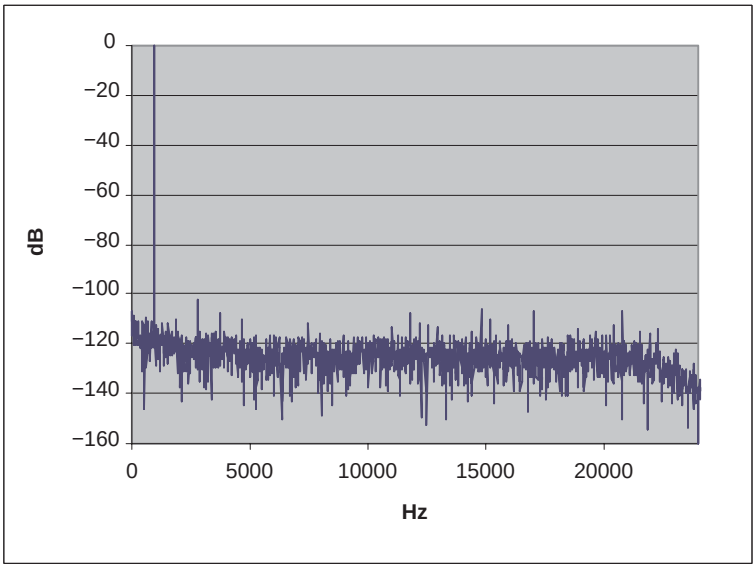


Figure 8. DAC FFT Plot (T_A = 25°C, 48 ksps, 0 dB, 1 kHz Input, AVDD = 3.3 V, R_L = 10 kΩ)

OVERVIEW

The TSC2102 is a highly integrated touch screen controller with stereo audio DAC for portable computing, communication, and entertainment applications. A register-based architecture eases integration with microprocessor-based systems through a standard SPI bus. All peripheral functions are controlled through the registers and onboard state machines.

The TSC2102 consists of the following blocks (refer to the block diagram):

- Touch Screen Interface
- Battery Monitors
- Auxiliary Input
- Temperature Monitor
- Audio DAC

Communication with the TSC2102 is via standard SPI serial interface. This interface requires that the slave select signal be driven low to communicate with the TSC2102. Data is then shifted into or out of the TSC2102 under control of the host microprocessor, which also provides the serial data clock. Control of the TSC2102 and its functions is accomplished by writing to different registers in the TSC2102. A simple command protocol is used to address the 16-bit registers. Registers control the operation of the A/D converter and audio DAC.

Control of the TSC2102 and its functions is accomplished by writing to different registers in the TSC2102. A simple command protocol is used to address the 16−bit registers. Registers control the operation of the A/D converter and audio DAC.

The TSC2102 audio serial interface is exclusively used by the stereo DAC and supports four audio interface modes (I2S, DSP, right justified, and left justified) to receive digital audio data from the host processor.

A typical application of the TSC2102 is shown in Figure 9.

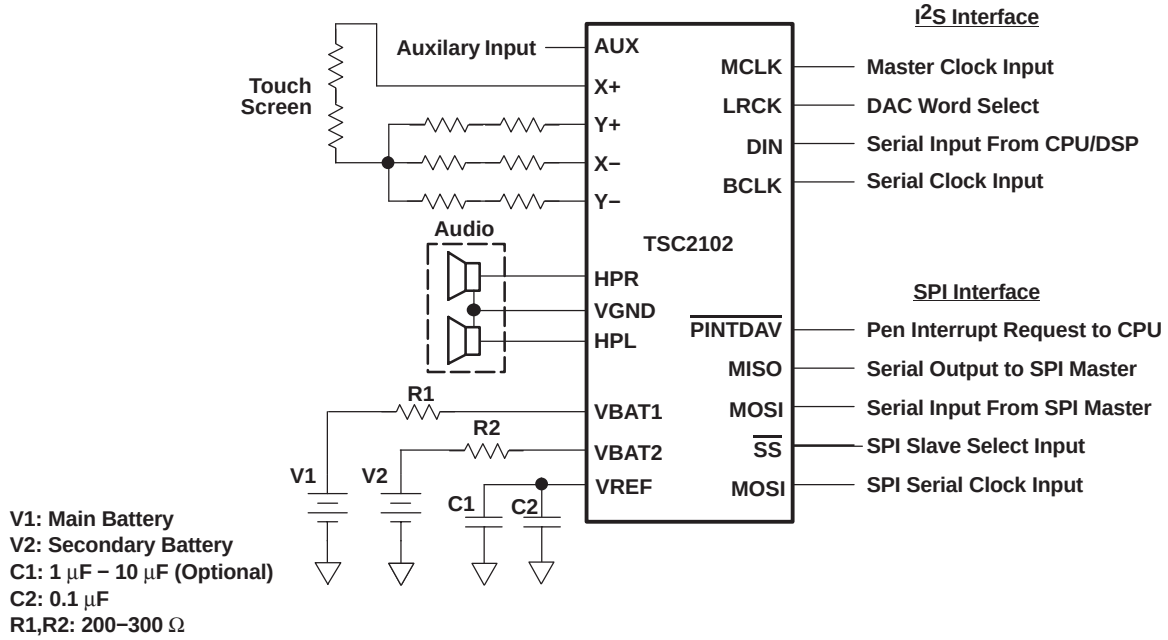


Figure 9. Typical Circuit Configuration

OPERATION—TOUCH SCREEN

A resistive touch screen works by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where a screen is touched by an input stylus, pen, or finger. The change in the resistance ratio marks the location on the touch screen.

The TSC2102 supports the resistive 4-wire configurations (see Figure 9). The circuit determines location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure.

The 4-Wire Touch Screen Coordinate Pair Measurement

A 4-wire touch screen is constructed as shown in Figure 10. It consists of two transparent resistive layers separated by insulating spacers.

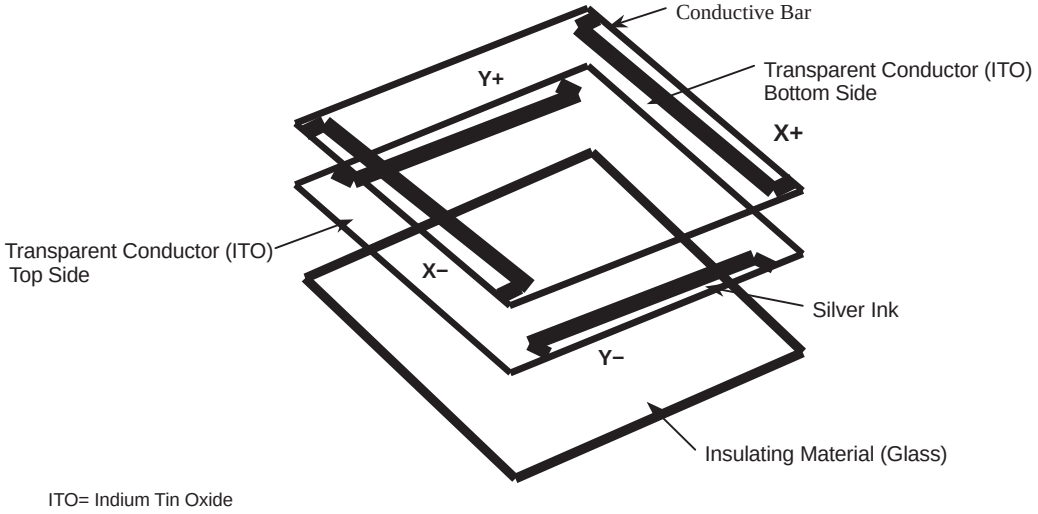


Figure 10. 4-Wire Touch Screen Construction

The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The ADC converts the voltage measured at the point the panel is touched. A measurement of the Y position of the pointing device is made by connecting the X+ input to an ADC, turning on the Y drivers, and digitizing the voltage seen at the X+ input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead does not affect the conversion due to the high input impedance of the A/D converter.

Voltage is then applied to the other axis, and the A/D converts the voltage representing the X position on the screen. This provides the X and Y coordinates to the associated processor.

Measuring touch pressure (Z) can also be done with the TSC2102. To determine pen or finger touch, the pressure of the *touch* needs to be determined. Generally, it is not necessary to have very high performance for this test; therefore, the 8-bit resolution mode is recommended (however, calculations are shown with the 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2102 supports two methods. The first method requires knowing the X-plate resistance, measurement of the X-Position, and two additional cross panel measurements (Z_2 and Z_1) of the touch screen (see Figure 11). Using equation 1 calculates the touch resistance:

$$R_{TOUCH} = R_{X-plate} \times \frac{X-position}{4096} \left(\frac{Z_2}{Z_1} - 1 \right) \quad (1)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-Position and Y-Position, and Z_1. Using equation 2 also calculates the touch resistance:

$$R_{TOUCH} = \frac{R_{X-plate} \times X-position}{4096} \left(\frac{4096}{Z_1} - 1 \right) - R_{Y-plate} \times \left(1 - \frac{Y-position}{4096} \right) \quad (2)$$

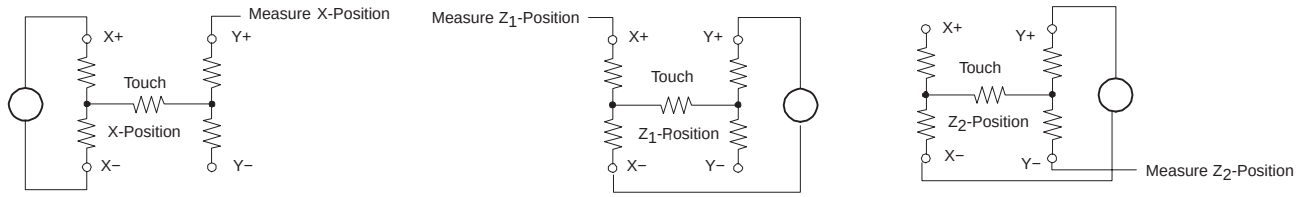


Figure 11. Pressure Measurement

When the touch panel is pressed or touched, and the drivers to the panel are turned on, the voltage across the touch panel often overshoots and then slowly settles (decays) to a stable dc value. This is due to mechanical bouncing which is caused by vibration of the top layer sheet of the touch panel when the panel is pressed. This settling time must be accounted for, or else the converted value will be in error. Therefore, a delay must be introduced between the time the driver for a particular measurement is turned on, and the time measurement is made.

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen, i.e. noise generated by the LCD panel or back-light circuitry. The value of these capacitors provides a low-pass filter to reduce the noise, but causes an additional settling time requirement when the panel is touched.

Several solutions to this problem are available in the TSC2102. A programmable delay time is available which sets the delay between turning the drivers on and making a conversion. This is referred to as the panel voltage stabilization time, and is used in some of the modes available in the TSC2102. In other modes, the TSC2102 can be commanded to turn on the drivers only without performing a conversion. Time can then be allowed before the command is issued to perform a conversion.

The TSC2102 touch screen interface can measure position (X, Y) and pressure (Z). Determination of these coordinates is possible under three different modes of the A/D converter: (1) conversion controlled by the TSC2102, initiated by detection of a touch; (2) conversion controlled by the TSC2102, initiated by the host responding to the $\overline{\text{PINTDAV}}$ signal; or (3) conversion completely controlled by the host processor.

Touch-Screen A/D Converter

The analog inputs of the TSC2102 are shown in Figure 12. The analog inputs (X, Y, and Z touch panel coordinates, battery voltage monitors, chip temperature and auxiliary input) are provided via a multiplexer to the successive approximation register (SAR) analog-to-digital (A/D) converter. The A/D architecture is based on a capacitive redistribution architecture, which inherently includes a sample/hold function.

A unique configuration of low on-resistance switches allows an unselected A/D input channel to provide power and an accompanying pin to provide ground for driving the touch panel. By maintaining a differential input to the converter and a differential reference input architecture, it is possible to negate errors caused by the driver switch on-resistances.

The A/D is controlled by an A/D converter control register. Several modes of operation are possible, depending upon the bits set in the control register. Channel selection, scan operation, averaging, resolution, and conversion rate may all be programmed through this register. These modes are outlined in the sections below for each type of analog input. The results of conversions made are stored in the appropriate result register.

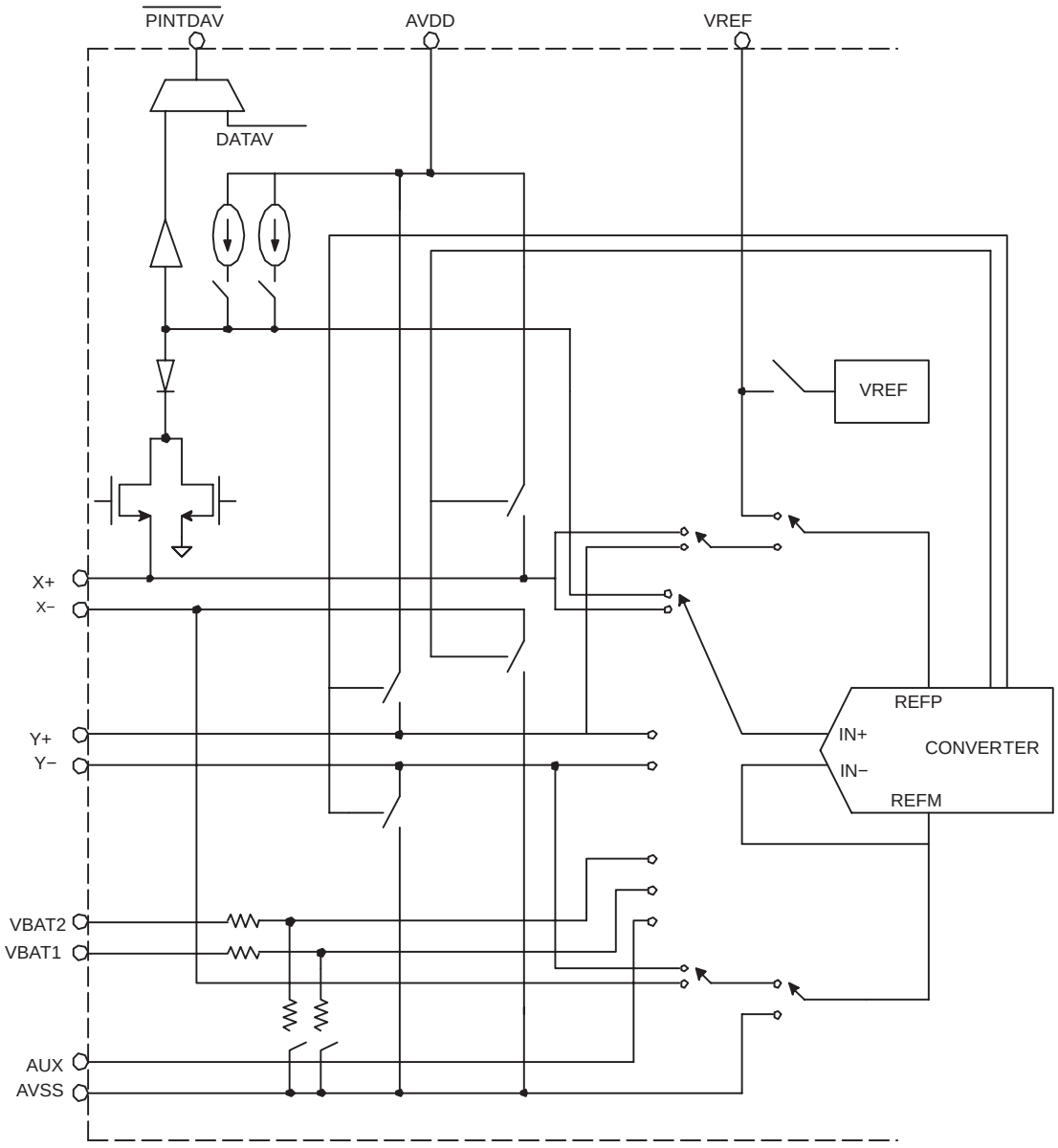


Figure 12. Simplified Diagram of the Analog Input Section

Data Format

The TSC2102 output data is in unsigned binary format and can be read from the registers over the SPI interface.

Reference

The TSC2102 has an internal voltage reference that can be set to 1.25 V or 2.5 V through the reference control register.

The internal reference voltage must only be used in the single-ended mode for battery monitoring, temperature measurement, and for utilizing the auxiliary inputs. Optimal touch screen performance is achieved when using a ratiometric conversion, thus all touch screen measurements are done automatically in the ratiometric mode.

An external reference can also be applied to the VREF pin, and the internal reference can be turned off.

Variable Resolution

The TSC2102 provides three different resolutions for the ADC: 8-, 10- or 12-bits. Lower resolutions are often practical for measurements such as touch pressure. Performing the conversions at lower resolution reduces the amount of time it takes for the ADC to complete its conversion process, which lowers power consumption.

Conversion Clock and Conversion Time

The TSC2102 contains an internal 8-MHz clock, which is used to drive the state machines inside the device that perform the many functions of the part. This clock is divided down to provide a clock to run the ADC. The division ratio for this clock is set in the ADC control register. The ability to change the conversion clock rate allows the user to choose the optimal value for resolution, speed, and power. If the 8-MHz clock is used directly, the ADC is limited to 8-bit resolution; using higher resolutions at this speed does not result in accurate conversions. Using a 4-MHz conversion clock is suitable for 10-bit resolution; 12-bit resolution requires that the conversion clock run at 1 or 2 MHz.

Regardless of the conversion clock speed, the internal clock runs nominally at 8 MHz. The conversion time of the TSC2102 is dependent upon several functions (see the section *Touch Screen Conversion Initiated at Touch Detect* in this data sheet). While the conversion clock speed plays an important role in the time it takes for a conversion to complete, a certain number of internal clock cycles is needed for proper sampling of the signal. Moreover, additional times, such as the panel voltage stabilization time, can add significantly to the time it takes to perform a conversion. Conversion time can vary depending upon the mode in which the TSC2102 is used. Throughout this data sheet, internal and conversion clock cycles are used to describe the times that many functions take to execute. Considering the total system design, these times must be taken into account by the user.

When the audio DAC is powered down, the touch screen A/D uses an internal oscillator for conversions. However, to save power whenever the audio DAC is powered up, the internal oscillator is powered down and MCLK and BCLK are used to clock the touch screen A/D.

Touch Detect/Data Available

The pen interrupt/data available ($\overline{\text{PINTDAV}}$) output function is detailed in Figure 13. While in the power-down mode, the Y– driver is ON and connected to AVSS and the X+ pin is connected through an on-chip pullup resistor to AVDD. In this mode, the X+ pin is also connected to a digital buffer and mux to drive the $\overline{\text{PINTDAV}}$ output. When the panel is touched, the X+ input is pulled to ground through the touch screen, and the pen−interrupt signal goes LOW due to the current path through the panel to AVSS, initiating an interrupt to the processor. During the measurement cycles for X− and Y− position, the X+ input is disconnected from the pen-interrupt circuit to prevent any leakage current from the pullup resistor flowing through the touch screen, and thus causing conversion errors.

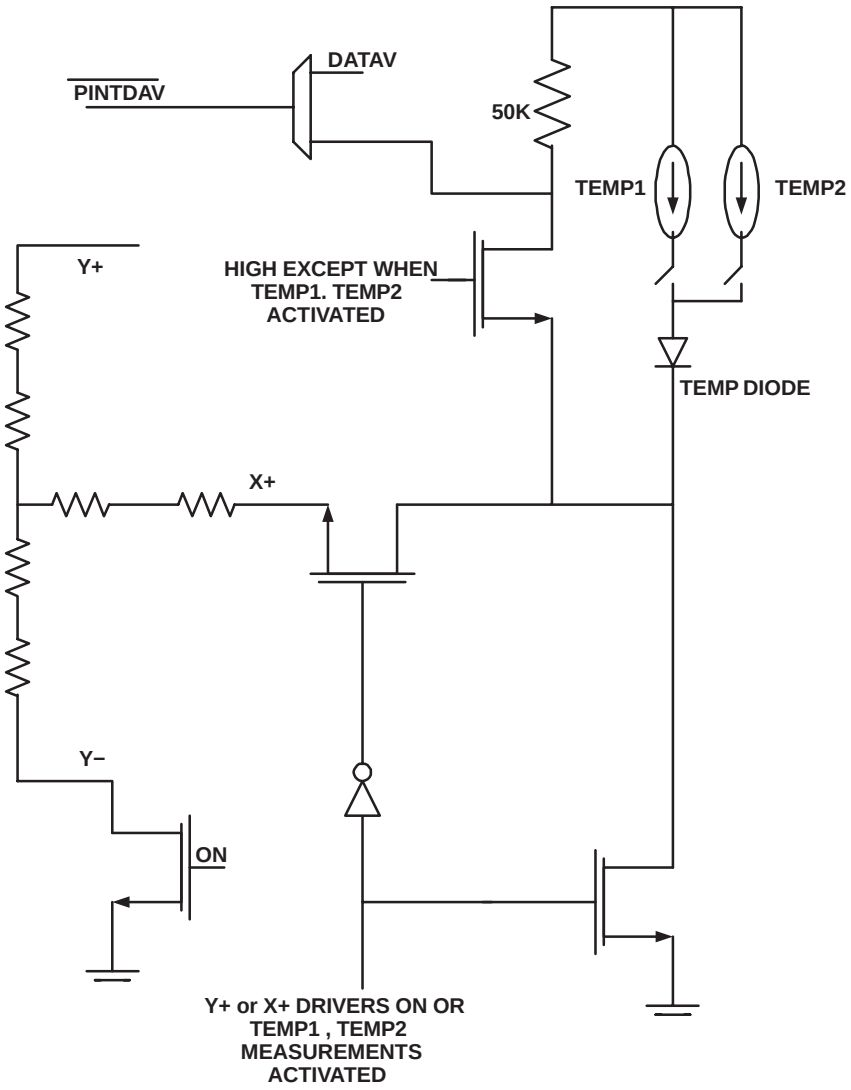


Figure 13. $\overline{\text{PINTDAV}}$ Functional Block Diagram

In modes where the TSC2102 needs to detect if the screen is still touched (for example, when doing a $\overline{\text{PINTDAV}}$ initiated X, Y, and Z conversion), the TSC2102 must reset the drivers so that the 50-k resistor is connected. Because of the high value of this pullup resistor, any capacitance on the touch screen inputs causes a long delay time, and may prevent the detection from occurring correctly. To prevent this, the TSC2102 has a circuit that allows any screen capacitance to be *precharged*, so that the pullup resistor does not have to be the only source for the charging current. The time allowed for this precharge, as well as the time needed to sense if the screen is still touched, can be set in the configuration control register D5−D0 of REG05H/Page1.

This does point out, however, the need to use the minimum capacitor values possible on the touch screen inputs. These capacitors may be needed to reduce noise, but too large a value increases the needed precharge and sense times, as well as panel voltage stabilization time.

The function of $\overline{\text{PINTDAV}}$ output is programmable and controlled by writing to the bits D15−D14 of REG 01H/Page1 as described in the Table 1.

Table 1. Programmable $\overline{\text{PINTDAV}}$ Functionality

D15−D14	$\overline{\text{PINTDAV}}$ FUNCTION
00	Acts as PEN interrupt (active low) only. When PEN touch is detected, $\overline{\text{PINTDAV}}$ goes low.(1)
01	Acts as data available (active low) only. The $\overline{\text{PINTDAV}}$ goes low as soon as one set of ADC conversions are completed for data of X,Y, XYZ, battery input, or auxiliary input selected by D13−D10 in REG00H/Page1. The resulting ADC output is stored in the appropriate registers. The $\overline{\text{PINTDAV}}$ remains low and goes high only after this complete set of registers selected by D13−D10 REG00H/Page1 is read out.
10 11	Acts as both PEN interrupt and data available. When PEN touch is detected, $\overline{\text{PINTDAV}}$ goes low and remains low. The $\overline{\text{PINTDAV}}$ goes high only after one set of A/D conversions is completed for data of X,Y, XYZ, battery input, or auxiliary input selected by D13−D10 in REG00H/Page1.

(1) See the section *Conversion Time Calculation for the TSC2102* in this data sheet for timing diagrams and conversion time calculations.

Pen-touch detect circuit is disabled during hardware power down.

Touch Screen Measurements

The touch screen ADC can be controlled by the host processor or can be self−controlled to offload processing from the host processor. Bit D15 of REG00H/Page1 sets the control mode of the TSC2102 touch screen ADC; and bit D12 of REG01H/Page 1 can be read to check the control mode status.

Conversion Controlled by TSC2102 Initiated at Touch Detect

In this mode, the TSC2102 detects when the touch panel is touched and causes the $\overline{\text{PINTDAV}}$ line to go low. At the same time, the TSC2102 starts up its internal clock. Assuming the part was configured to convert XY coordinates, it then turns on the Y drivers, and after a programmed panel voltage stabilization time, powers up the ADC and converts the Y coordinate. If averaging is selected, several conversions may take place; when data averaging is complete, the Y coordinate result is stored in the Y register.

If the screen is still touched at this time, the X drivers are enabled, and the process repeats, but measuring instead the X coordinate, storing the result in the X register.

If only X and Y coordinates are to be measured, then the conversion process is complete. The time it takes to complete this process depends upon the selected resolution, internal conversion clock rate, averaging selected, panel voltage stabilization time, and precharge and sense times.

If the pressure of the touch is also to be measured, the process continues in the same way, measuring the Z1 and Z2 values, and placing them in the Z1 and Z2 registers. As before, this process time depends upon the settings described above.

See the section *Conversion Time Calculation for the TSC2102* in this data sheet for timing diagrams and conversion time calculations.

Conversion Controlled by TSC2102 Initiated by the Host

In this mode, the TSC2102 detects when the touch panel is touched and causes the pen-interrupt signal line to go low. The host recognizes the interrupt request, and then writes to the ADC control register (D13−D10 REG00H/Page1) to select one of the touch screen scan functions. The host can either choose to initiate one of the scan functions, in which case the TSC2102 controls the driver turnons, and wait times (e.g. upon receiving the interrupt the host can initiate the continuous scan function X−Y−Z1−Z2 after which the TSC2102 controls the rest of conversion). The host can also choose to control each aspect of conversion by controlling the driver turnons and start of conversions. For example, upon receiving the interrupt request, the host turns on the X drivers. After waiting for the settling time, the host then addresses the TSC2102 again, this time requesting an X coordinate conversion, and so on.

The main difference between this mode and the previous mode is that the host, not the TSC2102, controls the touch screen scan functions.

See the section *Conversion Time Calculation for the TSC2102* in this data sheet for timing diagrams and conversion time calculations.

Temperature Measurement

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the TSC2102 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the 25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes.

The TSC2102 offers two modes of temperature measurement. The first mode requires a single reading to predict the ambient temperature. A diode, as shown in Figure 14, is used during this measurement cycle. This voltage is typically 600 mV at 25°C with a 20-µA current through it. The absolute value of this diode voltage can vary a few millivolts. During the final test of the end product, the diode voltage must be stored at a known temperature. Further calibration can be done to calculate the precise temperature coefficient of the particular device. This method has a temperature resolution of approximately 0.3 °C/LSB and accuracy of approximately 1°C.

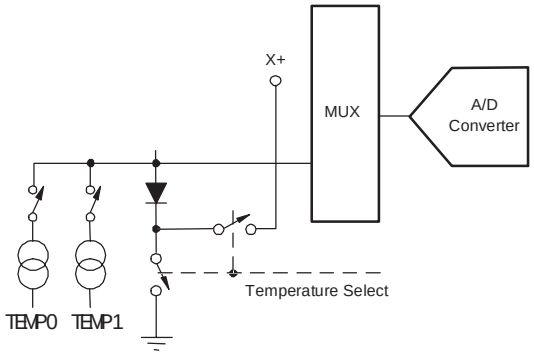


Figure 14. Functional Block Diagram of Temperature Measurement Mode

The second mode uses a two-measurement (differential) method. This mode requires a second conversion with a current 82 times larger. The voltage difference between the first (TEMP1) and second (TEMP2) conversion, using 82 times the bias current, is represented by:

$$\frac{kT}{q} \times \ln(N)$$

where:

N is the current ratio = 82

k = Boltzmann's constant ($1.38054 \bullet 10^{-23}$ electrons volts/degrees Kelvin)

q = the electron charge ($1.602189 \bullet 10^{-19}$ °C)

T = the temperature in degrees Kelvin

This method provides resolution of approximately 1.5°C/LSB and accuracy of approximately 1°C. The equation for the relation between differential code and temperature may vary slightly from device to device and can be calibrated at final system test by the user.

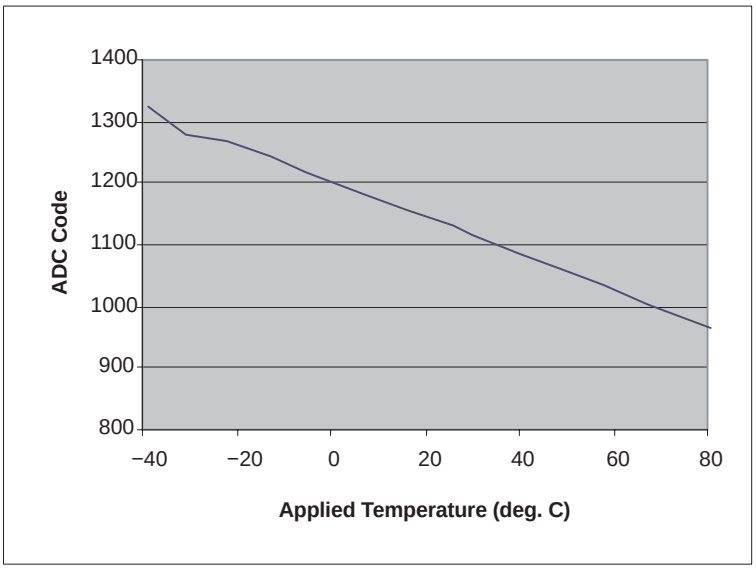


Figure 15. Typical Plot for Single Measurement Method

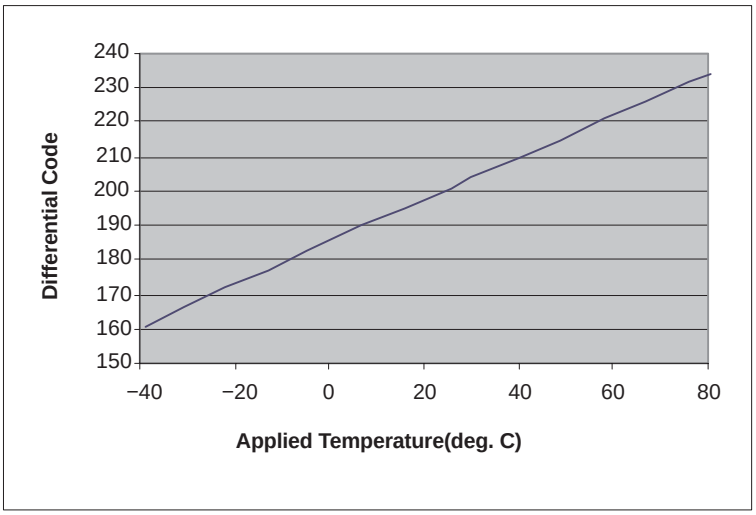


Figure 16. Typical Plot for Differential Measurement Method

Temperature measurement can only be done in host controlled mode.

Battery Measurement

An added feature of the TSC2102 is the ability to monitor the battery voltage at the input side of a voltage regulator (LDO or dc/dc converter), as shown in Figure 17. The battery voltage can vary from 0.5 V to 6 V while maintaining the analog supply voltage to the TSC2102 in the range of 2.7 V to 3.6 V. The input voltage (VBAT1 or VBAT2) is divided down by a factor of 6 so that a 6.0-V battery voltage is represented as 1.0 V to the ADC.It is advisable to add a series resistor of 200 to 300 Ω while connecting the battery terminal to the input pin (VBAT1 or VBAT2) as shown in Figure 17. Thus, the resultant voltage converted by the ADC is given by:

$$V_{conv} = \frac{2.0K}{12.0K + R} \times V_{battery}$$

The internal resistors, which make up the resistor divider, are subject to ±20% device-to-device variation. In order to minimize power consumption, the divider is only on during the sampling of the battery input.

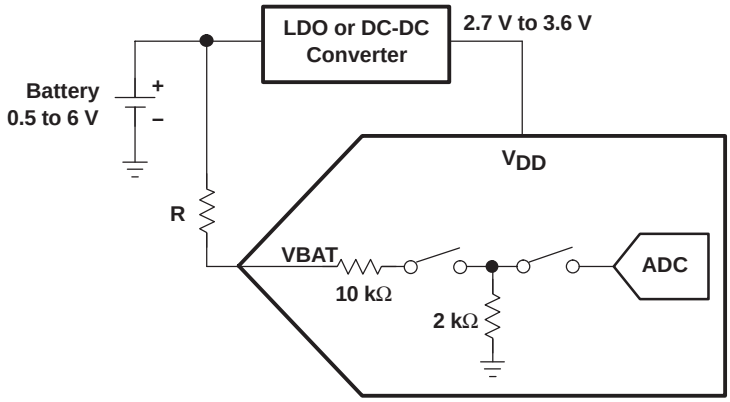


Figure 17. Battery Measurement Functional Block Diagram

Battery measurement can only be done in host controlled mode.

See the section *Conversion Time Calculation for the TSC2102* and subsection *Non Touch Measurement Operation* in this data sheet for timing diagrams and conversion time calculations.

Auxiliary Measurement

The auxiliary voltage input (AUX) can be measured in much the same way as the battery inputs. Applications might include external temperature sensing, ambient light monitoring for controlling the back-light, or sensing the current drawn from the battery. The auxiliary input can also be monitored continuously in scan mode.

Auxiliary measurement can only be done in host controlled mode.

See the section *Conversion Time Calculation for the TSC2102* and subsection *Non Touch Measurement Operation* in this data sheet for timing diagrams and conversion time calculations.

Port Scan

If making measurements of BAT1, BAT2, and AUX is desired on a periodic basis, the port scan mode can be used. This mode causes the TSC2102 to sample and convert both battery inputs and the auxiliary input. At the end of this cycle, the battery and auxiliary result registers contain the updated values. Thus, with one write to the TSC2102, the host can cause three different measurements to be made.

Port scan can only be done in host−controlled mode.

See the section *Conversion Time Calculation for the TSC2102* and subsection *Port Scan Operation* in this data sheet for timing diagrams and conversion time calculations.

Hardware Reset

The device requires hardware reset (active low) after power up. A hardware reset pulse initializes all the internal registers and counters.

Hardware Power Down

The device powers down all the internal circuitry to save power. All the register contents are maintained. Some counters maintain their value. The hardware power-down circuit also disables the pen-touch detect circuit.

OPERATION− STEREO AUDIO DAC

Audio Analog I/O

The TSC2102 has one stereo headphone output capable of driving a 16-Ω load at over 25 mW (with 3.3-V supply) (HPR, HPL). The headphone driver can be bypassed by setting D12 in the control register 05H/Page2 to 0. The TSC2102 also has a virtual ground (VGND) output, which can be optionally used to connect to the ground terminal of headphones to eliminate the ac-coupling capacitor at the headphone output terminal. Bit D8 of control register 05H/Page2 controls the VGND amplifier. A special circuit has been included in the TSC2102 to insert a short keyclick sound into the stereo audio output, even when the audio DAC is powered down. The keyclick sound is used to provide feedback to the user when a particular button is pressed or item is selected. The specific sound of the keyclick can be adjusted by varying several register bits that control its frequency, duration, and amplitude.

Digital Audio Interface

Digital audio data samples can be transmitted between the TSC2102 and the CPU via the audio data serial port (BCLK, LRCK, DIN) that can be configured to transfer digital data in four different formats: right justified, left justified, I2S, and DSP. The four modes are MSB first and operate with variable word length of 16/20/24/32 bits. The TSC2102 audio data serial port can operate in master or slave mode. The word-select signal (LRCK) and bit clock signal (BCLK) are output in master mode and input in slave mode, and both can be turned off by software power down. The LRCK also is the synchronization signal for DIN and represents the sampling rate of the DAC. All registers, including those pertaining to audio functionality, are only configured via the SPI bus.

- **DAC SAMPLING RATE**

  The audio-control-1 register (Register 00H, Page 2) determines the sampling rates of DAC, which is scaled down from the reference rate (Fsref) of either 44.1 kHz or 48 kHz, which is selectable by bit D13 of control register 06H/Page2. The frequency of the LRCK represents the sampling rate of the DAC. At power up, it is configured as an I2S SLAVE with the DAC operating at Fsref.

- **WORD SELECT SIGNALS**

  The word select signal (LRCK) indicates the channel being transmitted:

  − LRCK = 0: left channel for I2S mode

  − LRCK = 1: right channel for I2S mode

  For other modes, check the timing diagrams below.

- **256−S TRANSFER MODE**

  In the 256-S mode, the BCLK rate always equals 256 times the LRCK frequency. In the 256-S transfer mode, the combination of the 48-ksps sampling rate and left-justified mode is not supported.

- **CONTINUOUS TRANSFER MODE**

  In continuous transfer mode, the BCLK rate always equals two times the word length times the LRCK frequency.

- **RIGHT-JUSTIFIED MODE**

  In right-justified mode, the LSB of the left channel is valid on the rising edge of the BCLK preceding the falling edge of LRCK. Similarly, the LSB of the right channel is valid on the rising edge of the BCLK preceding the rising edge of LRCK.

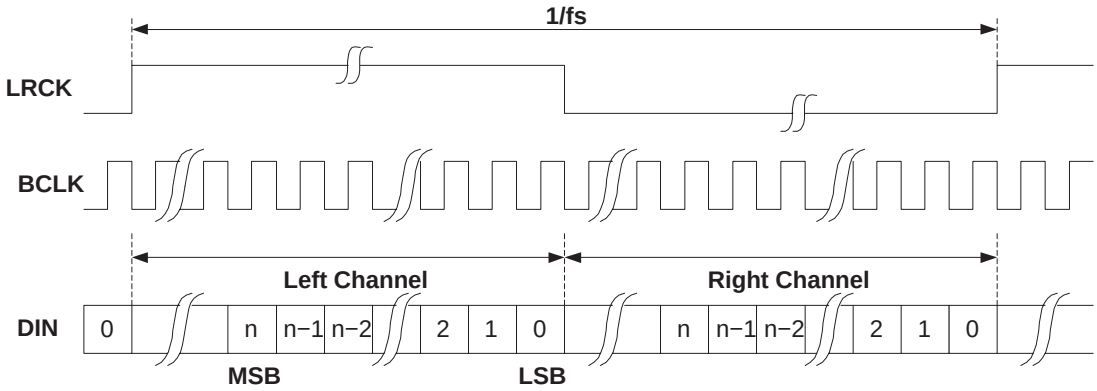


Figure 18. Timing Diagram for Right-Justified Mode

- **LEFT-JUSTIFIED MODE**

In left−justified mode, the MSB of the right channel is valid on the rising edge of the BCLK following the falling edge of LRCK. Similarly the MSB of the left channel is valid on the rising edge of the BCLK following the rising edge of LRCK.

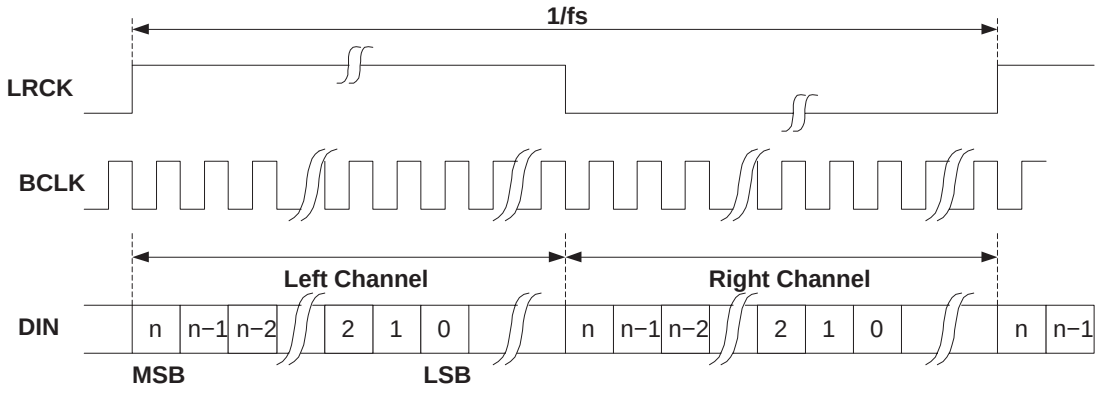


Figure 19. Timing Diagram for Left-Justified Mode

- **I2S MODE**

In I2S mode, the MSB of the left channel is valid on the second rising edge of the BCLK after the falling edge of LRCK. Similarly, the MSB of the right channel is valid on the second rising edge of the BCLK after the rising edge of LRCK.

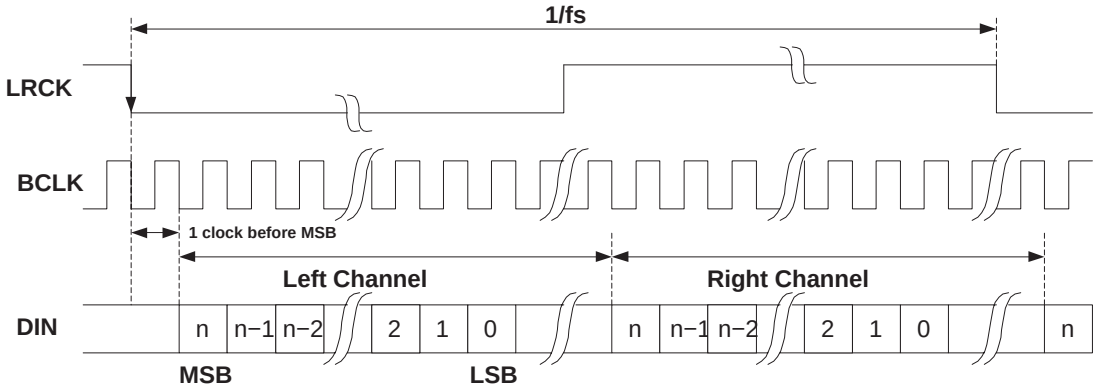


Figure 20. Timing Diagram for I2S Mode

- **DSP MODE**

In DSP mode, the falling edge of LRCK starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of BCLK.

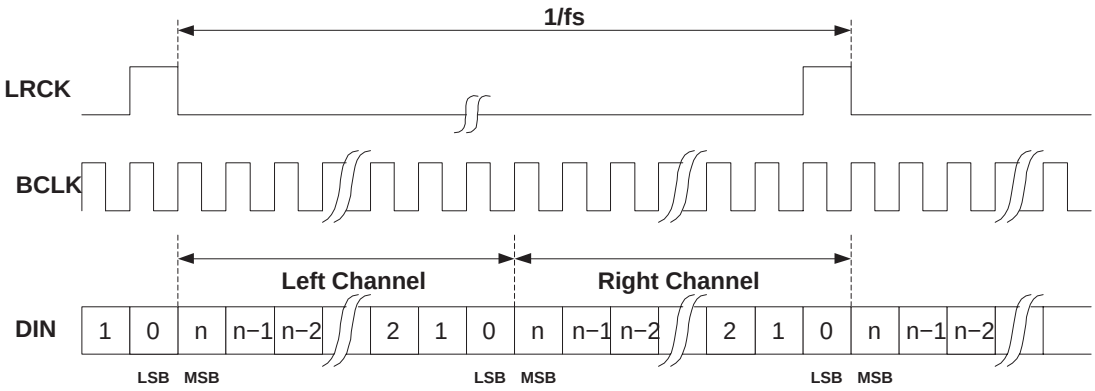


Figure 21. Timing Diagram for DSP Mode

STEREO AUDIO DAC

The TSC2102 includes a stereo audio DAC, which can operate with a maximum sampling rate of 48 kHz and can support all standard audio rates of 8 kHz, 11.025 kHz, 12 kHz, 16kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz.

When the DAC is operating, the TSC2102 requires an audio MCLK input applied. The user is required to set D13 of control register 06H/Page2 to indicate which Fsref rate is being used. If the DAC is powered up, then the touch screen ADC runs off the MCLK and BCLK, and the internal oscillator is powered down to save power.

Each channel of the stereo audio DAC consists of a digital audio processing block, a digital interpolation filter, digital delta-sigma modulator, and analog reconstruction filter. The DAC is designed to provide enhanced performance at low sample rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20 kHz. This is realized by keeping the upsampled rate constant at 128 x Fsref and changing the oversampling ratio as the input sample rate is changed. For Fsref of 48 kHz, the digital delta-sigma modulator always operates at a rate of 6.144 MHz. This ensures that quantization noise generated within the delta-sigma modulator stays low within the frequency band below 20 kHz at all sample rates. Similarly, for Fsref rate of 44.1 kHz, the digital delta-sigma modulator always operates at a rate of 5.6448 MHz.

PLL

The TSC2102 has an on chip PLL to generate the needed internal audio clocks from the clock available in the system. The PLL supports a MCLK varying from 2 MHz to 50 MHz and is register programmable to enable generation of the required sampling rates from a wide range of system clocks.

The DAC sampling rate is given by:

DAC_FS = Fsref/N

where, Fsref is 44.1 kHz or 48 kHz and N =1, 1.5, 2, 3, 4, 5, 6 are register programmable.

The PLL can be enabled or disabled using register programmability.

- When PLL is disabled

$$Fsref = \frac{MCLK}{128 \times Q}$$

Q = 2, 3…17

- When PLL is enabled

$$Fsref = \frac{MCLK \times K}{2048 \times P}$$

P = 1, 2, 3, …, 8

K = J.D

J = 1, 2, 3, ….,64

D = 0, 1, 2, …, 9999

where, D is the 4-digit fractional part of K with lagging zeros (e.g. if K = 8.5, then D = 5000 and if K = 8.02, then D = 200).

P, J and D are register programmable.

- When D = 0, the following condition needs to be satisfied

$$2\ MHz \leq \frac{MCLK}{P} \leq 20\ MHz$$

- When D ≠ 0, the following condition needs to be satisfied

$$10\ MHz \leq \frac{MCLK}{P} \leq 20\ MHz$$

Example 1:

For MCLK = 12 MHz and Fsref = 44.1 kHz

P = 1, K = 7.5264 $\Rightarrow$ J = 7, D = 5264

Example 2:

For MCLK = 12 MHz and Fsref = 48.0 kHz

P = 1, K = 8.192 $\Rightarrow$ J = 8, D = 1920

Digital Audio Processing

The DAC channel consists of optional filters for de-emphasis and bass, treble, midrange level adjustment, or speaker equalization. The de-emphasis function is only available for sample rates of 32 kHz, 44.1 kHz, and 48 kHz. The transfer function consists of a pole with time constant of 50 μs and a zero with time constant of 15 μs. Frequency response plots are given in the *Audio Codec Filter Frequency Responses* section of this data sheet.

The DAC digital effects processing block also includes a fourth order digital IIR filter with programmable coefficients (one set per channel). The filter is implemented as cascade of two biquad sections with frequency response given by:

$$\left(\frac{N0 + 2 \times N1 \times z^{-1} + N2 \times z^{-2}}{32768 - 2 \times D1 \times z^{-1} - D2 \times z^{-2}}\right)\left(\frac{N3 + 2 \times N4 \times z^{-1} + N5 \times z^{-2}}{32768 - 2 \times D4 \times z^{-1} - D5 \times z^{-2}}\right)$$

The N and D coefficients are fully programmable, and the entire filter can be enabled or bypassed. The coefficients for this filter implement a variety of sound effects with bass boost or treble boost as the most commonly used in portable audio applications. The default N and D coefficients in the part are given by:

N0 = N3 = 27619 D1 = D4 = 32131

N1 = N4 = −27034 D2 = D5 = −31506

N2 = N5 = 26461

and implement a shelving filter with 0-dB gain from dc to approximately 150 Hz, at which point it rolls off to 3-dB attenuation for higher frequency signals, thus giving a 3-dB boost to signals below 150 Hz. The N and D coefficients are represented by 16-bit twos complement numbers with values ranging from 32767 to −32768. Frequency response plots are given in the *Audio Codec Filter Frequency Responses* section of this data sheet.

Interpolation Filter

The interpolation filter upsamples the output of the digital audio processing block by the required oversampling ratio. It provides a linear phase output with a group delay of 21/Fs.

In addition, the digital interpolation filter provides enhanced image filtering to reduce signal images caused by the upsampling process that are below 20 kHz. For example, upsampling an 8-kHz signal produces signal images at multiples of 8 kHz, i.e., 8 kHz, 16 kHz, 24 kHz, etc. The images at 8 kHz and 16 kHz are below 20 kHz and still audible to the listener, therefore, they must be filtered heavily to maintain a good quality output. The interpolation filter is designed to maintain at least 65-dB rejection of images that land below 7.455 Fs. Passband ripple for all sample-rate cases (from 20 Hz to 0.45 Fs) is ±0.06 dB maximum

Delta-Sigma DAC

The audio digital-to-analog converter incorporates a third order multibit delta-sigma modulator with 768/512/384/256/192/128 times oversampling followed by an analog reconstruction filter. The DAC provides high-resolution, low-noise performance, using oversampling and noise shaping techniques. The analog reconstruction filter design consists of a 6 tap analog FIR filter followed by a continuous time RC filter. The analog FIR operates at 6.144 MHz (128x48 kHz, for Fsref of 48 kHz) or at 5.6448 MHz (128x44.1 kHz, for Fsref of 44.1 kHz). The DAC analog performance can be degraded by excessive clock jitter on the MCLK input. Therefore, care must be taken to keep jitter on this clock to a minimum.

DAC Digital Volume Control

The DAC has a digital volume control block, which implements a programmable gain. The volume level can be varied from 0dB to –63.5 dB in 0.5 dB steps, in addition to a mute bit, independently for each channel. The volume level of both channels can also be changed simultaneously by the master volume control. The gain is implemented with a soft-stepping algorithm, which only changes the actual volume by one step per input sample, either up or down, until the desired volume is reached. The rate of soft-stepping can be slowed to one step per two input samples through D1 of control register 04H/Page2.

Because of soft-stepping, the host does not know when the DAC has actually been muted. This may be important if the host wishes to mute the DAC before making a significant change, such as changing sample rates. In order to help with this situation, the part provides a flag back to the host via a read-only register bit (D2−D3 of control register 04H/Page2) that alerts the host when the part has completed the soft-stepping and the actual volume has reached the desired volume level.

The TSC2102 also includes functionality to detect when the user switches on or off the de-emphasis or bass-boost functions, then first (1) soft-mute the DAC volume control, (2) change the operation of the digital effects processing, and (3) soft-unmute the TSC2102. This avoids any possible pop/clicks in the audio output due to instantaneous changes in the filtering. A similar algorithm is used when first powering up or down the DAC. The circuit begins operation at power up with the volume control muted, then soft-steps it up to the desired volume level. At power down, the logic first soft-steps the volume down to a mute level, then powers down the circuitry.

Headphone Driver

The TSC2102 features a stereo headphone driver that can deliver 25 mW per channel at 3.3-V supply, into 16-Ω load. The headphones can be connected in a single-ended configuration using ac-coupling capacitors, or the capacitors can be removed and virtual ground (VGND) connection powered. These two configurations are shown in Figure 22. If the headphone amplifiers are not needed, such as when the external audio amplifier is used, then the headphone drivers can be bypassed to save power using register programming. When bypassed, the HPR and HPL outputs act as line level outputs capable of driving a load of 10 kΩ minimum.

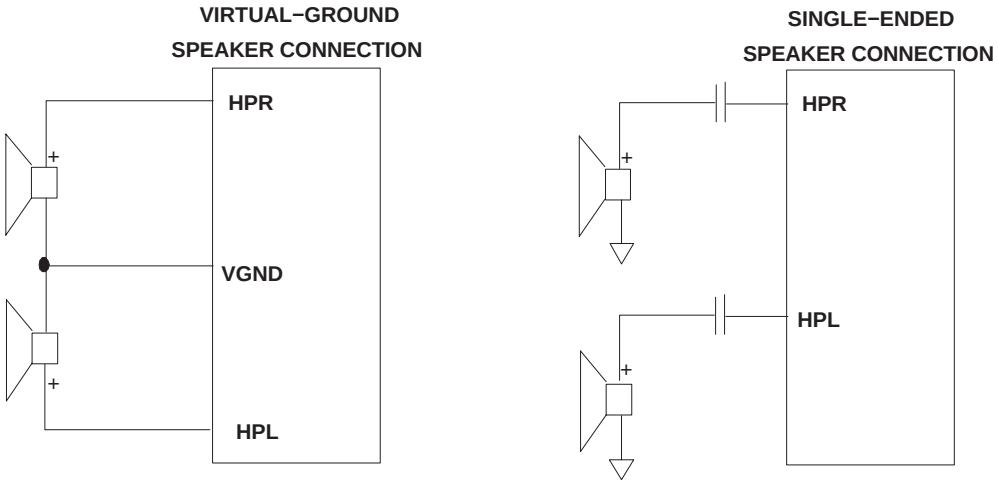


Figure 22. Connection Diagram for DAC Outputs

KEYCLICK

A special circuit has also been included for inserting a square-wave signal into the analog output signal path based on register control. This functionality is intended for generating keyclick sounds for user feedback. Register 04H/Page2 contains bits that control the amplitude, frequency, and duration of the square−wave signal. The frequency of the signal can be varied from 62.5 Hz to 8 kHz and its duration can be programmed from 2 periods to 32 periods. Whenever this register is written, the square wave is generated and coupled into the audio output, going to both the outputs. The keyclick enable bit D15 of control register 04H/Page2 is reset after the duration of keyclick is played out. This capability is available even when the DAC is powered down.

SPI DIGITAL INTERFACE

All TSC2102 control registers are programmed through a standard SPI bus. The SPI allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master generates the synchronizing clock and initiates transmissions. The SPI slave devices depend on a master to start and synchronize transmissions.

A transmission begins when initiated by a master SPI. The byte from the master SPI begins shifting in on the slave SPIDIN (MOSI) pin under the control of the master serial clock. As the byte shifts in on the SPIDIN pin, a byte shifts out on the SPIDOUT (MISO) pin to the master shift register.

The idle state of the serial clock for the TSC2102 is low, which corresponds to a clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The TSC2102 interface is designed so that with a clock phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI pin and the slave begins driving its SPIDOUT pin on the first serial clock edge. The $\overline{SS}$ pin can remain low between transmissions; however, the TSC2102 only interprets command words which are transmitted after the falling edge of $\overline{SS}$.

TSC2102 COMMUNICATION PROTOCOL

Register Programming

The TSC2102 is entirely controlled by registers. Reading and writing these registers is controlled by an SPI master and accomplished by the use of a 16-bit command, which is sent prior to the data for that register. The command is constructed as shown in Figure 23.

The command word begins with a R/W bit, which specifies the direction of data flow on the SPI serial bus. The following 4 bits specify the page of memory this command is directed to, as shown in Table 2. The next six bits specify the register address on that page of memory to which the data is directed. The last five bits are reserved for future use and should be written only with zeros.

Table 2. Page Addressing

PG3	PG2	PG1	PG0	PAGE ADDRESSED
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

To read all the first page of memory, for example, the host processor must send the TSC2102 the command 0x8000 – this specifies a read operation beginning at page 0, address 0. The processor can then start clocking data out of the TSC2102. The TSC2102 automatically increments its address pointer to the end of the page; if the host processor continues clocking data out past the end of a page, the TSC2102 sends back the value 0xFFFF.

Likewise, writing to page 1 of memory consists of the processor writing the command 0x0800, which specifies a write operation, with PG0 set to 1, and all the ADDR bits set to 0. This results in the address pointer pointing at the first location in memory on Page 1. See the section on the TSC2102 memory map for details of register locations

BIT 15 MSB	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB
R/W*	PG3	PG2	PG1	PG0	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	0	0	0	0	0

Figure 23. TSC2102 Command Word

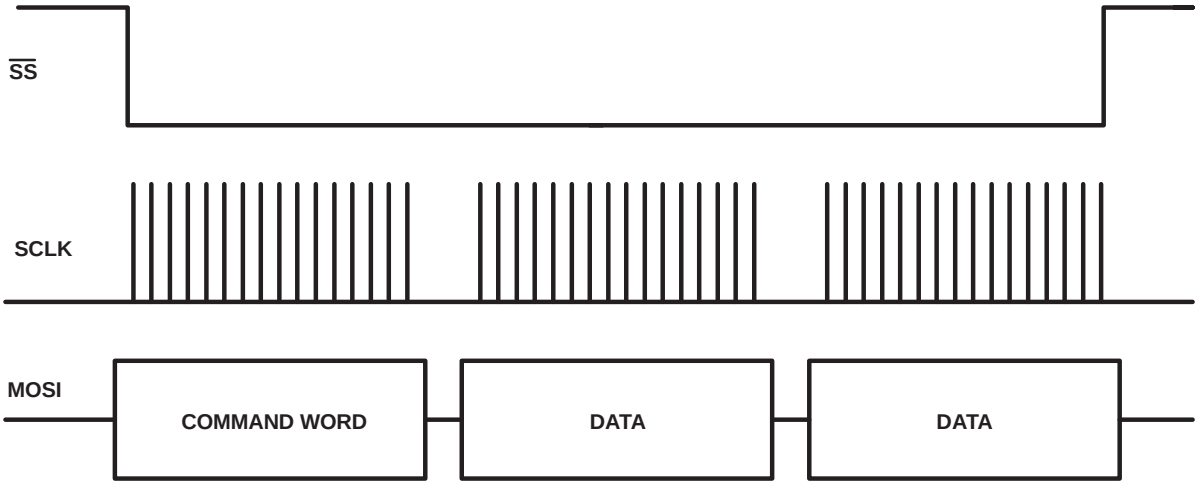


Figure 24. Write Operation for TSC2102 SPI Interface

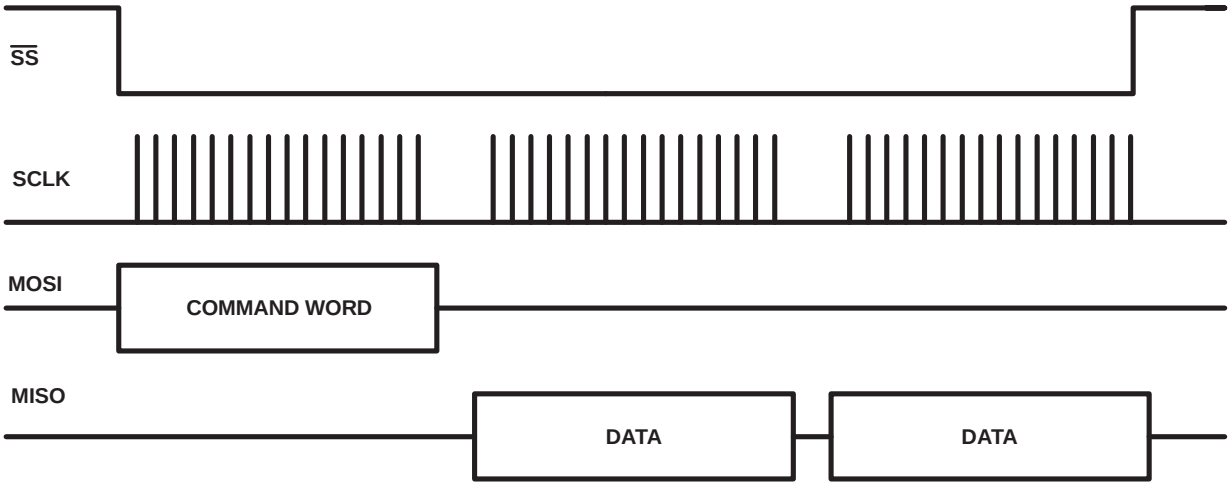


Figure 25. Read Operation for TSC2102 SPI Interface

TSC2102 MEMORY MAP

The TSC2102 has several 16-bit registers, which allow control of the device as well as providing a location for results from the TSC2102 to be stored until read by the host microprocessor. These registers are separated into three pages of memory in the TSC2102: a data page (Page 0) and control pages (Page 1 and Page 2). The memory map is shown in Table 3.

Table 3. Memory Map

Page 0: Touch Screen Data Registers		Page 1: Touch Screen Control Registers		Page 2: Audio Control Registers	
ADDR	**REGISTER**	**ADDR**	**REGISTER**	**ADDR**	**REGISTER**
00	X	00	TSC ADC	00	Audio Control 1
01	Y	01	Status	01	Reserved
02	Z1	02	Reserved	02	DAC Volume Control
03	Z2	03	Reference	03	Reserved
04	Reserved	04	Reset	04	Audio Control 2
05	BAT1	05	Configuration	05	Stereo DAC Power Control
06	BAT2	06	Reserved	06	Audio Control 3
07	AUX	07	Reserved	07	Audio Bass−Boost Filter Coefficients
08	Reserved	08	Reserved	08	Audio Bass−Boost Filter Coefficients
09	TEMP1	09	Reserved	09	Audio Bass−Boost Filter Coefficients
0A	TEMP2	0A	Reserved	0A	Audio Bass−Boost Filter Coefficients
0B	Reserved	0B	Reserved	0B	Audio Bass−Boost Filter Coefficients
0C	Reserved	0C	Reserved	0C	Audio Bass−Boost Filter Coefficients
0D	Reserved	0D	Reserved	0D	Audio Bass−Boost Filter Coefficients
0E	Reserved	0E	Reserved	0E	Audio Bass−Boost Filter Coefficients
0F	Reserved	0F	Reserved	0F	Audio Bass−Boost Filter Coefficients
10	Reserved	10	Reserved	10	Audio Bass−Boost Filter Coefficients
11	Reserved	11	Reserved	11	Audio Bass−Boost Filter Coefficients
12	Reserved	12	Reserved	12	Audio Bass−Boost Filter Coefficients
13	Reserved	13	Reserved	13	Audio Bass−Boost Filter Coefficients
14	Reserved	14	Reserved	14	Audio Bass−Boost Filter Coefficients
15	Reserved	15	Reserved	15	Audio Bass−Boost Filter Coefficients
16	Reserved	16	Reserved	16	Audio Bass−Boost Filter Coefficients
17	Reserved	17	Reserved	17	Audio Bass−Boost Filter Coefficients
18	Reserved	18	Reserved	18	Audio Bass−Boost Filter Coefficients
19	Reserved	19	Reserved	19	Audio Bass−Boost Filter Coefficients
1A	Reserved	1A	Reserved	1A	Audio Bass−Boost Filter Coefficients
1B	Reserved	1B	Reserved	1B	PLL Programmability
1C	Reserved	1C	Reserved	1C	PLL Programmability
1D	Reserved	1D	Reserved	1D	Audio Control 4
1E	Reserved	1E	Reserved	1E	Reserved
1F	Reserved	1F	Reserved	1F	Reserved

TSC2102 CONTROL REGISTERS

This section describes each of the registers shown in the memory map of Table 3. The registers are grouped according to the function they control. In the TSC2102, bits in control registers can refer to slightly different functions depending upon whether you are reading the register or writing to the register.

TSC2102 Data Registers (Page 0)

The data registers of the TSC2102 hold data results from conversion performed by the touch screen ADC. All of these registers default to 0000H upon reset. These registers are *read only*.

X, Y, Z1, Z2, BAT1, BAT2, AUX, TEMP1 and TEMP2 Registers

The results of all A/D conversions are placed in the appropriate data register. The data format of the result word, R, of these registers is right-justified, as follows:

BIT 15 MSB	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB
0	0	0	0	R11 MSB	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0 LSB

PAGE 1 CONTROL REGISTER MAP

REGISTER 00H: Touch Screen ADC Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	PSTCM	R/W	0(for read status) 0(for write status)	Pen Status/Control Mode. READ 0 => There is no screen touch (default) 1 => The pen is down WRITE 0 => Host controlled touch screen conversions(default). 1=> TSC2102 controlled touch screen conversions.
D14	ADST	R/W	1(for read status) 0(for write status)	A/D Status. READ 0 => ADC is busy 1 => ADC is not busy (default) WRITE 0 => Normal mode. (default) 1 => Stop conversion and power down. Power down happens immediately

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D13−10	ADSCM	R/W	0000	A/D Scan Mode. 0000 => No scan 0001 => Touch screen scan function: X and Y coordinates are converted and the results returned to X and Y data registers. Scan continues until either the pen is lifted or a stop bit is sent. 0010 => Touch screen scan function: X, Y, Z1 and Z2 coordinates are converted and the results returned to X, Y, Z1 and Z2 data registers. Scan continues until either the pen is lifted or a stop bit is sent. 0011 => Touch screen scan function: X coordinate is converted and the results returned to X data register. 0100 => Touch screen scan function: Y coordinate is converted and the results returned to Y data register. 0101 => Touch screen scan function: Z1 and Z2 coordinates are converted and the results returned to Z1 and Z2 data registers. 0110 => BAT1 input is converted and the result is returned to the BAT1 data register. 0111 => BAT2 input is converted and the result is returned to the BAT2 data register. 1000 => AUX input is converted and the result is returned to the AUX data register. 1001 => Scan function :AUX input is converted and the result is returned to the AUX data register. Scan continues until stop bit is sent. 1010 => TEMP1 is converted and the result is returned to the TEMP1 data register. 1011 => Port scan function: BAT1, BAT2 and AUX inputs are measured and the results returned to the appropriate data registers. 1100 => TEMP2 is converted and the result is returned to the TEMP2 data register. 1101 => Turn on X+, X− drivers 1110 => Turn on Y+, Y− drivers 1111 => Turn on Y+, X− drivers
D9−D8	RESOL	R/W	00	Resolution Control. The A/D converter resolution is specified with these bits. 00 => 12−bit resolution 01 => 8−bit resolution 10 => 10−bit resolution 11 => 12−bit resolution
D7−D6	ADAVG	R/W	00	Converter Averaging Control. These two bits allow you to specify the number of averages the converter performs selected by bit D0, which selects either mean filter or median filter. Mean Filter / Median filter 00 => No average / No average 01 => 4−data average / 5-data average 10 => 8−data average / 9-data average 11 => 16−data average / 15-data average
D5−D4	ADCR	R/W	00	Conversion Rate Control. These two bits specify the internal clock rate which the A/D converter uses to perform a single conversion. These bits are the same whether reading or writing. $t_{conv} = \frac{N + 4}{f_{INTCLK}}$ where f_{INTCLK} is the internal clock frequency. For example, with 12-bit resolution and a 2-MHz internal clock frequency, the conversion time is 8.0 µs. This yields an effective throughput rate of 125 kHz. 00 => 8-MHz internal clock rate (use for 8-bit resolution only) 01 => 4-MHz internal clock rate (use for 8-bit/10-bit resolution only) 10 => 2-MHz internal clock rate 11 => 1-MHz internal clock rate

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D3−D1	PVSTC	R/W	000	Panel Voltage Stabilization Time Control. These bits allow you to specify a delay time from the time the touch screen drivers are enabled to the time the voltage is sampled and a conversion is started. This allows the user to adjust for the settling of the individual touch panel and external capacitances. 000 => 0-µs stabilization time 001 => 100-µs stabilization time 010 => 500-µs stabilization time 011 => 1-ms stabilization time 100 => 5-ms stabilization time 101 => 10-ms stabilization time 110 => 50-ms stabilization time 111 => 100-ms stabilization time
D0	AVGFS	R/W	0	Average Filter select 0 => Mean filter 1 => Median filter

REGISTER 01H: Status Register

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15−D14	$\overline{\text{PINTDAV}}$	R/W	10	Pen Interrupt or Data Available. These two bits program the function of the $\overline{\text{PINTDAV}}$ pin. 00 => Acts as PEN interrupt (active low) only. When PEN touch is detected, $\overline{\text{PINTDAV}}$ goes low. 01 => Acts as data available (active low) only. The $\overline{\text{PINTDAV}}$ goes low as soon as one set of ADC conversion(s) is completed. For scan mode, $\overline{\text{PINTDAV}}$ remains low as long as all the appropriate registers have not been read out. 10 => Acts as both PEN interrupt and data available. When PEN touch is detected, $\overline{\text{PINTDAV}}$ goes low. $\overline{\text{PINTDAV}}$ goes high once all the selected conversions are over. 11 => Same as 10 Note: See the section *Conversion Time Calculation for the TSC2102* in this data sheet for timing diagrams and conversion time calculations.
D13	PWRDN	R	0	TSC−ADC Power down status 0 => TSC−ADC is active 1 => TSC−ADC stops conversion and powers down
D12	HCTLM	R	0	Host Controlled Mode Status 0 => Host controlled mode 1 => Self (TSC2102) controlled mode
D11	DAVAIL	R	0	Data Available Status 0 => No data available. 1 => Data is available(i.e one set of conversion is done) Note:− This bit gets cleared only after all the converted data have been completely read out.
D10	XSTAT	R	0	X Data Register Status 0 => No new data is available in X−data register 1 => New data for X−coordinate is available in register Note: This bit gets cleared only after the converted data of X coordinate has been completely read out of the register.
D9	YSTAT	R	0	Y Data Register Status 0 => No new data is available in Y−data register 1 => New data for Y−coordinate is available in register Note: This bit gets cleared only after the converted data of Y coordinate has been completely read out of the register.
D8	Z1STAT	R	0	Z1 Data Register Status 0 => No new data is available in Z1−data register 1 => New data is available in Z1−data register Note: This bit gets cleared only after the converted data of Z1 coordinate has been completely read out of the register.

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D7	Z2STAT	R	0	Z2 Data Register Status 0 => No new data is available in Z2−data register 1 => New data is available in Z2−data register Note: This bit gets cleared only after the converted data of Z2 coordinate has been completely read out of the register.
D6	B1STAT	R	0	BAT1 Data Register Status 0 => No new data is available in BAT1−data register 1 => New data is available in BAT1−data register Note: This bit gets cleared only after the converted data of BAT1 has been completely read out of the register.
D5	B2STAT	R	0	BAT2 Data Register Status 0 => No new data is available in BAT2−data register 1 => New data is available in BAT2−data register Note: This bit gets cleared only after the converted data of BAT2 has been completely read out of the register.
D4	AXSTAT	R	0	AUX Data Register Status 0 => No new data is available in AUX−data register 1 => New data is available in AUX−data register Note: This bit gets cleared only after the converted data of AUX has been completely read out of the register.
D3		R	0	Reserved
D2	T1STAT	R	0	TEMP1 Data Register Status 0 => No new data is available in TEMP1−data register 1 => New data is available in TEMP1−data register Note: This bit gets cleared only after the converted data of TEMP1 has been completely read out of the register.
D1	T2STAT	R	0	TEMP2 Data Register Status 0 => No new data is available in TEMP2−data register 1 => New data is available in TEMP2−data register Note: This bit gets cleared only after the converted data of TEMP2 has been completely read out of the register.
D0		R	0	Reserved

REGISTER 02H: Reserved

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15−D0		R	FFFFH	Reserved

REGISTER 03H: Reference Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15−D5		R	000H	Reserved
D4	VREFM	R/W	0	Voltage Reference Mode. This bit configures the VREF pin as either external reference or internal reference. 0 => External reference 1 => Internal reference
D3−D2	RPWUDL	R/W	00	Reference Power Up Delay. These bits allow for a delay time for measurements to be made after the reference powers up, thereby assuring that the reference has settled 00 => 0 µs 01 => 100 µs 10 => 500 µs 11 => 1000 µs Note: This is valid only when the device is programmed for internal reference and Bit D1 = 1, i.e., reference is powered down between the conversions if not required.

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D1	RPWDN	R/W	1	Reference Power Down. This bit controls the power down of the internal reference voltage. 0 => Powered up at all times. 1 => Powered down between conversions. Note: when D4 = 0, i.e. device is in external reference mode, then the internal reference is powered down always.
D0	IREFV	R/W	0	Internal Reference Voltage. This bit selects the internal voltage reference level for the TSC ADC. 0 => VREF = 1.25 V 1 => VREF = 2.50 V

REGISTER 04H: Reset Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15−D0	RSALL	R/W	FFFFH	Reset All. Writing the code 0xBB00, as shown below, to this register causes the TSC2102 to reset all its registers to their default, power−up values. 1011101100000000 => Reset all registers Others => Do not write other sequences to this register.

REGISTER 05H: Configuration Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15−D6		R	000H	Reserved. Write only zeros to these bits.
D5−D3	PRECTM	R/W	000	Precharge Time. These bits set the amount of time allowed for precharging any pin capacitance on the touch screen prior to sensing if a screen touch is happening. 000 => 20 µs 001 => 84 µs 010 => 276 µs 011 => 340 µs 100 => 1.044 ms 101 => 1.108 ms 110 => 1.300 ms 111 => 1.364 ms
D2−D0	RPWUDL	R/W	000	Sense Time. These bits set the amount of time the TSC2102 waits to sense whether the screen is being touched, when converting a coordinate value. 000 => 32 µs 001 => 96 µs 010 => 544 µs 011 => 608 µs 100 => 2.080 ms 101 => 2.144 ms 110 => 2.592 ms 111 => 2.656 ms

PAGE 2 CONTROL REGISTER MAP

REGISTER 00H: Audio Control 1

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15−D12		R	0000	Reserved. Write only 0000 to this location.
D11−D10	WLEN	R/W	00	Codec Word Length 00 => Word length = 16 bit 01 => Word length = 20 bit 10 => Word length = 24 bit 11 => Word length = 32 bit
D9−D8	DATFM	R/W	00	Digital Data Format 00 => I2S mode 01 => DSP mode 10 => Right justified 11 => Left justified
D7−D6		R	00	Reserved. Write only 00 to this location.
D5−D0	DACFS	R/W	000	DAC Sampling Rate 000000 => DAC FS = Fsref/1 001001 => DAC FS = Fsref/(1.5) 010010 => DAC FS = Fsref/2 011011=> DAC FS = Fsref/3 100100 => DAC FS = Fsref/4 101101 => DAC FS = Fsref/5 110110 => DAC FS = Fsref/6 111111 => DAC FS = Fsref/6 others => Not allowed Note: Fsref is either 48 kHz or 44.1 kHz

REGISTER 01H: Reserved

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15−D0		R	FF00H	Reserved. Write only FF00H to this location.

REGISTER 02H: DAC Volume Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	DALMU	R/W	1	DAC Left Channel Mute 1 => DAC left channel muted 0 => DAC left channel not muted
D14−D8	DALVL	R/W	1111111	DAC Left Channel Volume Control 1111111 => DAC left channel Vol = 0 dB 0000001 => DAC left channel Vol = −0.5 dB 0000010 => DAC left channel Vol = −1.0 dB 1111101 => DAC left channel Vol = −62.5 dB 1111110 => DAC left channel Vol = −63.0 dB 0000000 => DAC left channel Vol = −63.5 dB
D7	DARMU	R/W	1	DAC Right Channel Mute 1 => DAC right channel muted 0 => DAC right channel not muted
D6−D0	DARVL	R/W	1111111	DAC Right Channel Volume Control 1111111 => DAC right channel Vol = 0 dB 0000001 => DAC right channel Vol = −0.5 dB 0000010 => DAC right channel Vol = −1.0 dB 1111101 => DAC right channel Vol = −62.5 dB 1111110 => DAC right channel Vol = −63.0 dB 0000000 => DAC right channel Vol = −63.5 dB

REGISTER 03H: Reserved

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15−D0		R	1000101100000000	Reserved. Write only 8B00H to this location.

REGISTER 04H: Audio Control 2

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	KCLEN	R/W	0	Keyclick Enable 0 => Keyclick disabled 1 => Keyclick enabled Note: This bit is automatically cleared after giving out the keyclick signal length equal to the programmed value.
D14−D12	KCLAC	R/W	100	Keyclick Amplitude Control 000 => Lowest amplitude 100 => Medium amplitude 111 => Highest amplitude
D11		R	0	Reserved. Write only 0 to this location.
D10−D8	KCLFRQ	R/W	100	Keyclick Frequency 000 => 62.5Hz 001 => 125Hz 010 => 250Hz 011 => 500Hz 100 => 1kHz 101 => 2kHz 110 => 4kHz 111 => 8kHz
D7−D4	KCLLN	R/W	0001	Keyclick Length 0000 => 2 periods key click 0001 => 4 periods key click 0010 => 6 periods key click 0011 => 8 periods key click all other values => 32 periods key click
D3	DLGAF	R	0	DAC Left Channel PGA Flag (Read Only) 0 => Gain applied /= PGA register setting 1 => Gain applied = PGA register setting. Note: This flag indicates when the soft-stepping for DAC left channel is completed
D2	DRGAF	R	0	DAC Right Channel PGA Flag (Read Only) 0 => Gain applied /= PGA register setting 1 => Gain applied = PGA register setting. Note: This flag indicates when the soft-stepping for DAC right channel is completed
D1	DASTC	R/W	0	DAC Channel PGA Soft-Stepping Control 0 => 0.5dB change every LRCK 1 => 0.5dB change every 2 LRCK
D0		R	0	Reserved. Write only 0 to this location.

REGISTER 05H: Stereo DAC Power Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	PWDNC	R/W	1	Codec Power-Down Control 0 => Codec powered up 1 => Codec powered down
D14−D13		R	01	Reserved. Write only 01 to this location.
D12	DAODRC	R/W	0	DAC Output Driver Control 0 => Headphone driver bypassed 1 => Headphone driver enabled
D11		R	1	Reserved. Write only 1 to this location.
D10	DAPWDN	R/W	1	DAC Power-Down Control 0 => Power up the DAC 1 => Power down the DAC
D9		R	1	Reserved. Write only 1 to this location.
D8	VGPWDN	R/W	1	Driver Virtual Ground Power Down 0 => Power up the VGND amp 1 => Power down the VGND amp
D7		R	1	Reserved. Write only 1 to this location.
D6	DAPWDF	R	1	DAC Power-Down Flag 0 => DAC power down is not complete 1 => DAC power down is complete
D5−D2		R	1000	Reserved. Write only 1000 to this location.
D1	BASSBC	R/W	0	Bass Boost Control 0 => Disable bass boost filter 1 => Enable bass boost filter
D0	DEEMPF	R/W	0	De−Emphasis Filter Enable 0 => Disable de-emphasis filter 1 => Enable de-emphasis filter

REGISTER 06H: Audio Control 3

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15−D14	DMSVOL	R/W	00	DAC Channel Master Volume Control 00 => Left channel and right channel have independent volume controls. 01 => Left channel volume control is the programmed value of the right channel volume control. 10 => Right channel volume control is the programmed value of the left channel volume control. 11 => same as 00
D13	REFFS	R/W	0	Reference Sampling Rate 0 => Fsref = 48.0kHz 1 => Fsref = 44.1kHz
D12	DAXFM	R/W	0	Master Transfer Mode 0 => Continuous data transfer mode 1 => 256−s data transfer mode
D11	SLVMS	R/W	0	Audio Master Slave Selection 0 => TSC2102 is slave DAC 1 => TSC2102 is master DAC
D10−D8		R	000	Reserved. Write only 000 to this location.
D7	DALOVF	R	0	DAC Left Channel Overflow Flag (Read Only) 0 => DAC left channel data is within saturation limits 1 => DAC left channel data has exceeded saturation limits Note : Once this flag is set to 1, it gets cleared only when user reads this register.
D6	DAROVF	R	0	DAC Right Channel Overflow Flag (Read Only) RESET VAL = 0 0 => DAC right channel data is within saturation limits 1 => DAC right channel data has exceeded saturation limits Note : Once this flag is set to 1, it is cleared only when user reads this register
D5−D3		R	000	Reserved. Write only 000 to this location.
D2−D0	REVID	R	001	Revision ID. This field represents the silicon revision and should always read 001.

REGISTER 07H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	L_N0	R/W	27619	Left channel bass-boost coefficient N0.

REGISTER 08H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	L_N1	R/W	−27034	Left channel bass-boost coefficient N1.

REGISTER 09H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	L_N2	R/W	26461	Left channel bass-boost coefficient N2.

REGISTER 0AH: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	L_N3	R/W	27619	Left channel bass-boost coefficient N3.

REGISTER 0BH: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	L_N4	R/W	−27034	Left channel bass-boost coefficient N4.

REGISTER 0CH: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	L_N5	R/W	26461	Left channel bass-boost coefficient N5.

REGISTER 0DH: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	L_D1	R/W	32131	Left channel bass-boost coefficient D1.

REGISTER 0EH: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	L_D2	R/W	−31506	Left channel bass-boost coefficient D2.

REGISTER 0FH: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	L_D4	R/W	32131	Left channel bass-boost coefficient D4.

REGISTER 10H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	L_D5	R/W	−31506	Left channel bass-boost coefficient D5.

REGISTER 11H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	R_N0	R/W	27619	Right channel bass-boost coefficient N0.

REGISTER 12H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	R_N1	R/W	−27034	Right channel bass-boost coefficient N1.

REGISTER 13H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	R_N2	R/W	26461	Right channel bass-boost coefficient N2.

REGISTER 14H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	R_N3	R/W	27619	Right channel bass-boost coefficient N3.

REGISTER 15H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	R_N4	R/W	−27034	Right channel bass-boost coefficient N4.

REGISTER 16H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	R_N5	R/W	26461	Right channel bass-boost coefficient N5.

REGISTER 17H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	R_D1	R/W	32131	Right channel bass-boost coefficient D1.

REGISTER 18H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	R_D2	R/W	−31506	Right channel bass-boost coefficient D2.

REGISTER 19H: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	R_D4	R/W	32131	Right channel bass-boost coefficient D4.

REGISTER 1AH: Audio Bass Boost Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15−D0	R_D5	R/W	−31506	Right channel bass-boost coefficient D5.

REGISTER 1BH: PLL Programmability

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	PLLEN	R/W	0	PLL Enable 0 => Disable PLL 1 => Enable PLL
D14−D11	QVAL	R/W	0010	Q value. Valid only if D15 = 0. 0000 => 16 0001 => 1 0010 => 2 1110 => 14 1111 => 15
D10−D8	PVAL	R/W	000	P value. Valid only if D15 = 1. 000=> 8 001=> 1 010 => 2 110 => 6 111 => 7
D7−D2	JVAL	R/W	000001	J value. Valid only if D15 = 1. 000001 => 1 000010 => 2 111101 => 61 111110 => 62 111111 => 63
D1−D0	Reserved	R	00	Reserved. Write only 00 to this location.

REGISTER 1CH: PLL Programmability

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15−D2	DVAL	R/W	0 (in decimal)	D value. Used when PLL is enabled. D value is valid from 0000 to 9999 in decimal. Programmed value greater than 9999 is treated as 9999 00000000000000 => 0 decimal 00000000000001 => 1 decimal
D1−D0	Reserved	R	00	Reserved (write only 00)

REGISTER 1DH: Audio Control 4

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	Reserved	R	0	Reserved. Write only 0 to this location.
D14	DASTPD	R/W	0	DAC Soft-Stepping Control 0 => Soft-stepping is enabled 1 => Soft-stepping is disabled
D13−D2	Reserved	R	000000000000	Reserved. Write only 000000000000 in this location.
D1−D0	Reserved	R	XX	Reserved (write only 00)

LAYOUT

The following layout suggestions should provide optimum performance from the TSC2102. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly *clean* power and grounds because most of the internal components are very low power. This situation means less bypassing for the converter power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care must be taken with the physical layout of the TSC2102 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an *n-bit* SAR converter, there are *n windows* in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the timing of the critical *n windows*.

With this in mind, power to the TSC2102 must be clean and well bypassed. A 0.1-µF ceramic bypass capacitor must be placed as close to the device as possible. A 1-µF to 10-µF capacitor may also be needed if the impedance between the TSC2102 supply pins and the system power supply is high.

The VREF pin requires a minimum bypass capacitor of 0.1 µF, although a larger value can be used to reduce the reference noise level. If an external reference voltage originates from an op-amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The TSC2102 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high frequency noise can be filtered out, voltage variation due to line frequency (50 Hz or 60 Hz) can be difficult to remove.

The ground pins must be connected to a clean ground point. In many cases, this is the *analog* ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry or battery connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care must be taken with the connection between the converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection must be as short and robust as possible. Loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch-screen applications (e.g., applications that require a back-lit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause *flickering* of the converted ADC data. Several things can be done to reduce this error, such as utilizing a touch screen with a bottom-side metal layer connected to ground. This couples the majority of noise to ground. Additionally, filtering capacitors, from Y+, Y–, X+, and X– to ground, can also help. Note, however, that the use of these capacitors increases screen settling time and requires longer panel voltage stabilization times, as well as increased precharge and sense times for the $\overline{\text{PINTDAV}}$ circuitry of the TSC2102.

CONVERSION TIME CALCULATIONS FOR THE TSC2102

Touch Screen Conversion Initiated At Touch Detect

The time needed to get a converted X/Y coordinate for reading can be calculated by (not including the time needed to send the command over the SPI bus):

$$t_{coordinate} = 2 \times \left[\frac{\left(t_{PRE} + t_{SNS} + t_{PVS}\right)}{125\ ns}\right] \times t_{OSC} + 2 \times \left\{N_{AVG}\left[\left(N_{BITS} + 1\right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12\right] + 1\right\}$$

$$\times t_{OSC} + 18 \times t_{OSC} + n_2 \times t_{OSC} + n_3 \times t_{OSC}$$

where:

$t_{coordinate}$ = time to convert X/Y coordinate

t_{PVS} = Panel voltage stabilization time

t_{PRE} = precharge time

t_{SNS} = sense time

N_{AVG} = number of averages; for no averaging, N_{AVG} = 1

N_{BITS} = number of bits of resolution

f_{conv} = A/D converter clock frequency

t_{OSC} = Oscillator clock period

n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

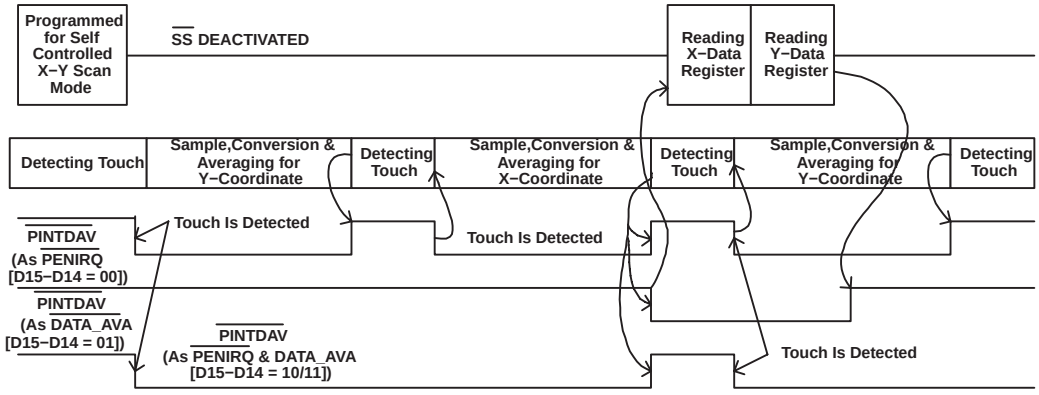
n_2 = 4 ; if t_{PVS} = 0 µs

0 ; if $t_{PVS} \neq$ 0 µs

n_3 = 0 ; if t_{SNS} = 32 µs

2 ; if $t_{SNS} \neq$ 32 µs

NOTE: The above formula is exactly valid only when the audio DAC is powered down. Also, after touch detect, the formula holds true from second conversion onwards. For continuous touch and D15−D14 = 00/10/11, the high duration of the PINTDAV signal is given by $t_{PRE} + t_{SNS}$ with an oscillator clock of 8 MHz.



The time for a complete X/Y/Z1/Z2 coordinate conversion is given by(not including the time needed to send the command over the SPI bus):

$$t_{coordinate} = 3 \times \left[\frac{\left(t_{PRE} + t_{SNS} + t_{PVS}\right)}{125\ ns}\right] \times t_{OSC} + 4 \times \left\{N_{AVG}\left[\left(N_{BITS} + 1\right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12\right] + 1\right\}$$

$$\times t_{OSC} + 33 \times t_{OSC} + n_2 \times t_{OSC} + n_3 \times t_{OSC}$$

n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

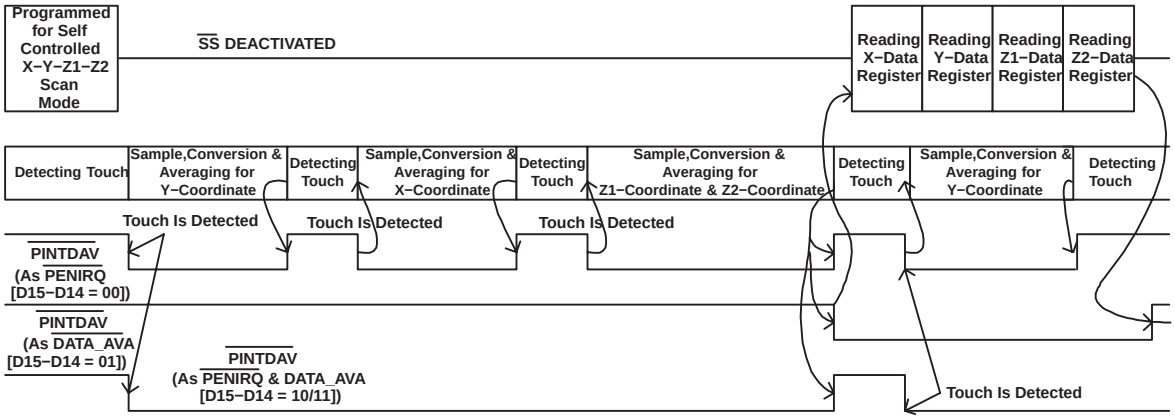
n_2 = 4 ; if t_{PVS} = 0 µs

0 ; if $t_{PVS} \neq$ 0 µs

n_3 = 0 ; if t_{SNS} = 32 µs

3 ; if $t_{SNS} \neq$ 32 µs

NOTE: The above formula is exactly valid only when the audio DAC is powered down. Also after touch detect the formula holds true from second conversion onwards. For continuous touch and D15−D14 = 00/10/11, the high duration of the $\overline{\text{PINTDAV}}$ signal is given by $t_{PRE} + t_{SNS}$ with an oscillator clock of 8 MHz.



Touch Screen Conversion Initiated by the Host

The time needed to convert any single coordinate either X or Y under host control (not including the time needed to send the command over the SPI bus) is given by:

$$t_{coordinate} = \left[\frac{\left(t_{PVS}\right)}{125\ ns}\right] \times t_{OSC} + \left\{N_{AVG}\left[\left(N_{BITS} + 1\right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12\right] + 1\right\}$$

$$\times t_{OSC} + 14 \times t_{OSC} + n_2 \times t_{OSC}$$

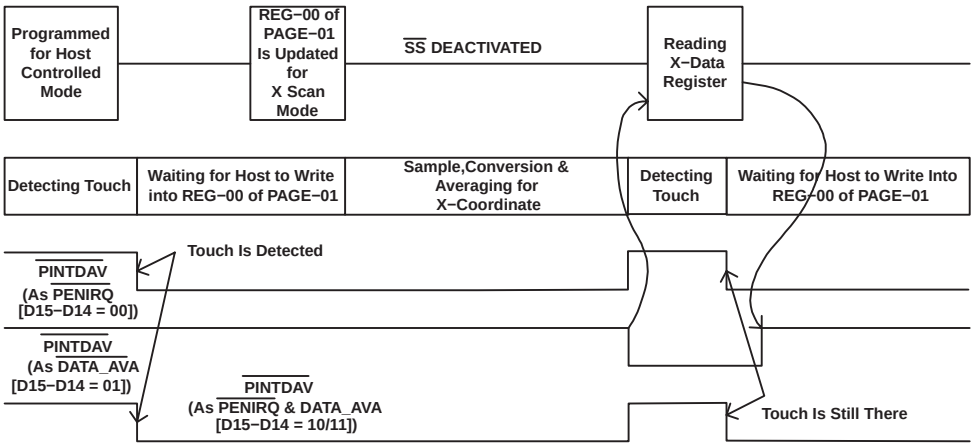
n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

n_2 = 2 ; if t_{PVS} = 0 µs

0 ; if $t_{PVS} \neq$ 0 µs

NOTE: For continuous touch and D15−D14 = 00/10/11, the high duration of the $\overline{\text{PINTDAV}}$ signal is given by $t_{PRE} + t_{SNS}$ with an oscillator clock of 8 MHz.



The time needed to convert the Z coordinate under host control (not including the time needed to send the command over the SPI bus) is given by:

$$t_{coordinate} = \left[\frac{\left(t_{PVS}\right)}{125\ ns}\right] \times t_{OSC} + 2 \times \left\{N_{AVG}\left[\left(N_{BITS} + 1\right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12\right] + 1\right\}$$

$$\times\ t_{OSC} + 20 \times t_{OSC} + n_2 \times t_{OSC}$$

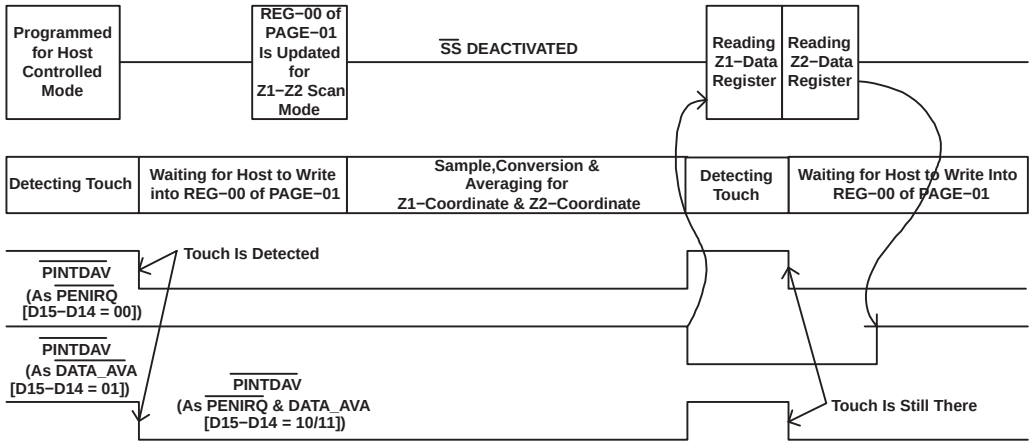
n_1 = 6 ; if f_{conv} = 8 MHz

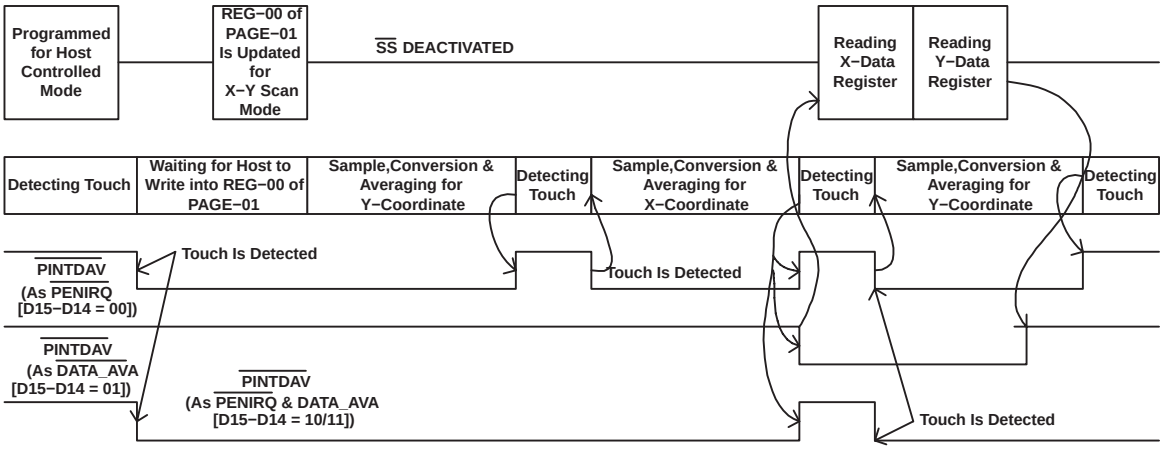
7 ; if $f_{conv} \neq$ 8 MHz

n_2 = 2 ; if t_{PVS} = 0 µs

0 ; if $t_{PVS \neq}$ 0 µs

NOTE: For continuous touch and D15−D14 = 00/10/11, the high duration of the $\overline{\text{PINTDAV}}$ signal is given by $t_{PRE} + t_{SNS}$ with an oscillator clock of 8 MHz.





Non-Touch Screen Measurement Operation

The time needed to make temperature, auxiliary, or battery measurements is given by:

$$t = \left\{ N_{AVG} \left[\left(N_{BITS} + 1 \right) \times \frac{8\ MHz}{f_{conv}} + n_1 + n_2 \right] + 1 \right\} \times t_{OSC} + 15 \times t_{OSC} + n_3 \times t_{OSC}$$

where:

n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

n_2 = 24 ; if measurement is for TEMP1 case

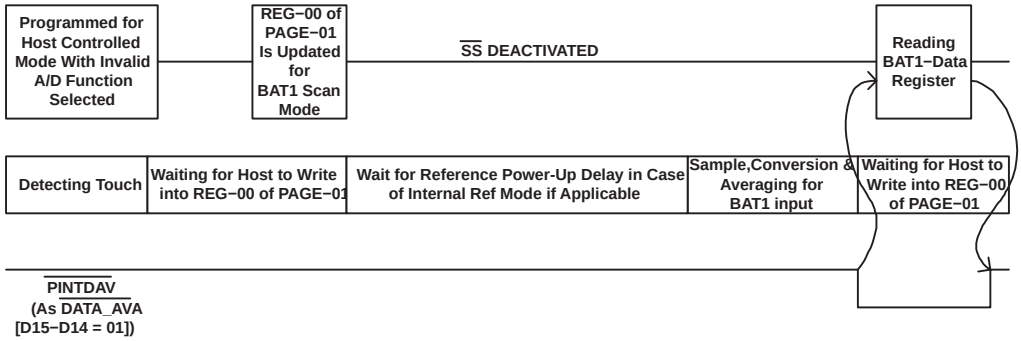
12 ; if measurement is for other than TEMP1 case

n_3 = 0 ; if external reference mode is selected

3 ; if t_{REF} = 0 µs or reference is programmed for power up all the time.

1 + t_{REF} /125 ns; if $t_{REF} \neq$ 0 µs and reference needs to power down between conversions.

t_{REF} is the reference power up delay time.



The time needed for continuous AUX conversion in scan mode is given by:

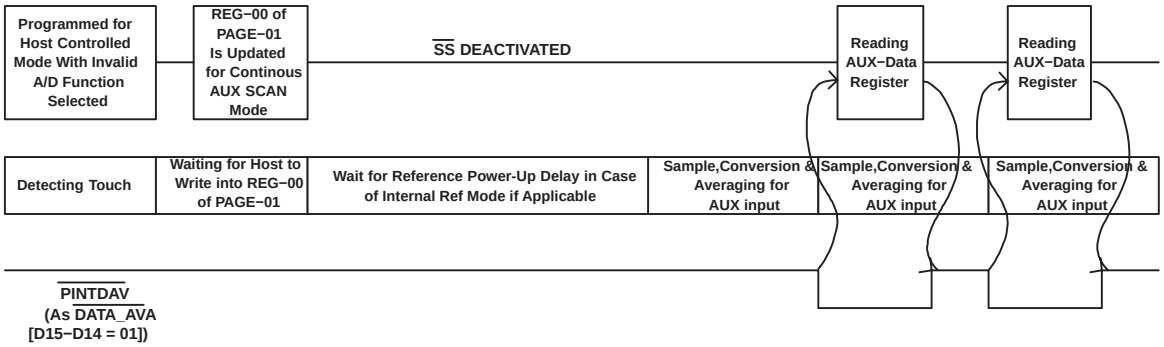
$$t = \left\{ N_{AVG} \left[\left(N_{BITS} + 1 \right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12 \right] + 1 \right\} \times t_{OSC} + 8 \times t_{OSC}$$

where:

n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

NOTE: The above equation is valid only from second conversion onwards.



Port Scan Operation

The time needed to complete one set of port scan conversions is given by:

$$t = 3 \times \left\{ N_{AVG} \left[\left(N_{BITS} + 1 \right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12 \right] + 1 \right\} \times t_{OSC} + 31 \times t_{OSC} + n_2 \times t_{OSC}$$

where:

n_1 = 6 ; if f_{conv} = 8 MHz

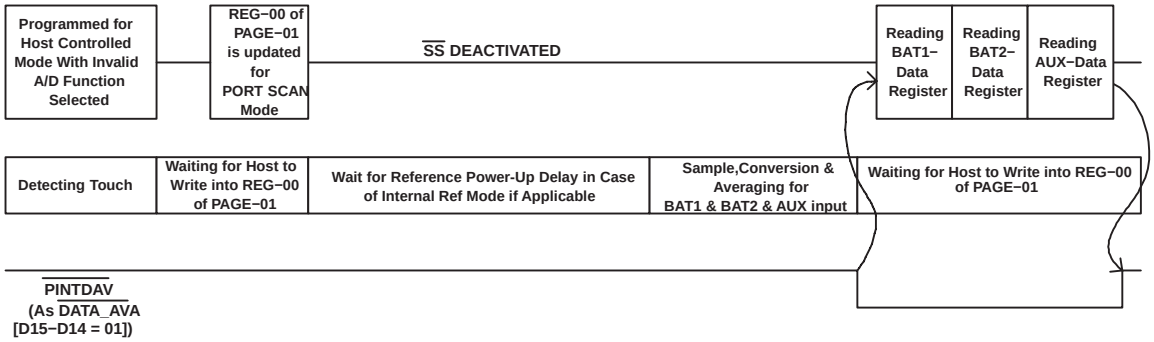
7 ; if $f_{conv} \neq$ 8 MHz

n_2 = 0 ; if external reference mode is selected

3 ; if t_{REF} = 0 µs or reference is programmed for power up all the times.

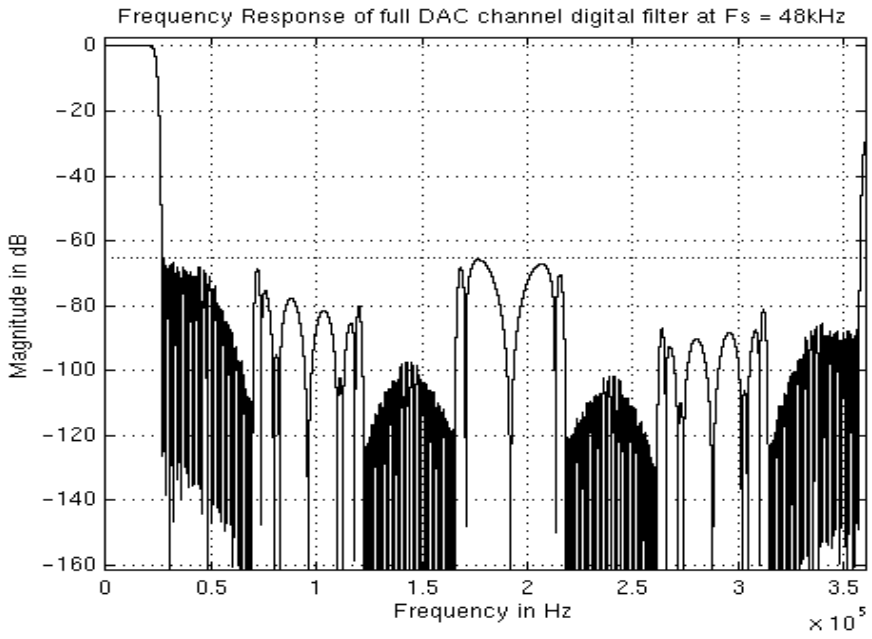
1 + t_{REF} /125 ns; if $t_{REF} \neq$ 0 µs and reference needs to power down between conversions.

t_{REF} is the reference power up delay time.

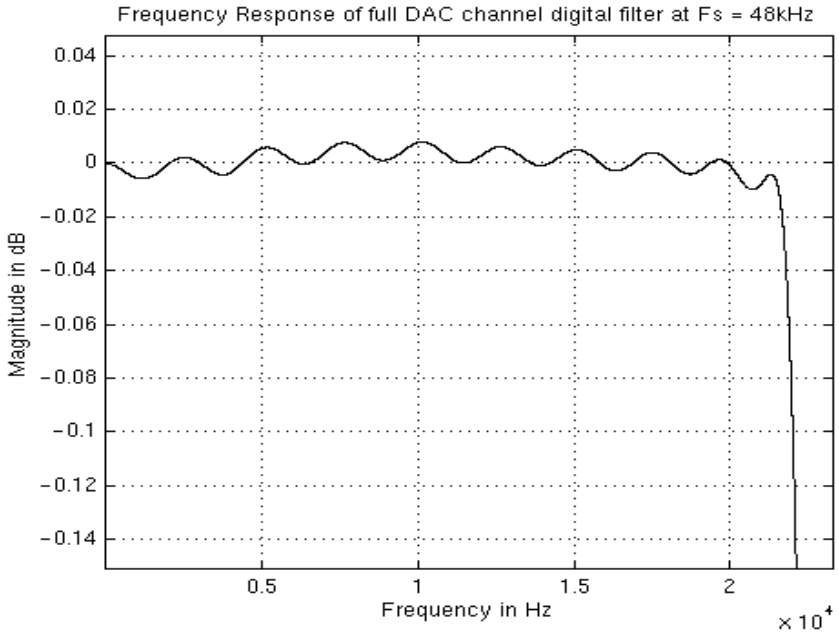


DAC CHANNEL DIGITAL FILTER

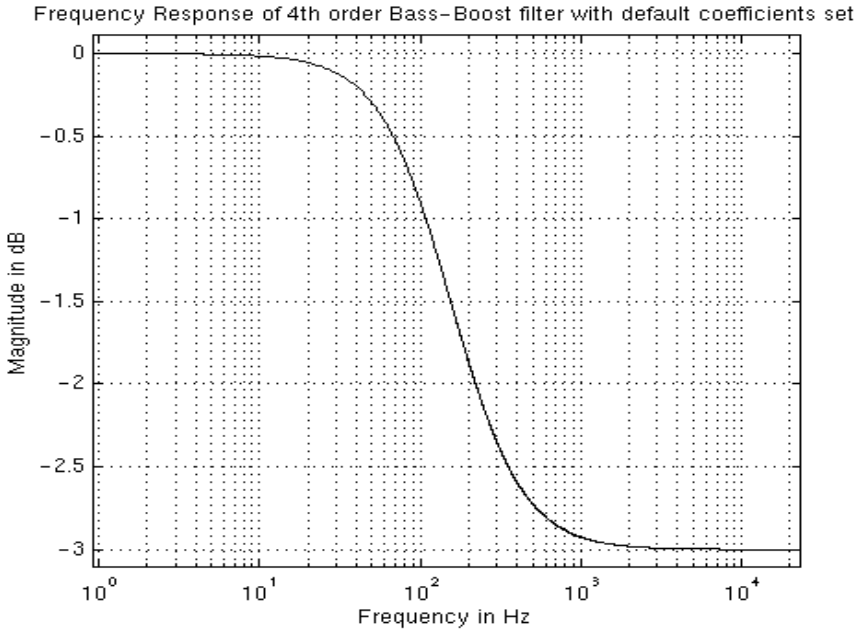
DAC Channel Digital Filter Frequency Response



DAC Channel Digital Filter Pass-Band Frequency Response

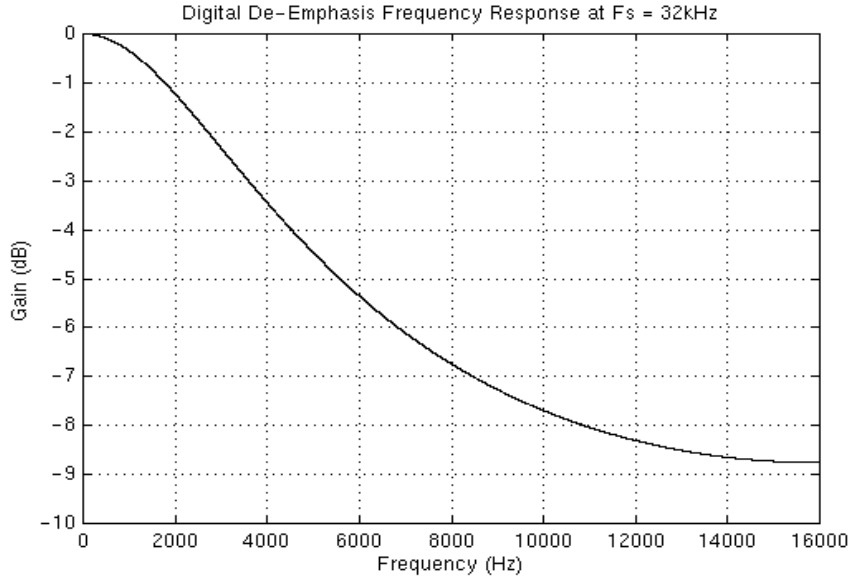


DEFAULT BASS-BOOST FREQUENCY RESPONSE AT 48 ksps

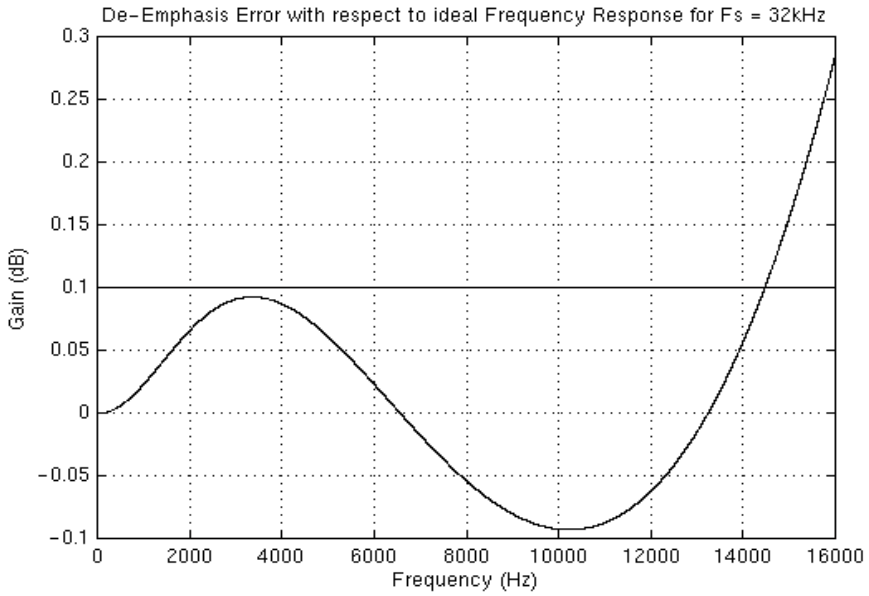


DE-EMPHASIS FILTER FREQUENCY RESPONSE

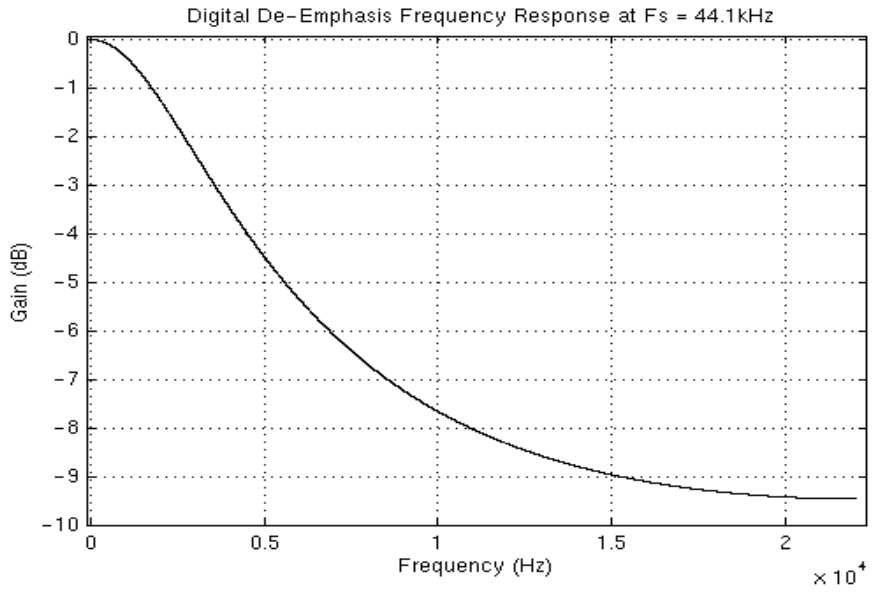
De-Emphasis Filter Response at 32 ksps



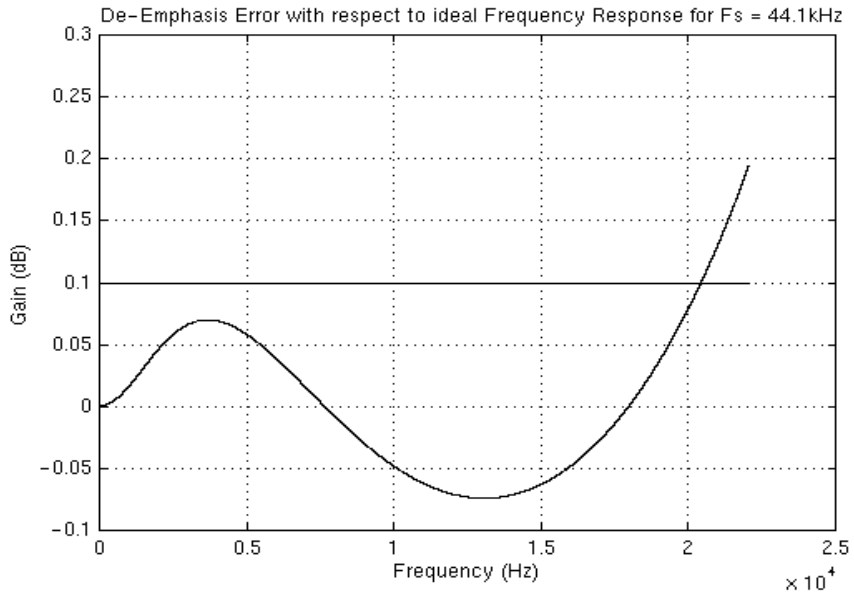
De-Emphasis Error at 32 ksps



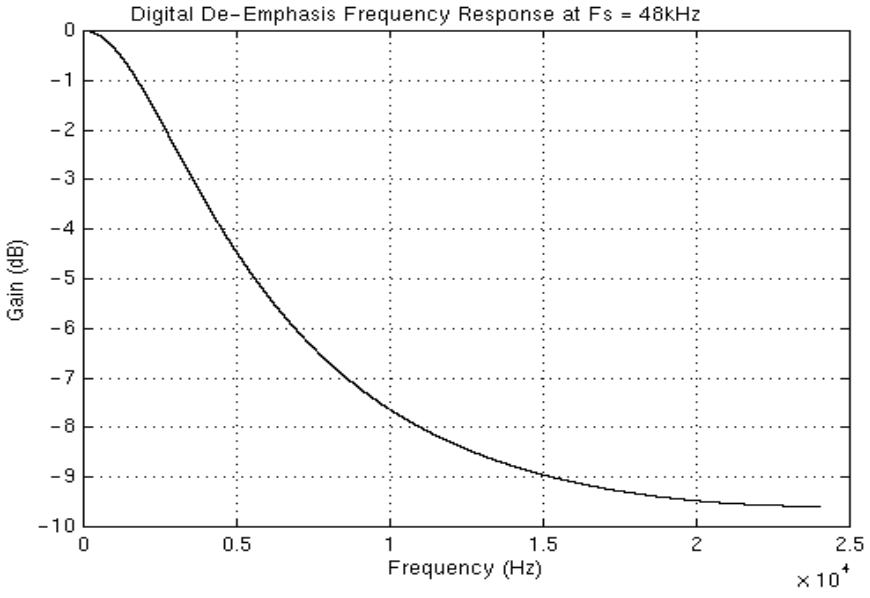
De-Emphasis Filter Frequency Response at 44.1 ksps



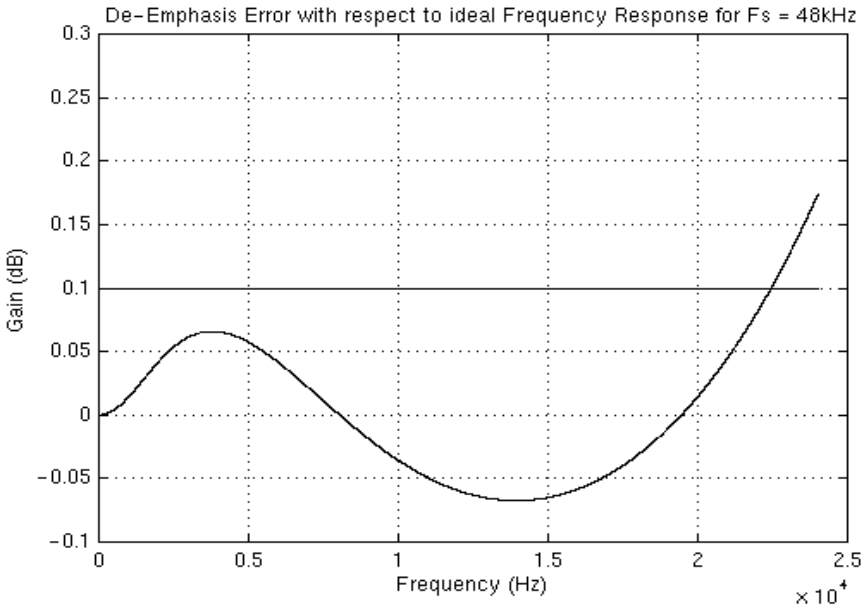
De-Emphasis Error at 44.1 ksps



De-Emphasis Frequency Response at 48 ksps



De-Emphasis Error at 48 ksps



PLL PROGRAMMING

The on-chip PLL in the TSC2102 can be used to generate sampling clocks from a wide range of MCLK's available in a system. The PLL works by generating oversampled clocks with respect to Fsref (44.1 kHz or 48 kHz). Frequency division generates all other internal clocks. The table below gives a sample programming for PLL registers for some standard MCLKs when PLL is required. Whenever the MCLK is of the form of N*128*Fsref (N=2,3…), PLL is not required.

Fsref = 44.1 kHz

MCLK (MHz)	P	J	D	ACHIEVED FSREF	% ERROR
2.8224	1	32	0	44100.00	0.0000
5.6448	1	16	0	44100.00	0.0000
12	1	7	5264	44100.00	0.0000
13	1	6	9474	44099.71	0.0007
16	1	5	6448	44100.00	0.0000
19.2	1	4	7040	44100.00	0.0000
19.68	1	4	5893	44100.30	−0.0007
48	4	7	5264	44100.00	0.0000

Fsref = 48 kHz

MCLK (MHz)	P	J	D	ACHIEVED FSREF	% ERROR
2.048	1	48	0	48000.00	0.0000
3.072	1	32	0	48000.00	0.0000
4.096	1	24	0	48000.00	0.0000
6.144	1	16	0	48000.00	0.0000
8.192	1	12	0	48000.00	0.0000
12	1	8	1920	48000.00	0.0000
13	1	7	5618	47999.71	0.0006
16	1	6	1440	48000.00	0.0000
19.2	1	5	1200	48000.00	0.0000
19.68	1	4	9951	47999.79	0.0004
48	4	8	1920	48000.00	0.0000

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TSC2102IDA	ACTIVE	TSSOP	DA	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TSC2102IDAG4	ACTIVE	TSSOP	DA	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TSC2102IDAR	ACTIVE	TSSOP	DA	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TSC2102IDARG4	ACTIVE	TSSOP	DA	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

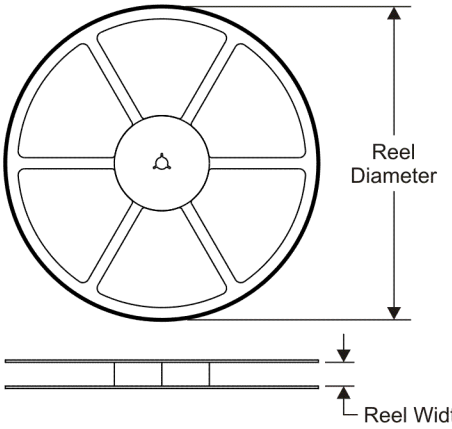
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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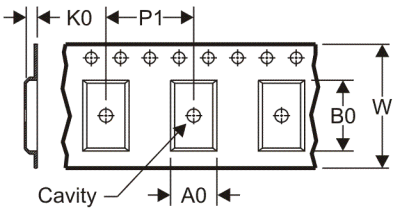
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

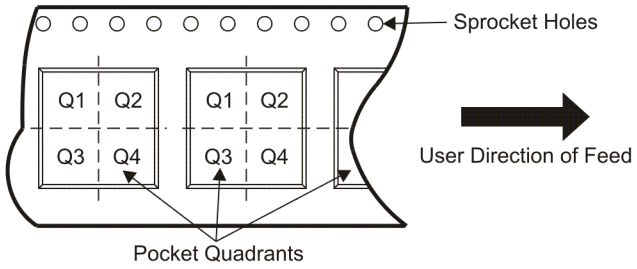


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

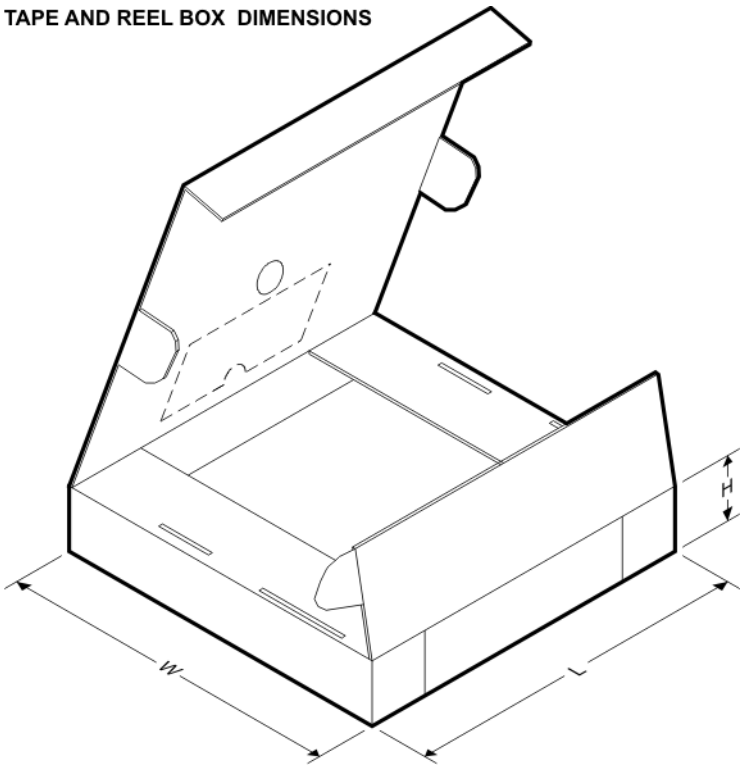
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2102IDAR	TSSOP	DA	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

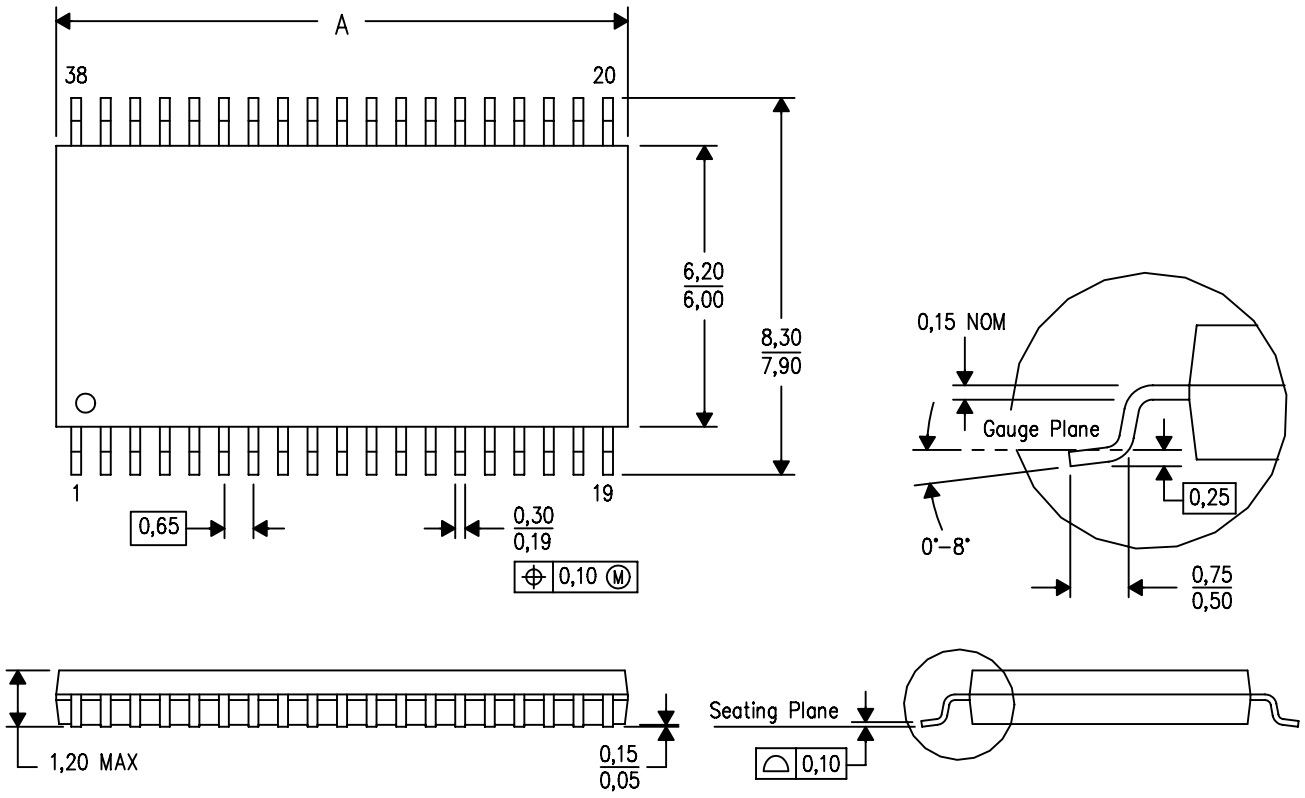


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2102IDAR	TSSOP	DA	32	2000	346.0	346.0	41.0

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN



DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
△D MO–153 Variation	DB–1	DC	DD–1

4040066/F 01/2009

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
△D Falls within JEDEC MO–153, except 30 pin body length.

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