Overview of TSB42AC3

FEATURES

- **50-MHz Host Interface Frequency Allows Direct Connection to Host With Bus Speeds up to 50 MHz**
- **Programmable 10K Byte Total for Asynchronous, Isochronous, and General Receive FIFO**
- **Separate ACK FIFO Register Decreases ACK-tracking Burden on the Host**
- **Additional Programmable Status Output to Pins, Including *cd* and *paccom* Bits to Aid External DMA**
- **Supports 1394 Transfer Rates of 100, 200, and 400 Mbit/s in Cable Environment**
- **Supports 1394 Transfer Rates of 50 and 100 Mbit/s in Backplane Environment**
- **Generic 32-Bit Host Bus Interface**
- **Completely Software Compatible With the TSB12LV01B**
- **IEEE 1149.1 JTAG Interface to Support Board Level Scan Testing**
- **Operates from a 3.3-V Power Supply**
- **Support Provisions of IEEE 1394–1995 (1394) Standard for High-Performance Serial Bus**
- **High Performance 100-Pin TQFP Package**

DESCRIPTION

The TSB42AC3 is a 1394-1995 general purpose link layer ideal for a wide-range of applications, including motion control, motor control, video, and process control. The TSB42AC3 provides a high-performance interface with the capability of transferring data between the 32-bit host controller and the 1394 PHY-link interface. The 1394 PHY-link interface provides the connection to the 1394 physical layer device (PHY) and is supported by the link-layer controller (LLC). The LLC provides the control for transmitting and receiving 1394 packet data between the FIFO and PHY-link interface at rates of 50 (backplane only), 100, 200, and 400 Mbit/s.

The TSB42AC3 has a 32-bit, 50-MHz host interface, which makes connection to most 32-bit hosts fairly easy. The LLC also provides the capability to receive status from the PHY and to access the PHY control and status registers by the application software.

An internal 10K-byte memory is provided that can be configured as multiple variable-size FIFOs and eliminates the need for external FIFOs. Separate FIFOs can be user configured to support asynchronous transmit, isochronous transmit, and general 1394 receive transfer operations. These functions are accomplished by appropriately sizing the asynchronous transmit FIFO (ATF) and isochronous transmit FIFO (ITF). Once the ATF and ITF size are programmed, the remaining memory space is assigned to the general receive FIFO (GRF).

The TSB42AC3 has a separate ACK FIFO register that is capable of retaining up to six acknowledges returned by external nodes in response to the asynchronous packets transmitted from the TSB42AC3. This allows host software to load multiple asynchronous packets in the ATF, then return at a later time to retrieve and process the acknowledges returned from the receiving destination nodes.

New status bits were added to the programmable output status pins. The start/end of packet bit (cd bit) and the packet complete (paccom bit) may now be brought out to a pin for control of external hardware.

NOTE:

This product is for high-volume applications only. For a complete datasheet or more information contact support@ti.com.

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