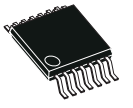
TS615

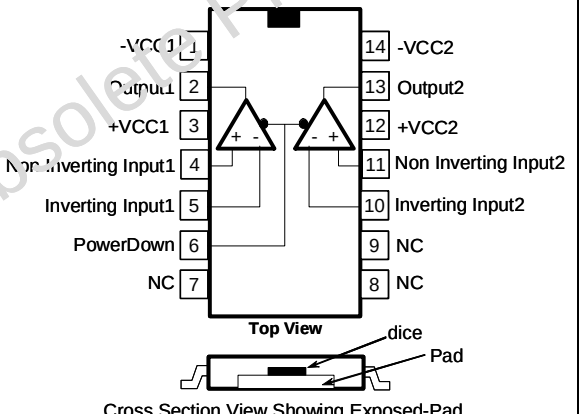
Dual Wide-Band Operational Amplifier with High Output Current

- **Low noise: 2.5 nV/√Hz**
- **High output current: 420 mA**
- **Very low harmonic and intermodulation distortion**
- **High slew rate: 410 V/µs**
- **-3 dB bandwidth: 40 MHz @ gain = 12 dB on 25 Ω single-ended load**
- **21.2 Vp-p differential output swing on 50 Ω load, 12 V power supply**
- **Current feedback structure**
- **5 V to 12 V power supply**
- **Specified for 20 Ω and 50 Ω differential load**
- **Power down function with short-circuited output to keep matching with the line in sleep mode**



P
TSSOP14 Exposed-Pad
(Plastic Micropackage)

Pin Connections (top view)



Cross Section View Showing Exposed-Pad.
This pad must be connected to a (-Vcc) copper area on the PCB.

Description

The TS615 is a dual operational amplifier featuring a high output current of 410 mA. This driver can be configured differentially for driving signals in telecommunication systems using multiple carriers. The TS615 is ideally suited for xDSL (High Speed Asymmetrical Digital Subscriber Line) applications. This circuit is capable of driving a 10 Ω or 25 Ω load on a range of power supplies: ±2.5 V, 5 V, ±6 V or +12 V. The TS615 is capable of reaching a -3 dB bandwidth of 40 MHz on a 25 Ω load with a 12 dB gain. This device is designed for high slew rates and demonstrates low harmonic distortion and intermodulation. The TS615 offers a power-down function in order to decrease power consumption. During sleep mode, the device short circuits its output in order to keep the impedance matched to the line. The TS615 is housed in TSSOP14 exposed-pad plastic package for a very low thermal resistance.

Applications

- **Line driver for xDSL**
- **Multiple video line driver**

Order Codes

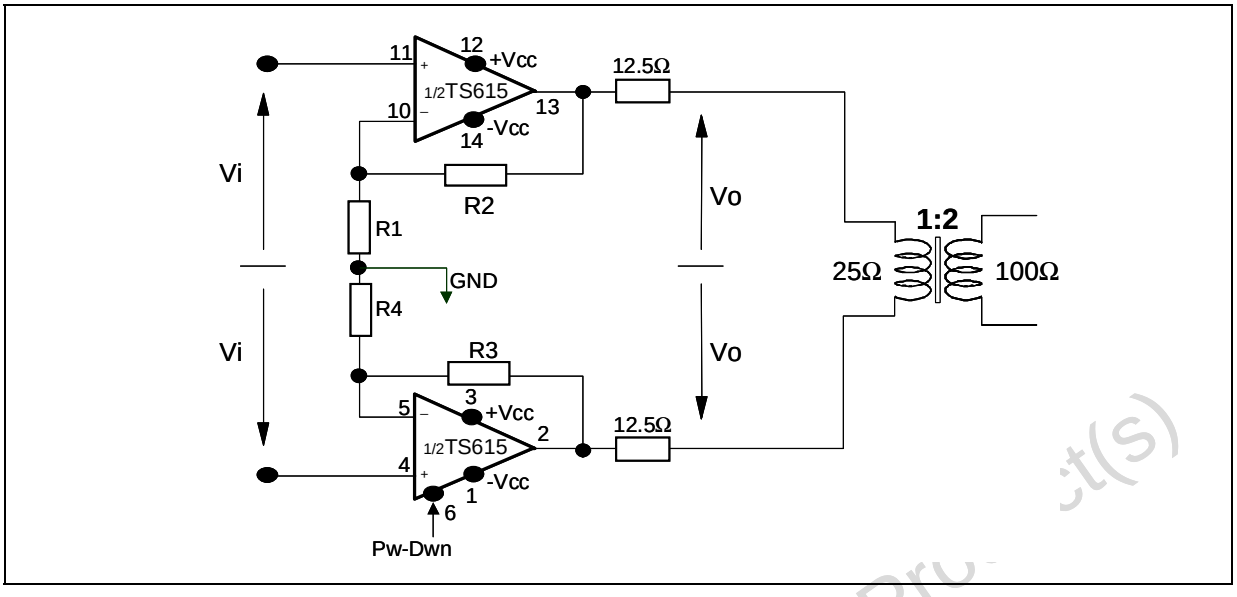
Part Number	Temperature Range	Package	Packaging	Marking
TS615IPWT	-40, +85°C	TSSOP (Thin Shrink Outline Package)	Tape & Reel	TS615

Obsolete Product(s) - Obsolete Product(s)

1 Typical Application

Figure 1 shows a schematic of a typical xDSL application using the TS615.

Figure 1. Differential line driver for xDSL applications



Obsolete Product(s) - Obsolete Product(s)

2 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage [1]	±7	V
Vid	Differential Input Voltage [2]	±2	V
V_{in}	Input Voltage Range [3]	±6	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{std}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thjc}	Thermal Resistance Junction to Case	4	°C/W
R_{thja}	Thermal Resistance Junction to Ambient Area	40	°C/W
$P_{max.}$	Maximum Power Dissipation (@25°C)	3.1	W
ESD except pins 4, 5, 10, 11	CDM: Charged Device Model HBM: Human Body Model MM: Machine Model	1.5 2 200	kV kV V
ESD only pins 4, 5, 10, 11	CDM: Charged Device Model HBM: Human Body Model MM: Machine Model	1 1 100	kV kV V
	Output Short Circuit	[4]	

1) All voltage values, except differential voltage are with respect to network terminal.

2) Differential voltage are non-inverting input terminal with respect to the inverting input terminal.

3) The magnitude of input and output voltage must never exceed V_{CC} +0.3V.

4) An output current limitation protects the circuit from transient currents. Short-circuits can cause excessive heating. Destructive dissipation can result from short circuit on amplifiers.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
VCC	Power Supply Voltage	±2.5 to ±6	V
Vicm	Common Mode Input Voltage	-VCC+1.5V to +VCC-1.5V	V

Obsolete Product(s) - Obsolete Product(s)

3 Electrical Characteristics

Table 3. V_{CC} = ±6V, R_{fb}=910Ω,T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input Offset Voltage	T_{amb}		1.25	3.5	mV
		$T_{min.} < T_{amb} < T_{max.}$		2.1		
ΔV_{io}	Differential Input Offset Voltage	T_{amb} = 25°C			2.5	mV
I_{ib+}	Positive Input Bias Current	T_{amb}		6	30	µA
		$T_{min.} < T_{amb} < T_{max.}$		7.8		
I_{ib-}	Negative Input Bias Current	T_{amb}		3	15	µA
		$T_{min.} < T_{amb} < T_{max.}$		3.2		
Z_{IN+}	Input(+) Impedance			82		kΩ
Z_{IN-}	Input(-) Impedance			54		Ω
C_{IN+}	Input(+) Capacitance			1		pF
CMR	Common Mode Rejection Ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	ΔV_{ic} = ±4.5V	58	63		dB
		$T_{min.} < T_{amb} < T_{max.}$		61		
SVR	Supply Voltage Rejection Ratio 20 log ($\Delta V_{cc}/\Delta V_{io}$)	ΔV_{cc}=±2.5V to ±6V	72	79		dB
		$T_{min.} < T_{amb} < T_{max.}$		78		
I_{CC}	Total Supply Current per Operator	No load		14	17	mA
Dynamic performance and output characteristics						
R_{OL}	Open Loop Transimpedance	V_{out} = 7Vp-p, R_L = 25Ω	5	21		MΩ
		$T_{min.} < T_{amb.} < T_{max.}$		8.9		
BW	-3dB Bandwidth	Small Signal V_{out}<20mVp A_V = 12dB, R_L = 25Ω	25	40		MHz
	Full Power Bandwidth	Large Signal V_{out}=3Vp A_V = 12dB, R_L = 25Ω		26		
	Gain Flatness @ 0.1dB	Small Signal V_{out}<20mVp A_V = 12dB, R_L = 25Ω		7		MHz
Tr	Rise Time	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω		10.6		ns
Tf	Fall Time	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω		12.2		ns
Ts	Settling Time	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω		50		ns
SR	Slew Rate	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω	330	410		V/µs
V_{OH}	High Level Output Voltage	R_L=25Ω Connected to GND	4.8	5.1		V
V_{OL}	Low Level Output Voltage	R_L=25Ω Connected to GND		-5.5	-5.2	V
I_{out}	Output Sink Current	V_{out} = -4Vp	-350	-530		mA
		$T_{min.} < T_{amb} < T_{max.}$		-440		
	Output Source Current	V_{out} = +4Vp	330	420		
		$T_{min.} < T_{amb} < T_{max.}$		365		

Obsolete Product(s) - Obsolete Product(s)

Table 3. V_{CC} = ±6V, R_{fb}=910Ω,T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Noise and distortion						
eN	Equivalent Input Noise Voltage	F = 100kHz		2.5		nV/√Hz
iNp	Equivalent Input Noise Current (+)	F = 100kHz		15		pA/√Hz
iNn	Equivalent Input Noise Current (-)	F = 100kHz		21		pA/√Hz
HD2	2nd Harmonic distortion (differential configuration)	V_{out} = 14Vp-p, A_V = 12dB F= 110kHz, R_L = 50Ω diff.		-87		dBc
HD3	3rd Harmonic distortion (differential configuration)	V_{out} = 14Vp-p, A_V = 12dB F= 110kHz, R_L = 50Ω diff.		-83		dBc
IM2	2nd Order Intermodulation Product (differential configuration)	F1= 100kHz, F2 = 110kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-76		dBc
		F1= 370kHz, F2 = 400kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-75		
IM3	3rd Order Intermodulation Product (differential configuration)	F1 = 100kHz, F2 = 110kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-88		dBc
		F1 = 370kHz, F2 = 400kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-87		

Obsolete Product(s) - Obsolete Product(s)

Table 4. V_{CC} = ±2.5V, R_{fb}=910Ω,T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input Offset Voltage	T_{amb}		0.5	2.5	mV
		$T_{min.} < T_{amb} < T_{max.}$		1.2		
ΔV_{io}	Differential Input Offset Voltage	T_{amb} = 25°C			2.5	mV
I_{ib+}	Positive Input Bias Current	T_{amb}		5	30	µA
		$T_{min.} < T_{amb} < T_{max.}$		8		
I_{ib-}	Negative Input Bias Current	T_{amb}		0.8	11	µA
		$T_{min.} < T_{amb} < T_{max.}$		1.24		
Z_{IN+}	Input(+) Impedance			71		kΩ
Z_{IN-}	Input(-) Impedance			62		Ω
C_{IN+}	Input(+) Capacitance			1.5		pF
CMR	Common Mode Rejection Ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	ΔV_{ic} = ±1V	55	60		dB
		$T_{min.} < T_{amb.} < T_{max.}$		58		
SVR	Supply Voltage Rejection Ratio 20 log ($\Delta V_{cc}/\Delta V_{io}$)	ΔV_{cc}=±2V to ±2.5V	63	77		dB
		$T_{min.} < T_{amb.} < T_{max.}$		76		
I_{CC}	Total Supply Current per Operator	No load		11.9	15	mA
Dynamic performance and output characteristics						
R_{OL}	Open Loop Transimpedance	V_{out} = 2Vp-p, R_L = 10Ω	2	5.4		MΩ
		$T_{min.} < T_{amb.} < T_{max.}$		2.1		
BW	-3dB Bandwidth	Small Signal V_{out}<20mVp A_V = 12dB, R_L = 10Ω	20	30		MHz
	Full Power Bandwidth	Large Signal V_{out}= 1.4Vp A_V = 12dB, R_L = 10Ω		20		
	Gain Flatness @ 0.1dB	Small Signal V_{out}<20mVp A_V = 12dB, R_L = 10Ω		5.7		MHz
Tr	Rise Time	V_{out} = 2.8Vp-p, A_V = 12dB R_L = 10Ω		11		ns
Tf	Fall Time	V_{out} = 2.8Vp-p, A_V = 12dB R_L = 10Ω		11.5		ns
Ts	Settling Time	V_{out} = 2.2Vp-p, A_V = 12dB R_L = 10Ω		39		ns
SR	Slew Rate	V_{out} = 2.2Vp-p, A_V = 12dB R_L = 10Ω	100	130		V/µs
V_{OH}	High Level Output Voltage	R_L=10Ω Connected to GND	1.5	1.75		V
V_{OL}	Low Level Output Voltage	R_L=10Ω Connected to GND		-2.05	-1.8	V
I_{out}	Output Sink Current	V_{out} = -1.25Vp	-350	-470		mA
		$T_{min.} < T_{amb} < T_{max.}$		-450		
	Output Source Current	V_{out} = +1.25Vp	200	270		
		$T_{min.} < T_{amb} < T_{max.}$		245		

Obsolete Product(s) - Obsolete Product(s)

Table 4. V_{CC} = ±2.5V, R_{fb}=910Ω,T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Noise and distortion						
eN	Equivalent Input Noise Voltage	F = 100kHz		2.5		nV/√Hz
iNp	Equivalent Input Noise Current (+)	F = 100kHz		15		pA/√Hz
iNn	Equivalent Input Noise Current (-)	F = 100kHz		21		pA/√Hz
HD2	2nd Harmonic distortion (differential configuration)	V_{out} = 6Vp-p, A_V = 12dB F= 110kHz, R_L = 20Ω diff.		-97		dBc
HD3	3rd Harmonic distortion (differential configuration)	V_{out} = 6Vp-p, A_V = 12dB F= 110kHz, R_L = 20Ω diff.		-98		dBc
IM2	2nd Order Intermodulation Product (differential configuration)	F1= 100kHz, F2 = 110kHz V_{out} = 6Vp-p, A_V = 12dB R_L = 20Ω diff.		-86		dBc
		F1= 370kHz, F2 = 400kHz V_{out} = 6Vp-p, A_V = 12dB R_L = 20Ω diff.		-88		
IM3	3rd Order Intermodulation Product (differential configuration)	F1 = 100kHz, F2 = 110kHz V_{out} = 6Vp-p, A_V = 12dB R_L = 20Ω diff.		-90		dBc
		F1 = 370kHz, F2 = 400kHz V_{out} = 6Vp-p, A_V = 12dB R_L = 20Ω diff.		-85		

Power-down mode features

The power-down command is a MOS input featuring a high input impedance.

Table 5. V_{CC} = ±2.5V, 5V, ±6V or 12V, T_{amb} = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{pdw}	Pin (6) Threshold Voltage for Power Down Mode				V
	Low Level	$-V_{CC}$		$-V_{CC}$+0.8	
	High Level	$-V_{CC}$+2		$+V_{CC}$	
Icc_{pdw}	Power Down Mode Total Current Consumption@ V_{CC}=5V		69	80	µA
	Power Down Mode Total Current Consumption@ V_{CC}=12V		148	180	µA
R_{pdw}	Power Down Mode Output Impedance @ V_{CC}=5V		19	23	Ω
	Power Down Mode Output Impedance @ V_{CC}=12V		15.3	19	Ω
C_{pdw}	Power Down Mode Output Capacitance		63		pF

Power down control	Circuit status
V_{pdw}=Low Level	Active
V_{pdw}=High Level	Standby

Obsolete Product(s) - Obsolete Product(s)

Figure 2. Load configuration
Load: R_L=25Ω, V_{CC}=±6V

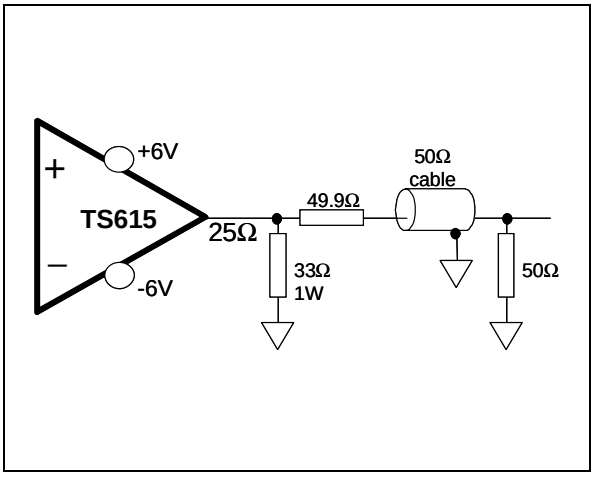


Figure 3. Closed loop gain vs. frequency
A_V=+1

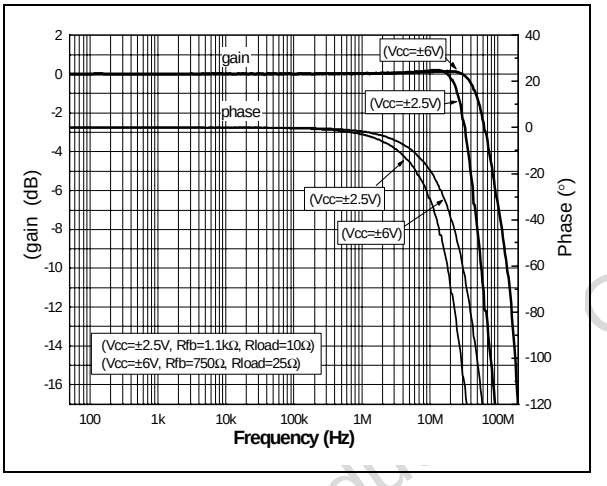


Figure 4. Closed loop gain vs. frequency
A_V=+2

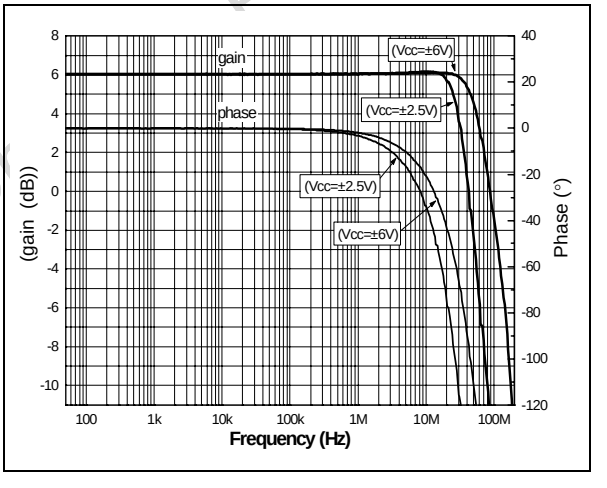


Figure 5. Load configuration
Load: R_L=10Ω, V_{CC}=±2.5V

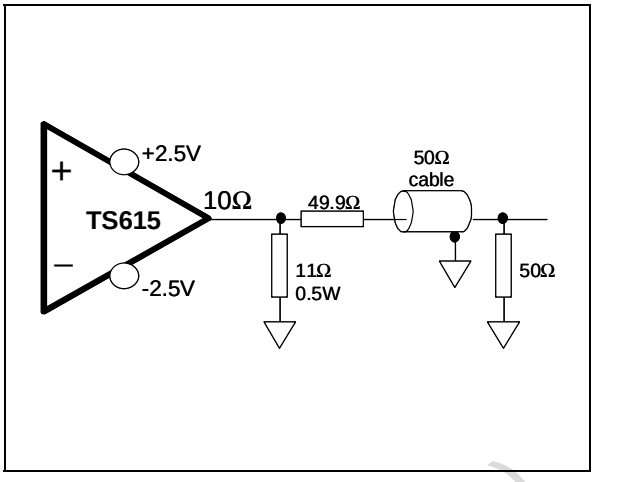


Figure 6. Closed loop gain vs. frequency
A_V=-1

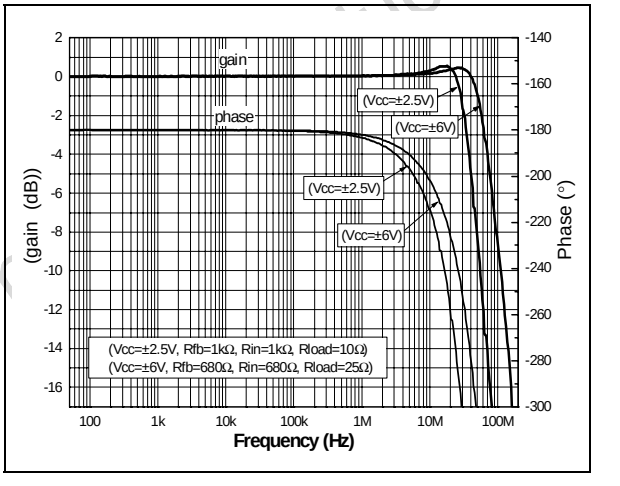


Figure 7. Closed loop gain vs. frequency
A_V=-2

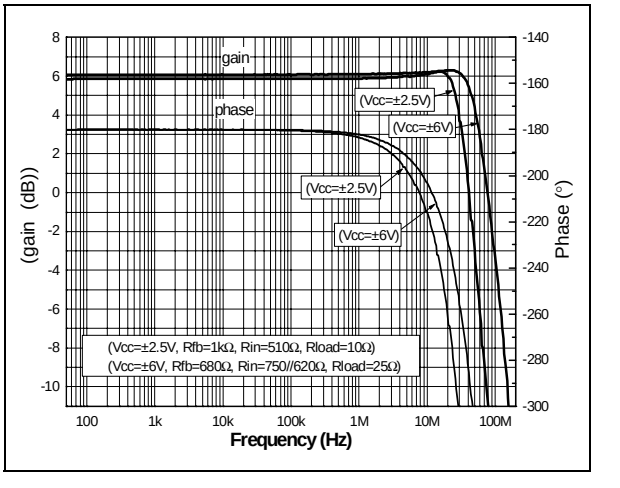


Figure 8. Closed loop gain vs. frequency A_V=+4

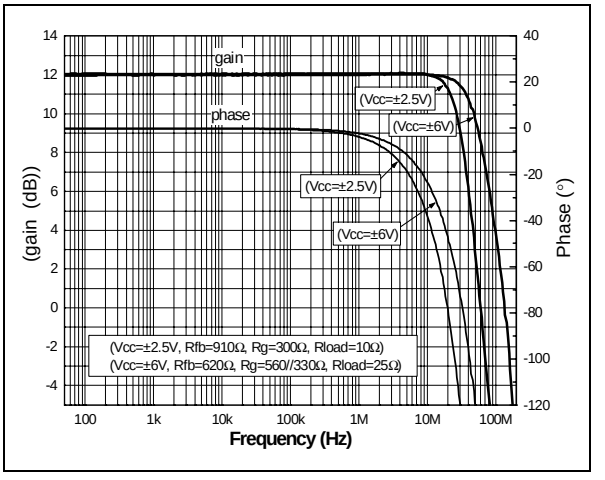


Figure 9. Closed loop gain vs. frequency A_V=+8

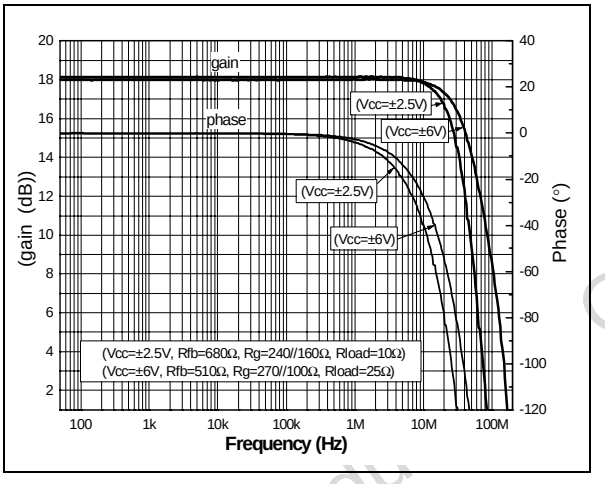


Figure 10. Bandwidth vs. temperature: A_V=+4, R_{fb}=910Ω

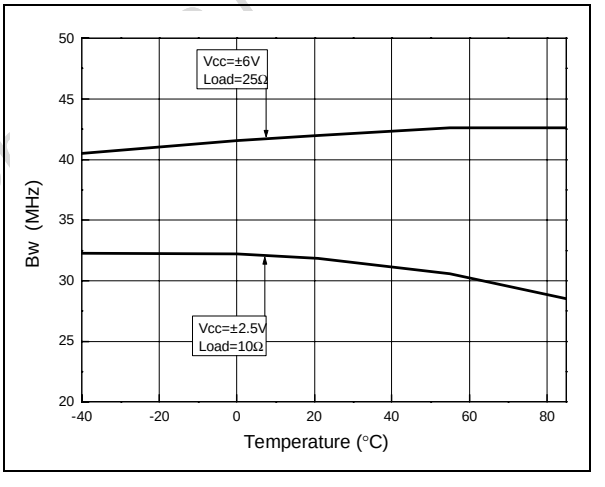


Figure 11. Closed loop gain vs. frequency A_V=-4

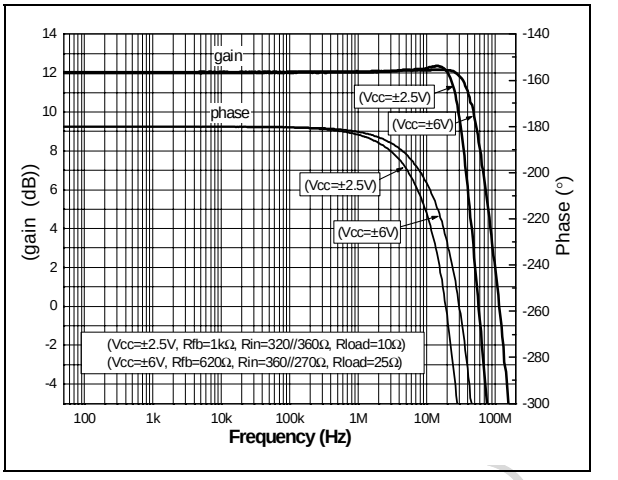


Figure 12. Closed loop gain vs. frequency A_V=-8

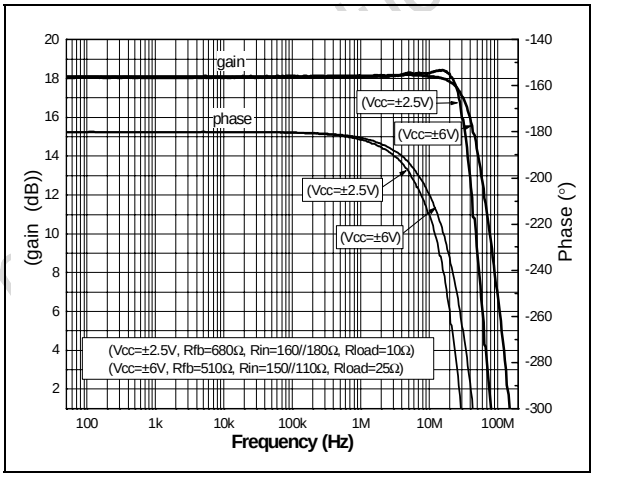


Figure 13. Positive slew rate: A_V=+4, R_{fb}=620Ω, V_{CC}=±6V, R_L=25Ω

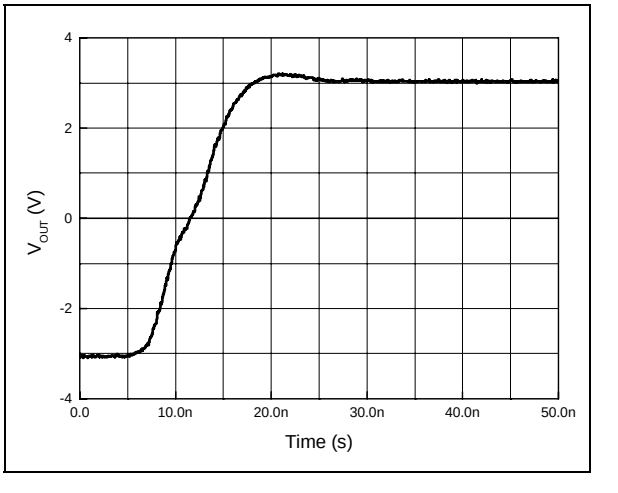


Figure 14. Positive slew rate: A_V=+4, R_{fb}=910Ω, V_{CC}=±2.5V, R_L=10Ω

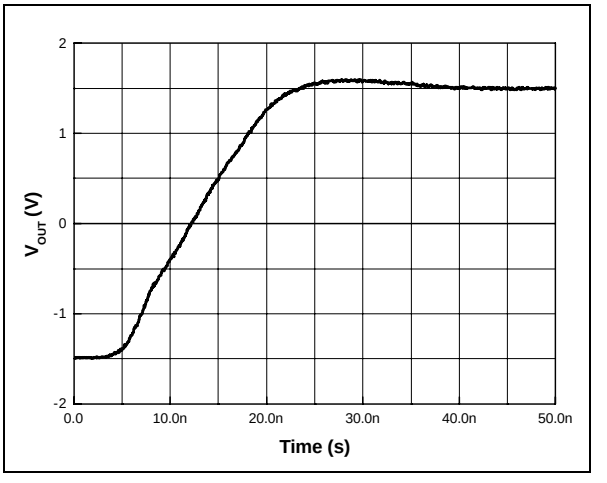


Figure 15. Negative slew rate: A_V=+4, R_{fb}=620Ω, V_{CC}=±6V, R_L=25Ω

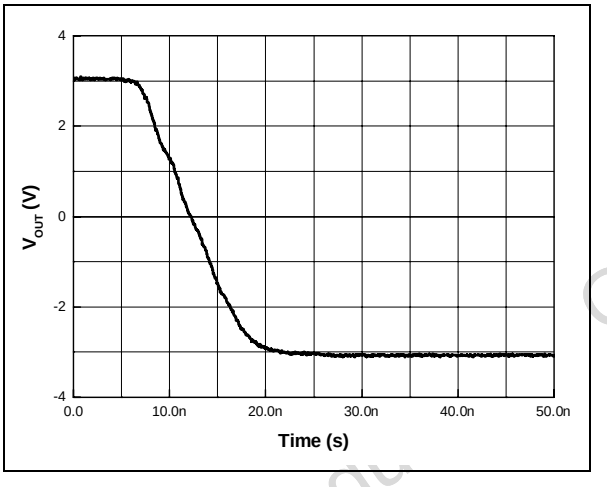


Figure 16. Negative slew rate: A_V=+4, R_{fb}=910Ω, V_{CC}=±2.5V, R_L=10Ω

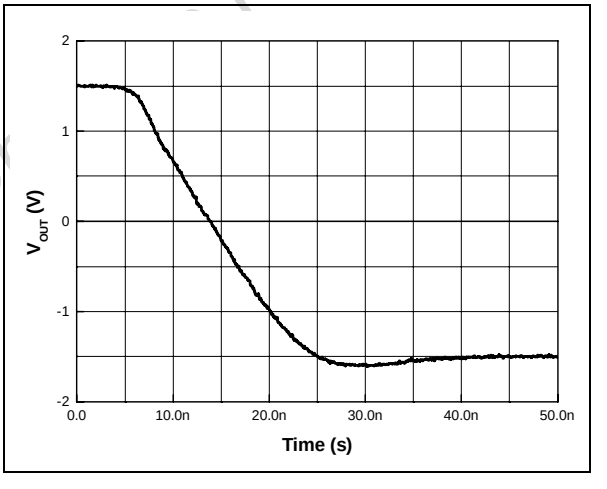


Figure 17. Positive slew rate: A_V= - 4, R_{fb}=620Ω, V_{CC}=±6V, R_L=25Ω

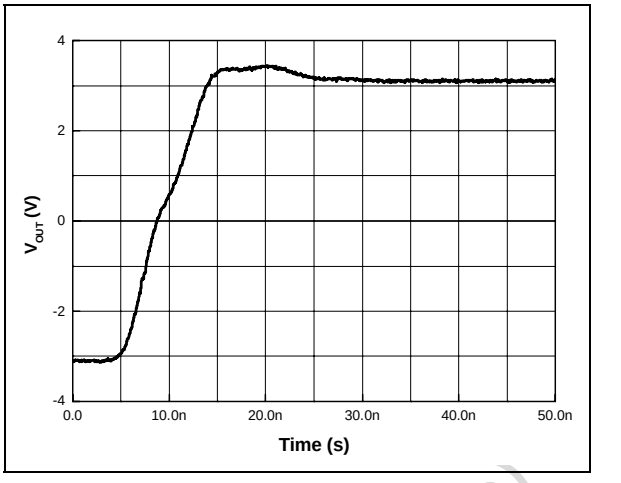


Figure 18. Positive slew rate: A_V= - 4, R_{fb}=910Ω, V_{CC}=±2.5V, R_L=10Ω

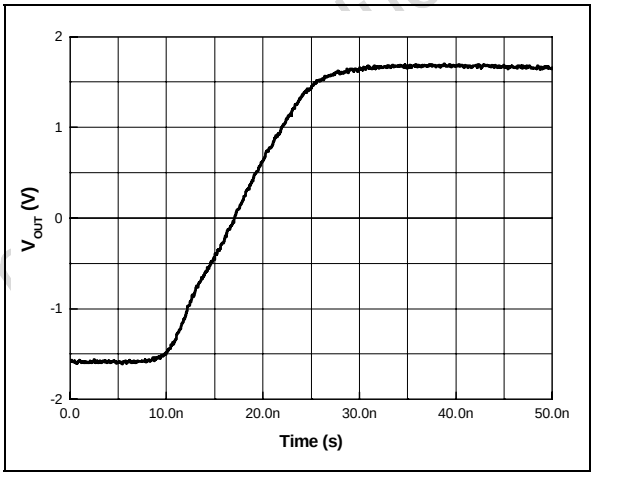


Figure 19. Negative slew rate: A_V= - 4, R_{fb}=620Ω, V_{CC}=±6V, R_L=25Ω

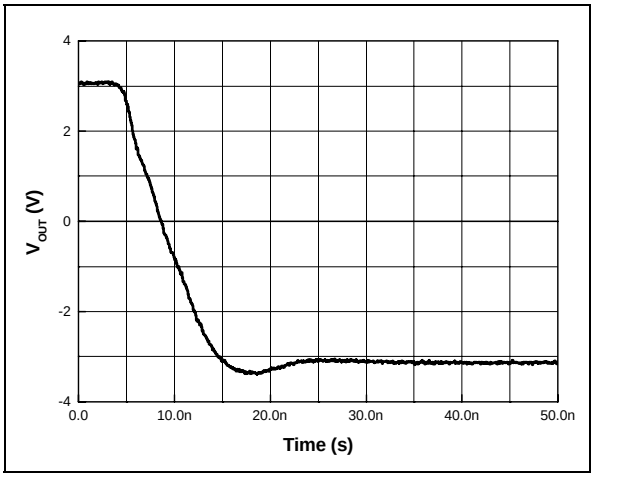


Figure 20. Negative slew rate: A_V= - 4, R_{fb}=910Ω, V_{CC}=±2.5V, R_L=10Ω

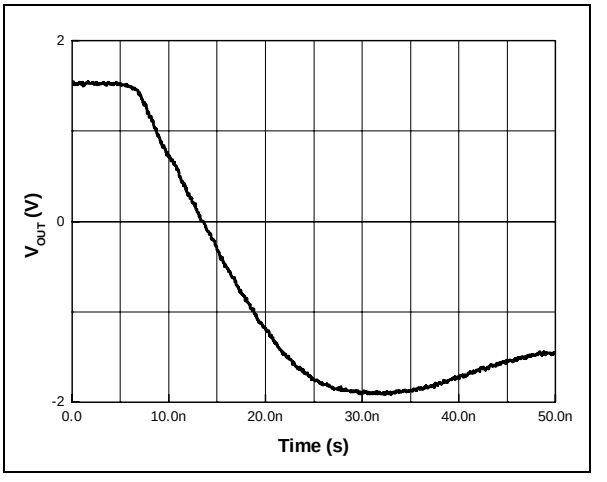


Figure 21. Slew rate vs. temperature: A_V=+4, R_{fb}=910Ω, V_{CC}=±2.5V, R_L=10Ω

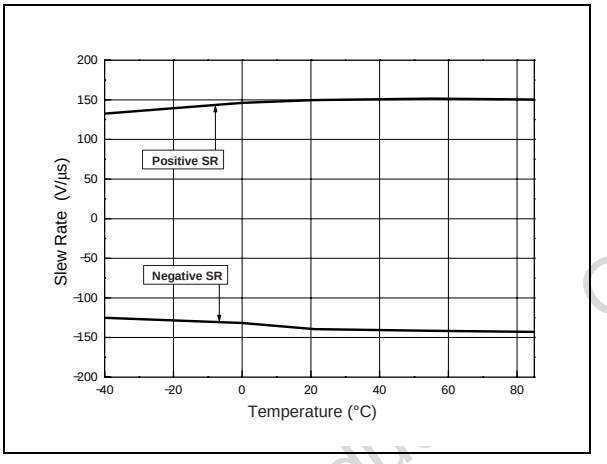


Figure 22. Slew rate vs. temperature: A_V=+4, R_{fb}=910Ω, V_{CC}=±6V, R_L=25Ω

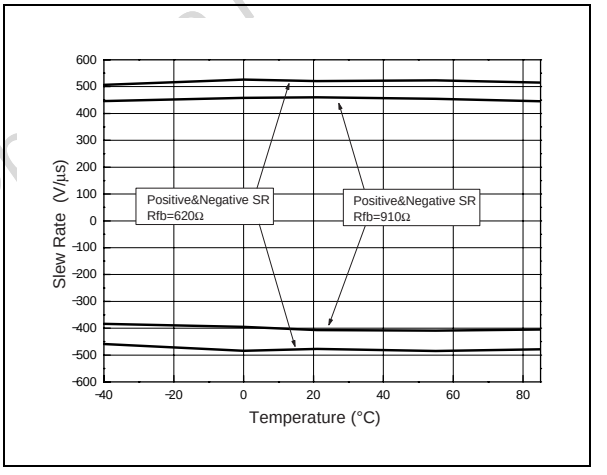


Figure 23. Input voltage noise level: A_V=+92, R_{fb}=910Ω, Input+ connected to Gnd via 10Ω

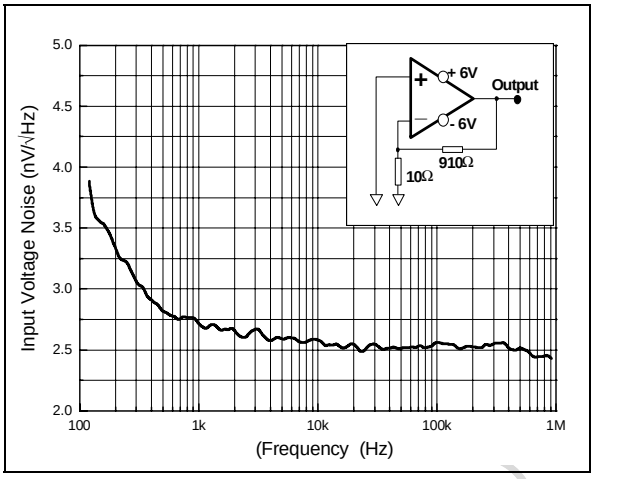


Figure 24. Transimpedance vs. temperature, open loop

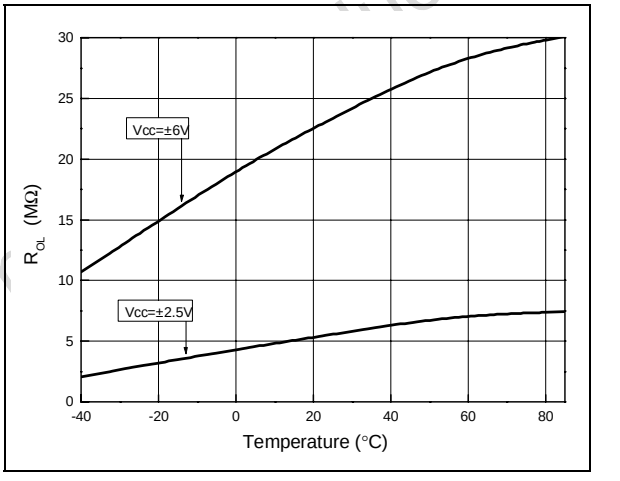


Figure 25. Icc vs. power supply Open loop, no load

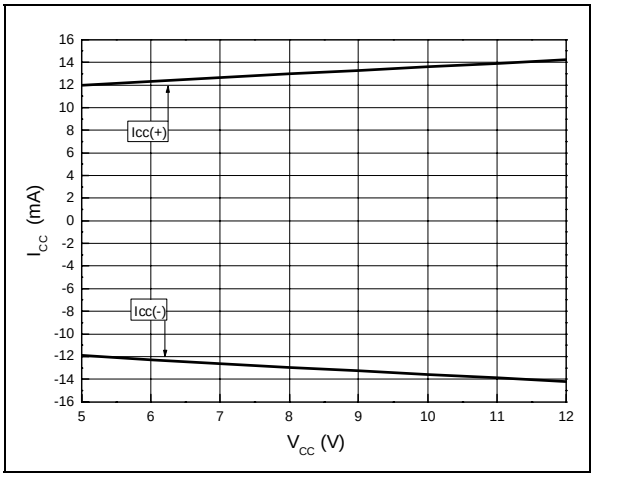


Figure 26. Iib vs. power supply
Open loop, no load

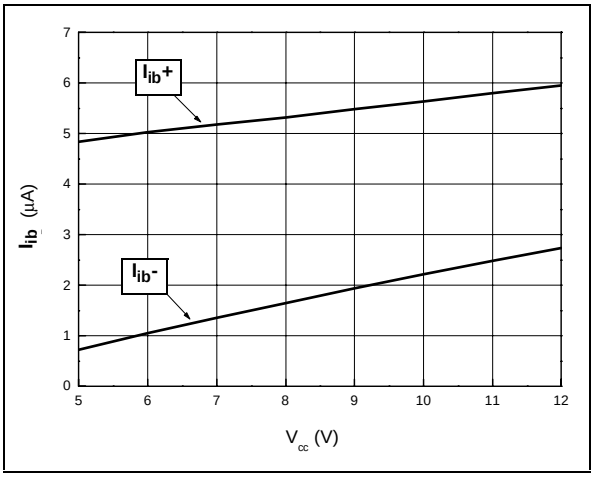


Figure 27. Iib(-) vs. temperature
Open loop, no load

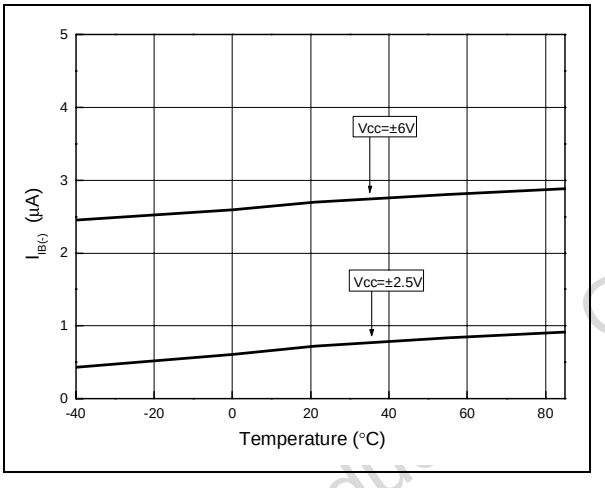


Figure 28. Icc vs. temperature
Open loop, no load

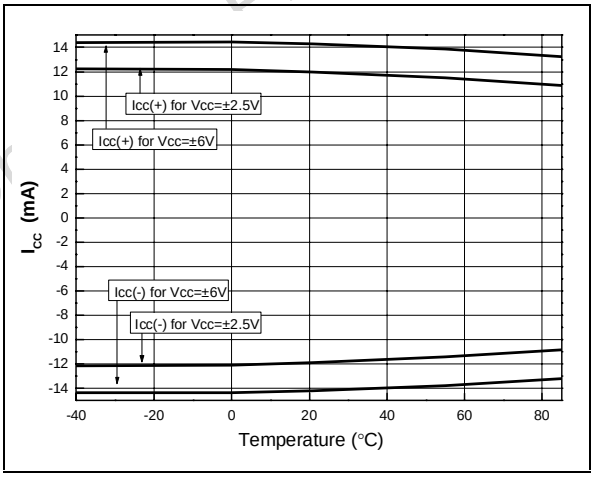


Figure 29. Iib(+) vs. temperature
Open loop, no load

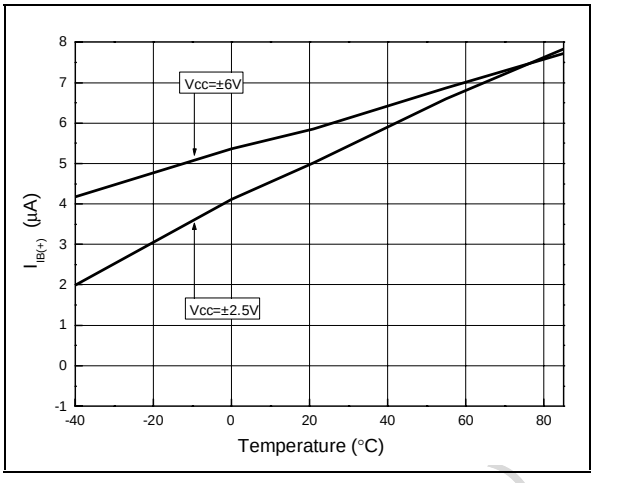


Figure 30. Voh & Vol vs. power supply
Open loop, R_L=25Ω

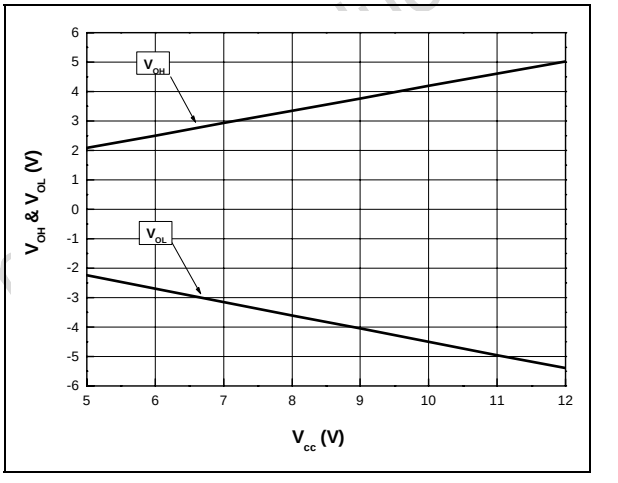
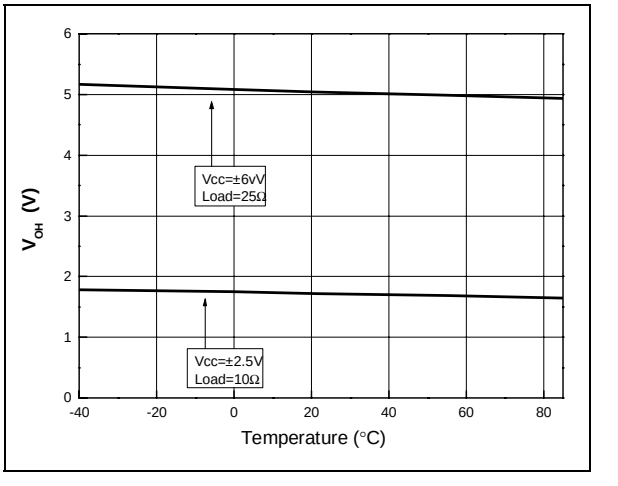


Figure 31. Voh vs. temperature
Open loop



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Figure 32. Vol vs. temperature
Open loop

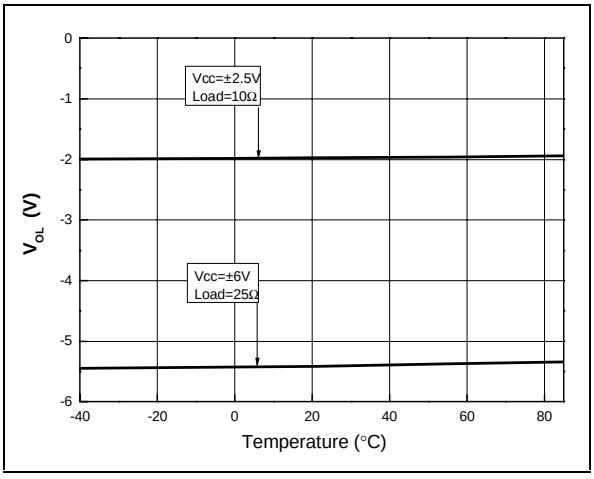


Figure 33. Differential Vio vs. temperature
Open loop, no load

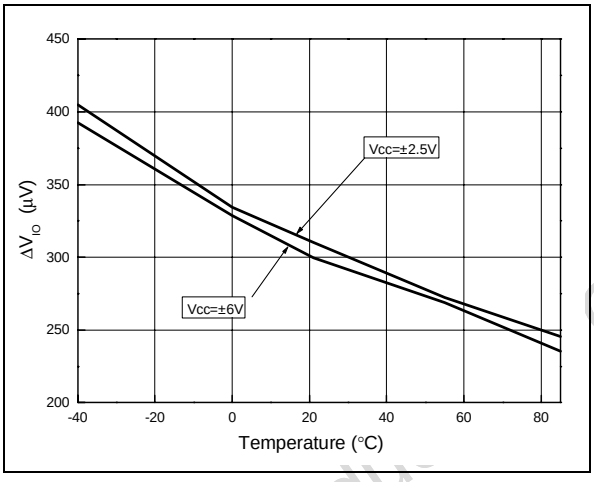


Figure 34. Vio vs. temperature
Open loop, no load

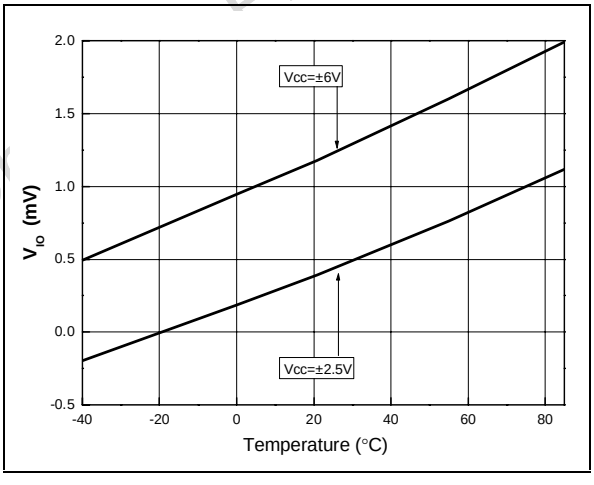


Figure 35. CMR vs. temperature
Open loop, no load

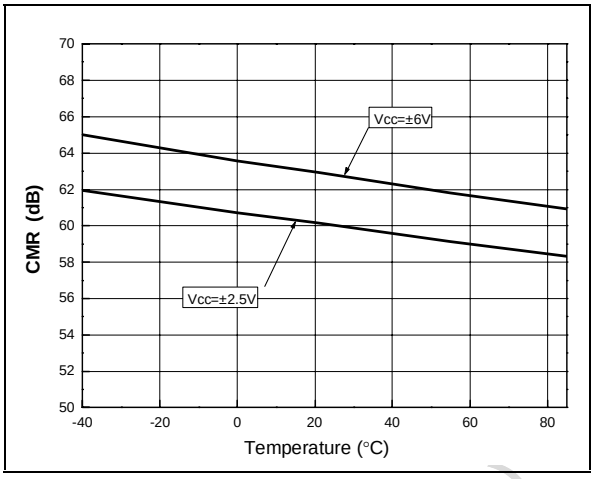


Figure 36. SVR vs. temperature
Open loop, no load

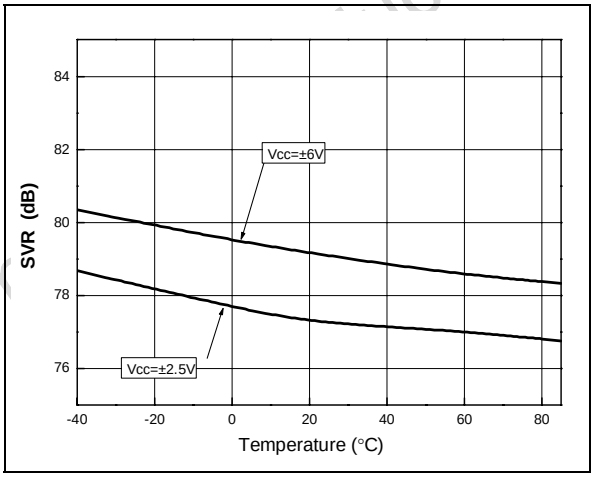


Figure 37. Iout vs. temperature
Open loop, V_{CC}=±6V, R_L=10Ω

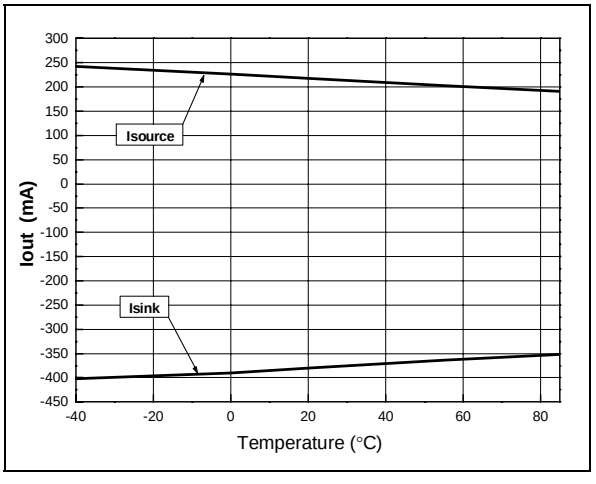


Figure 38. Iout vs. temperature
Open loop, V_{CC}=±2.5V, R_L=25Ω

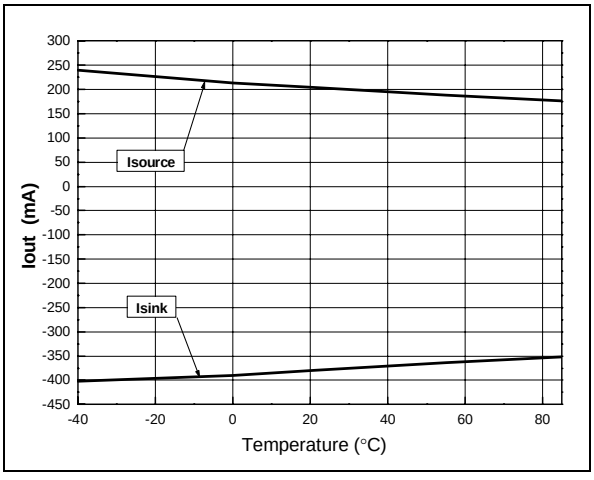


Figure 39. Maximum output amplitude vs. load: A_V=+4, R_{fb}=620Ω, V_{CC}=±6V

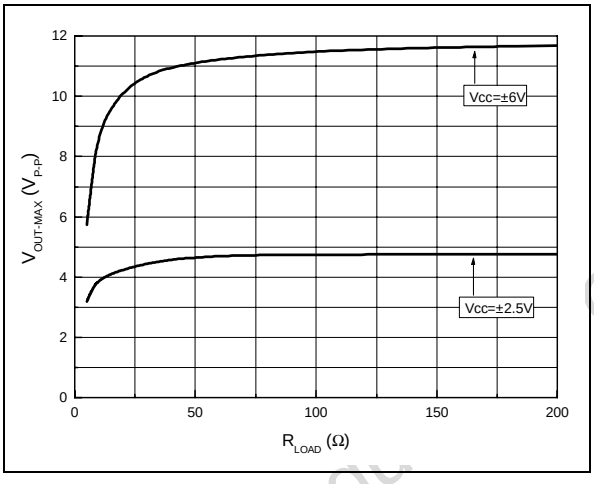


Figure 40. Isink vs. output amplitude
V_{CC}=±2.5V, open loop, no load

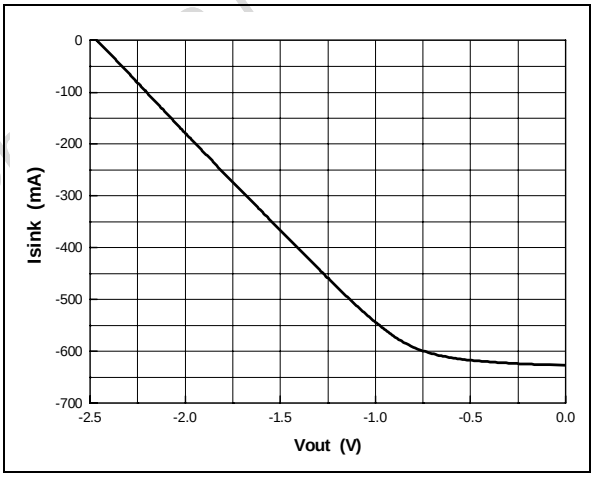


Figure 41. Isource vs. output amplitude
V_{CC}=±2.5V, open loop, no load

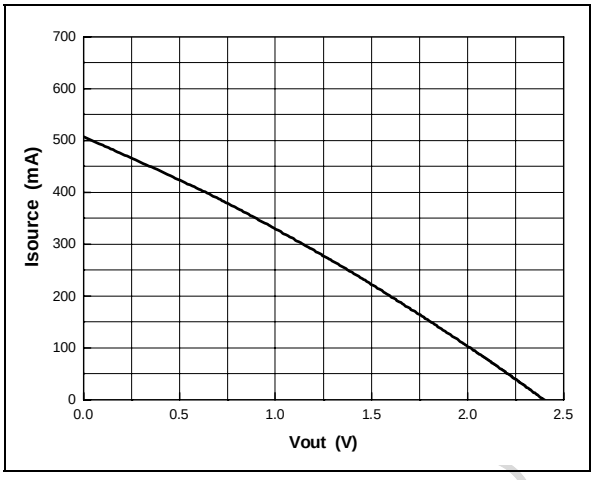


Figure 42. Isink vs. output amplitude
V_{CC}=±6V, open loop, no load

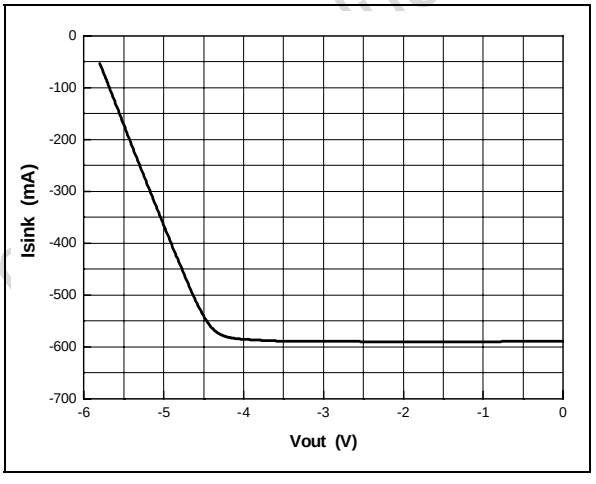


Figure 43. Isource vs. output amplitude
V_{CC}=±6V, open loop, no load

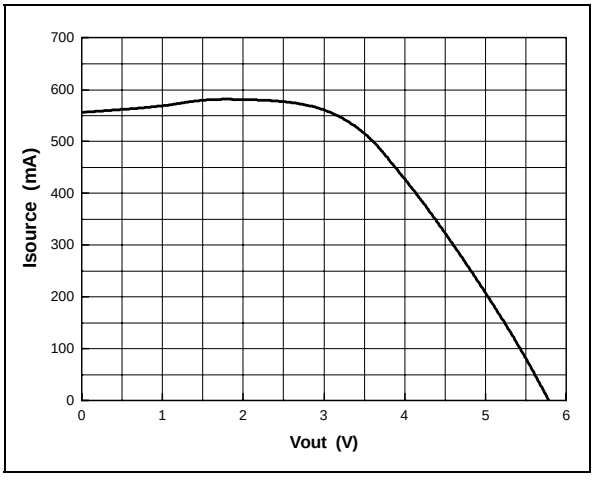
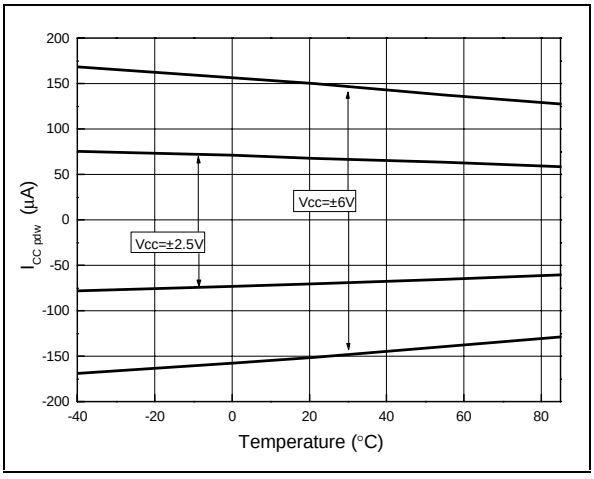


Figure 44. Icc (power down) vs. temperature no load, open loop

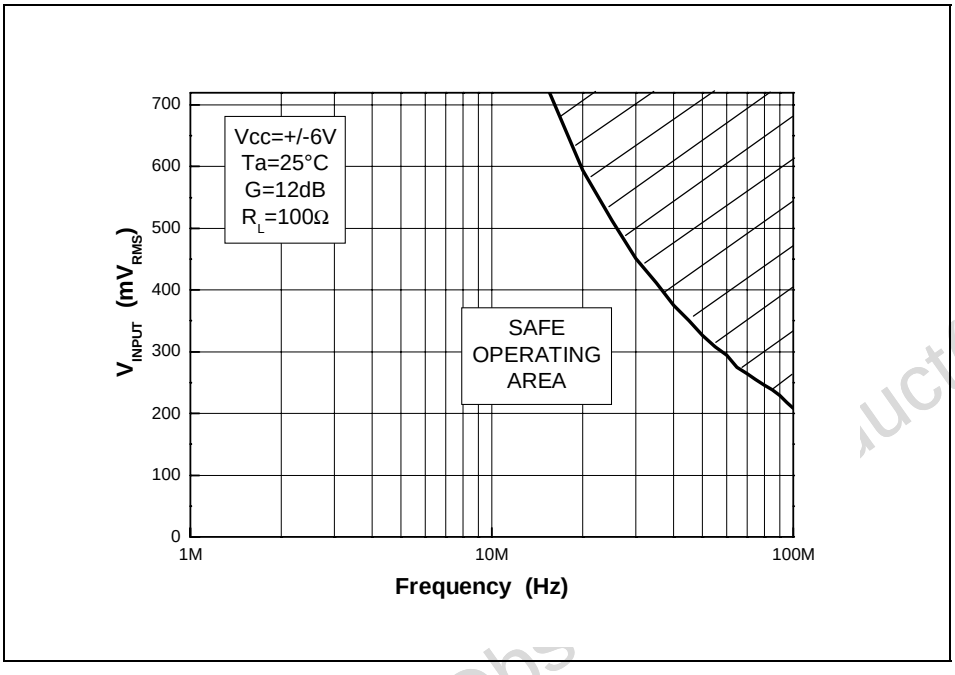


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4 Safe Operating Area

Figure 45 shows the safe operating zone for the TS615. The curve shows the input level vs. the input frequency—a characteristic curve which must be considered in order to ensure a good application design. In the dash-lined zone, the consumption increases, and this increased consumption could do damage to the chip if the temperature increases

Figure 45. Safe operating area



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5 Intermodulation Distortion Product

The non-ideal output of the amplifier can be described by the following series, due to a non-linearity in the input-output amplitude transfer:

$$V_{out} = C_o + C_1 V_{in} + C_2 V_{in}^{\ 2} \ldots + C_n V_{in}^{\ n}$$

where the single-tone input is V_{in}=Asinωt, and C_0 is the DC component, $C_1(V_{in})$ is the fundamental, C_n is the amplitude of the harmonics of the output signal V_{out}.

A one-frequency (one-tone) input signal contributes to a harmonic distortion. A two-tone input signal contributes to a harmonic distortion and an intermodulation product.

This intermodulation product, or rather, the study of the intermodulation distortion of a two-tone input signal is the first step in characterizing the amplifiers capability for driving multi-tone signals.

The two-tone input is equal to:

$$V_{in} = A\sin\omega_1 t + B\sin\omega_2 t$$

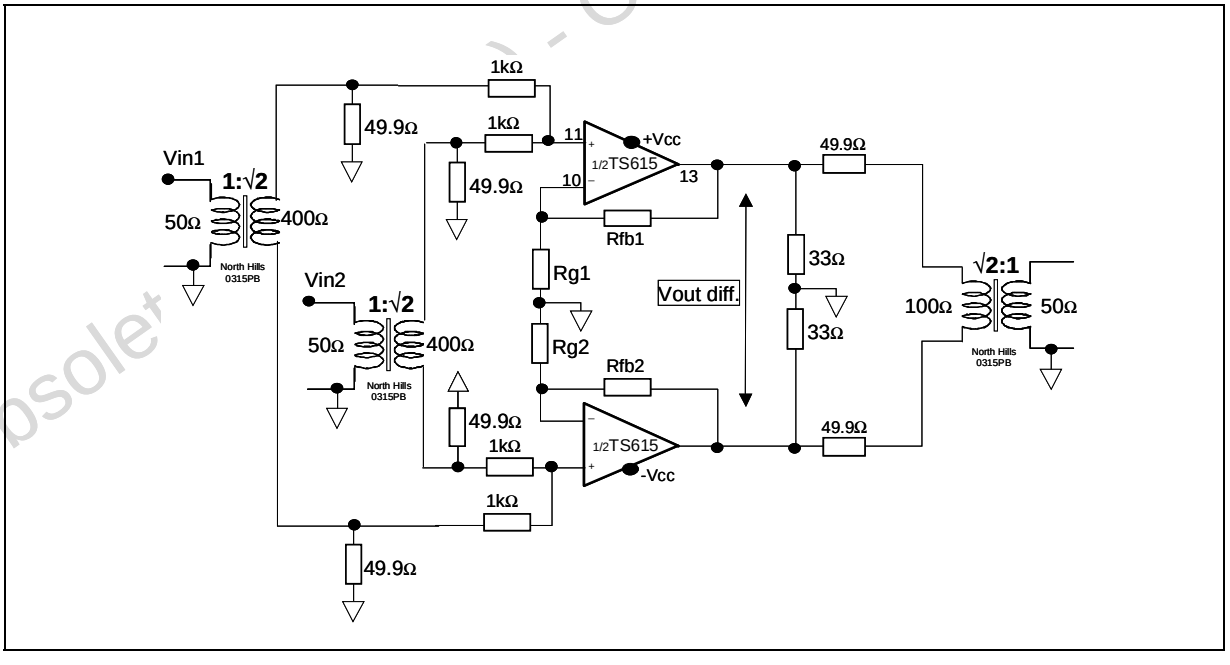
giving:

$$V_{out} = C_0 + C_1(A\sin\omega_1 t + B\sin\omega_2 t) + C_2(A\sin\omega_1 t + B\sin\omega_2 t)^2 \ldots + C_n(A\sin\omega_1 t + B\sin\omega_2 t)^n$$

In this expression, we can extract distortion terms and intermodulations terms from a single sine wave: second-order intermodulation terms IM2 by the frequencies $(\omega_1-\omega_2)$ and $(\omega_1+\omega_2)$ with an amplitude of $C2A^2$ and third-order intermodulation terms IM3 by the frequencies $(2\omega_1-\omega_2)$, $(2\omega_1+\omega_2)$, $(-\omega_1+2\omega_2)$ and $(\omega_1+2\omega_2)$ with an amplitude of $(3/4)C3A^3$.

We can measure the intermodulation product of the driver by using the driver as a mixer via a summing amplifier configuration. In doing this, the non-linearity problem of an external mixing device is avoided.

Figure 46. Non-inverting summing amplifier



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The following graphs show the IM2 and the IM3 of the amplifier in different configurations. The two-tone input signal is created by a Marconi 2026 multisource generator. Each tone has the same amplitude. The measurement was carried out using an HP3585A spectrum analyzer.

Figure 47. Intermodulation vs. output amplitude: 370 kHz & 400 kHz, A_V = +1.5, R_{fb} = 1 kΩ, R_L = 14 Ω diff., V_{CC} = ±2.5 V

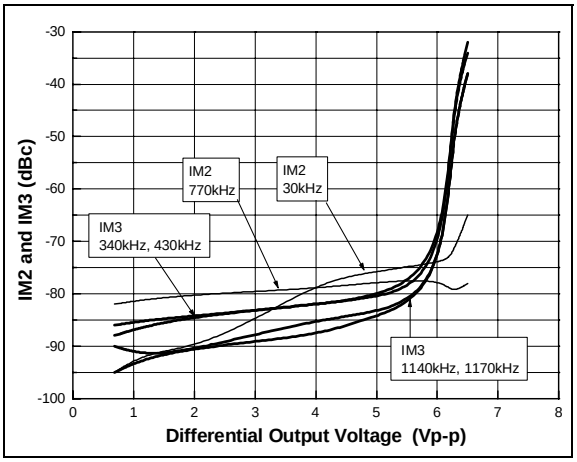


Figure 48. Intermodulation vs. output amplitude: 370 kHz & 400 kHz, A_V = +1.5, R_{fb} = 1 kΩ, R_L = 28 Ω diff., V_{CC} = ±2.5 V

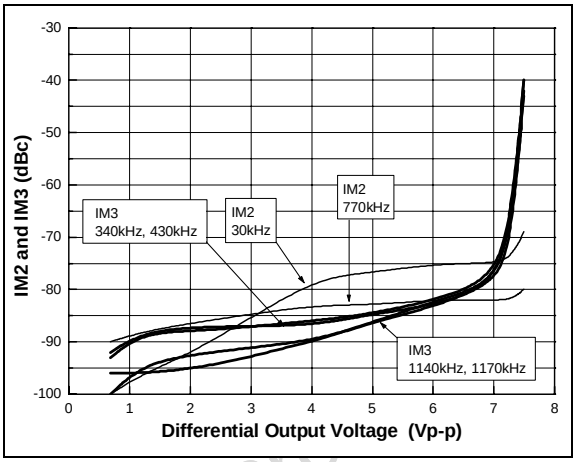


Figure 49. Intermodulation vs. gain: 370kHz & 400kHz, R_L=20Ω diff., Vout=6Vpp, V_{CC}=±2.5V

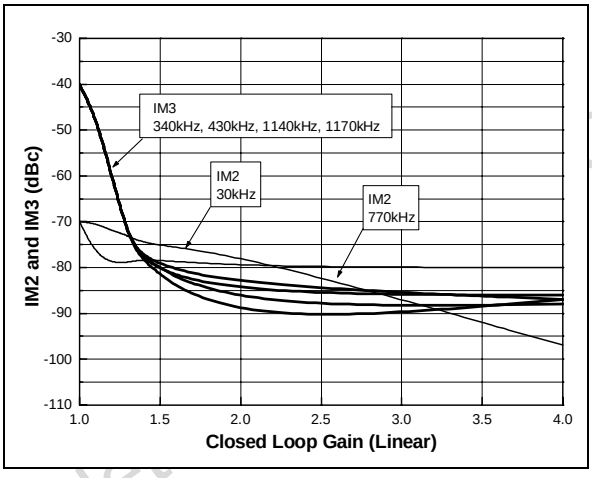
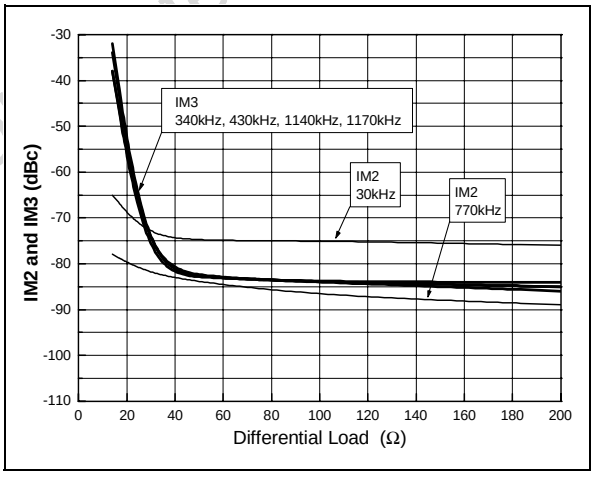


Figure 50. Intermodulation vs. Load: 370kHz & 400kHz, A_V=+1.5, R_{fb}=1kΩ, Vout=6.5Vpp, V_{CC}=±2.5V



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Figure 51. Intermodulation vs. Output Amplitude: 100kHz & 110kHz, A_V=+4, R_{fb}=620Ω, R_L=200Ω diff., V_{CC}=±6V

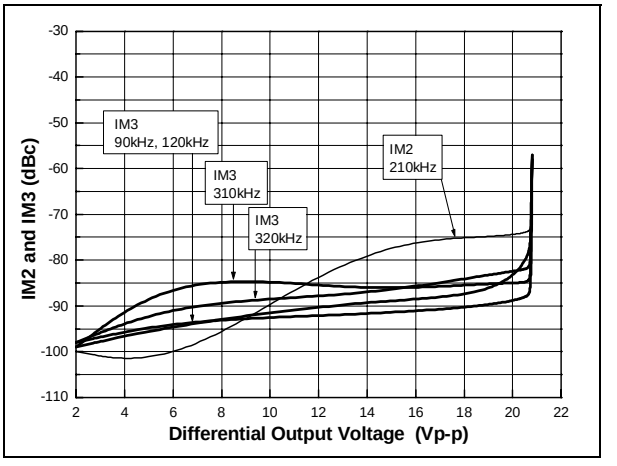


Figure 52. Intermodulation vs. Output Amplitude: 100kHz & 110kHz, A_V=+4, R_{fb}=620Ω, R_L=50Ω diff., V_{CC}=±6V

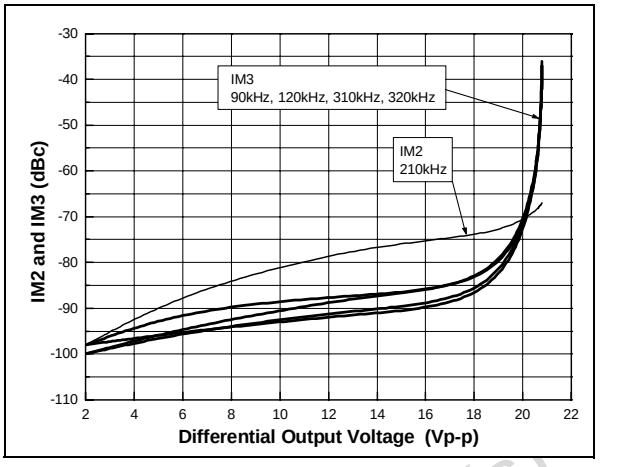


Figure 53. Intermodulation vs. Frequency Range: A_V=+4, R_{fb}=620Ω, R_L=50Ω diff., Vout=16Vpp, V_{CC}=±6V

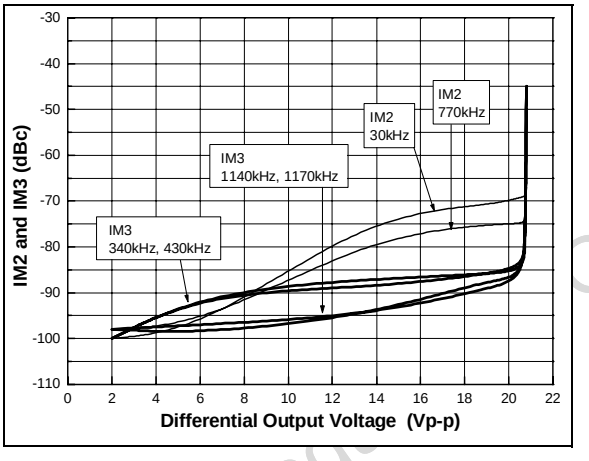
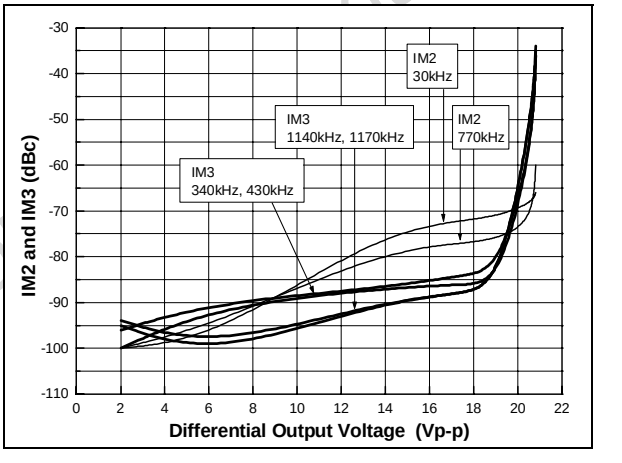


Figure 54. Intermodulation vs. Output Amplitude: 370kHz & 400kHz, A_V=+4, R_{fb}=620Ω, R_L=50Ω diff., V_{CC}=±6V



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6 Printed Circuit Board Layout Considerations

In the ADSL frequency rangey, printed circuit board parasites can affect the closed-loop performance.

The use of a proper ground plane on both sides of the PCB is necessary to provide low inductance and a low resistance common return. The most important factors affecting gain flatness and bandwidth are stray capacitance at the output and inverting input. To minimize capacitance, the space between signal lines and ground plane should be maximized. Feedback component connections must be as short as possible in order to decrease the associated inductance which affects high-frequency gain errors. It is very important to choose the smallest possible external components—for example, surface mounted devices (SMD)—in order to minimize the size of all DC and AC connections.

6.1 Thermal information

The TS615 is housed in an exposed-pad plastic package. As described in *Figure 55*, this package has a lead frame upon which the dice is mounted. This lead frame is exposed as a thermal pad on the underside of the package. The thermal contact is direct with the dice. This thermal path provides an excellent thermal performance.

The thermal pad is electrically isolated from all pins in the package. It must be soldered to a copper area of the PCB underneath the package. Through these thermal paths within this copper area, heat can be conducted away from the package. The copper area **must** be connected to $-V_{CC}$ available on pin 4.

Figure 55. Exposed-pad package

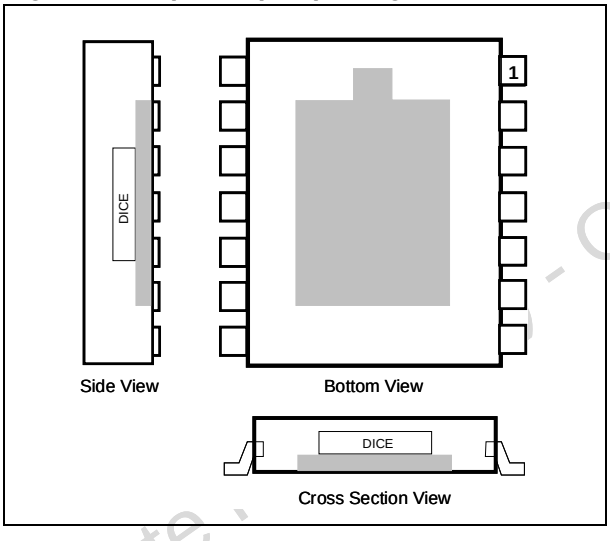
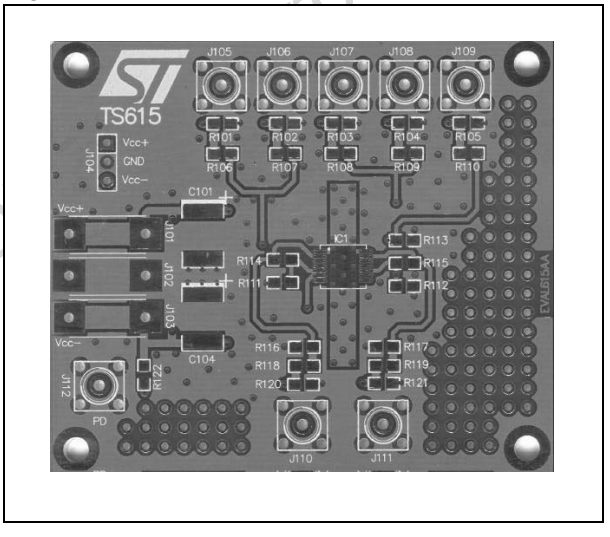


Figure 56. Evaluation board



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Figure 57. Schematic diagram

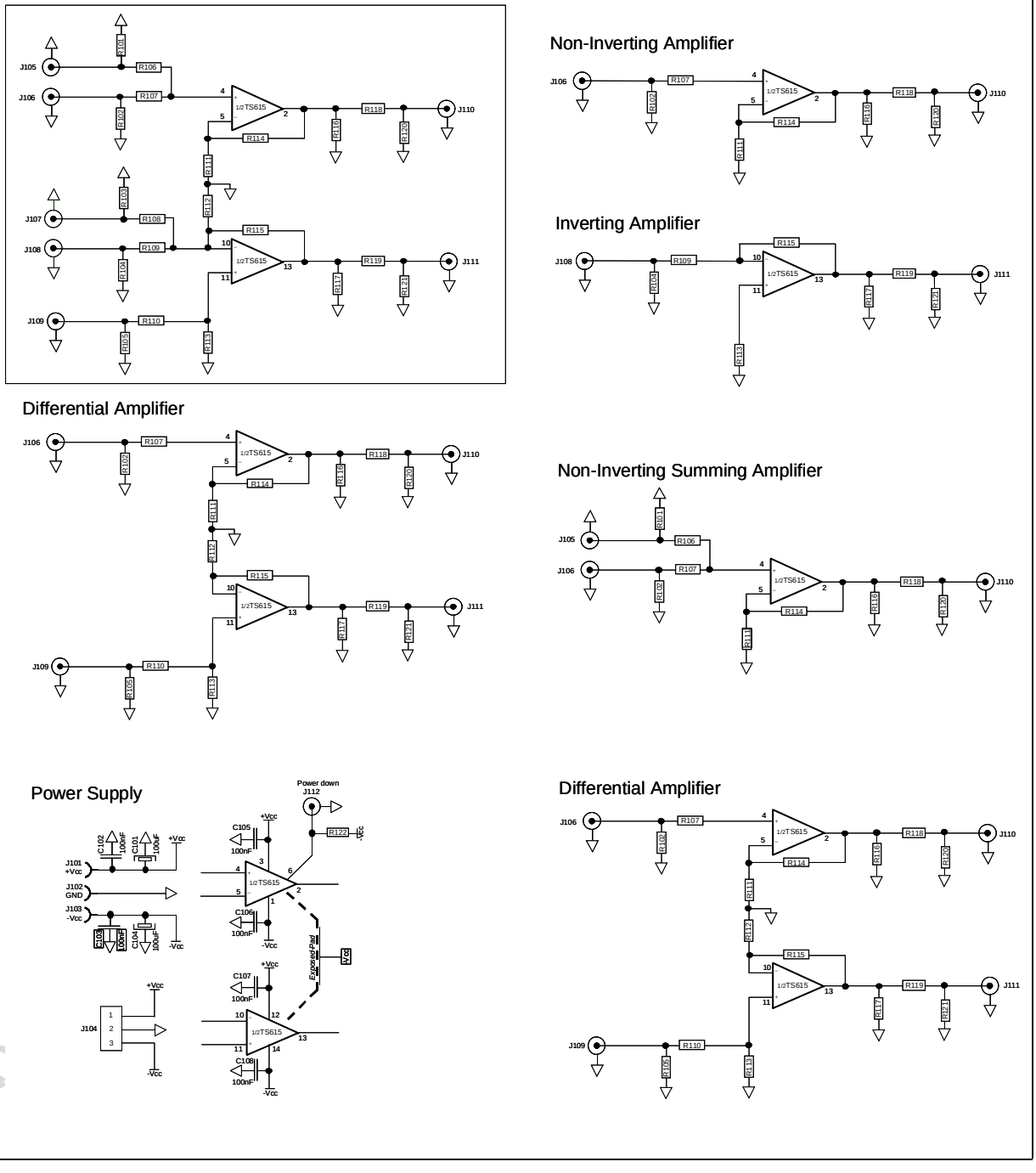


Figure 58. Component locations - top side

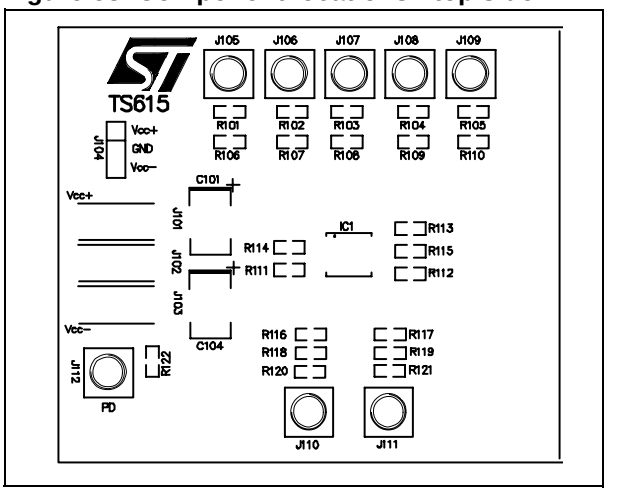


Figure 59. Component locations - bottom side

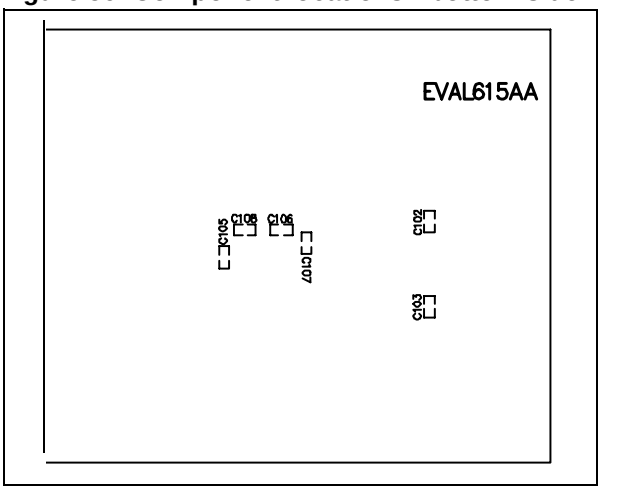


Figure 60. Top side board layout

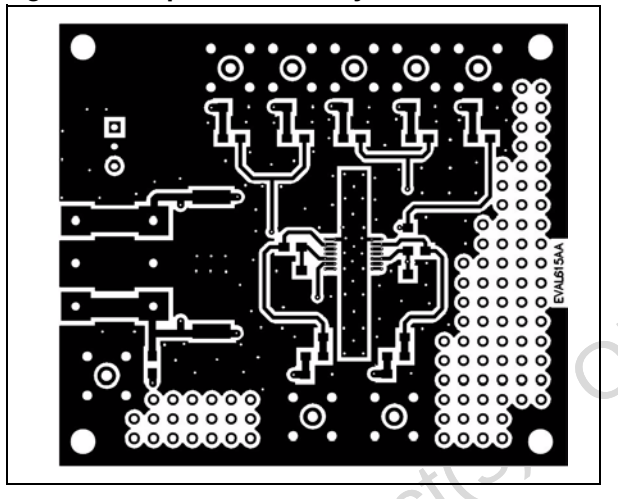
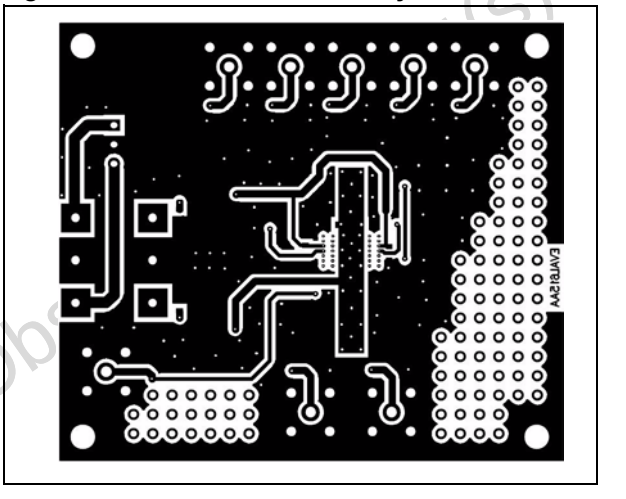


Figure 61. Bottom side board layout



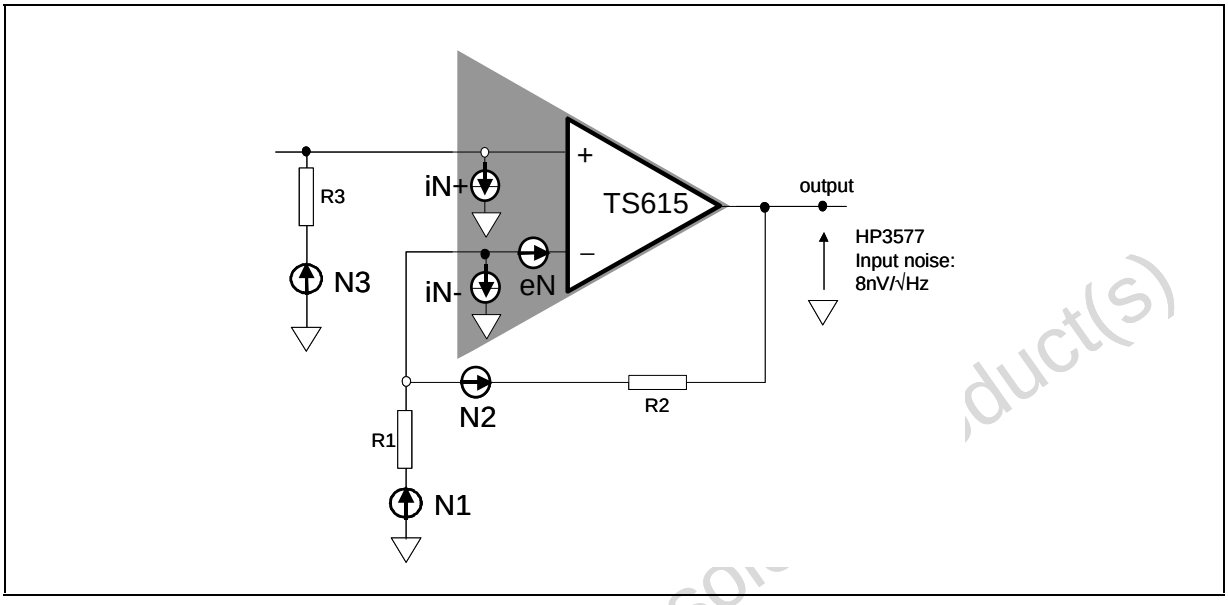
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7 Noise Measurements

The noise model is shown in *Figure 62*, where:

- eN: input voltage noise of the amplifier
- iNn: negative input current noise of the amplifier
- iNp: positive input current noise of the amplifier

Figure 62. Noise model



The closed loop gain is:

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

The six noise sources are:

$$V1 = eN \times \left(1 + \frac{R2}{R1}\right)$$

$$V2 = iNn \times R2$$

$$V3 = iNp \times R3 \times \left(1 + \frac{R2}{R1}\right)$$

$$V4 = -\frac{R2}{R1} \times \sqrt{4kTR1}$$

$$V5 = \sqrt{4kTR2}$$

$$V6 = \left(1 + \frac{R2}{R1}\right)\sqrt{4kTR3}$$

We assume that the thermal noise of a resistance R is:

$$\sqrt{4kTRDF}$$

where ΔF is the specified bandwidth.

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On a 1Hz bandwidth the thermal noise is reduced to

$$\sqrt{4kTR}$$

where k is Boltzmann's constant, equals to 1374 x 10^{-23}J/°K. T is the temperature (°K).

The output noise eNo is calculated using the Superposition Theorem. However eNo is not the sum of all noise sources, but rather the square root of the sum of the square of each noise source, as shown in *Equation 1*.

$$eNo = \sqrt{V1^2 + V2^2 + V3^2 + V4^2 + V5^2 + V6^2} \quad \textit{Equation 1}$$

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 \quad \textit{Equation 2}$$
$$\ldots + \left(\frac{R2}{R1}\right)^2 \times 4kTR1 + 4kTR2 + \left(1 + \frac{R2}{R1}\right)^2 \times 4kTR3$$

The input noise of the instrumentation must be extracted from the measured noise value. The real output noise value of the driver is:

$$eNo = \sqrt{(Measured)^2 - (instrumentation)^2} \quad \textit{Equation 3}$$

The input noise is called the Equivalent Input Noise as it is not directly measured but is evaluated from the measurement of the output divided by the closed loop gain (eNo/g).

After simplification of the fourth and the fifth term of *Equation 2* we obtain:

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 \ldots + g \times 4kTR2 + \left(1 + \frac{R2}{R1}\right)^2 \times 4kTR3 \quad \textit{Equation 4}$$

7.1 Measurement of *eN*

If we assume a short-circuit on the non-inverting input (R3=0), *Equation 4* becomes:

$$eNo = \sqrt{eN^2 \times g^2 + iNn^2 \times R2^2 + g \times 4kTR2} \quad \textit{Equation 5}$$

In order to easily extract the value of eN, the resistance R2 will be chosen as low as possible. On the other hand, the gain must be large enough:

- **R1=10Ω**, **R2=910Ω**, **R3=0, Gain=92**
- **Equivalent Input Noise**: 2.57nV/√Hz
- **Input Voltage Noise**: eN=2.5nV/√Hz

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7.2 Measurement of *iNn*

To measure the negative input current noise iNn, we set R3=0 and use *Equation 5*. This time the gain must be lower in order to decrease the thermal noise contribution:

- **R1=100Ω**, **R2=910Ω**, **R3=0, gain=10.1**
- **Equivalent input noise**: 3.40nV/√Hz
- **Negative input current noise**: iNn =21pA/√Hz

7.3 Measurement of *iNp*

To extract iNp from *Equation 3*, a resistance R3 is connected to the non-inverting input. The value of R3 must be chosen in order to keep its thermal noise contribution as low as possible against the iNp contribution.

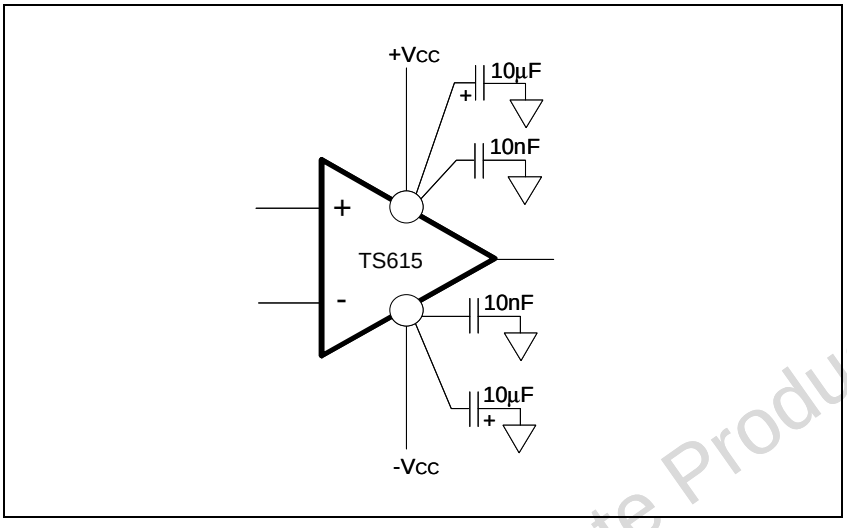
- **R1=100Ω**, **R2=910Ω**, **R3=100Ω**, **Gain=10.1**
- **Equivalent input noise**: 3.93nV/√Hz
- **Positive input current noise**: iNp=15pA/√Hz
- **Conditions:** Frequency=100kHz, V_{CC}=±2.5V
- **Instrumentation**: HP3585A Spectrum Analyzer (the input noise of the HP3585A is 8nV/√Hz)

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8 Power Supply Bypassing

Correct power supply bypassing is very important for optimizing performance in high-frequency ranges. Bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor greater than 1µF is necessary to minimize the distortion. For a better quality bypassing, a capacitor of 10nF is added using the same implementation conditions. Bypass capacitors must be incorporated for both the negative and the positive supply.

Figure 63. Circuit for power supply bypassing



8.1 Single power supply

The TS615 can operate with power supplies ranging from 12V to 5V. The power supply can either be single (12V or 5V referenced to ground), or dual (such as ±6V and ±2.5V).

In the event that a single supply system is used, new biasing is necessary to assume a positive output dynamic range between 0V and $+V_{CC}$ supply rails. Considering the values of V_{OH} and V_{OL}, the amplifier will provide an output dynamic from +0.5V to 10.6V on 25Ω load for a 12V supply and from 0.45V to 3.8V on 10Ω load for a 5V supply.

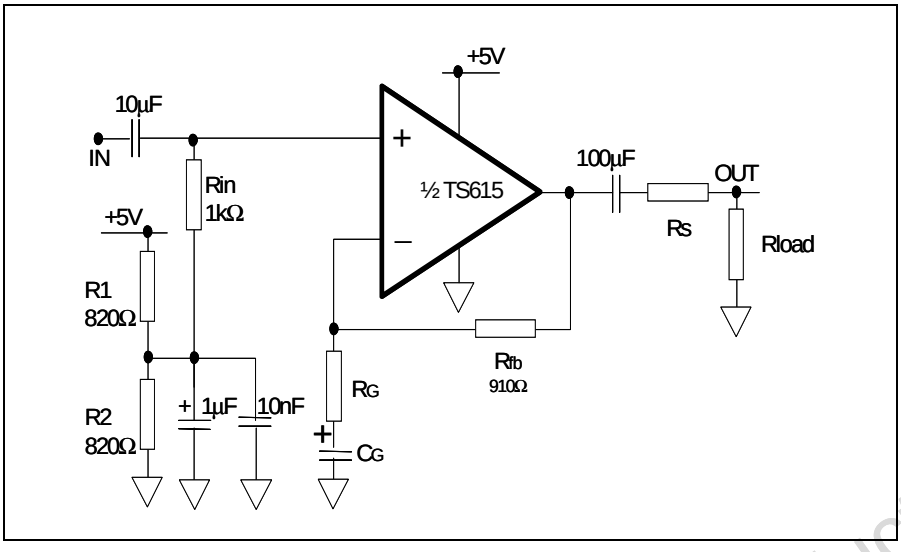
The amplifier must be biased with a mid-supply (nominally $+V_{CC}/2$), in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply, such as a virtual ground using an operational amplifier or a two-resistance divider (which is the cheapest solution). A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current (30µA max.) as the 1% of the current through the resistance divider to keep a stable mid-supply, two resistances of 2.2kΩ can be used in the case of a 12V power supply and two resistances of 820Ω can be used in the case of a 5V power supply.

The input provides a high-pass filter with a break frequency below 10Hz which is necessary to remove the original 0 volt DC component of the input signal, and to fix it at $+V_{CC}/2$.

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Figure 64 shows a schematic of a 5V single power supply configuration

Figure 64. Circuit for +5V single supply

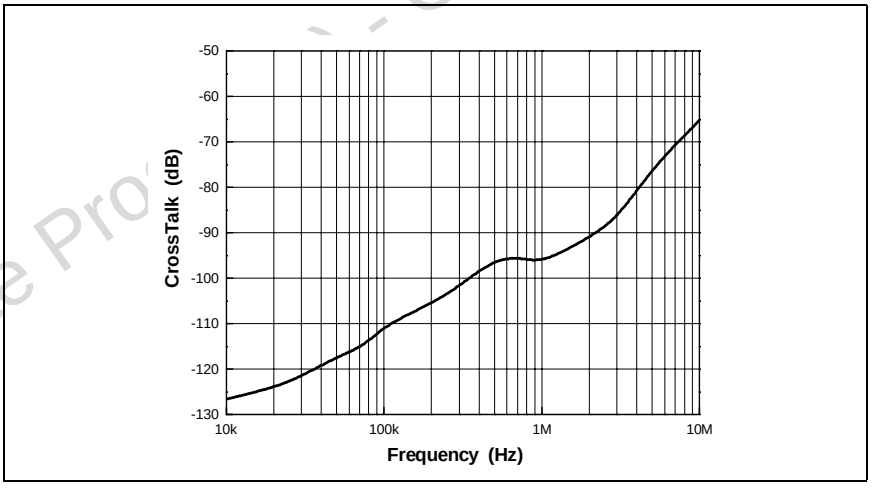


8.2 Channel separation and crosstalk

Figure 65 shows an example of crosstalk from one amplifier to a second amplifier. This phenomenon, accentuated at high frequencies, is unavoidable and intrinsic to the circuit itself.

Nevertheless, the PCB layout also has an effect on the crosstalk level. Capacitive coupling between signal wires, distance between critical signal nodes and power supply bypassing are the most significant factors.

Figure 65. Crosstalk vs. frequency: A_V=+4, R_{fb}=620Ω, V_{CC}=±6V, Vout=2Vp

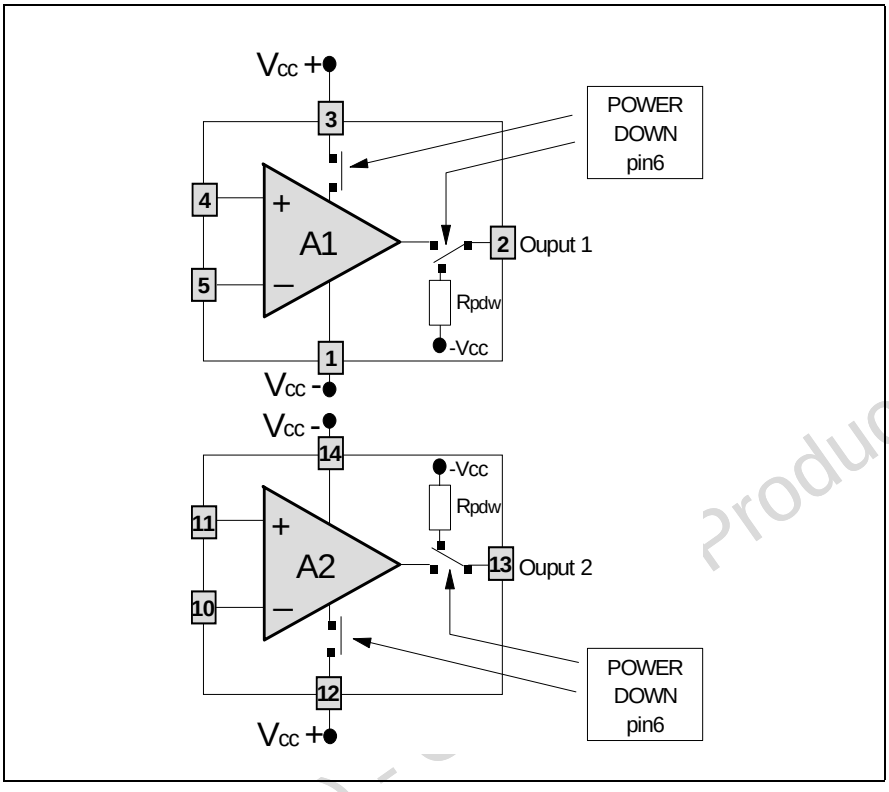


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9 Power Down Mode Behavior

Please note that the short-circuited output in power-down mode is referenced to ($-V_{CC}$). No problems appear when used in differential mode. Nevertheless, when used in single-ended mode on a load referenced to GND, the ($-V_{CC}$) level contributes to a current consumption through the load.

Figure 66. Equivalent schematic



As shown in *Figure 66*, the interest of having an output short-circuit in power-down mode is to keep the best impedance matching between the system and the twisted pair telephone line when the modem is in sleep mode. By doing this, the modem can be woken up with a signal from the line without any damage

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to this signal. This concept is particularly intended for the ADSL-over-voice modems, where the modem in sleep mode, and must be woken up by the phone call.

Figure 67. Matching in sleep mode

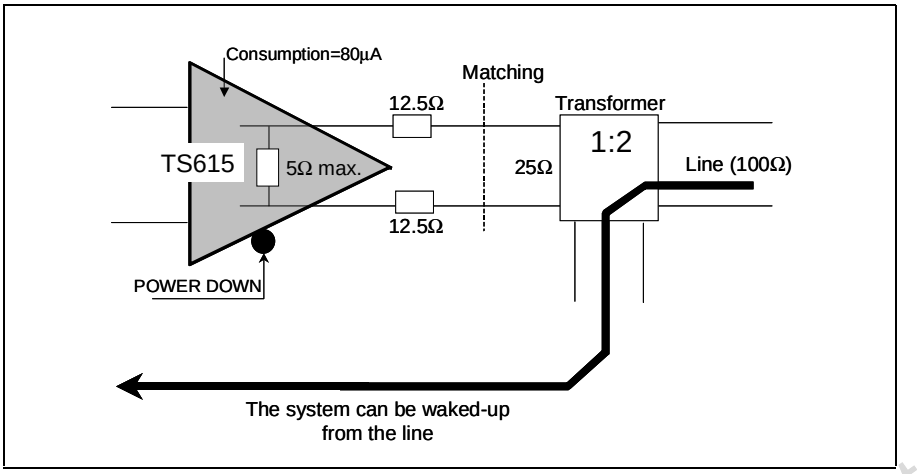


Figure 68. Standby mode. Time On>Off

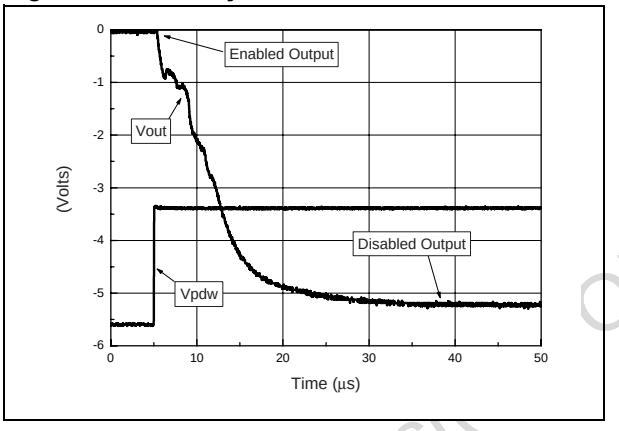


Figure 69. Standby mode. Time Off>On

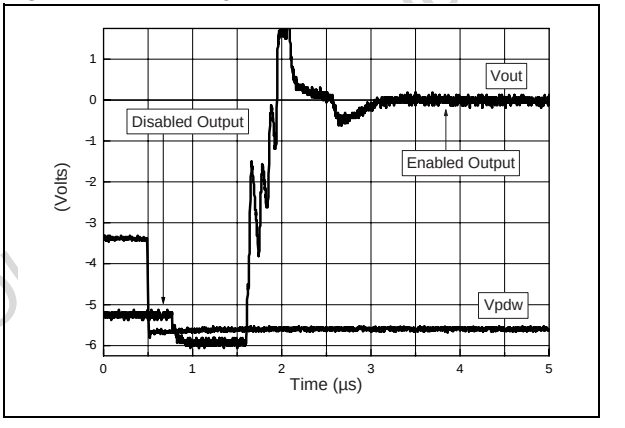
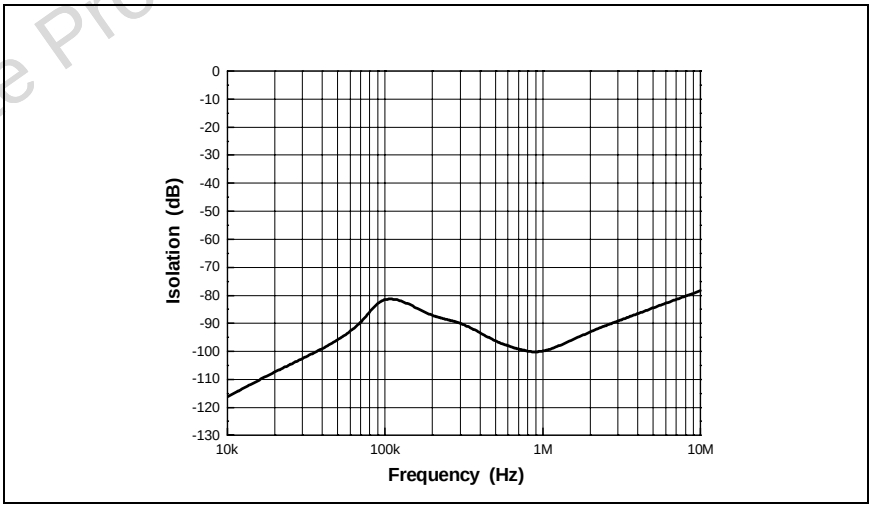


Figure 70. Standby mode. input/output isolation vs. frequency: A_V=+4, R_{fb}=620Ω, V_{CC}=±6V, Vout=3Vp



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10 Choosing the Feedback Circuit

As described on *Figure 72* on page 31, the TS615 requires a 620 Ω feedback resistor to optimize the bandwidth with a gain of 12 dB for a 12 V power supply. Nevertheless, due to production test constraints, the TS615 is tested with the same feedback resistor for 12 V and 5 V power supplies (910Ω).

Table 6. Closed-loop gain - feedback components

V_{CC} (V)	Gain	R_{fb} (Ω)
±6	+1	750
	+2	680
	+4	620
	+8	510
	-1	680
	-2	680
	-4	620
	-8	510
±2.5	+1	1.1k
	+2	1k
	+4	910
	+8	680
	-1	1k
	-2	1k
	-4	910
	-8	680

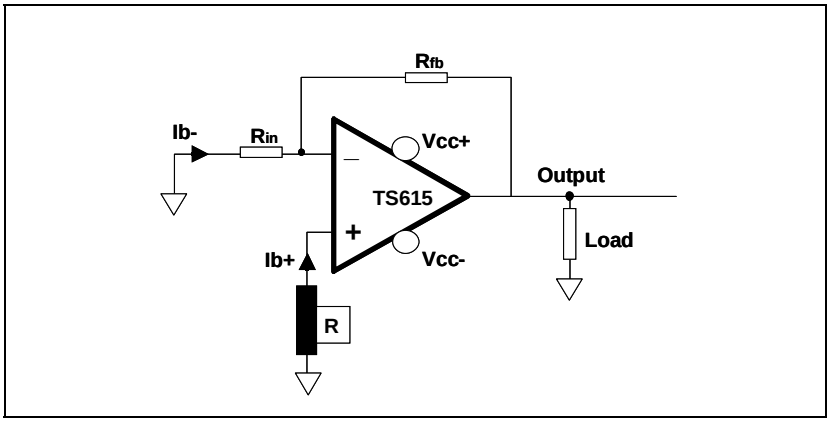
10.1 The bias of an inverting amplifier

A resistance is necessary to achieve a good input biasing, such as resistance R, shown in *Figure 71*.

The magnitude of this resistance is calculated by assuming the negative and positive input bias current. The aim is to compensate for the offset bias current, which could affect the input offset voltage and the output DC component. Assuming Ib-, Ib+, R_{in}, R_{fb} and a zero volt output, the resistance R will be:

$$R = R_{in} // R_{fb}$$

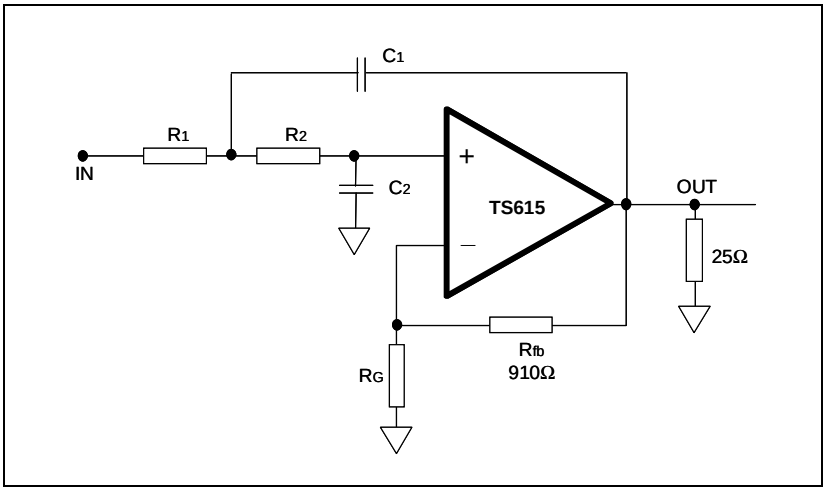
Figure 71. Compensation of the input bias current



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10.2 Active filtering

Figure 72. Low-pass active filtering. Sallen-Key



From the resistors R_{fb} and R_G we can directly calculate the gain of the filter in a classical, non-inverting amplification configuration:

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

We assume the following expression as the response of the system:

$$T_{j\omega} = \frac{Vout_{j\omega}}{Vin_{j\omega}} = \frac{g}{1 + 2\zeta\frac{j\omega}{\omega_c} + \frac{(j\omega)^2}{\omega_c^2}}$$

The cutoff frequency is not gain-dependent and so becomes:

$$\omega_c = \frac{1}{\sqrt{R1R2C1C2}}$$

The damping factor is calculated by the following expression:

$$\zeta = \frac{1}{2}\omega_c(C_1R_1 + C_1R_2 + C_2R_1 - C_1R_1g)$$

The higher the gain the more sensitive the damping factor is. When the gain is higher than 1, it is preferable to use some very stable resistor and capacitor values. In the case of R1=R2:

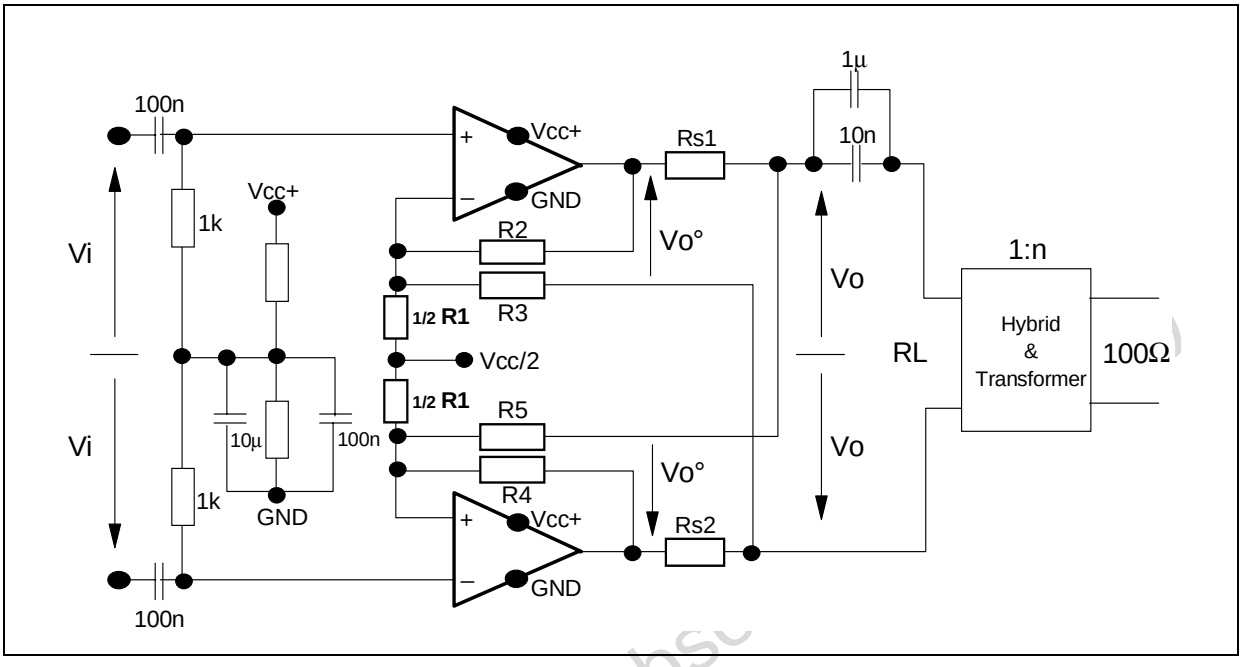
$$\zeta = \frac{2C_2 - C_1\frac{R_{fb}}{R_g}}{2\sqrt{C_1C_2}}$$

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11 Increasing the Line Level Using Active Impedance Matching

With passive matching, the output signal amplitude of the driver must be twice the amplitude on the load. To go beyond this limitation an active matching impedance can be used. With this technique, it is possible to maintain good impedance matching with an amplitude on the load higher than half of the output driver amplitude. This concept is shown in *Figure 73* for a differential line.

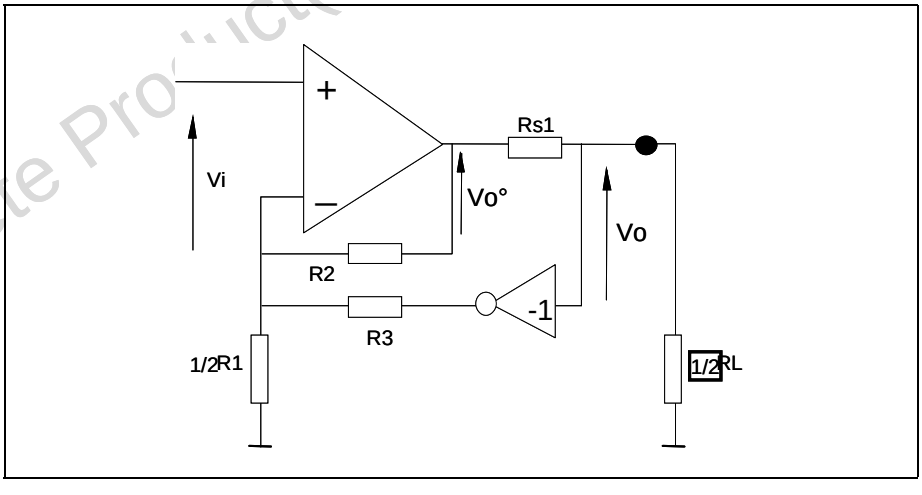
Figure 73. TS615 as a differential line driver with active impedance matching



Component calculation

Let us consider the equivalent circuit for a single-ended configuration, as shown in *Figure 74*.

Figure 74. Single-ended equivalent circuit



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First let's consider the unloaded system. We can assume that the currents through R1, R2 and R3 are respectively:

$$\frac{2Vi}{R1}, \frac{(Vi - Vo^{\circ})}{R2} \text{ and } \frac{(Vi + Vo)}{R3}$$

As Vo° equals Vo without load, the gain in this case becomes:

$$G = \frac{Vo(noload)}{Vi} = \frac{1 + \frac{2R2}{R1} + \frac{R2}{R3}}{1 - \frac{R2}{R3}}$$

The gain, for the loaded system is given by *Equation 6*:

$$GL = \frac{Vo(withload)}{Vi} = \frac{1}{2}\frac{1 + \frac{2R2}{R1} + \frac{R2}{R3}}{1 - \frac{R2}{R3}} \quad \textit{Equation 6}$$

The system shown in *Figure 74* is an ideal generator with a synthesized impedance acting as the internal impedance of the system. From this, the output voltage becomes:

$$Vo = (ViG) - (Ro \cdot Iout) \quad \textit{Equation 7}$$

where Ro is the synthesized impedance and Iout the output current.

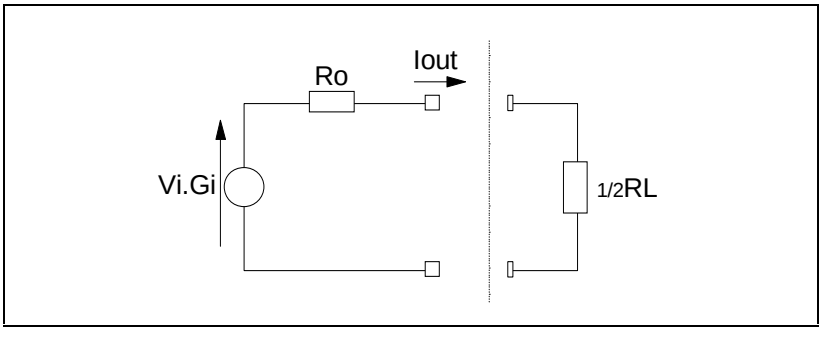
On the other hand Vo can be expressed as:

$$Vo = \frac{Vi\left(1 + \frac{2R2}{R1} + \frac{R2}{R3}\right)}{1 - \frac{R2}{R3}} - \frac{Rs1Iout}{1 - \frac{R2}{R3}} \quad \textit{Equation 8}$$

By identification of both *Equation 7* and *Equation 8*, the synthesized impedance is, with Rs1=Rs2=Rs:

$$Ro = \frac{Rs}{1 - \frac{R2}{R3}} \quad \textit{Equation 9}$$

Figure 75: Equivalent schematic. Ro is the synthesized impedance



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Let us write Vo°=kVo, where k is the matching factor varying between 1 and 2. If we assume that the current through R3 is negligible, we can calculate the output resistance, Ro:

$$Ro = \frac{kVoRL}{RL + 2Rs1}$$

After choosing the k factor, Rs will equal to 1/2RL(k-1).

For a good impedance matching we assume that:

$$Ro = \frac{1}{2}RL \qquad \textit{Equation 10}$$

From *Equation 9* and *Equation 10*, we derive:

$$\frac{R2}{R3} = 1 - \frac{2Rs}{RL} \qquad \textit{Equation 11}$$

By fixing an arbitrary value of R2, *Equation 11* becomes:

$$R3 = \frac{R2}{1 - \frac{2Rs}{RL}}$$

Finally, the values of R2 and R3 allow us to extract R1 from *Equation 6*, so that:

$$R1 = \frac{2R2}{2\left(1 - \frac{R2}{R3}\right)GL - 1 - \frac{R2}{R3}} \qquad \textit{Equation 12}$$

with GL the required gain.

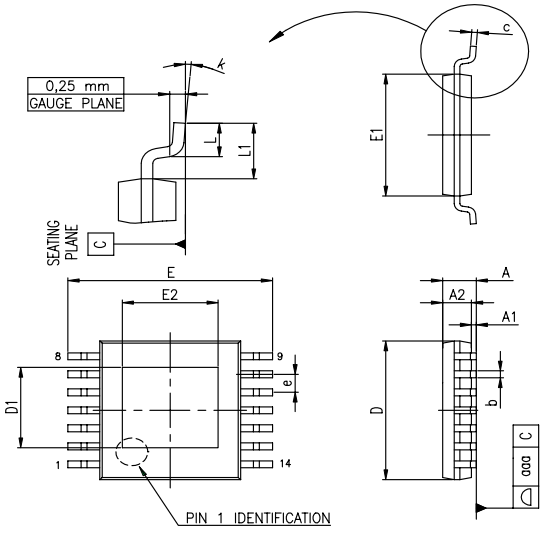
Table 7. Components calculation for impedance matching implementation

GL (gain for the loaded system)	GL is fixed for the application requirements GL=Vo/Vi=0.5(1+2R2/R1+R2/R3)/(1-R2/R3)
R1	2R2/[2(1-R2/R3)GL-1-R2/R3]
R2 (=R4)	Arbitrarily fixed
R3 (=R5)	R2/(1-Rs/0.5RL)
Rs	0.5RL(k-1)
Load viewed by each driver	kRL/2

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12 Package Mechanical Data

TSSOP14 EXPOSED PAD MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
D1	1.7			0.067		
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	1.5			0.059		
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



13 Revision History

Date	Revision	Description of Changes
01 Nov 2002	1	First Release
03 Dec 2004	2	General grammatical and formatting changes to entire document. Specific changes: • Moved note in *Table 3* to *Chapter 10: Choosing the Feedback Circuit* on page 30. • Added *Chapter 4: Safe Operating Area* on page 16. • Simplified mathematical representations of the intermodulation product in *Chapter 5: Intermodulation Distortion Product* on page 17. • In *Chapter 6: Printed Circuit Board Layout Considerations* on page 20, change from “The copper area *can* be connected to (-Vcc) available on pin 4.” to “The copper area **must** be connected to -Vcc available on pin 4.”. • In *Section 10.1: The bias of an inverting amplifier* on page 30, change of section title, and correction of referred figure to *Figure 71*.

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