



TS4909 low power stereo headphone amplifier evaluation board user guidelines

Introduction

This application note concerns the DEMOTS4909 evaluation board, designed to evaluate the TS4909 low power stereo headphone amplifier with capacitor-less output.

In this document, you will find:

- a brief description of the TS4909 audio amplifier
- a description of the evaluation board and all of its components
- the layout of the evaluation board

About the TS4909

The TS4909 is a stereo audio amplifier designed to drive headphones in portable applications.

The integrated phantom ground is a circuit topology that eliminates the heavy output coupling capacitors. This is of primary importance in portable applications where space constraints are very high. A single-ended configuration is also available, offering even lower power consumption because the phantom ground can be switched off.

Specially designed for applications requiring low power supplies, the TS4909 is capable of delivering 52mW of continuous average power into a 32Ω load with less than 1% THD+N from a 3V power supply. Pop & click noise during switch-on and switch-off phases is eliminated thanks to integrated circuitry.

Key features of the TS4909 include:

- No output coupling capacitors necessary
- Pop & click noise reduction circuitry
- Operating from $V_{CC} = 2.2V$ to 5.5V
- Standby mode active low
- Output power:
 - 158mW @5V, into 16Ω with 1% THD+N max (1kHz)
 - 52mW @3.0V into 32Ω with 1% THD+N max (1kHz)
- Ultra low current consumption: 2.0mA typ. @3V
- Ultra low standby consumption: 10nA typ.
- High signal-to-noise ratio 105dB typ. @5V
- High crosstalk immunity: 110dB (F=1kHz)
- PSRR: 72dB (F=1kHz), inputs grounded
- Low t_{WU} : 50ms in PHG mode, 100ms in SE mode
- Available in lead-free DFN10 3x3mm

For complete information about the TS4909, refer to the datasheet.

1 Description of the evaluation board

The DEMOTS4909 evaluation board is designed for the TS4909 low power stereo headphone amplifier with capacitor-less output.

The gain (A_V) is set at 1 V/V for both channels and can be adapted if necessary with a modification of R1 or R2 values for the Left channel, and R3 or R4 values for the Right channel.

Table 1. Gain per channel

Channel	Gain (V/V)
Left	$A_V = \frac{R_2}{R_1}$
Right	$A_V = \frac{R_4}{R_3}$

C1 with R1 (and C3 with R3) create an input high-pass filter with a cut-off frequency of 24.1Hz. C8 with a 16Ω load (and C9 with a 32Ω load) create an output high-pass filter with a cut-off frequency of 45.2Hz (22.6Hz). For information on how to change the value of the cut-off frequency, refer to the datasheet.

The C2 and C4 component locations are empty in order to add a low-pass filter if required.

Table 2. Evaluation board connectors

Connector	Description
P1	Connector for setting PHG or SE configuration of the TS4909: –  the pins 1 and 2 are shorted, output stage is in SE mode –  the pins 2 and 3 are shorted, output stage is in PHG mode The connector pins are connected: – 1 to V_{CC} – 2 to SE/PHG control – 3 to GND
P2	Power connector (V _{CC} and GND). Power supply voltage from 2.2V to 5.5V.
P3	Output signal connector. The connector pins are: – 1&2: SE output 1 (GND and active signal) – 3&4: PHG output 1 (PHG reference voltage output and active signal) – 5&6: PHG output 2(active signal and PHG reference voltage output) – 7&8: SE output 2 (active signal and GND)
P4	Standby control connector: –  the pins 1 and 2 are shorted, the TS4909 is in operation mode –  the pins 2 and 3 are shorted, the TS4909 is in standby mode The connector pins are connected: – 1 to V_{CC} – 2 to standby control – 3 to GND
P5	Input signal connector (GND and active input signal). Pins 1 and 2 for input 1 and pins 3 and 4 for input 2.

Caution: When you apply the power supply through P2, **do not** invert the polarity because it would destroy the amplifier at U1.

Figure 1. Schematic diagram

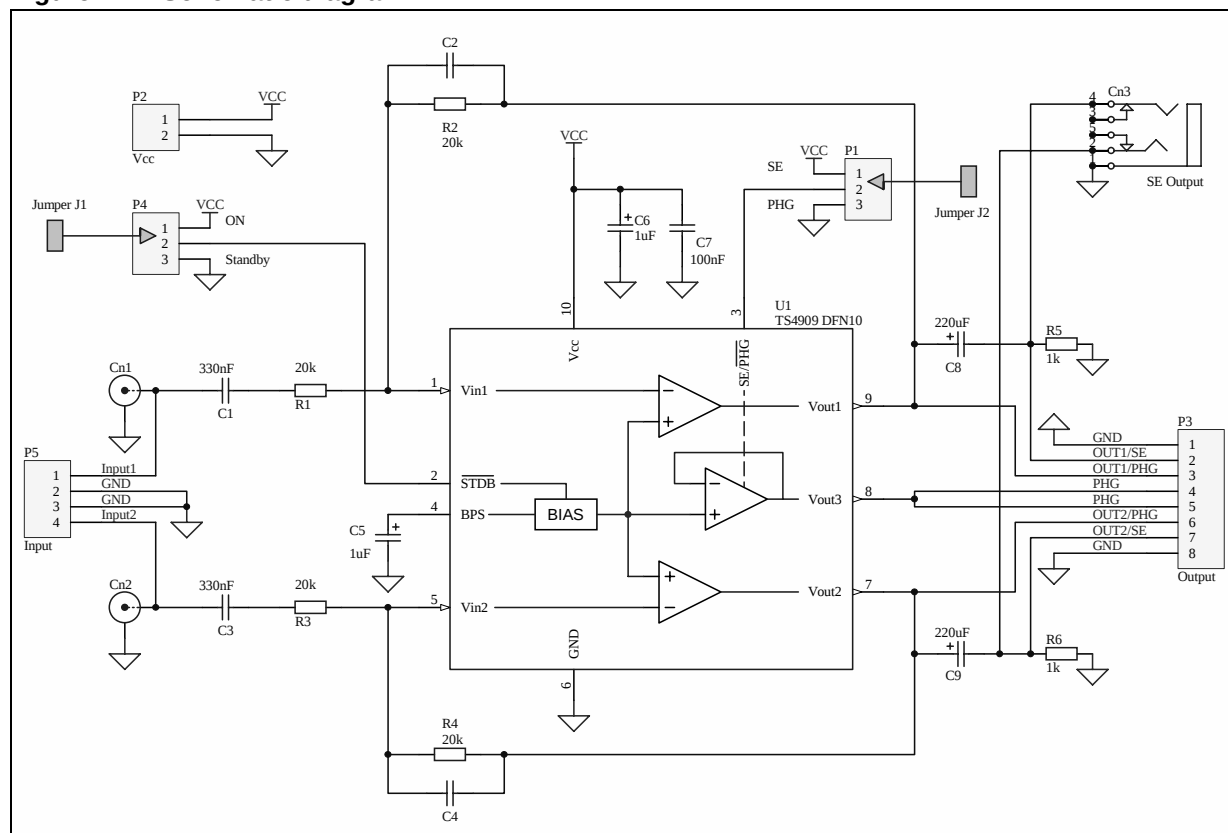


Table 3. Component list for the evaluation board

Designation	Quantity	Description
C1, C3	2	330nF/16V, ceramic capacitors, 0805
C2, C4	0	Not connected, 0603
C7	1	100nF/16V, ceramic capacitors, 0805
C5, C6	2	1μF/50V, electrolytic capacitor
C8, C9	2	220μF/10V, electrolytic capacitor
P2	1	2-pin header 2.54mm pitch
P3, P4	2	3-pin header 2.54mm pitch
P3	1	8-pin header 2.54mm pitch
P5	1	4-pin header 2.54mm pitch
J1, J2	2	Jumper, 2.54mm pitch
Cn1, Cn2	2	Not connected, phono plug
Cn3	1	Not connected, stereo headphone jack 3.5
U1	1	TS4909

2 Evaluation board layout

The following schematics show the layers and the top view of the evaluation board.

Figure 2. PCB top layer

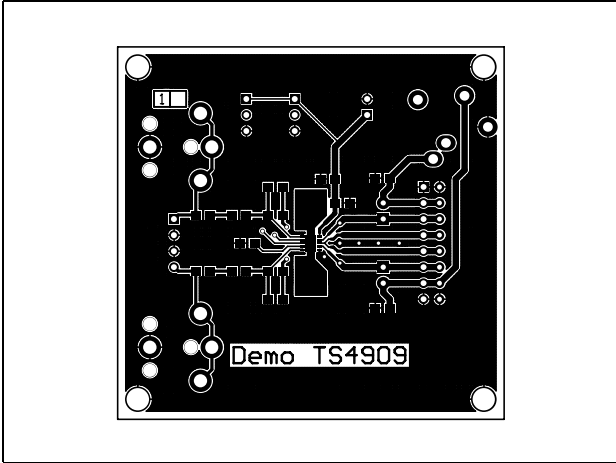


Figure 3. PCB bottom layer

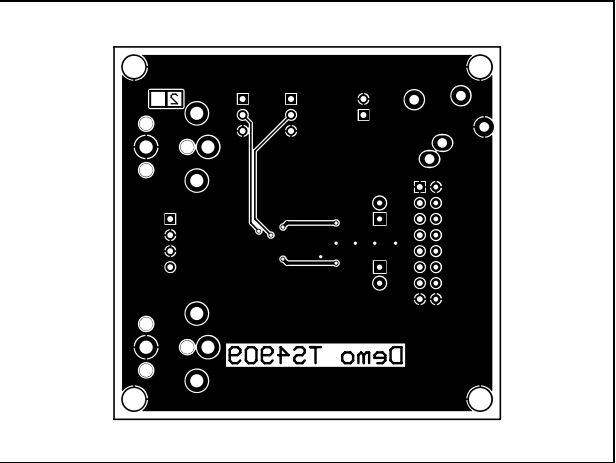
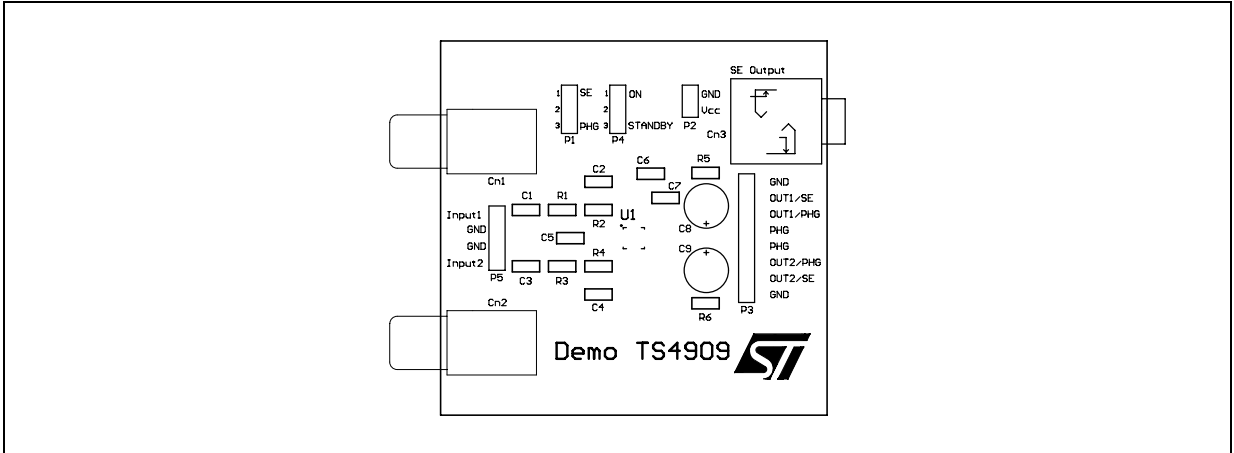


Figure 4. Top view of evaluation board



3 Revision history

Table 4. Document revision history

Date	Revision	Changes
23-Sep-2007	1	Initial release.

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