TRU050

Complete VCXO based Phase-Locked Loop



The TRU050, VCXO based PLL

Features

- Output Frequencies to 65.536 MHz
- 5.0 V or 3.3Vdc Operation
- Tri-State Output
- Holdover on Loss of Signal Alarm
- VCXO with CMOS Outputs
- 0/70° or –40/85°C Temperature Range
- Ceramic SMD Package
- RoHS/Lead Free Compliant

Description

The VI TRU050 is a user-configurable crystal-based PLL integrated circuit. It includes a digital phase detector, op-amp, VCXO and additional integrated functions for use in digital synchronization applications. Loop filter software is available as well SPICE models for circuit simulation.

Applications

- Frequency Translation
- Clock Smoothing
- NRZ Clock Recovery
- DSLAM, ADM, ATM, Aggregation, Optical Switching/Routing, Base Station
- Low Jitter PLL's

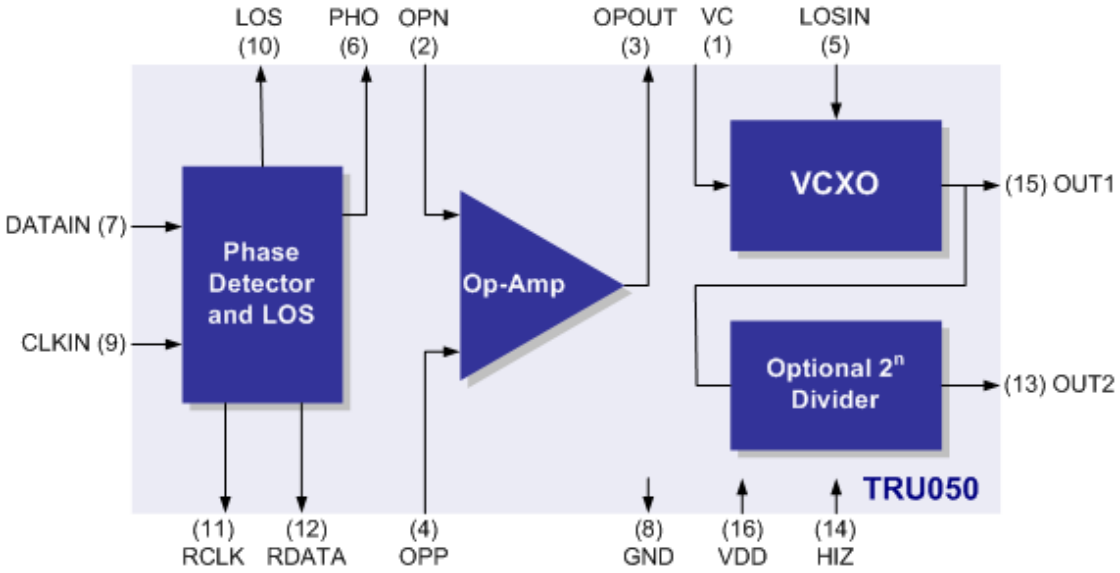


Figure 1. TRU050 Block Diagram

Performance Characteristics

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Output Frequency (*ordering option*) Out 1, 5V option Out 1, 3.3V option		 1.000 1.000		 65.636 51.840	 MHz MHz
Supply Voltage [1] +5 +3.3	V_{DD}	 4.5 3.0	 5.0 3.3	 5.5 3.6	 V V
Supply Current	I_{DD}			65	mA
Output Logic Levels Output Logic High[2] Output Logic Low[2]	 V_{OH} V_{OL}	 2.5		 0.5	 V V
Output Transition Times Rise Time[2] Fall Time[2]	 t_R t_F			 5 5	 ns ns
Input Logic Levels Output Logic High[2] Output Logic Low[2]	 V_{IH} V_{IL}	 2.0		 0.5	 V V
Loss of Signal Indication Output Logic High[2] Output Logic Low[2]	 V_{OH} V_{OL}	 2.5		 0.5	 V V
Nominal Frequency on Loss of Signal Output 1 Output 2				 ±75 ±75	 ppm ppm
Symmetry or Duty Cycle[3] Out 1 Out 2 RCLK	 SYM1 SYM2 RCLK			 40/60 45/55 40/60	 % % %
Absolute Pull Range, *ordering option* over operating temp, aging, power supply variations	APR	±50 ±80 ±100			ppm
Test Conditions for APR (+5V option)	V_C	0.5		4.5	V
Test Conditions for APR (+3.3V option)	V_C	0.3		3.0	V
Gain Transfer			Positive		
Phase Detector Gain +5V option +3.3V Option			 0.53 0.35		 rad/V rad/V
Operating temperature, *ordering option*			0/70 or –40/85		°C
Control Voltage Leakage Current	I_{VCXO}			±1	uA

1. A good quality 0.01uF in parrallel with a 0.1 uf capacitor should be located as close to pin 16 to ground as possible.
2. Figure 1 defines these parameters. Figure 2 illustrates the equivalent five-gate TTL load and operating conditions under which these parameters are tested and specified. Loads greater than 15 pF will adversely effect rise/fall time and duty cycle.
3. Symmetry is defined as (ON TIME/PERIOD with Vs=-1.4 V for both 5V and 3.3V operation.

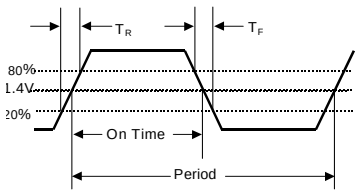


Figure 2. Output Waveform

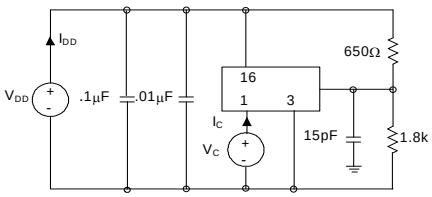


Figure 3. OUT1, OUT2, RDATA and RCLK
Test Conditions (25±5°C)

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	7	Vdc
Storage Temperature	Tstorage	-55/125	°C
Soldering Temperature/Duration	T_{PEAK} / t_P	260 / 40	°C/sec
Clock and Data Input Range	CLKIN, DATAIN	Gnd-0.5 to V_{DD} +0.5	V

Reliability

The TRU050 is capable of meeting the following qualification tests.

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014, 100% Tested
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

Although ESD protection circuitry has been designed into the the TRU050, proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model.

Table 4. ESD Ratings

Model	Minimum	
Human Body Model	1500V	MIL-STD 3015
Charged Device Model	1000V	JESD 22-C101

TRU050 Theory of Operation

Phase Detector

The phase detector has two buffered inputs, DATAIN and CLKIN, which are designed to switch at 1.4 volts. DATAIN is designed to accept an NRZ data stream but may also be used for clock signals which have about a 50% duty cycle. CLKIN is connected to OUT1 or OUT2, or a divided version of one of these outputs. CLKIN and DATAIN and are protected by ESD diodes and should not exceed the power supply voltage or ground by more than a few hundred millivolts.

The phase detector is basically a latched flip flop/exclusive-or gate/differential amplifier filter design to produce a DC signal proportional to the phase between the CLKIN and DATAIN signals, see figure 4 for a block diagram and figure 5 for a open loop transfer curve. This simplies the PLL design as the designer does not have to filter narrow pulse signal to a DC level. Under locked conditions the rising edge CLKIN will be centered in the middle of the DATAIN signal, see figure 6.

The phase detector gain is 0.53V/rad x data density for 5volt operation, and 0.35V/rad x data density for 3.3 volt operation. Data density = 1.0 for clock signals and is system dependent on coding and design for NRZ signals, but 0.25 could be used as a starting point for data density.

The phase detector output is a DC signal for DATAIN frequencies greater than 1MHz but produces signficant ripple when inputs are less than 200kHz. Additional filtering is required for low input frequency applications such as 8kHz frequency translation, see figures 8 and 9.

Under closed loop conditions the active filter has a blocking capacitor which provides a very high DC gain, so under normal locked conditions and input frequencies >1MHz, PHO will be about $V_{DD}/2$ and will not vary signifigantly with changes in input frequency (within lock range). The control (voltage pin 1) will vary according to the input frequency offset, but PHO will remain relatively constant.

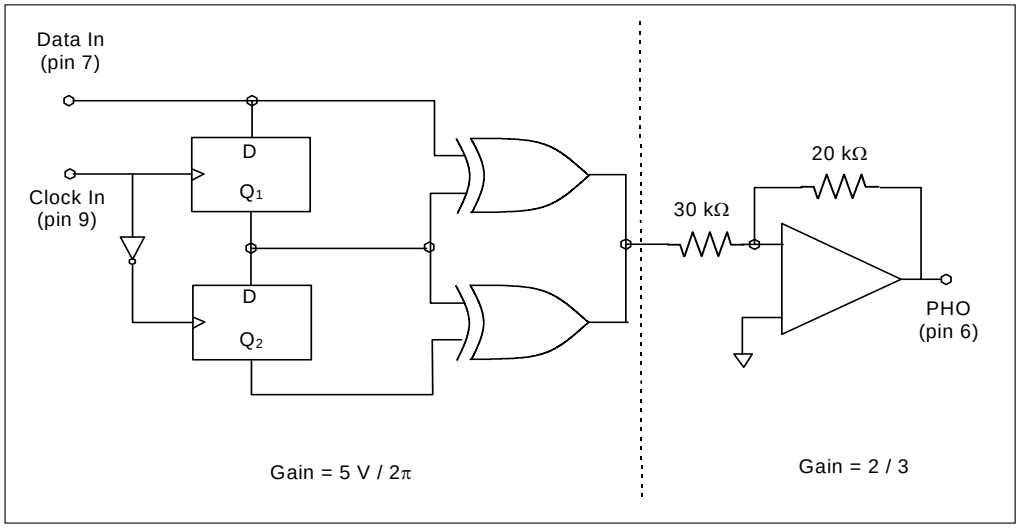


Figure 4. Simplified Phase Detector Block Diagram

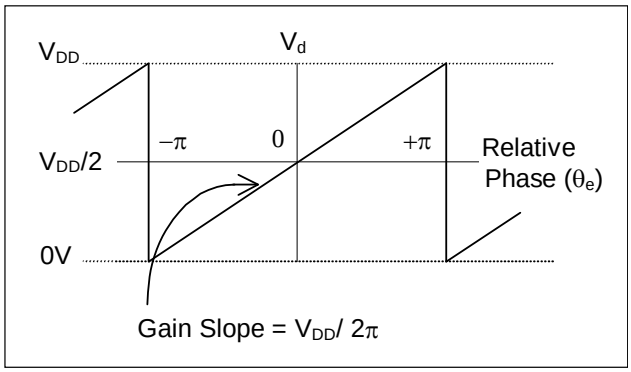


Figure 5. Open Loop Phase Detector Transfer Curve

Recovered Clock and Data Alignment Outputs

The TRU050 is designed to recover an imbedded clock from an NRZ data signal and retime it with a data pattern. In this application, the VCXO frequency is exactly the same frequency as the NRZ data rate and the outputs are taken off Pin 11, RCLK, and Pin 12, RDATA. Under locked conditions, the falling edge of RCLK is centered in the RDATA pattern. Also, there is a 1.5 clock cyle delay between DATAIN and RDATA. Figure 6 shows the relationship between the DATAIN, CLKIN, RDATA and RCLK.

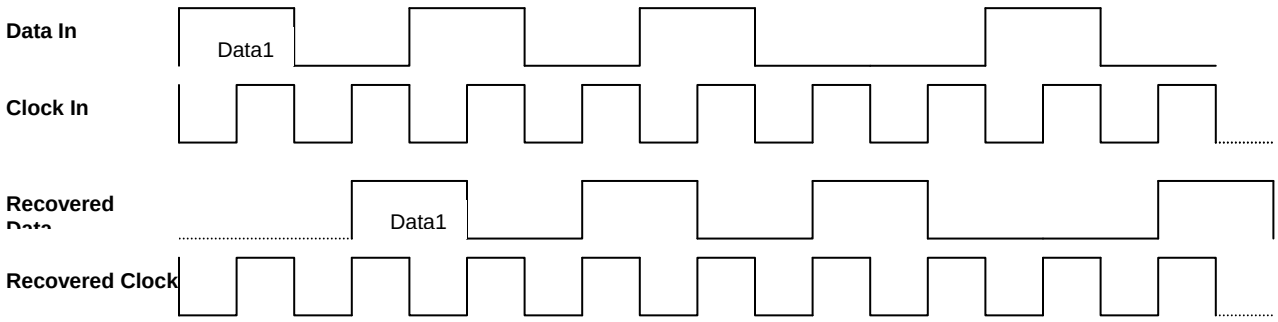


Figure 6. Clock and Data Timing Relationships for the NRZ data

Other RZ encoding schemes such as Manchester or AMI can be accomidated by using a TRU050 at twice the baud rate.

Loss of Signal, LOS and LOSIN

The LOS circuit provides an output alarm flag when the DATAIN input signal is lost. The LOS output is normally a logic low and is set to a logic high after 256 consecutive clock periods on CLKIN with no detected DATAIN transitions. This signal can be used to either flag external alarm circuits and/or drive the TRU050's LOSIN input. When LOSIN is set to a logic high, the VCXO control voltage (pin 1) is switched to an internal voltage which centers OUT1 and OUT2 to center frequency +/-75ppm. Also, LOS automatically closes the op amp feedback which means the op-amp is a unity gain buffer and will produce a DC voltage equal to the +op amp voltage (pin 4), usually VDD/2.

VCXO and Absolute Pull Range (APR) Specification

The TRU050's VCXO is a varactor tuned crystal oscillator, which produces an output frequency proportional to the control voltage (pin 1). The frequency deviation of the TRU050 VCXO is specified in terms of Absolute Pull Range (APR). APR provides the user with a guaranteed specification for minimum available frequency deviation over all operating conditions. Operating conditions include operating temperature range, power supply variation, and differences in output loading and changes due to aging.

A TRU050 VCXO with an APR of +/-50 ppm will track a +/-50 ppm reference source over all operating conditions. The fourth character of the product code in Table 6 specifies absolute Pull Range (APR). Please see Vectron's web site, www.vectron.com, for the APR Application Note.

APR is tested at 0.5 and 4.5 volts for a 5 volt option and 0.3 and 3.0 volts for the 3.3 volt option.

VCXO Aging

Quartz stabilized oscillators typically exhibit a small shift in output frequency during aging. The major factors, which lead to this shift, are changes in the mechanical stress on the crystal and mass-loading of foreign material on the crystal.

As the oscillator ages, relaxation of the crystal mounting stress or transfer of environmental stress through the package to the crystal mounting arrangement can lead to frequency variations. VI has minimized these two effects through the use of a miniature AT-Cut strip resonator crystal, which allows a superior mounting arrangement, and results in minimal relaxation and almost negligible environmental stress transfer.

VI has eliminated the impact of mass loading by ensuring hermetic integrity and minimizing outgassing by limiting the number of internal components through the use of ASIC technology. Mass-loading on the crystal generally results in a frequency decrease and is typically due to outgassing of material within a hermetic package or from contamination by external material in a less than hermetic package.

Under normal operating conditions with an operating temperature of 40°C, the TRU050 will typically exhibit 2 ppm aging in the first year of operation. The device will then typically exhibit 1 ppm aging the following year with a logarithmic decline each year thereafter.

Divide-By Feature

The lowest available VCXO OUT 1 frequency is 12.000MHz. To achieve lower frequencies, such as 1.544 or 2.048 MHz, OUT1 is divided by a 2^n counter , where n=1 to 8 and is the OUT2 frequency. This results in a divide by 2,4,8…256 option and is wire-bonded at the factory, so it is user selectable upon ordering only. To achieve 1.544 or 2.048MHz, a TRU050 at 24.704 with a divide by 16 or a TRU050 16.384 with a divide-by 8 would be used. Additional external divide-by circuits can be used to further lower or change the input frequency range.

A disabled Out2 is available.

Loop Filter

A PLL is a feedback system which forces the output frequency to lock in both phase and frequency to the input frequency. While there will be some phase error, theory states there is no frequency error. The loop filter design will dictate many key parameters such as jitter reduction, stability, lock range and acquisition time. Be advised that many textbook equations describing loop dynamics, such as capture range or lockin time, are based on ideal systems. Such equations may not be accurate for real systems due to nonlinearities, DC offsets, noise and don't take into account the limited VCXO bandwidth. This section deals with some real world design examples. Also, there is loop filter software on the Vectron web site, plus experienced applications engineers are eager to assist in this process. Common TRU050 PLL applications are shown in figures 7 and 8 (frequency translation), 9 (clock recovery) and 10 (clock smoothing).

Of primary concern to the designer is selecting a loop filter that insures lock-in, stability and provides adequete filtering of the input signal. A good starting point for the the loop filter bandwidth is 100ppm times the DATAIN frequency. An example would be translating an 8kHz signal to 44. 736MHz – DS3 – which is = 100 ppm x kHz = 8Hz . So for 8kHz inputs, ~ 8 Hz loop bandwidth may be reasonable and figures 7 and 8 show and 8kHz to DS3 and 8kHz to 19.440 MHz frequency translation designs.

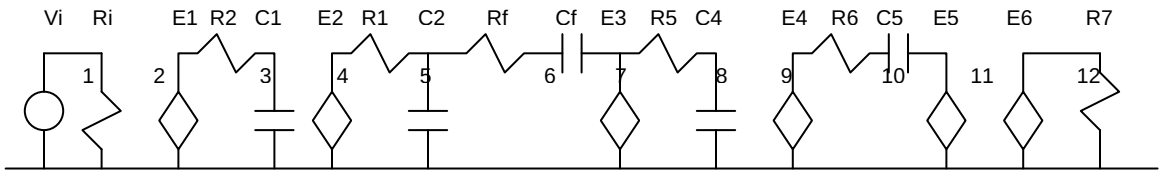
It's fairly easy to set a low loop bandwidth for large frequency translations such as 8kHz to 44.736MHz, but becomes more difficult for clock smoothing applications such as 19.440MHz in and 19.440MHz output. In this example, 100ppm x 19.440MHz is about 2kHz and may be too high to reject kow frequency jitter. A good way to resolve this is to lower the input frequency such as dividing the input frequency down. The loop filter bandwidth becomes lower since 100ppm * DATAIN is lowered. Figure 10 shows an example of how to design a low loop bandwith on a relatively high input signal and still maintain a wide lock range. The "100ppm * DATAIN frequency" loop filter bandwidth can then be tailored to the application, since lower bandwidthds are desriable to clean up and or translate clock signals and higher bandwidths may be needed for clock recovery of NRZ signals.

There is no known accurate formula for calculating acquisition time and so the best way to provide realisitc figures is to measure the lock time for a TRU050. Aquistion time was measured to be 3 to 5 seconds by measuring the control voltage in an 8kHz to 34.368 MHz frequency translation application - similar to the application in figure 7 and 8, to sub 10 milliseconds for NRZ data patterns such as figure 9. It may be tempting reduce the damping factor to 0.7 or 1.0 in order to increase aquisition time; but, it degrades stability and will not signifigantly decrease lock time. This is due to the fact that most VCXO's have a 10kHz bandwidth so setting a 100kHz loop bandwidth is impossible. A damping factor of 4 is fairly conservative and allows for excellent stability.

Some general quidelines for selecting loop filter include: Values should be less than 1Megohm and at least 10Kohm between the PHO and OPN, the capacitor should be low leakage and a polarized capacitor is acceptable, the R/C's should be located physically close to the TRU050 . Also, the loop filter software available on the web site was written for 5 volt operation, a simple way to calculate values for 3.3 volt operation is to times the data density by 0.66 (3.3V / 5V).

SPICE models are another design aid. In most cases a new PLL TRU050 design is calculated by using the software and verified with SPICE models, and depending on the circumstances evaluated in the applications lab. The simple active pi model is in figure 7. Loop filter values can be modified to suit the system requirements and application. There are many excellent references on designing PLL's, such as "Phase-Locked Loops, Theory, Design and Applications", by Roland E Best McGraw-Hill; however, there is loop filter software on the Vectron web site, plus experienced applications engineers eager to assist in this process.

Figure 7. SPICE Model



*****TRU050 ac Loop model
vi 1 0 ac 1
ri 1 0 1K

*****Phase Detector
e1 2 0 1 0 1 (for closed loop response use: e1 2 0 1 12 1)
r2 2 3 30K
c1 2 0 60p

*****Phase Detector Gain=0.53 x Data Density (Data Density=1 for clocks) for 5 volt operation and = 0.35 * Data Density for 3.3 volt operation
e2 4 0 3 0 .**35**

*****Loop filter
r1 4 5 **60K**
c2 5 0 10p
rf 5 6 **90K**
cf 6 7 **1.0u**
e3 7 0 5 0 –10000

***** VCXO, Input Bandwidth=50kHz
r5 7 8 160K
c4 8 0 20p

*****VCXO Gain x 2pi (Example, use OUT1 x 100ppm x 2 x pi)
e4 9 0 8 0 **12214**

*****1/S model
r6 9 10 1000
c5 10 11 0.001
e5 11 0 10 0 –1e6

****Divide by N
e6 12 0 11 0 **1**
r8 12 0 1K

The bold numbers are user selectable R/C, data density, VCXO frequency and divide-by values, and are from figure 11.

Layout Considerations

To achieve stable, low noise performance good analog layout techniques should be incorporated and a partial list includes:

The TRU050 should be treated more like an analog device and the power supply should be well decoupled with good quality RF 0.01 uf and 0.1uf capacitors. In some cases, a pi filter such as a large capacitor (10uF) to ground, a series ferrite bead or inductor, and 0.01 uf and 100 pf capacitor to ground to decouple the device supply is used.

The traces for the OUT1, OUT2, RCLK and RDATA ouputs should be kept as short as possible. It is common practice to use a series resistor – 50 to 100 ohms – in order to reduce reflections if these traces are more than a couple of inches long. Also OUT1, OUT2 RCLK and RDATA should not be routed directly underneath the device.

The op-amp loop filter components should be kept as close to the device as possible and the feedback capacitor should be located close the op-amp input terminal. The loop filter capacitor(s) should be low leakage and polarized capacitors are allowed keeping this is mind.

Unused outputs should be left floating and it is not required to load or terminate them (such as an PECL or ECL output). Loading unused outputs will only increase current consumption.

Typical Application Circuits

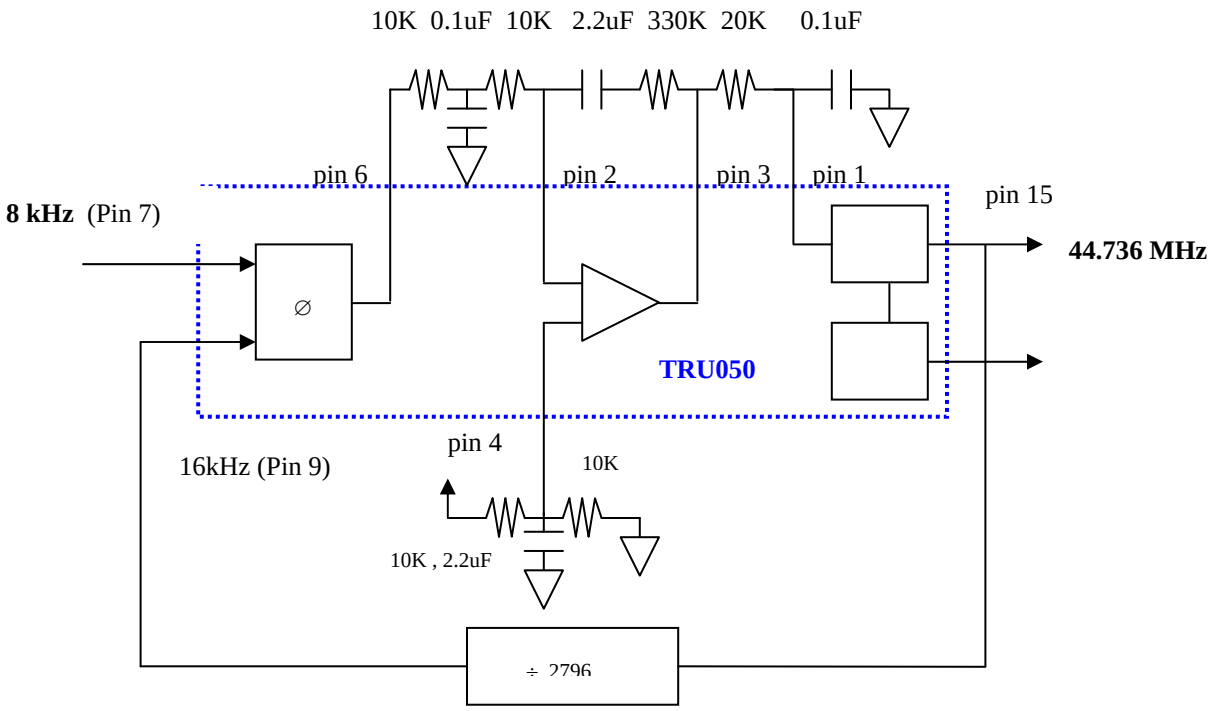
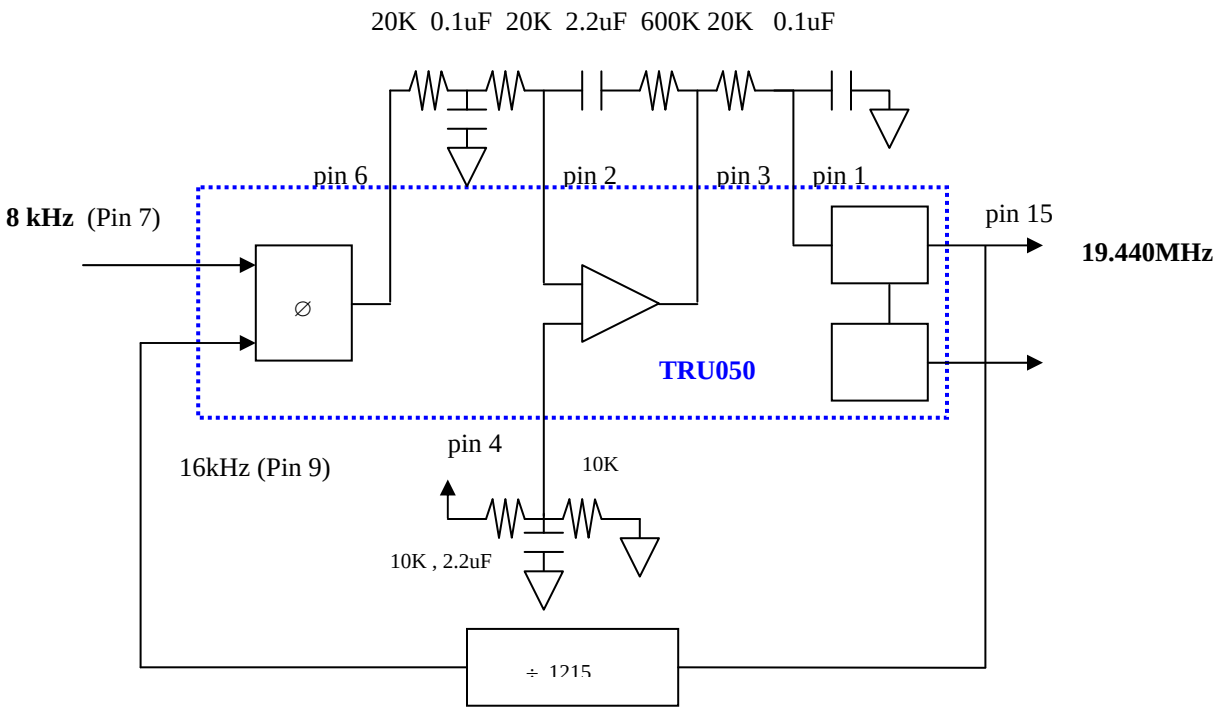
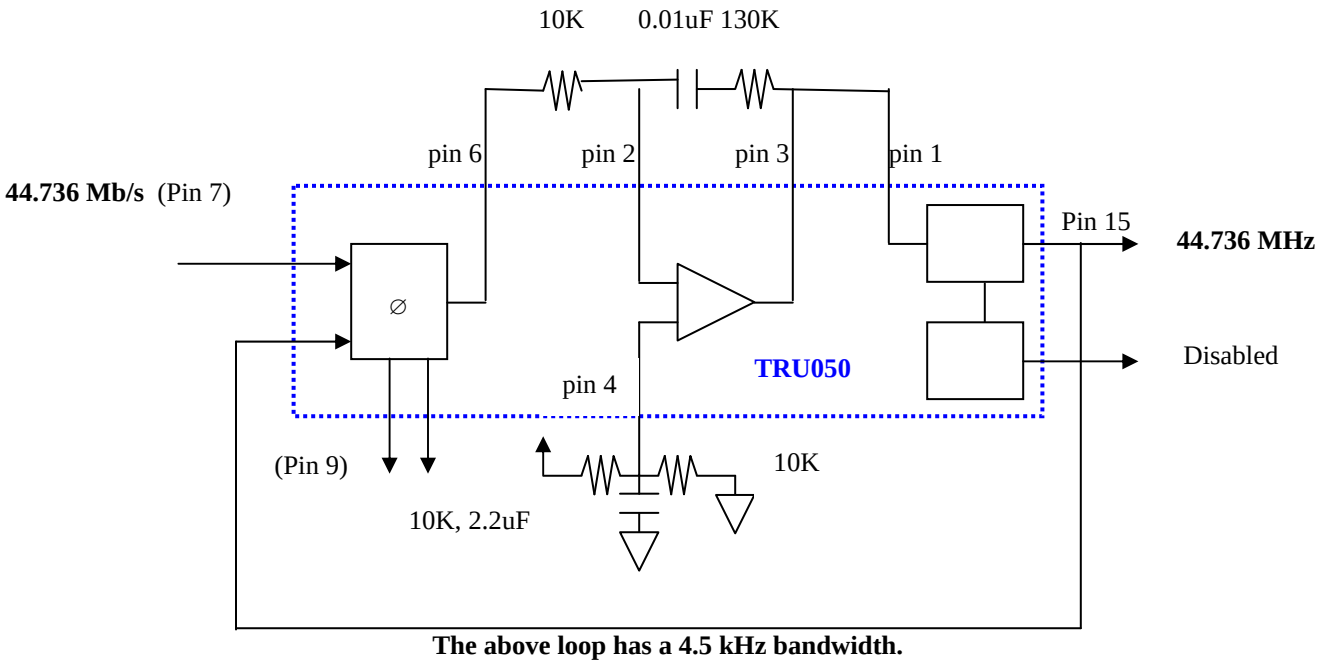


Figure 8. 8kHz to DS3 Frequency Translation



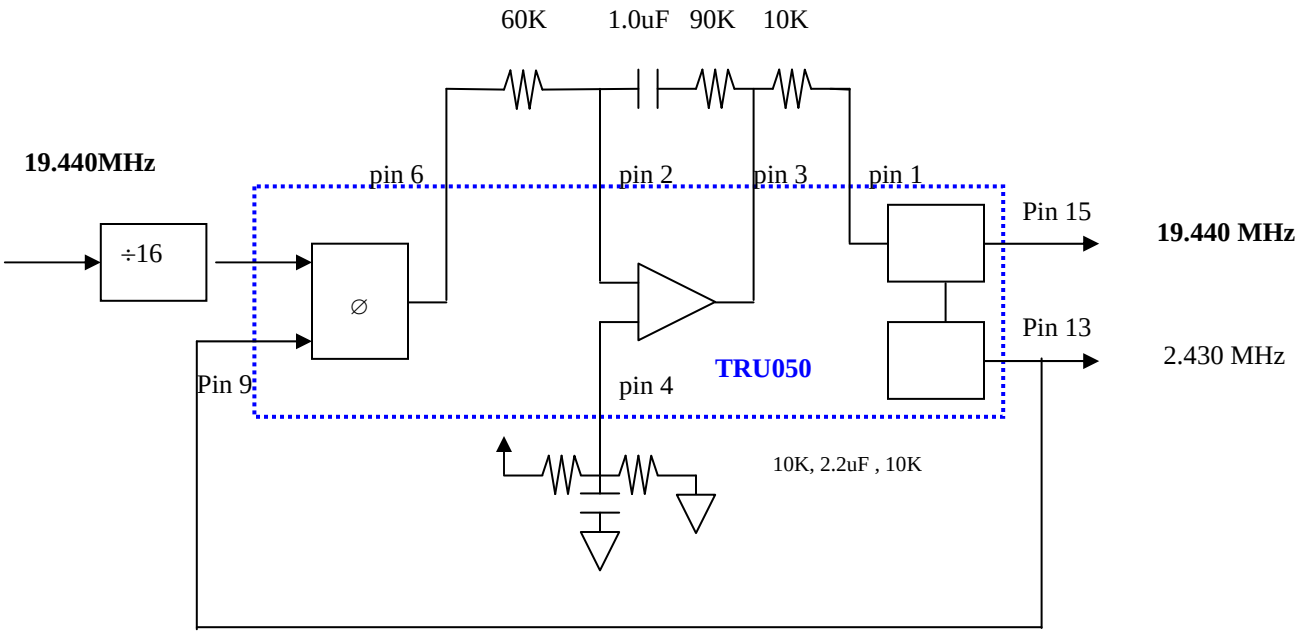
The above loop has a 10 Hz bandwidth.

Figure 9. 8kHz to 19.44MHz Frequency Translation



The above loop has a 4.5 kHz bandwidth.

Figure 10. DS3 NRZ Clock Recovery



The above loop has a 125 Hz bandwidth.

Figure 11. 19.440 Clock Smoothing

Table 5. Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The TRU050 device is hermetically sealed so an aqueous wash is not an issue.

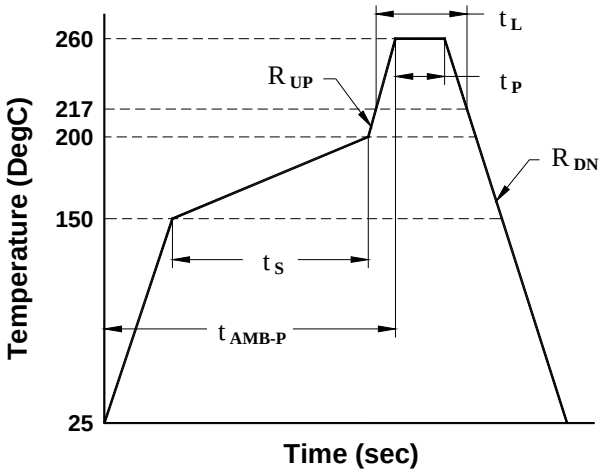


Figure 12. Suggested IR profile

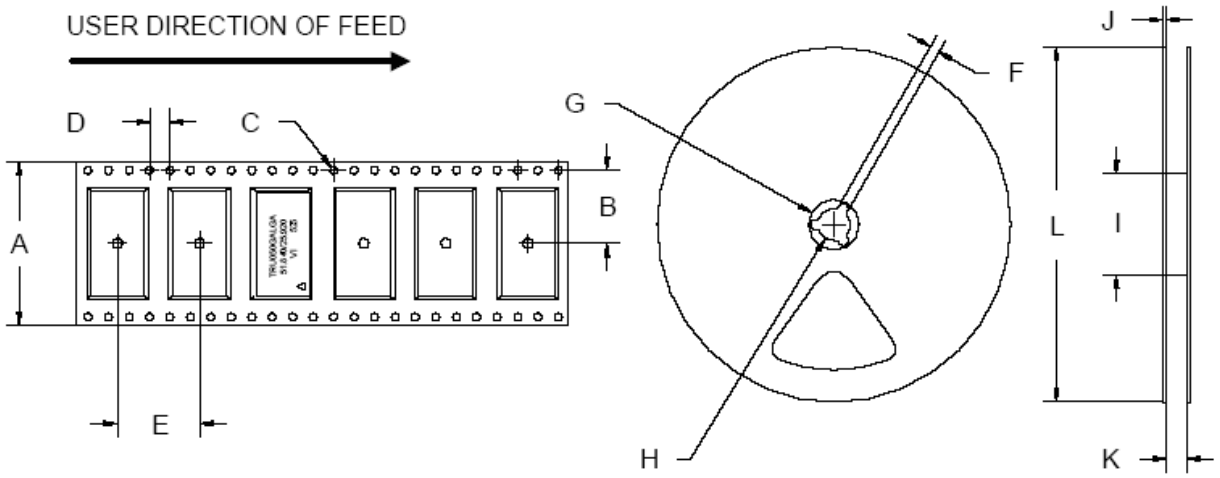


Figure 13. Tape and Reel Diagram

Table 6. Tape and Reel Information													
Tape Dimensions (mm)						**Reel Dimensions (mm)**							
Dimension	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**	**L**	**# Per Reel**
Tolerance	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Min**	**Min**	**Typ**	**Min**	**Typ**	**Max**	**Typ**	
TRU050	32	14.2	1.5	4	16	1.78	21	13.0	100	5	33.1	330	200

Package Outline Diagrams

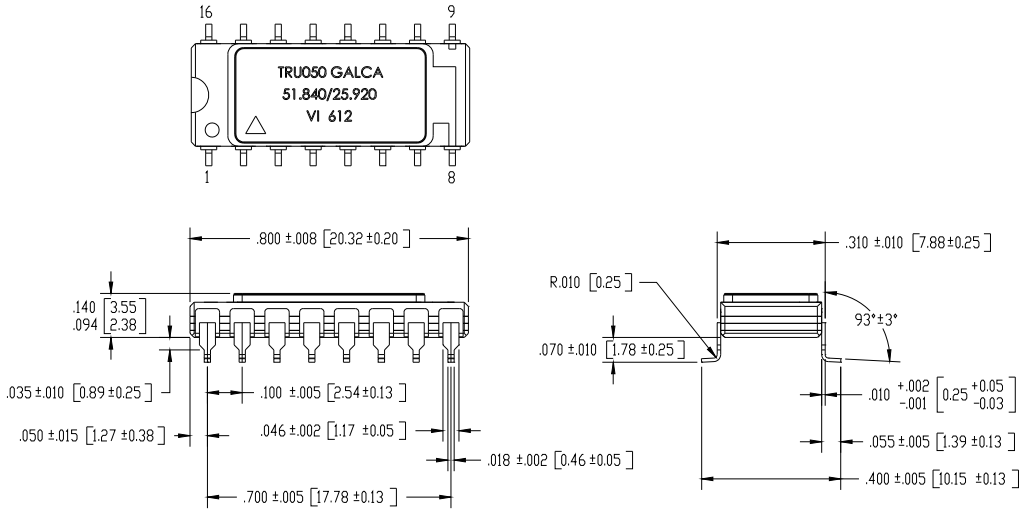


Figure 14. "Gull Wing Lead" Package

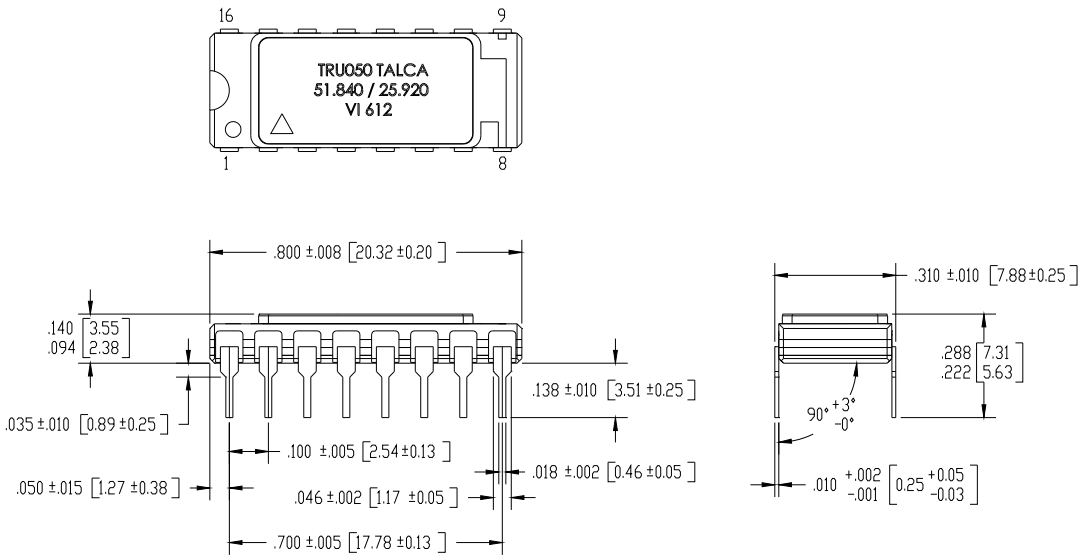


Figure 15. "Thru Hole Lead" Package

Table 7. Pin Functions

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	OPN	Op-Amp Negative Input
3	OPOUT	Op-Amp Output
4	OPP	Op-Amp Positive Input
5	LOSIN	INPUT (Used with LOS) Logic 0, VCXO control voltage is enabled. Logic 1, VCXO control voltage (pin 1) is disabled and OUT1 and OUT2 are within +/-75 ppm of center frequency Has Internal pull-down resistor
6	PHO	Phase detector output
7	DATAIN	Phase detector Input signal (TTL switching thresholds)
8	GND	Cover and Electrical Ground
9	CLKIN	Phase detector Clock signal (TTL switching thresholds)
10	LOS	OUTPUT (Used with LOSIN) Logic 1 if there are no transitions detected at DATAIN after 256 clock cycles at CLKIN. As soon as a transition occurs at DATAIN, LOS is set to logic low.
11	RCLK	Recovered Clock
12	RDATA	Recovered Data
13	Output 2	Divided-down VCXO Output, or No Output
14	HIZ	INPUT Logic 0, OUT1, OUT2, RCLK, RDATA are set to a high impedance state. Logic 1, OUT1, OUT2, RCLK, RDATA are active. Has Internal pull-up resistor
15	Output 1	VCXO Output
16	V_{DD}	Power Supply Voltage (3.3 V ±10% or 5.0 V ±10%)

Ordering information

Table 8. Standard OUT1 Frequencies

12.0000000	12.2880000	12.6240000	13.8240000	16.0000000	16.1280000	16.3840000	16.7770000	16.8960000	17.9200000
18.4320000	19.4400000	20.0000000	20.4800000	22.1184000	22.5790000	24.5760000	25.0000000	25.2480000	27.0000000
28.0000000	30.7200000	32.0000000	32.7680000	33.3300000	34.3680000	35.3280000	38.8800000	40.0000000	40.9600000
41.2416000	41.9430000	44.7360000	47.4570000	49.1520000	49.4080000	50.0000000	51.8400000	61.4400000	62.2080000
65.5360000									

** Other frequencies may be available upon request*

Table 9. Part Number Builder

TRU050 - G A L G A - xxMxxxxxxx

Lead Style

T: Thru hole

G: Gull Wing

Divide by

A=2

B=4

C=8

D=16

E=32

F=64

G=128

H=256

K=Disabled

Frequency (See Above)

1M00000000 – 65M5360000

Power Supply

A: 5.0V

B: 3.3 V

Absolute Pull Range

G: ±50

N: ±80

H: ±100

Temperature Range

C: 0 to 70 °C

L: -40 to 85 °C

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Tel: 1-88-VECTRON-1 • Fax: 1-888-FAX-VECTRON

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Revision History

Date	Approved	Description
26AUG2008	BW	Part number frequency format revised from xx.xxx MHz to xxMxxxxxxx.