TRF7964A Multiprotocol Fully Integrated 13.56-MHz RFID Reader and Writer IC

1 Device Overview

1.1 Features

- Completely Integrated Protocol Handling for ISO/IEC 15693, ISO/IEC 18000-3, ISO/IEC 14443 A and B, and FeliCa™
- Integrated State Machine for ISO/IEC 14443 A Anticollision (Broken Bytes) Operation
- Input Voltage Range: 2.7 VDC to 5.5 VDC
- Programmable Output Power: +20 dBm (100 mW), +23 dBm (200 mW)
- Programmable I/O Voltage Levels From 1.8 VDC to 5.5 VDC
- Programmable System Clock Frequency Output (RF, RF/2, RF/4) from 13.56-MHz or 27.12-MHz Crystal or Oscillator
- Integrated Voltage Regulator Output for Other System Components (MCU, Peripherals, Indicators), 20 mA (Max)
- Programmable Modulation Depth
- Dual Receiver Architecture With RSSI for Elimination of "Read Holes" and Adjacent Reader System or Ambient In-Band Noise Detection
- Programmable Power Modes for Ultra Low-Power System Design (Power Down <1 µA)
- Parallel or SPI Interface (With 127-Byte FIFO)
- Temperature Range: –40°C to 110°C
- 32-Pin QFN Package (5 mm × 5 mm)

1.2 Applications

- Public Transport or Event Ticketing
- Passport or Payment (POS) Reader Systems
- Product Identification or Authentication
- Medical Equipment or Consumables
- Access Control, Digital Door Locks

1.3 Description

The TRF7964A device is an integrated analog front end (AFE) and multiprotocol data-framing device for a 13.56-MHz NFC/RFID reader and writer system supporting ISO/IEC 14443 A and B, Sony FeliCa, and ISO/IEC 15693. Pin-to-pin and firmware compatible with the superset device TRF7970A. Built-in programming options make the device suitable for a wide range of applications for proximity and vicinity identification systems.

The device is configured by selecting the desired protocol in the control registers. Direct access to all control registers allows fine tuning of various reader parameters as needed.

The TRF7964A device supports data rates up to 848 kbps with all framing and synchronization tasks for the ISO protocols onboard. Other standards and even custom protocols can be implemented by using one of the direct modes the device offers. These direct modes let the user fully control the AFE and also gain access to the raw subcarrier data or the unframed, but already ISO-formatted, data and the associated (extracted) clock signal.

The receiver system has a dual-input receiver architecture to maximize communication robustness. The receivers also include various automatic and manual gain control options. The received signal strength from transponders, ambient sources, or internal levels is available in the RSSI register.

A SPI or parallel interface can be used for the communication between the MCU and the TRF7964A device. When the built-in hardware encoders and decoders are used, transmit and receive functions use a 127-byte FIFO register. For direct transmit or receive functions, the encoders or decoders can be bypassed so the MCU can process the data in real time.

The TRF7964A device supports a wide supply voltage range of 2.7 V to 5.5 V and data communication levels from 1.8 V to 5.5 V for the MCU I/O interface.

The transmitter has selectable output power levels of 100 mW (+20 dBm) or 200 mW (+23 dBm) equivalent into a 50-Ω load when using a 5-V supply and supports OOK and ASK modulation with selectable modulation depth.

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The built-in programmable auxiliary voltage regulator delivers up to 20 mA to supply an MCU and additional external circuits within the reader system.

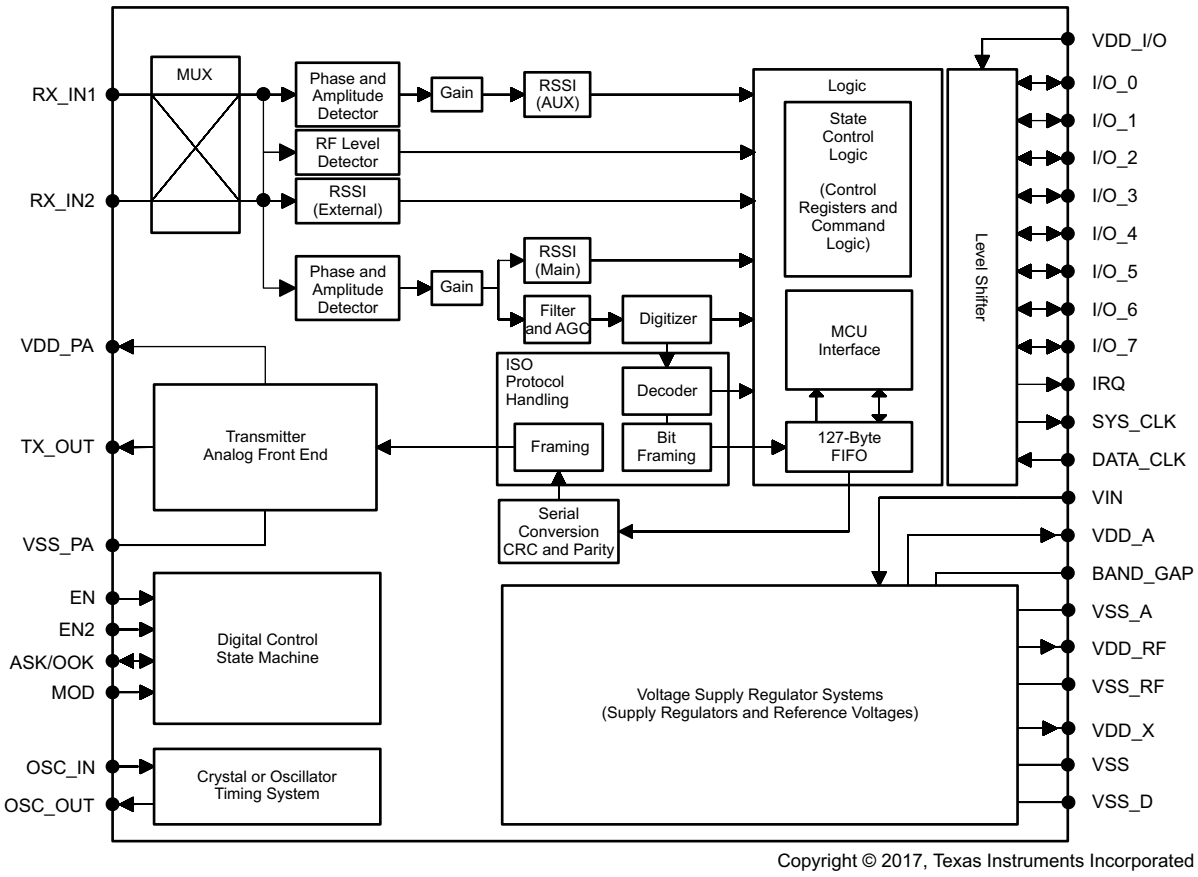
Start evaluating the TRF7964A multiprotocol transceiver IC with the DLP-7970ABP of the superset device.

Device Information

PART NUMBER	PACKAGE	BODY SIZE
TRF7964ARHB	VQFN (32)	5 mm × 5 mm

1.4 Functional Block Diagram

Figure 1-1 shows the block diagram.



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Figure 1-1. Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 28, 2017 to March 11, 2020	Page
• Removed links to obsolete EVMs in Section 1.3 *Description*	2
• Removed "(Optional)" from the step that begins "Write the Regulator and I/O Control register (0x0B)..." in Section 6.11 *TRF7964A Initialization*	45
• Updated linked documents in Section 7.4 *Reader Antenna Design Guidelines*	69
• Removed obsolete EVMs in Section 8.3 *Tools and Software*	71

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3 Device Characteristics

Table 3-1 lists the supported modes of operation for the TRF7964A device.

Table 3-1. Supported Protocols

SUPPORTED PROTOCOLS					
ISO/IEC 14443 A and B				ISO/IEC 15693, ISO/IEC 18000-3 (Mode 1)	FeliCa
106 kbps	212 kbps	424 kbps	848 kbps		212 kbps, 424 kbps
✓	✓	✓	✓	✓	✓

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI Wireless Connectivity Connect more with the industry's broadest wireless connectivity portfolio.

Products for NFC / RFID TI provides one of the industry's most differentiated NFC and RFID product portfolios and is your solution to meet a broad range of NFC connectivity and RFID identification needs.

Companion Products for TRF7964A Review products that are frequently purchased or used with this product.

Reference Designs for TRF7964A The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

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4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pinout for the 32-pin RHB package.

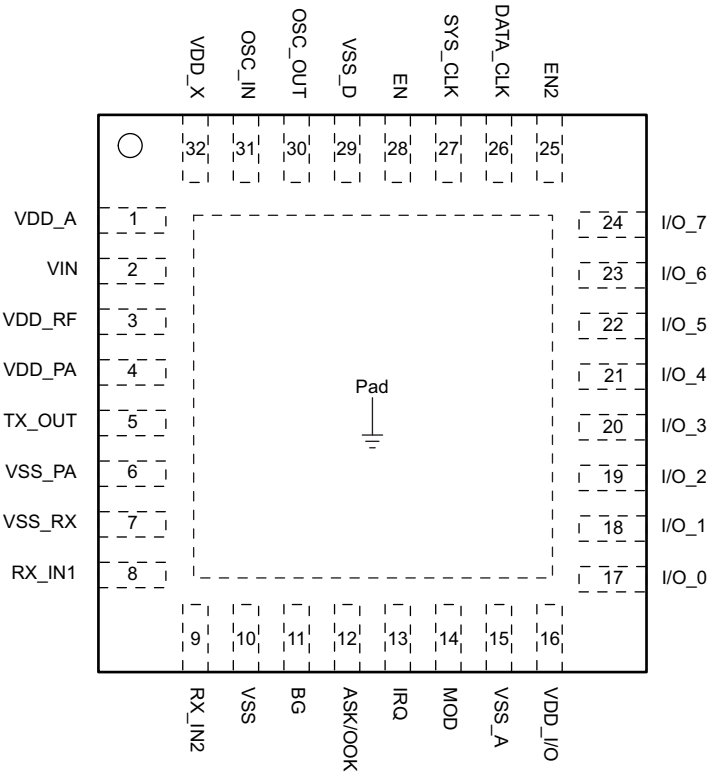


Figure 4-1. 32-Pin RHB Package (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals.

Table 4-1. Terminal Functions

TERMINAL		TYPE (1)	DESCRIPTION
NAME	NO.		
V_{DD_A}	1	OUT	Internal regulated supply (2.7 V to 3.4 V) for analog circuitry
V_{IN}	2	SUP	External supply input to chip (2.7 V to 5.5 V)
V_{DD_RF}	3	OUT	Internal regulated supply (2.7 V to 5 V), normally connected to V_{DD_PA} (pin 4)
V_{DD_PA}	4	INP	Supply for PA; normally connected externally to V_{DD_RF} (pin 3)
TX_OUT	5	OUT	RF output (selectable output power, 100 mW or 200 mW, with V_{DD} = 5 V)
V_{SS_PA}	6	SUP	Negative supply for PA; normally connected to circuit ground
V_{SS_RX}	7	SUP	Negative supply for RX inputs; normally connected to circuit ground
RX_IN1	8	INP	Main RX input
RX_IN2	9	INP	Auxiliary RX input
V_{SS}	10	SUP	Chip substrate ground
BAND_GAP	11	OUT	Bandgap voltage (V_{BG} = 1.6 V); internal analog voltage reference
ASK/OOK	12	BID	Selection between ASK and OOK modulation (0 = ASK, 1 = OOK) for direct mode 0 or 1. Can be configured as an output to provide the received analog signal output.

(1) SUP = Supply, INP = Input, BID = Bidirectional, OUT = Output

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Table 4-1. Terminal Functions (continued)

TERMINAL		TYPE (1)	DESCRIPTION
NAME	NO.		
IRQ	13	OUT	Interrupt request
MOD	14	INP	External data modulation input for direct mode 0 or 1
		OUT	Subcarrier digital data output (see registers 0x1A and 0x1B)
V_{SS_A}	15	SUP	Negative supply for internal analog circuits; connected to GND
$V_{DD_I/O}$	16	INP	Supply for I/O communications (1.8 V to V_{IN}) level shifter. V_{IN} should be never exceeded.
I/O_0	17	BID	I/O pin for parallel communication
I/O_1	18	BID	I/O pin for parallel communication
I/O_2	19	BID	I/O pin for parallel communication TX enable (in special direct mode)
I/O_3	20	BID	I/O pin for parallel communication TX data (in special direct mode)
I/O_4	21	BID	I/O pin for parallel communication Slave select signal in SPI mode
I/O_5	22	BID	I/O pin for parallel communication Data clock output in direct mode 1 and special direct mode
I/O_6	23	BID	I/O pin for parallel communication MISO for serial communication (SPI) Serial bit data output in direct mode 1 or subcarrier signal in direct mode 0
I/O_7	24	BID	I/O pin for parallel communication. MOSI for serial communication (SPI)
EN2	25	INP	Selection of power down mode. If EN2 is connected to V_{IN}, then V_{DD_X} is active during power down mode 2 (for example, to supply the MCU).
DATA_CLK	26	INP	Data clock input for MCU communication (parallel and serial)
SYS_CLK	27	OUT	If EN = 1 (EN2 = don't care) the system clock for MCU is configured. Depending on the crystal that is used, options are as follows (see register 0x09): 13.56-MHz crystal: Off, 3.39 MHz, 6.78 MHz, or 13.56 MHz 27.12-MHz crystal: Off, 6.78 MHz, 13.56 MHz, or 27.12 MHz If EN = 0 and EN2 = 1, then system clock is set to 60 kHz
EN	28	INP	Chip enable input (If EN = 0, then chip is in sleep or power-down mode).
V_{SS_D}	29	SUP	Negative supply for internal digital circuits
OSC_OUT	30	OUT	Crystal or oscillator output
OSC_IN	31	INP	Crystal or oscillator input
		OUT	Crystal oscillator output
V_{DD_X}	32	OUT	Internally regulated supply (2.7 V to 3.4 V) for digital circuit and external devices (for example, an MCU)
Thermal Pad	PAD	SUP	Chip substrate ground

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5 Specifications

5.1 Absolute Maximum Ratings(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		–0.3	6	V
I_{IN}	Maximum current V_{IN}			150	mA
T_J	Maximum operating virtual junction temperature	Any condition		140	°C
		Continuous operation, long-term reliability(3)		125	°C
T_{STG}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to substrate ground terminal V_{SS}.
(3) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability or lifetime of the device.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V
		Machine model (MM)	±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage		2.7	5	5.5	V
T_A	Operating ambient temperature		–40	25	110	°C
T_J	Operating virtual junction temperature		–40	25	125	°C
V_{IL}	Input voltage, logic low	I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2, ASK/OOK, MOD			0.2 × $V_{DD_I/O}$	V
V_{IH}	Input voltage threshold, logic high	I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2, ASK/OOK, MOD	0.8 × $V_{DD_I/O}$			V

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5.4 Electrical Characteristics

TYP operating conditions are T_A = 25°C, VIN = 5 V, full-power mode (unless otherwise noted)
MIN and MAX operating conditions are over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage			0.2 × $V_{DD_I/O}$		V
V_{OH}	High-level output voltage			0.8 × $V_{DD_I/O}$		V
I_{PD1}	Supply current in power down mode 1	All building blocks disabled, including supply-voltage regulators; measured after 500-ms settling time (EN = 0, EN2 = 0)		0.5	5	µA
I_{PD2}	Supply current in power down mode 2 (sleep mode)	The SYS_CLK generator and V_{DD_X} remain active to support external circuitry; measured after 100-ms settling time (EN = 0, EN2 = 1)		120	200	µA
I_{STBY}	Supply current in stand-by mode	Oscillator running, supply-voltage regulators in low-consumption mode (EN = 1, EN2 = x)		1.9	3.5	mA
I_{ON1}	Supply current without antenna driver current	Oscillator, regulators, RX and AGC active, TX is off		10.5	14	mA
I_{ON2}	Supply current, TX (half power)	Oscillator, regulators, RX and AGC and TX active, P_{OUT} = 100 mW		70	78	mA
I_{ON3}	Supply current, TX (full power)	Oscillator, regulators, RX and AGC and TX active, P_{OUT} = 200 mW		130	150	mA
V_{POR}	Power-on-reset voltage	Input voltage at V_{IN}	1.4	2	2.6	V
V_{BG}	Bandgap voltage (pin 11)	Internal analog reference voltage	1.5	1.6	1.7	V
V_{DD_A}	Regulated output voltage for analog circuitry (pin 1)	V_{IN} = 5 V	3.1	3.4	3.8	V
V_{DD_X}	Regulated supply for external circuitry	Output voltage pin 32, V_{IN} = 5 V	3.1	3.4	3.8	V
I_{VDD_Xmax}	Maximum output current of V_{DD_X}	Output current pin 32, V_{IN} = 5 V			20	mA
R_{RFOUT}	Antenna driver output resistance (1)	Half-power mode, V_{IN} = 2.7 V to 5.5 V		8	12	Ω
		Full-power mode, V_{IN} = 2.7 V to 5.5 V		4	6	
R_{RFIN}	RX_IN1 and RX_IN2 input resistance		4	10	20	kΩ
V_{RF_INmax}	Maximum RF input voltage at RX_IN1 and RX_IN2	V_{RF_INmax} should not exceed V_{IN}		3.5		V_{pp}
V_{RF_INmin}	Minimum RF input voltage at RX_IN1 and RX_IN2 (input sensitivity) (2)	$f_{SUBCARRIER}$ = 424 kHz		1.4	2.5	mV_{pp}
		$f_{SUBCARRIER}$ = 848 kHz		2.1	3	
f_{SYS_CLK}	SYS_CLK frequency	In power mode 2, EN = 0, EN2 = 1	25	60	120	kHz
f_C	Carrier frequency	Defined by external crystal		13.56		MHz
$t_{CRYSTAL}$	Crystal run-in time	Time until oscillator stable bit is set (register 0x0F) (3)		3		ms
f_{D_CLKmax}	Maximum DATA_CLK frequency (4)	Depends on capacitive load on the I/O lines, TI recommends 2 MHz (4)	2	4	10	MHz
R_{OUT}	Output resistance I/O_0 to I/O_7			500	800	Ω
R_{SYS_CLK}	Output resistance R_{SYS_CLK}			200	400	Ω

(1) Antenna driver output resistance
(2) Measured with subcarrier signal at RX_IN1 or RX_IN2 and measured the digital output at MOD pin with register 0x1A bit 6 = 1.
(3) Depends on the crystal parameters and components
(4) TI recommends a DATA_CLK speed of 2 MHz. Higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400 Ω (12-ns time constant when 30-pF load used).

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5.5 Thermal Resistance Characteristics

PACKAGE	θ_{JC}	θ_{JA} (1)	POWER RATING (2)	
			$T_A \le 25°C$	$T_A \le 85°C$
RHB (32 pin)	31°C/W	36.4°C/W	2.7 W	1.1 W

(1) This data was taken using the JEDEC standard high-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the temperature at which distortion starts to increase substantially. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

5.6 Switching Characteristics

TYP operating conditions are T_A = 25°C, VIN = 5 V, full-power mode (unless otherwise noted)
MIN and MAX operating conditions are over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LO/HI}$	DATA_CLK time high or low, one half of DATA_CLK at 50% duty cycle	Depends on capacitive load on the I/O lines (1)	250	62.5	50	ns
$t_{STE,LEAD}$	Slave select lead time, slave select low to clock			200		ns
$t_{STE,LAG}$	Slave select lag time, last clock to slave select high			200		ns
$t_{STE,DIS}$	Slave select disable time, slave select rising edge to next slave select falling edge		300			ns
$t_{SU,SI}$	MOSI input data setup time		15			ns
$t_{HD,SI}$	MOSI input data hold time		15			ns
$t_{SU,SO}$	MISO input data setup time		15			ns
$t_{HD,SO}$	MISO input data hold time		15			ns
$t_{VALID,SO}$	MISO output data valid time	DATA_CLK edge to MISO valid, $C_L \le 30$ pF	30	50	75	ns

(1) TI recommends a DATA_CLK speed of 2 MHz. Higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400 Ω (12-ns time constant when 30-pF load used).

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6 Detailed Description

6.1 Overview

6.1.1 RFID – Reader and Writer

The is a high-performance 13.56-MHz HF RFID transceiver IC composed of an integrated analog front end (AFE) and a built-in data framing engine for ISO/IEC 15693, ISO/IEC 14443 A and B, and FeliCa. This includes data rates up to 848 kbps for ISO/IEC 14443 with all framing and synchronization tasks on board (in default mode). This architecture lets the customer build a complete cost-effective yet high-performance multiprotocol 13.56-MHz RFID system together with a low-cost microcontroller.

Other standards and even custom protocols can be implemented by using either of the direct modes that the device offers. These direct modes (0 and 1) allow the user to fully control the analog front end (AFE) and also gain access to the raw subcarrier data or the unframed but already ISO formatted data and the associated (extracted) clock signal.

The receiver system has a dual input receiver architecture. The receivers also include various automatic and manual gain control options. The received input bandwidth can be selected to cover a broad range of input subcarrier signal options.

The received signal strength from transponders, ambient sources, or internal levels is available through the RSSI register. The receiver output is selectable among a digitized subcarrier signal and any of the integrated subcarrier decoders. The selected subcarrier decoder delivers the data bit stream and the data clock as outputs.

The TRF7964A also includes a receiver framing engine. This receiver framing engine performs the CRC or parity check, removes the EOF and SOF settings, and organizes the data in bytes for ISO/IEC 14443 A and B, ISO/IEC 15693, and FeliCa protocols. Framed data is then accessible to the microcontroller (MCU) through a 127-byte FIFO register.

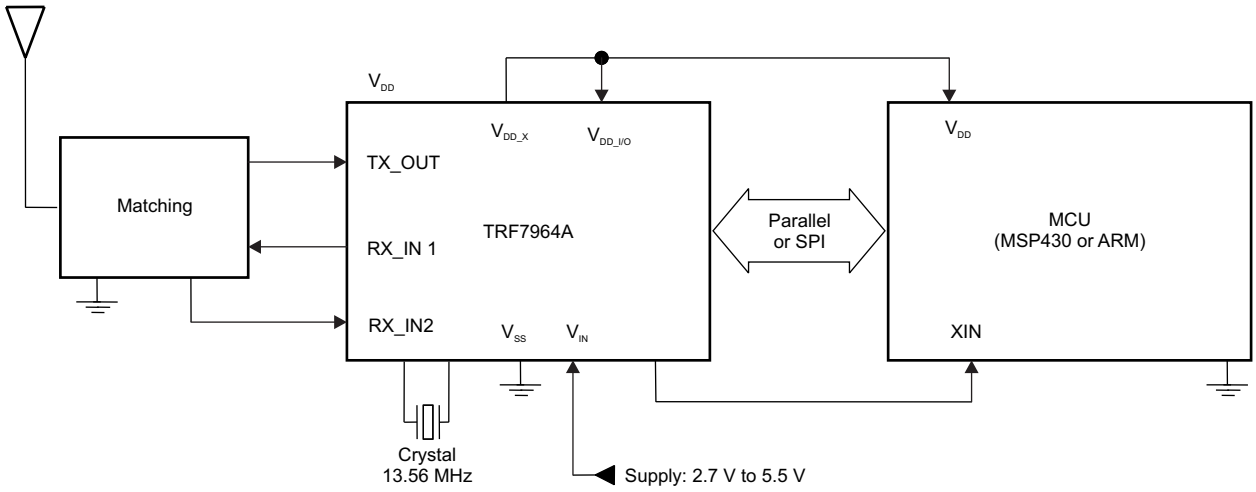


Figure 6-1. Application Block Diagram

A parallel or serial interface (SPI) can be used for the communication between the MCU and the TRF7964A reader. When the built-in hardware encoders and decoders are used, transmit and receive functions use a 127-byte FIFO register. For direct transmit or receive functions, the encoders and decoders can be bypassed so that the MCU can process the data in real time. The TRF7964A supports data communication voltage levels from 1.8 V to 5.5 V for the MCU I/O interface. The transmitter has selectable output-power levels of 100 mW (+20 dBm) or 200 mW (+23 dBm) equivalent into a 50-Ω load when using a 5-V supply.

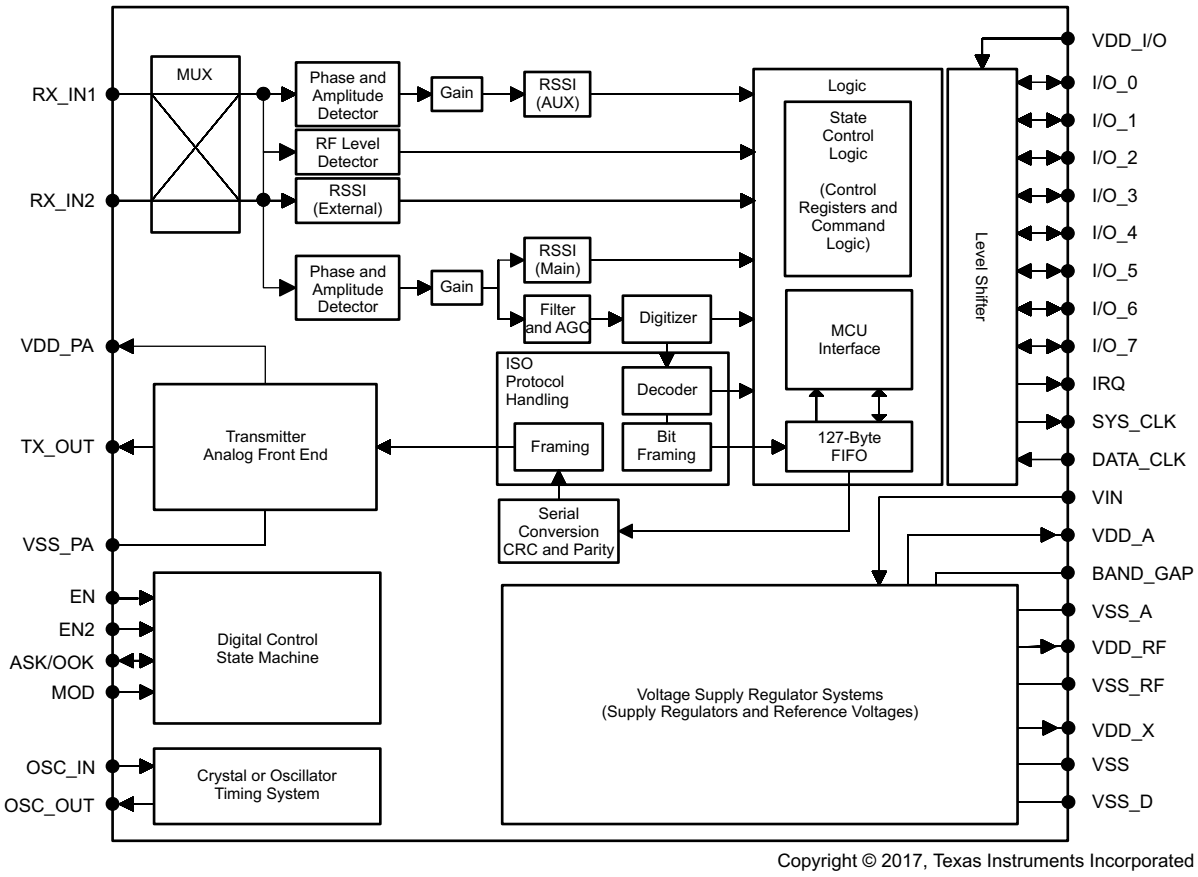
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The transmitter supports OOK and ASK modulation with selectable modulation depth. The TRF7964A also includes a data transmission engine that comprises low-level encoding for ISO/IEC 15693, ISO/IEC 14443 A and B, and FeliCa. Included with the transmit data coding is the automatic generation of Start Of Frame (SOF), End Of Frame (EOF), Cyclic Redundancy Check (CRC), and parity bits.

Several integrated voltage regulators ensure a proper power-supply noise rejection for the complete reader system. The built-in programmable auxiliary voltage regulator V_{DD_X} (pin 32), is able to deliver up to 20 mA to supply a microcontroller and additional external circuits within the reader system.

6.2 System Block Diagram

Figure 6-2 shows a block diagram of the TRF7964A.



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Figure 6-2. System Block Diagram

6.3 Power Supplies

The TRF7964A positive supply input V_{IN} (pin 2) sources three internal regulators with output voltages V_{DD_RF}, V_{DD_A} and V_{DD_X}. All regulators use external bypass capacitors for supply noise filtering and must be connected as indicated in reference schematics. These regulators provide a high power supply reject ratio (PSRR) as required for RFID reader systems. All regulators are supplied by V_{IN} (pin 2).

The regulators are not independent and have common control bits in register 0x0B for output voltage setting. The regulators can be configured to operate in either automatic or manual mode (register 0x0B, bit 7). The automatic regulator setting mode ensures an optimal compromise between PSRR and the highest possible supply voltage for RF output (to ensure maximum RF power output). The manual mode allows the user to manually configure the regulator settings. For applications in which the TRF7964A may be subjected to external noise, manually reducing the regulator settings can improve RF performance.

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6.3.1 Supply Arrangements

Regulator Supply Input: V_{IN}

The positive supply at V_{IN} (pin 2) has an input voltage range of 2.7 V to 5.5 V. V_{IN} provides the supply input sources for three internal regulators with the output voltages V_{DD_RF}, V_{DD_A}, and V_{DD_X}. External bypass capacitors for supply noise filtering must be used (per reference schematics).

NOTE

V_{IN} must be the highest voltage supplied to the TRF7964A.

RF Power Amplifier Regulator: V_{DD_RF}

The V_{DD_RF} (pin 3) regulator is supplying the RF power amplifier. The voltage regulator can be set for either 5-V or 3-V operation. External bypass capacitors for supply noise filtering must be used (per reference schematics). When configured for 5-V manual-operation, the V_{DD_RF} output voltage can be set from 4.3 V to 5 V in 100-mV steps. In 3-V manual-operation, the output can be programmed from 2.7 V to 3.4 V in 100-mV steps. The maximum output current capability for 5-V operation is 150 mA and for 3-V operation is 100 mA.

Analog Supply Regulator: V_{DD_A}

Regulator V_{DD_A} (pin 1) supplies the analog circuits of the device. The output voltage setting depends on the input voltage and can be set for 5-V and 3-V operation. When configured for 5-V manual-operation, the output voltage is fixed at 3.4 V. External bypass capacitors for supply noise filtering must be used (per reference schematics). When configured for 3-V manual-operation, the V_{DD_A} output can be set from 2.7 V to 3.4 V in 100-mV steps (see Table 6-2).

NOTE

The configuration of V_{DD_A} and V_{DD_X} regulators are not independent from each other. The V_{DD_X} output current should not exceed 20 mA.

Digital Supply Regulator: V_{DD_X}

The digital supply regulator V_{DD_X} (pin 32) provides the power for the internal digital building blocks and can also be used to supply external electronics within the reader system. When configured for 3-V operation, the output voltage can be set from 2.7 to 3.4 V in 100-mV steps. External bypass capacitors for supply noise filtering must be used (per reference schematics).

NOTE

The configuration of the V_{DD_A} and V_{DD_X} regulators are not independent from each other. The V_{DD_X} output current should not exceed 20 mA.

By default, the regulators are set in automatic regulator setting mode. In this mode, the regulators are automatically set every time the system is activated by setting EN input High or each time the automatic regulator setting bit, B7 in register 0x0B is set to a 1. The action is started on the 0 to 1 transition. This means that, if the user wants to rerun the automatic setting from a state in which the automatic setting bit is already high, the automatic setting bit (B7 in register 0x0B) should be changed: 1-0-1.

By default, the regulator setting algorithm sets the regulator outputs to a "Delta Voltage" of 400 mV below V_{IN}, but not higher than 5 V for V_{DD_RF} and 3.4 V for V_{DD_A} and V_{DD_A}.

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Power Amplifier Supply: V_{DD_PA}

The power amplifier of the TRF7964A is supplied through V_{DD_PA} (pin 4). The positive supply pin for the RF power amplifier is externally connected to the regulator output V_{DD_RF} (pin 3).

I/O Level Shifter Supply: $V_{DD_I/O}$

The TRF7964A has a separate supply input $V_{DD_I/O}$ (pin 16) for the built-in I/O level shifter. The supported input voltage ranges from 1.8 V to V_{IN}, not exceeding 5.5 V. Pin 16 is used to supply the I/O interface pins (I/O_0 to I/O_7), IRQ, SYS_CLK, and DATA_CLK pins of the reader. In typical applications, $V_{DD_I/O}$ is directly connected to V_{DD_X}, while V_{DD_X} also supplies the MCU. This ensures that the I/O signal levels of the MCU match the logic levels of the TRF7964A.

Negative Supply Connections: V_{SS}, V_{SS_TX}, V_{SS_RX}, V_{SS_A}, V_{SS_PA}

The negative supply connections V_{SS_X} of each functional block are all externally connected to GND.

The substrate connection is V_{SS} (pin 10), the analog negative supply is V_{SS_A} (pin 15), the logic negative supply is V_{SS_D} (pin 29), the RF output stage negative supply is V_{SS_PA} (pin 6), and the negative supply for the RF receiver V_{SS_RX} (pin 7).

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6.3.2 Supply Regulator Settings

The input supply voltage mode of the reader needs to be selected. This is done in the Chip Status Control register (0x00). Bit 0 in register 0x00 selects between 5-V or 3-V input supply voltage. The default configuration is 5 V, which reflects an operating supply voltage range of 4.3 V to 5.5 V. If the supply voltage is below 4.3 V, the 3-V configuration should be used.

As V_{DD_RF} is increased, the system can become more susceptible to noise coupling on the RX lines. For minimum noise coupling, TI recommends using the value of 0x00. For improved range, higher V_{DD_RF} voltages may be set, but complete system testing is required to determine the value which provides optimal performance.

The various regulators can be configured to operate in automatic or manual mode. This is done in the Regulator and I/O Control register (0x0B), as shown in Table 6-1 and Table 6-2.

Table 6-1. Supply Regulator Setting: 5-V System

REGISTER ADDRESS (hex)	OPTION BITS SETTING IN REGULATOR CONTROL REGISTER (1)								COMMENTS
	B7	B6	B5	B4	B3	B2	B1	B0	
Automatic Mode (default)									
0B	1	x	x	x	x	x	0	0	Automatic regulator setting 400-mV difference
Manual Mode									
0B	0	x	x	x	x	1	1	1	V_{DD_RF} = 5 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	1	0	V_{DD_RF} = 4.9 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	0	1	V_{DD_RF} = 4.8 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	0	0	V_{DD_RF} = 4.7 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	1	1	V_{DD_RF} = 4.6 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	1	0	V_{DD_RF} = 4.5 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	0	1	V_{DD_RF} = 4.4 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	0	0	V_{DD_RF} = 4.3 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V

(1) x = Don't care

Table 6-2. Supply Regulator Setting: 3-V System

REGISTER ADDRESS (hex)	OPTION BITS SETTING IN REGULATOR CONTROL REGISTER (1)								COMMENTS
	B7	B6	B5	B4	B3	B2	B1	B0	
Automatic Mode (default)									
0B	1	x	x	x	x	x	0	0	Automatic regulator setting 400-mV difference
Manual Mode									
0B	0	x	x	x	x	1	1	1	V_{DD_RF} = 3.4 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	1	0	V_{DD_RF} = 3.3 V, V_{DD_A} = 3.3 V, V_{DD_X} = 3.3 V
0B	0	x	x	x	x	1	0	1	V_{DD_RF} = 3.2 V, V_{DD_A} = 3.2 V, V_{DD_X} = 3.2 V
0B	0	x	x	x	x	1	0	0	V_{DD_RF} = 3.1 V, V_{DD_A} = 3.1 V, V_{DD_X} = 3.1 V
0B	0	x	x	x	x	0	1	1	V_{DD_RF} = 3.0 V, V_{DD_A} = 3.0 V, V_{DD_X} = 3.0 V
0B	0	x	x	x	x	0	1	0	V_{DD_RF} = 2.9 V, V_{DD_A} = 2.9 V, V_{DD_X} = 2.9 V
0B	0	x	x	x	x	0	0	1	V_{DD_RF} = 2.8 V, V_{DD_A} = 2.8 V, V_{DD_X} = 2.8 V
0B	0	x	x	x	x	0	0	0	V_{DD_RF} = 2.7 V, V_{DD_A} = 2.7 V, V_{DD_X} = 2.7 V

(1) x = Don't care

The regulator configuration function adjusts the regulator outputs by default to 400 mV below V_{IN} level, but not higher than 5 V for V_{DD_RF}, 3.4 V for V_{DD_A} and V_{DD_X}. This ensures the highest possible supply voltage for the RF output stage while maintaining an adequate PSRR (power supply rejection ratio).

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6.3.3 Power Modes

The chip has several power states, which are controlled by two input pins (EN and EN2) and several bits in the chip status control register (0x00) (see Table 6-3 and Table 6-4).

Table 6-3. 3.3-V Operation Power Modes(1)

MODE	EN2	EN	CHIP STATUS CONTROL REGISTER (0x00)	REGULATOR CONTROL REGISTER (0x0B)	TRANSMITTER	RECEIVER	SYS_CLK (13.56 MHz)	SYS_CLK (60 kHz)	V_{DD_X}	TYPICAL CURRENT (mA)	TYPICAL POWER OUT (dBm)
Power down	0	0	XX	XX	OFF	OFF	OFF	OFF	OFF	<0.001	-
Sleep mode	1	0	XX	XX	OFF	OFF	OFF	ON	ON	0.120	-
Standby mode at +3.3 VDC	X	1	80	00	OFF	OFF	ON	X	ON	2	-
Mode 1 at +3.3 VDC	X	1	00	00	OFF	OFF	ON	X	ON	3	-
Mode 2 at +3.3 VDC	X	1	02	00	OFF	ON	ON	X	ON	9	-
Mode 3 (half power) at +3.3 VDC	X	1	30	07	ON	ON	ON	X	ON	53	14.5
Mode 4 (full power) at +3.3 VDC	X	1	20	07	ON	ON	ON	X	ON	67	17

(1) X = Don't care

Table 6-4. 5-V Operation Power Modes(1)

MODE	EN2	EN	CHIP STATUS CONTROL REGISTER (0x00)	REGULATOR CONTROL REGISTER (0x0B)	TRANSMITTER	RECEIVER	SYS_CLK (13.56 MHz)	SYS_CLK (60 kHz)	V_{DD_X}	TYPICAL CURRENT (mA)	TYPICAL POWER OUT (dBm)
Power down	0	0	XX	XX	OFF	OFF	OFF	OFF	OFF	<0.001	-
Sleep mode	1	0	XX	XX	OFF	OFF	OFF	ON	ON	0.120	-
Standby mode at +5 VDC	X	1	81	07	OFF	OFF	ON	X	ON	3	-
Mode 1 at +5 VDC	X	1	01	07	OFF	OFF	ON	X	ON	5	-
Mode 2 at +5 VDC	X	1	03	07	OFF	ON	ON	X	ON	10.5	-
Mode 3 (half power) at +5 VDC	X	1	31	07	ON	ON	ON	X	ON	70	20
Mode 4 (full power) at +5 VDC	X	1	21	07	ON	ON	ON	X	ON	130	23

(1) X = Don't care

Table 6-3 and Table 6-4 show the configuration for the different power modes when using a 3.3-V or 5-V system supply, respectively. The main reader enable signal is pin EN. When EN is set high, all of the reader regulators are enabled, the 13.56-MHz oscillator is running and the SYS_CLK (output clock for external microcontroller) is also available.

The input pin EN2 has two functions:

- A direct connection from EN2 to V_{IN} to ensure the availability of the regulated supply V_{DD_X} and an auxiliary clock signal (60 kHz, SYS_CLK) for an external MCU. This mode (EN = 0, EN2 = 1) is intended for systems in which the MCU is also being supplied by the reader supply regulator (V_{DD_X}) and the MCU clock is supplied by the SYS_CLK output of the reader. This allows the MCU supply and clock to be available during sleep mode.
- EN2 enables the start-up of the reader system from complete power down (EN = 0, EN2 = 0). In this case the EN input is being controlled by the MCU (or other system device) that is without supply voltage during complete power down (thus unable to control the EN input). A rising edge applied to the EN2 input (which has an approximately 1-V threshold level) starts the reader supply system and 13.56-MHz oscillator (identical to condition EN = 1).

When user MCU is controlling EN and EN2, a delay of 1 ms between EN and EN2 must be used. If the MCU controls only EN, TI recommends connecting EN2 to either V_{IN} or GND, depending on the application MCU requirements for V_{DD_X} and SYS_CLK.

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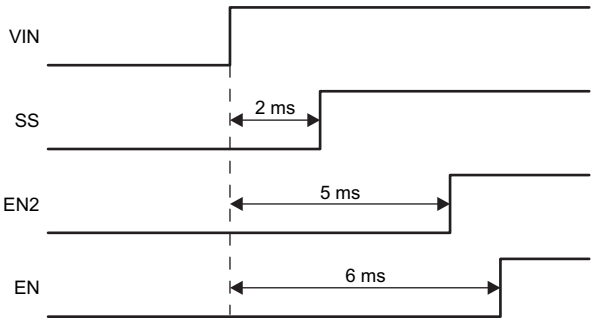


Figure 6-3. Nominal Start-up Sequence Using SPI With SS (MCU Controls EN2)

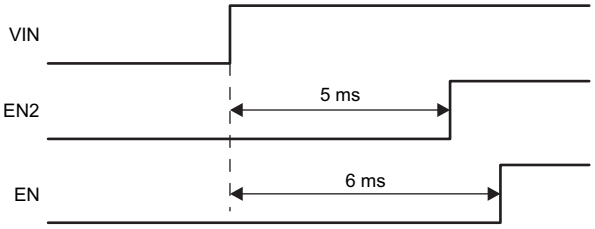


Figure 6-4. Nominal Start-up Sequence Using Parallel (MCU Controls EN2)

This start-up mode lasts until all of the regulators have settled and the 13.56-MHz oscillator has stabilized. If the EN input is set high (EN = 1) by the MCU (or other system device), the reader stays active. If the EN input is not set high (EN = 0) within 100 µs after the SYS_CLK output is switched from auxiliary clock (60 kHz) to high-frequency clock (derived from the crystal oscillator), the reader system returns to complete Power-Down Mode 1. This option can be used to wake-up the reader system from complete Power Down (PD Mode 1) by using a pushbutton switch or by sending a single pulse.

After the reader EN line is high, the other power modes are selected by control bits within the chip status control register (0x00). The power mode options and states are listed in Table 6-3.

When EN is set high (or on rising edge of EN2 and then confirmed by EN = 1) the supply regulators are activated and the 13.56-MHz oscillator is started. When the supplies are settled and the oscillator frequency is stable, the SYS_CLK output is switched from the auxiliary frequency of 60 kHz to the 13.56-MHz frequency derived from the crystal oscillator. At this point, the reader is ready to communicate and perform the required tasks. When this occurs, osc_ok (B6) of the RSSI Level and Oscillator Status register is set. The MCU can then program the Chip Status Control register 0x00 and select the operation mode by programming the additional registers.

- Standby Mode (bit 7 = 1 of register 0x00), the reader is capable of recovering to full operation in 100 µs.
- Mode 1 (active mode with RF output disabled, bit 5 = 0 and bit 1 = 0 of register 0x00) is a low power mode which allows the reader to recover to full operation within 25 µs.
- Mode 2 (active mode with only the RF receiver active, bit 1 = 1 of register 0x00) can be used to measure the external RF field (as described in RSSI measurements paragraph) if reader-to-reader anticollision is implemented.
- Modes 3 and 4 (active modes with the entire RF section active, bit 5 = 1 of register 0x00) are the normal modes used for normal transmit and receive operations.

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6.4 Receiver – Analog Section

6.4.1 Main and Auxiliary Receivers

The TRF7964A has two receiver inputs: RX_IN1 (pin 8) and RX_IN2 (pin 9). Each of the input is connected to an external capacitive voltage divider to ensure that the modulated signal from the tag is available on at least one of the two inputs. This architecture eliminates any possible communication holes that may occur from the tag to the reader.

The two RX inputs (RX_IN1 and RX_IN2) are multiplexed into two receivers - the main receiver and the auxiliary receiver. Only the main receiver is used for reception, the auxiliary receiver is used for signal quality monitoring. Receiver input multiplexing is controlled by bit B3 in the Chip Status Control register (address 0x00).

After start-up, RX_IN1 is multiplexed to the main receiver which is composed of an RF envelope detection, first gain and band-pass filtering stage, second gain and filtering stage with AGC. Only the main receiver is connected to the digitizing stage which output is connected to the digital processing block. The main receiver also has an RSSI measuring stage, which measures the strength of the demodulated signal (subcarrier signal).

The primary function of the auxiliary receiver is to monitor the RX signal quality by measuring the RSSI of the demodulated subcarrier signal (internal RSSI). After start-up, RX_IN2 is multiplexed to the auxiliary receiver. The auxiliary receiver has an RF envelope detection stage, first gain and filtering with AGC stage and finally the auxiliary RSSI block.

The default MUX setting is RX_IN1 connected to the main receiver and RX_IN2 connected to the auxiliary receiver. To determine the signal quality, the response from the tag is detected by the "main" (pin RX_IN1) and "auxiliary" (pin RX_IN2) RSSI. Both values measured and stored in the RSSI Levels and Oscillator Status register (address 0x0F). The MCU can read the RSSI values from the TRF7964A RSSI register and make the decision if swapping the input- signals is preferable or not. Setting B3 in Chip Status Control register (address 0x00) to 1 connects RX_IN1 (pin 8) to the auxiliary received and RX_IN2 (pin 9) to the main receiver.

The main and auxiliary receiver input stages are RF envelope detectors. The RF amplitude at RX_IN1 and RX_IN2 should be approximately 3 VPP for a V_{IN}supply level greater than 3.3 V. If the V_{IN} level is lower, the RF input peak-to-peak voltage level should not exceed the V_{IN}level.

6.4.2 Receiver Gain and Filter Stages

The first gain and filtering stage has a nominal gain of 15 dB with an adjustable band-pass filter. The band-pass filter has programmable 3-dB corner frequencies between 110 kHz to 450 kHz for the high-pass filter and 570 kHz to 1500 kHz for the low-pass filter. After the band-pass filter, there is another gain-and-filtering stage with a nominal gain of 8 dB and with frequency characteristics identical to the first band-pass stage.

The internal filters are configured automatically depending on the selected ISO communication standard in the ISO Control register (address 0x01). If required, additional fine tuning can be done by writing directly to the RX Special Setting registers (address 0x0A).

Table 6-5 shows the various settings for the receiver analog section. Setting B4, B5, B6, and B7 to 0 results in a band-pass characteristic of 240 kHz to 1.4 MHz, which is appropriate for ISO/IEC 14443 B 106 kbps, ISO/IEC 14443 A and B data rates of 212 kbps and 424 kbps, and FeliCa 424 kbps.

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Table 6-5. RX Special Setting Register (0x0A)

Function: Sets the gains and filters directly			
Default: 0x40 at POR = H or EN = L, and at each write to the ISO Control register (0x01). When bits B7, B6, B5 and B4 are all zero, the filters are set for ISO/IEC 14443 B (240 kHz to 1.4 MHz).			
Bit	**Name**	**Function**	**Description**
B7	C212	Band-pass 110 kHz to 570 kHz	Appropriate for 212-kHz subcarrier system (FeliCa)
B6	C424	Band-pass 200 kHz to 900 kHz	Appropriate for 424-kHz subcarrier used in ISO/IEC 15693
B5	M848	Band-pass 450 kHz to 1.5 MHz	Appropriate for Manchester-coded 848-kHz subcarrier used in ISO/IEC 14443 A and B
B4	hbt	Band-pass 100 kHz to 1.5 MHz Gain reduced for 18 dB	Appropriate for highest bit rate (848 kbps) used in high-bit-rate ISO/IEC 14443
B3	gd1	00 = Gain reduction 0 dB 01 = Gain reduction for 5 dB 10 = Gain reduction for 10 dB 11 = Gain reduction for 15 dB	Sets the RX gain reduction and reduces sensitivity
B2	gd2		
B1	Reserved		
B0	Reserved		

6.5 Receiver – Digital Section

The output of the TRF7964A analog receiver block is a digitized subcarrier signal and is the input to the digital receiver block, which consists of two sections that partly overlap. The digitized subcarrier signal is a digital representation of the modulation signal on the RF envelope. The two sections of the digital receiver block are the *protocol bit decoder* section and the *framing logic* section.

The protocol bit decoder section converts the subcarrier coded signal into a serial bit stream and a data clock. The decoder logic is designed for maximum error tolerance. This tolerance lets the decoder section successfully decode even partly corrupted subcarrier signals that would otherwise be lost due to noise or interference.

The framing logic section formats the serial bit stream data from the protocol bit decoder stage into data bytes. During the formatting process, special signals such as the start of frame (SOF), end of frame (EOF), start of communication, and end of communication are automatically removed. The parity bits and CRC bytes are also checked and removed. The end result is "clean or raw" data that is sent to the 127-byte FIFO register where it can be read by the external microcontroller system. Providing the data this way, in conjunction with the timing register settings of the TRF7964A, means that the firmware developer does not need to know the finer details of the ISO protocols to create a very robust application, especially in low-cost platforms in which code space is at a premium and high performance is still required.

The start of the receive operation (successfully received SOF) sets the IRQ flags in the IRQ Status register (0x0C). The end of the receive operation is signaled to the external system MCU by setting pin 13 (IRQ) to high. When data is received in the FIFO, an interrupt is sent to the MCU to signal that there is data to be read from the FIFO. The FIFO Status register (0x1C) should be used to provide the number of bytes that should be clocked out during the actual FIFO read. Additionally, an interrupt is sent to the MCU when the received data occupies 75% of the FIFO capacity to signal that the data should be removed from the FIFO. By default, that interrupt is triggered once the received data packet is longer than 124 bytes. This setting can be modified in the Adjustable FIFO IRQ Levels register (0x14).

Any error in the data format, parity, or CRC is detected and notified to the external system by setting pin 13 (IRQ) to high. The source condition of the interrupt is available in the IRQ Status register (0x0C). Section 6.14.3.3.1 describes the bit coding description of this register.

The framing section also supports bit-collision detection as specified in ISO/IEC 14443 A and ISO/IEC 15693. When a bit collision is detected, an interrupt request is sent and a flag is set in the IRQ Status register (0x0C). For ISO/IEC 14443 A specifically, the position of the bit collision is written in two registers: partly in the Collision Position register (0x0E) and partly in the Collision Position and Interrupt Mask register (0x0D) (bits B6 and B7).

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This collision position is presented as sequential bit number, where the count starts immediately after the start bit. This means a collision in the first bit of a UID would give the value 00 0001 0000 in these registers when their contents are combined after being read (the count starts with 0 and the first 16 bits are the command code and the number of valid bits [NVB] byte).

The receive section also contains two timers.

The RX wait time timer is controlled by the value in the RX Wait Time register (0x08). This timer defines the time interval after the end of the transmit operation during which the receive decoders are not active (held in reset state). This prevents false detections resulting from transients following the transmit operation. The value of the RX Wait Time register (0x08) defines the time in increments of 9.44 µs. This register is preset at every write to the ISO Control register (0x01) according to the minimum tag response time defined by each standard.

The RX no response timer is controlled by the RX No Response Wait Time register (0x07). This timer measures the time from the start of the slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in the IRQ Status register (0x0C). This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76 µs. This register is also preset automatically for every new protocol selection.

The main register controlling the digital part of the receiver is the ISO Control register (0x01). By writing to this register, the user selects the protocol to be used. With each new write in this register, all related registers are preset to their defaults for the protocol, so no further adjustments in other registers are needed for proper operation. Table 6-6 describes the bit fields of the ISO Control register (0x01).

NOTE

If changes to other registers are needed to fine-tune the system, those changes must be made after setting the ISO Control register (0x01).

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Table 6-6. Coding of the ISO Control Register

BIT	SIGNAL NAME	FUNCTION	COMMENTS
B7	rx_crc_n	Receiving without CRC	1 = No RX CRC 0 = RX CRC
B6	dir_mode	Direct mode type	0 = Output is subcarrier data 1 = Output is bit stream and clock from decoder selected by ISO bits
B5	rfid	RFID mode	0 = RFID reader mode 1 = Reserved (should be set to 0)
B4	iso_4	RFID	See Table 6-7 for B0:B4 settings based on ISO protocol used by application.
B3	iso_3	RFID	See Table 6-7 for B0:B4 settings based on ISO protocol used by application.
B2	iso_2	RFID	See Table 6-7 for B0:B4 settings based on ISO protocol used by application.
B1	iso_1	RFID	See Table 6-7 for B0:B4 settings based on ISO protocol used by application.
B0	iso_0	RFID	See Table 6-7 for B0:B4 settings based on ISO protocol used by application.

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Table 6-7. Coding of the ISO Control Register For RFID Mode (B5 = 0)

Iso_4	Iso_3	Iso_2	Iso_1	Iso_0	PROTOCOL	REMARKS
0	0	0	0	0	ISO/IEC 15693 low bit rate, one subcarrier, 1 out of 4	
0	0	0	0	1	ISO/IEC 15693 low bit rate, one subcarrier, 1 out of 256	
0	0	0	1	0	ISO/IEC 15693 high bit rate, one subcarrier, 1 out of 4	Default for RFID IC
0	0	0	1	1	ISO/IEC 15693 high bit rate, one subcarrier, 1 out of 256	
0	0	1	0	0	ISO/IEC 15693 low bit rate, double subcarrier, 1 out of 4	
0	0	1	0	1	ISO/IEC 15693 low bit rate, double subcarrier, 1 out of 256	
0	0	1	1	0	ISO/IEC 15693 high bit rate, double subcarrier, 1 out of 4	
0	0	1	1	1	ISO/IEC 15693 high bit rate, double subcarrier, 1 out of 256	
0	1	0	0	0	ISO/IEC 14443 A, bit rate 106 kbps	
0	1	0	0	1	ISO/IEC 14443 A high bit rate 212 kbps	RX bit rate when TX rate different from RX rate (see register 0x03)
0	1	0	1	0	ISO/IEC 14443 A high bit rate 424 kbps	
0	1	0	1	1	ISO/IEC 14443 A high bit rate 848 kbps	
0	1	1	0	0	ISO/IEC 14443 B, bit rate 106 kbps	
0	1	1	0	1	ISO/IEC 14443 B high bit rate 212 kbps	RX bit rate when TX rate different from RX rate (see register 0x03)
0	1	1	1	0	ISO/IEC 14443 B high bit rate 424 kbps	
0	1	1	1	1	ISO/IEC 14443 B high bit rate 848 kbps	
1	0	0	1	1	Reserved	
1	0	1	0	0	Reserved	
1	1	0	1	0	FeliCa 212 kbps	
1	1	0	1	1	FeliCa 424 kbps	

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6.5.1 Received Signal Strength Indicator (RSSI)

The TRF7964A incorporates in total three independent RSSI building blocks: Internal Main RSSI, Internal Auxiliary RSSI, and External RSSI. The internal RSSI blocks measure the amplitude of the subcarrier signal, and the external RSSI block measures the amplitude of the RF carrier signal at the receiver input.

6.5.1.1 Internal RSSI – Main and Auxiliary Receivers

Each receiver path has its own RSSI block to measure the envelope of the demodulated RF signal (subcarrier). Internal Main RSSI and Internal Auxiliary RSSI are identical however connected to different RF input pins. The Internal RSSI is intended for diagnostic purposes to set the correct RX path conditions.

The internal RSSI values can be used to adjust the RX gain settings or determine which RX path (main or auxiliary) provides the greater amplitude and, hence, to determine if the MUX may need to be reprogrammed to swap the RX input signal. The measuring system latches the peak value, so the RSSI level can be read after the end of each receive packet. The RSSI register values are reset with every transmission (TX) by the reader. This ensures an updated RSSI measurement for each new tag response.

The Internal RSSI has 7 steps (3 bit) with a typical increment of approximately 4 dB. The operating range is between 600 mV_{PP} and 4.2 V_{PP} with a typical step size of approximately 600 mV. Both Internal Main and Internal Auxiliary RSSI values are stored in the RSSI Levels and Oscillator Status register (0x0F). The nominal relationship between the input RF peak level and the RSSI value is shown in Figure 6-5.

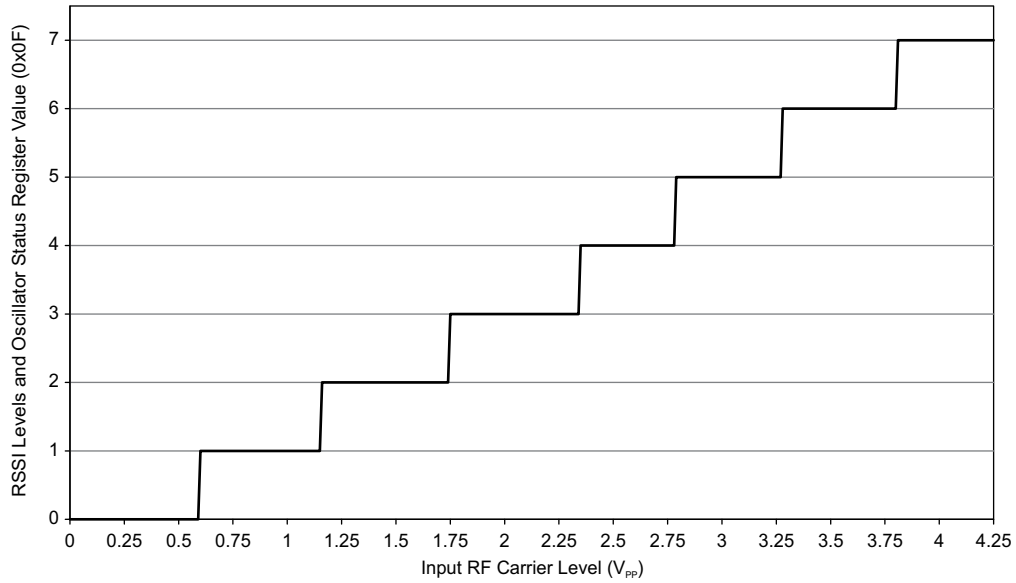


Figure 6-5. Digital Internal RSSI (Main and Auxiliary) Value vs RF Input Level in V_{PP} (V)

This RSSI measurement is done during the communication to the Tag; this means the TX must be on. Bit 1 in the Chip Status Control register (0x00) defines if Internal RSSI or the External RSSI value is stored in the RSSI Levels and Oscillator Status register (0x0F). Direct command 0x18 is used to trigger an Internal RSSI measurement.

6.5.1.2 External RSSI

The external RSSI is mainly used to check for any external 13.56-MHz signals at the receiver RX_IN1 input. The external RSSI measurement should be used before turning on the transmitter to prevent RF field collisions. This is especially important for active mode, when both devices emit their own RF field. The level of the RF signal received at the antenna is measured and stored in the RSSI Levels and Oscillator Status register (0x0F). Figure 6-6 shows the relationship between the voltage at the RX_IN1 input and the 3-bit code.

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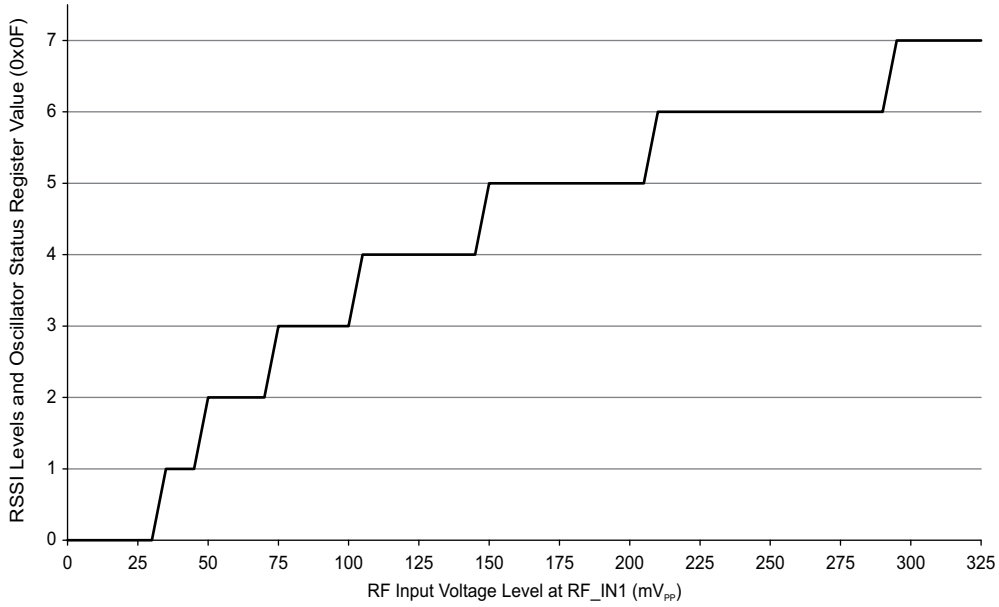


Figure 6-6. Digital External RSSI Value vs RF Input Level in V_{PP} (mV)

The relation between the 3-bit code and the external RF field strength (A/m) sensed by the antenna must be determined by calculation or by experiments for each antenna design. The antenna Q-factor and connection to the RF input influence the result. Direct command 0x19 is used to trigger an external RSSI measurement.

For clarity, to check the internal or external RSSI value independent of any other operation, the user must:

1. Set transmitter to desired state (on or off) using Bit 5 of Chip Status Control register (0x00) and enable receiver using Bit 1.
2. Check internal or external RSSI using direct commands 0x18 or 0x19, respectively. This action places the RSSI value in the RSSI register.
3. Delay at least 50 µs.
4. Read the RSSI register using direct command 0x0F; values range from 0x40 to 0x7F.
5. Repeat steps 1 to 4 as needed. The register is reset when it is read.

6.6 Oscillator Section

The 13.56-MHz or 27.12-MHz crystal (or oscillator) is controlled by the Chip Status Control register (0x00) and the EN and EN2 terminals. The oscillator generates the RF frequency for the RF output stage as well as the clock source for the digital section. The buffered clock signal is available at pin 27 (SYS_CLK) for any other external circuits. B4 and B5 inside the Modulation and SYS_CLK register (0x09) can be used to divide the external SYS_CLK signal at pin 27 by 1, 2, or 4.

Typical start-up time from complete power down is in the range of 3.5 ms.

During Power Down Mode 2 (EN = 0, EN2 = 1) the frequency of SYS_CLK is switched to 60 kHz (typical).

The crystal needs to be connected between pin 30 and pin 31. The external shunt capacitors values for C_1 and C_2 must be calculated based on the specified load capacitance of the crystal being used. The external shunt capacitors are calculated as two identical capacitors in series plus the stray capacitance of the TRF7964A and parasitic PCB capacitance in parallel to the crystal.

The parasitic capacitance (C_S, stray and parasitic PCB capacitance) can be estimated at 4 to 5 pF (typical).

As an example, using a crystal with a required load capacitance (C_L) of 18 pF, the calculation is shown in Equation 1.

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$C_1 = C_2 = 2 \times (C_L - C_S) = 2 \times (18\ pF - 4.5\ pF) = 27\ pF$ (1)

A 27-pF capacitor must be placed on pins 30 and 31 to ensure proper crystal oscillator operation.

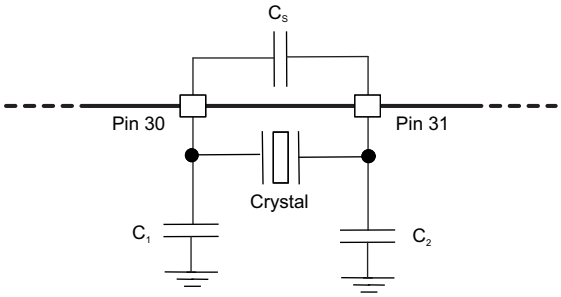


Figure 6-7. Crystal Block Diagram

Any crystal used with TRF7964A should meet the minimum characteristics in Table 6-8.

Table 6-8. Minimum Crystal Recommendations

PARAMETER	SPECIFICATION
Frequency	13.56 MHz or 27.12 MHz
Mode of operation	Fundamental
Type of resonance	Parallel
Frequency tolerance	±20 ppm
Aging	< 5 ppm/year
Operation temperature range	–40°C to 85°C

As an alternative, an external clock oscillator source can be connected to pin 31 to provide the system clock; pin 30 can be left open.

6.7 Transmitter – Analog Section

The 13.56-MHz oscillator generates the RF signal for the PA stage. The power amplifier consists of a driver with selectable output resistance of nominal 4 Ω or 8 Ω. The transmit power level is set by bit B4 in the Chip Status Control register (0x00). The transmit power levels are selectable between 100 mW (half power) or 200 mW (full power) when configured for 5-V automatic operation. The transmit power levels are selectable between 33 mW (half power) or 70 mW (full power) when configured for 3-V automatic operation.

The ASK modulation depth is controlled by bits B0, B1, and B2 in the Modulator and SYS_CLK Control register (0x09). The ASK modulation depth range can be adjusted between 7% to 30% or 100% (OOK).

External control of the transmit modulation depth is possible by setting the ISO Control register (0x01) to direct mode. While operating the TRF7964A in direct mode, the transmit modulation is made possible by selecting the modulation type ASK or OOK at pin 12. External control of the modulation type is made possible only if enabled by setting B6 in the Modulator and SYS_CLK Control register (0x09) to 1.

In normal operation mode, the length of the modulation pulse is defined by the protocol selected in the ISO Control register (0x01). With a high-Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length needs to be corrected by using the TX Pulse Length Control register (0x06).

If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 0x00, the pulse length is equal to the value of the register multiplied by 73.7 ns; therefore, the pulse length can be adjusted between 73.7 ns and 18.8 µs in 73.7-ns increments.

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6.8 Transmitter – Digital Section

The digital part of the transmitter is a mirror of the receiver. The settings controlled the ISO Control register (0x01) are applied to the transmitter just like the receiver. In the TRF7964A default mode the TRF7964A automatically adds these special signals: start of communication, end of communication, SOF, EOF, parity bits, and CRC bytes.

The data is then coded to modulation pulse levels and sent to the RF output stage modulation control unit. Similar to working with the receiver, this means that the external system MCU must only load the FIFO with data, and all the microcoding is done automatically, again saving the firmware developer code space and time. Additionally, all of the registers used for transmit parameter control are automatically preset to optimum values when a new selection is entered into the ISO Control register (0x01).

NOTE

The FIFO must be reset before starting any transmission with direct command 0x0F.

There are two ways to start the transmit operation:

- Send the transmit command and the number of bytes to be transmitted first, and then start to send the data to the FIFO. The transmission starts when first data byte is written into the FIFO.
- Load the number of bytes to be sent into registers 0x1D and 0x1E and load the data to be sent into the FIFO (address 0x1F), followed by sending a transmit command (see Direct Commands section). The transmission then starts when the transmit command is received.

NOTE

If the data length is longer than the FIFO, the TRF7964A notifies the external system MCU when most of the data from the FIFO has been transmitted by sending an interrupt request with a flag in the IRQ register to indicate a FIFO low or high status. The external system should respond by loading the next data packet into the FIFO.

At the end of a transmit operation, the external system MCU is notified by interrupt request (IRQ) with a flag in IRQ register (0x0C) indicating TX is complete (example value = 0x80).

The TX Length registers also support incomplete byte transmission. The high two nibbles in register 0x1D and the nibble composed of bits B4 through B7 in register 0x1E store the number of complete bytes to be transmitted. Bit B0 in register 0x1E is a flag indicating that there are also additional bits to be transmitted that do not form a complete byte. The number of bits is stored in bits B1 through B3 of the same register (0x1E).

Some protocols have options, and there are two sublevel configuration registers to select the TX protocol options.

- ISO/IEC 14443 B TX Options register (0x02). This register controls the SOF and EOF selection and EGT selection for the ISO/IEC 14443 B protocol.
- ISO/IEC 14443 A High Bit Rate Options and Parity register (0x03). This register enables the use of different bit rates for RX and TX operations in the ISO/IEC 14443 high bit rate protocol and also selects the parity method in the ISO/IEC 14443 A high bit rate protocol.

The digital section also has a timer. The timer can be used to start the transmit operation at a specified time in accordance with a selected event.

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6.9 Transmitter – External Power Amplifier and Subcarrier Detector

The TRF7964A can be used in conjunction with an external TX power amplifier or external subcarrier detector for the receiver path. In this case, certain registers must be programmed as shown here:

- Bit B6 of the Regulator and I/O Control register (0x0B) must be set to 1. This setting has two functions: first, to provide a modulated signal for the transmitter if needed, and second, to configure the TRF7964A receiver inputs for an external demodulated subcarrier input.
- Bit B3 of the Modulation and SYS_CLK Control register (0x09) must be set to 1 (see Section 6.14.3.2.8). This function configures the ASK/OOK pin for either a digital or analog output (B3 = 0 enables a digital output, B3 = 1 enables an analog output). The design of an external power amplifier requires detailed RF knowledge. There are also readily designed and certified high-power HF reader modules on the market.

6.10 TRF7964A IC Communication Interface

6.10.1 General Introduction

The communication interface to the reader can be configured in two ways: with a eight line parallel interface (D0:D7) plus DATA_CLK, or with a 4-wire Serial Peripheral Interface (SPI). The SPI interface uses traditional Master Out/Slave In (MOSI), Master In/Slave Out (MISO), Slave Select, and DATA_CLK lines.

These communication modes are mutually exclusive; that is, only one mode can be used at a time in the application.

When the SPI interface is selected, the unused I/O_2, I/O_1, and I/O_0 pins must be hard-wired as shown in Table 6-9. At power up, the TRF7964A samples the status of these three pins and then enters one of the possible SPI modes.

The TRF7964A always behaves as the slave device, and the microcontroller (MCU) behaves as the master device. The MCU initiates all communications with the TRF7964A, and the TRF7964A makes use of the Interrupt Request (IRQ) pin in both parallel and SPI modes to prompt the MCU for servicing attention.

Table 6-9. Pin Assignment in Parallel and Serial Interface Connection or Direct Mode

PIN	PARALLEL	PARALLEL (DIRECT MODE)	SPI WITH SS	SPI WITHOUT SS(1)
DATA_ CLK	DATA_CLK	DATA_CLK	DATA_CLK from master	DATA_CLK from master
I/O_7	A/D[7]	Not used	MOSI(2) = data in (reader in)	MOSI(2) = data in (reader in)
I/O_6	A/D[6]	Direct mode, data out (subcarrier or bit stream)	MISO(3) = data out (MCU out)	MISO(3) = data out (MCU out)
I/O_5(4)	A/D[5]	Direct mode, strobe – bit clock out	See (4).	See (4).
I/O_4	A/D[4]	Not used	SS – slave select(5)	Not used
I/O_3	A/D[3]	Not used	Not used	Not used
I/O_2	A/D[2]	Not used	At VDD	At VDD
I/O_1	A/D[1]	Not used	At VDD	At V_{SS}
I/O_0	A/D[0]	Not used	At V_{SS}	At V_{SS}
IRQ	IRQ interrupt	IRQ interrupt	IRQ interrupt	IRQ interrupt

(1) FIFO is not accessible in SPI without SS mode. See the *TRF7970A Silicon Errata* for detailed information.
(2) MOSI = master out, slave in
(3) MISO = master in, slave out
(4) I/O_5 pin is used only for information when data is put out of the chip (for example, reading 1 byte from the chip). It is necessary first to write in the address of the register (8 clocks) and then to generate another 8 clocks for reading out the data. The I/O_5 pin goes high during the second 8 clocks. But for normal SPI operations, I/O_5 pin is not used.
(5) Slave select pin is active low

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Communication is initialized by a start condition, which is expected to be followed by an Address/Command word (Adr/Cmd). The Adr/Cmd word is 8 bits long, and Table 6-10 shows its format.

Table 6-10. Address and Command Word Bit Distribution

BIT	DESCRIPTION	BIT FUNCTION	ADDRESS	COMMAND
B7	Command control bit	0 = Address 1 = Command	0	1
B6	Read/Write	0 = Write 1 = Read	R/W	0
B5	Continuous address mode	1 = Continuous mode	R/W	0
B4	Address/Command bit 4		Adr 4	Cmd 4
B3	Address/Command bit 3		Adr 3	Cmd 3
B2	Address/Command bit 2		Adr 2	Cmd 2
B1	Address/Command bit 1		Adr 1	Cmd 1
B0	Address/Command bit 0		Adr 0	Cmd 0

The MSB (bit 7) determines if the word is to be used as a command or as an address. The last two columns of Table 6-10 show the function of the separate bits if either address or command is written. Data is expected once the address word is sent. In continuous-address mode (Cont. mode = 1), the first data that follows the address is written (or read) to (from) the given address. For each additional data, the address is incremented by one. Continuous mode can be used to write to a block of control registers in a single stream without changing the address; for example, setup of the predefined standard control registers from the MCU nonvolatile memory to the reader. In noncontinuous address mode (simple addressed mode), only one data word is expected after the address.

Address Mode is used to write or read the configuration registers or the FIFO. When writing more than 12 bytes to the FIFO, the Continuous Address Mode should be set to 1.

Command Mode is used to enter a command resulting in reader action (for example, initialize transmission, enable reader, and turn reader on or off).

The following sections give examples of the expected communications between an MCU and the TRF7964A.

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6.10.1.1 Continuous Address Mode

Figure 6-8 summarizes the continuous address mode communication. Figure 6-8 and Figure 6-9 show the signals between the MCU and the TRF7964A.

Table 6-11. Continuous Address Mode

Start	Adr x	Data(x)	Data(x+1)	Data(x+2)	Data(x+3)	Data(x+4)	...	Data(x+n)	StopCont

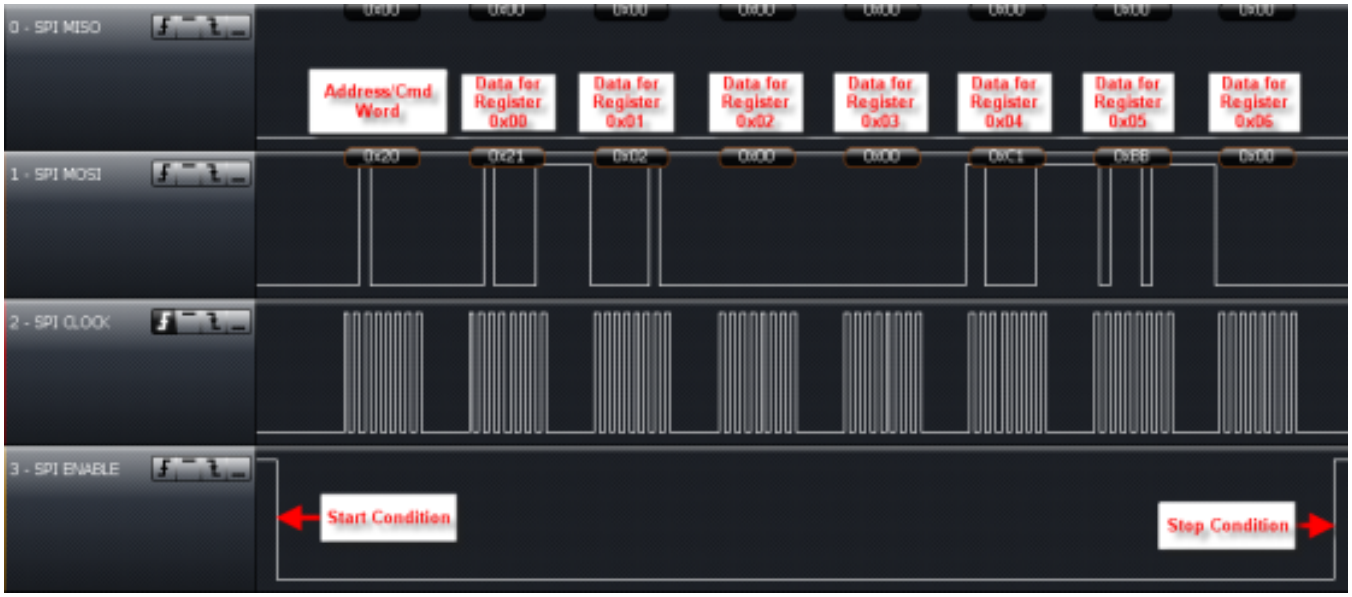


Figure 6-8. Continuous Address Register Write Example Starting With Register 0x00 Using SPI With SS

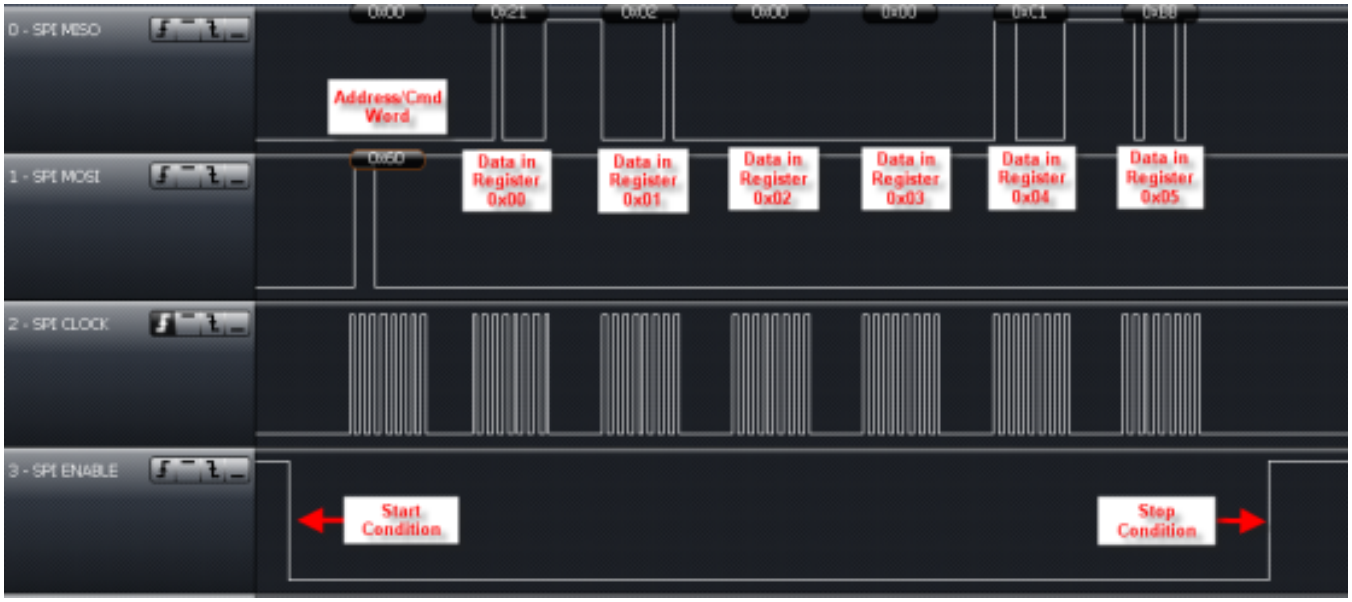


Figure 6-9. Continuous Address Register Read Example Starting With Register 0x00 Using SPI With SS

6.10.1.2 Noncontinuous Address Mode (Single Address Mode)

Table 6-12 summarizes the noncontinuous address (single address) mode communication. Figure 6-10 and Figure 6-11 show the signals between the MCU and the TRF7964A.

Table 6-12. Noncontinuous Address Mode (Single Address Mode)

Start	Adr x	Data(x)	Adr y	Data(y)	...	Adr z	Data(z)	StopSgl

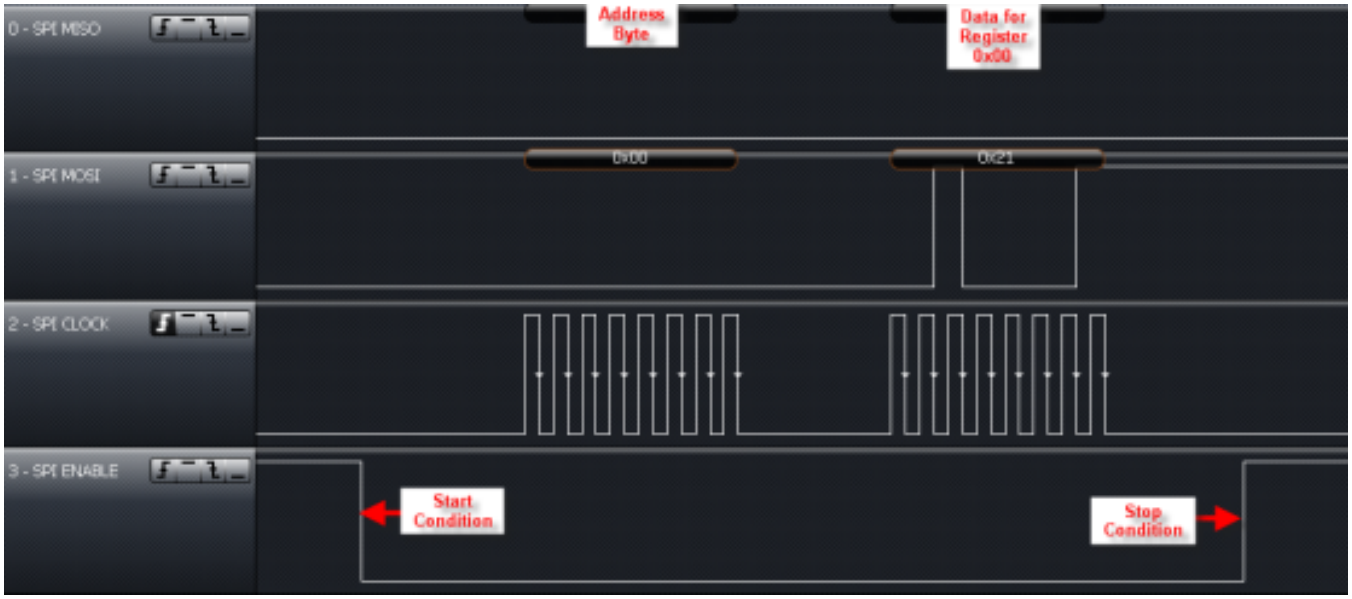


Figure 6-10. Single Address Register Write Example of Register 0x00 Using SPI With SS

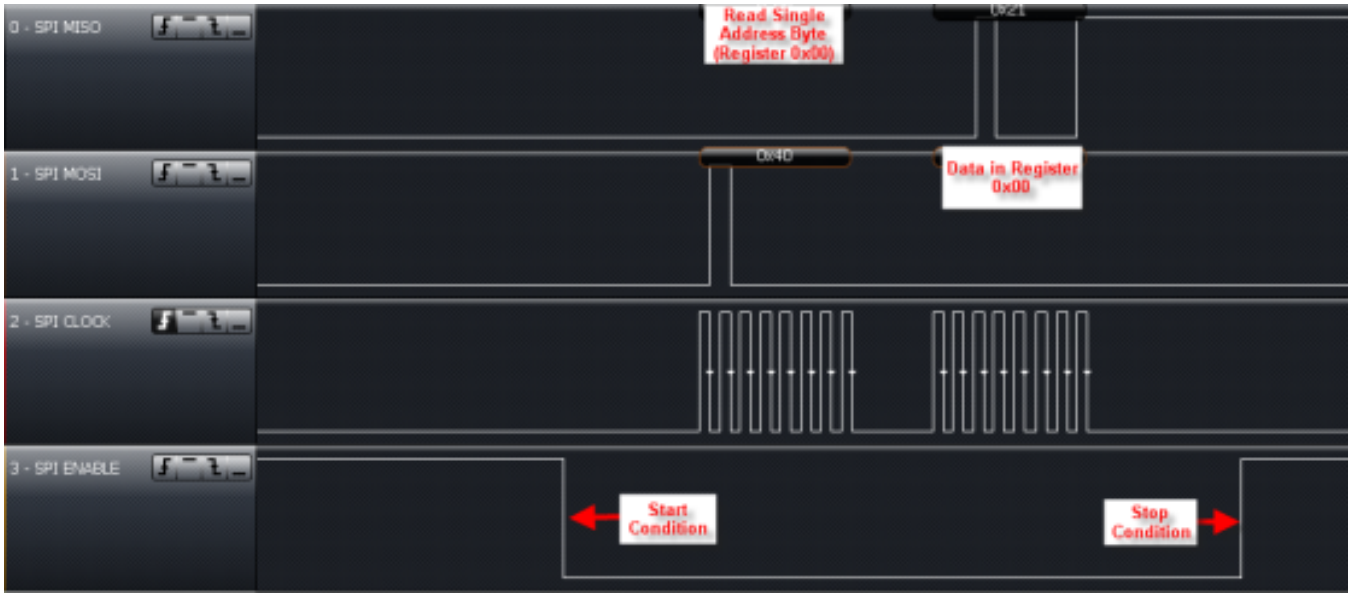


Figure 6-11. Single Address Register Read Example of Register 0x00 Using SPI With SS

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6.10.1.3 Direct Command Mode

Table 6-13 summarizes the direct command mode communication. Figure 6-12 shows the signals between the MCU and the TRF7964A.

Table 6-13. Direct Command Mode

Start	Cmd x	(Optional data or command)	Stop

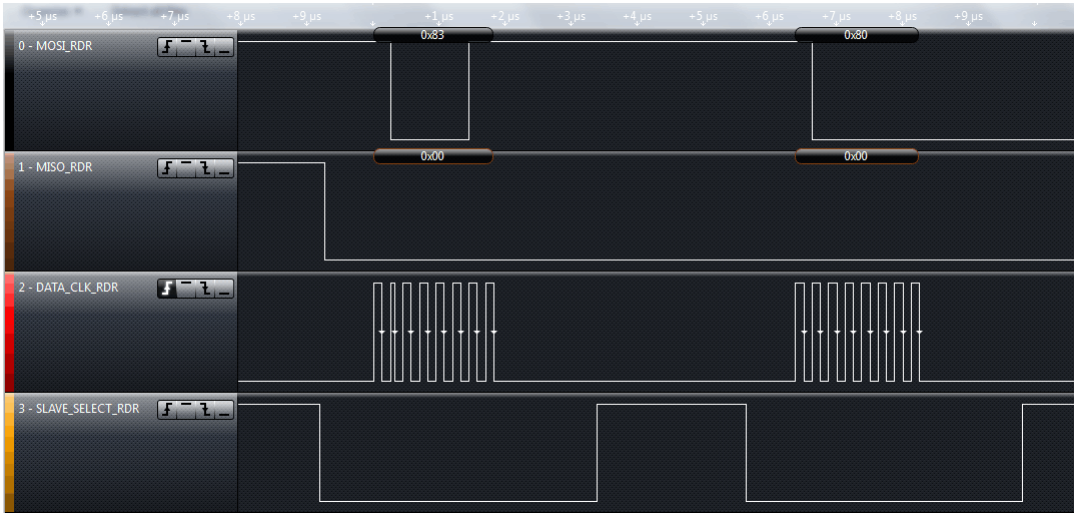


Figure 6-12. Direct Command Example of Sending 0x0F (Reset) Using SPI With SS

Section 6.13 describes the other direct command codes from the MCU to the TRF7964A IC.

6.10.1.4 FIFO Operation

The FIFO is a 127-byte register at address 0x1F with byte storage locations 0 to 126. FIFO data is loaded in a cyclical manner and can be cleared by a reset command (0x0F) (see Figure 6-12 showing this direct command).

Associated with the FIFO are two counters and three FIFO status flags. The first counter is a 7-bit FIFO byte counter (bits B0 to B6 in register 0x1C) that tracks the number of bytes loaded into the FIFO. If the number of bytes in the FIFO is n, the register value is n (number of bytes in FIFO register). For example, if 8 bytes are in the FIFO, the FIFO counter (Register 0x1C) has the hexadecimal value of 0x08 (binary value of 00001000).

A second counter (12 bits wide) indicates the number of bytes being transmitted (registers 0x1D and 0x1E) in a data frame. An extension to the transmission-byte counter is a 4-bit broken-byte counter also provided in register 0x1E (bits B0 to B3). Together these counters make up the TX length value that determines when the reader generates the EOF byte.

During transmission, the FIFO is checked for an almost-empty condition, and during reception for an almost-full condition. The maximum number of bytes that can be loaded into the FIFO in a single sequence is 127 bytes.

NOTE

The number of bytes in a frame, transmitted or received, can be greater than 127 bytes.

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During transmission, the MCU loads the TRF7964A FIFO (or during reception the MCU removes data from the FIFO), and the FIFO counter counts the number of bytes being loaded into the FIFO. Meanwhile, the byte counter keeps track of the number of bytes being transmitted. An interrupt request is generated if the number of bytes in the FIFO triggers the watermark levels, which are configured in the Adjustable FIFO IRQ Levels register (0x14). The default setting is for the interrupt to be triggered when receiving 124 bytes during RX or having 4 bytes remaining during TX. These watermark levels are used so that MCU can send new data or read the data as necessary. The MCU must also validate the number of data bytes to be sent, so as to not surpass the value defined in the TX Length Byte registers (0x1D and 0x1E). The MCU also signals the transmit logic when the last byte of data is sent or was removed from the FIFO during reception.

Figure 6-13 shows an example of checking the FIFO Status register using SPI with SS.

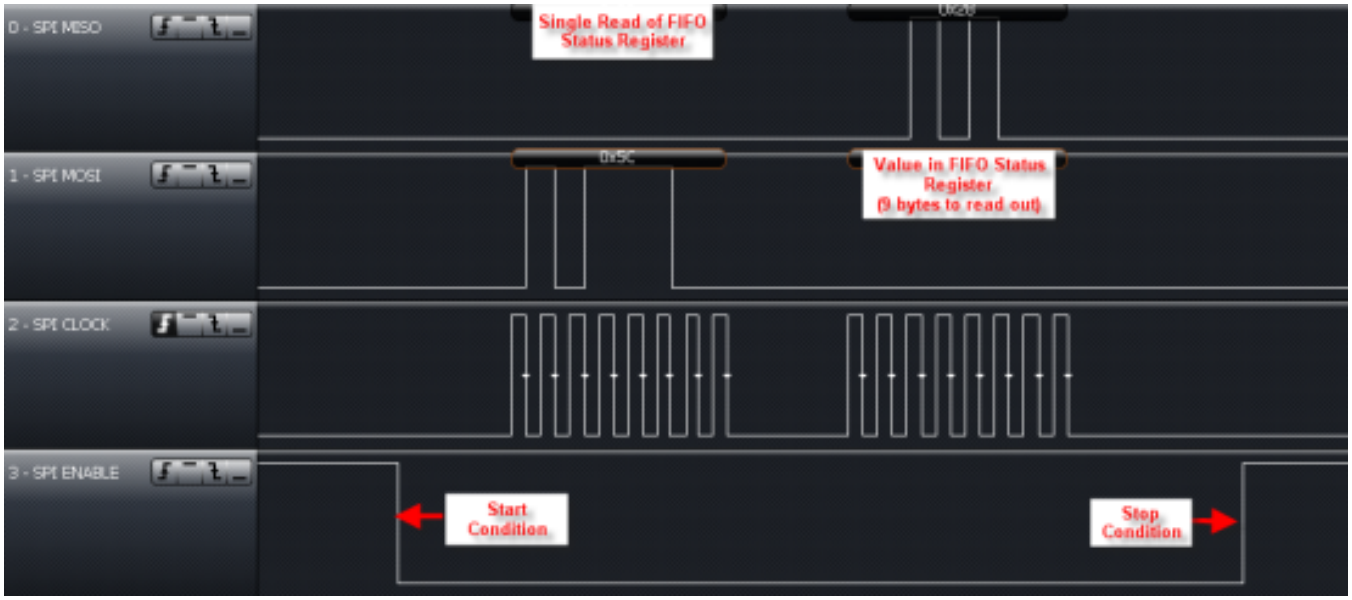


Figure 6-13. Example of Checking the FIFO Status Register Using SPI With SS

6.10.2 Parallel Interface Mode

In parallel mode, the start condition is generated on the rising edge of the I/O_7 pin while the CLK is high.

This is used to reset the interface logic. Figure 6-14, Figure 6-15, and Figure 6-16 show the sequence of the data, with an 8-bit address word first, followed by data.

Communication is ended by:

- The StopSmpl condition, where a falling edge on the I/O_7 pin is expected while CLK is high.
- The StopCont condition, where the I/O_7 pin must have a successive rising and falling edge while CLK is low to reset the parallel interface and be ready for the new communication sequence.
- The *StopSmpl* condition is also used to terminate the direct mode.

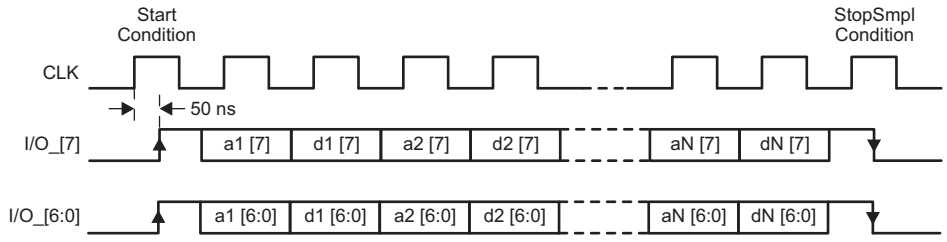


Figure 6-14. Parallel Interface Communication With Simple Stop Condition (StopSmpl)

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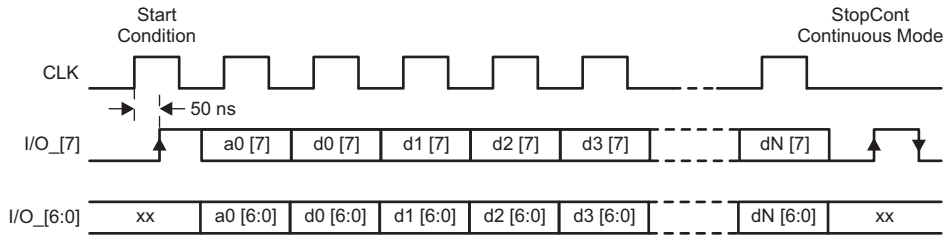


Figure 6-15. Parallel Interface Communication With Continuous Stop Condition (StopCont)

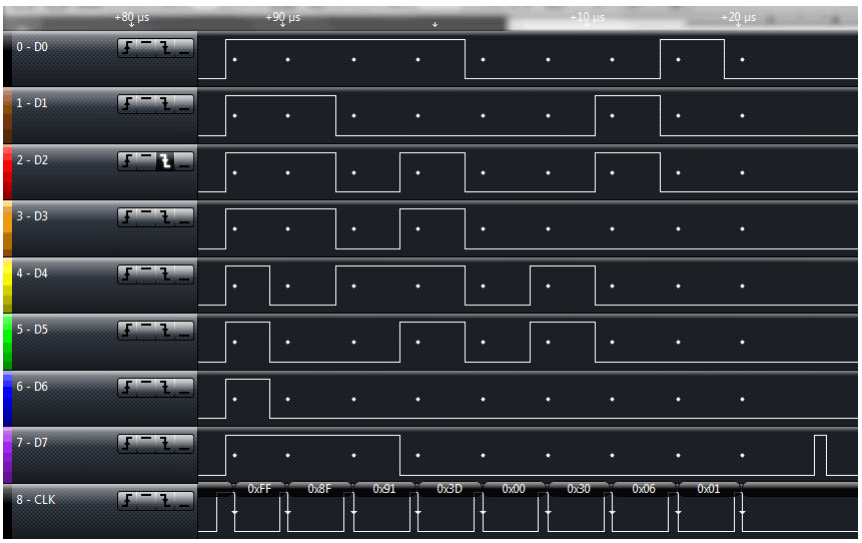


Figure 6-16. Example of Parallel Interface Communication With Continuous Stop Condition

6.10.3 Reception of Air Interface Data

At the start of a receive operation (when SOF is successfully detected), B6 is set in the IRQ Status register. An RX complete interrupt request is sent to the MCU at the end of the receive operation if the receive data string is shorter than or equal to the number of bytes configured in the Adjustable FIFO IRQ Levels register (0x14). An IRQ_FIFO interrupt request is sent to the MCU during the receive operation if the data string is greater than the level set in the Adjustable FIFO IRQ Levels register (0x14). After receiving an IRQ_FIFO or RX complete interrupt, the MCU must read the FIFO Status register (0x1C) to determine the number of bytes to be read from the FIFO. Next, the MCU must read the data in the FIFO. It is optional but recommended to read the FIFO Status register (0x1C) after reading FIFO data to determine if the receive is complete. In the case of an IRQ_FIFO, the MCU should expect either another IRQ_FIFO or RX complete interrupt. This is repeated until an RX complete interrupt is generated. The MCU receives the interrupt request, then checks to determine the reason for the interrupt by reading the IRQ Status register (0x0C), after which the MCU reads the data from the FIFO.

If the reader detects a receive error, the corresponding error flag is set (framing error, CRC error) in the IRQ Status register, indicating to the MCU that reception was not completed correctly.

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6.10.4 Data Transmission From MCU to TRF7964A

Before beginning data transmission, the FIFO should always be cleared with a reset command (0x0F). Data transmission is initiated with a selected command (see Section 6.13). The MCU then commands the reader to do a continuous write command (0x3D) starting from register 0x1D. Data written into register 0x1D is the TX Length Byte 1 (upper and middle nibbles), while the following byte in register 0x1E is the TX Length Byte 2 (lower nibble and broken byte length) (see Table 6-47 and Table 6-48) . Note that the TX byte length determines when the reader sends the end of frame (EOF) byte. After the TX length bytes are written, FIFO data is loaded in register 0x1F with byte storage locations 0 to 127. Data transmission begins automatically after the first byte is written into the FIFO. The loading of TX length bytes and the FIFO can be done with a continuous-write command, as the addresses are sequential.

At the start of transmission, the flag B7 (IRQ_TX) is set in the IRQ Status register, and at the end of the transmit operation, an interrupt is sent to inform the MCU that the task is complete.

6.10.5 Serial Interface Communication (SPI)

When an SPI interface is used, I/O pins I/O_2, I/O_1, and I/O_0 must be hard wired according to Table 6-9. On power up, the TRF7964A looks for the status of these pins and then enters into the corresponding mode.

The serial communications work in the same manner as the parallel communications with respect to the FIFO, except for the following condition. On receiving an IRQ from the reader, the MCU reads the TRF7964A IRQ Status register to determine how to service the reader. After this, the MCU must to do a dummy read to clear the reader's IRQ status register. The dummy read is required in SPI mode because the reader's IRQ status register needs an additional clock cycle to clear the register. This is not required in parallel mode because the additional clock cycle is included in the Stop condition. When first establishing communications with the TRF7964A, the SOFT_INIT (0x03) and IDLE (0x00) commands should be sent first from the MCU (see Table 6-14).

The procedure for a dummy read is as follows (see Figure 6-17 and Figure 6-18):

1. Start the dummy read:
    1. When using slave select (SS): set SS bit low.
    2. When not using SS: start condition is when Data Clock is high (see Table 6-9).
2. Send address word to IRQ status register (0x0C) with read and continuous address mode bits set to 1 (see Table 6-9).
3. Read 1 byte (8 bits) from IRQ status register (0x0C).
4. Dummy-read 1 byte from register 0x0D (collision position and interrupt mask).
5. Stop the dummy read:
    1. When using slave select (SS): set SS bit high.
    2. When not using SS: stop condition when Data Clock is high.

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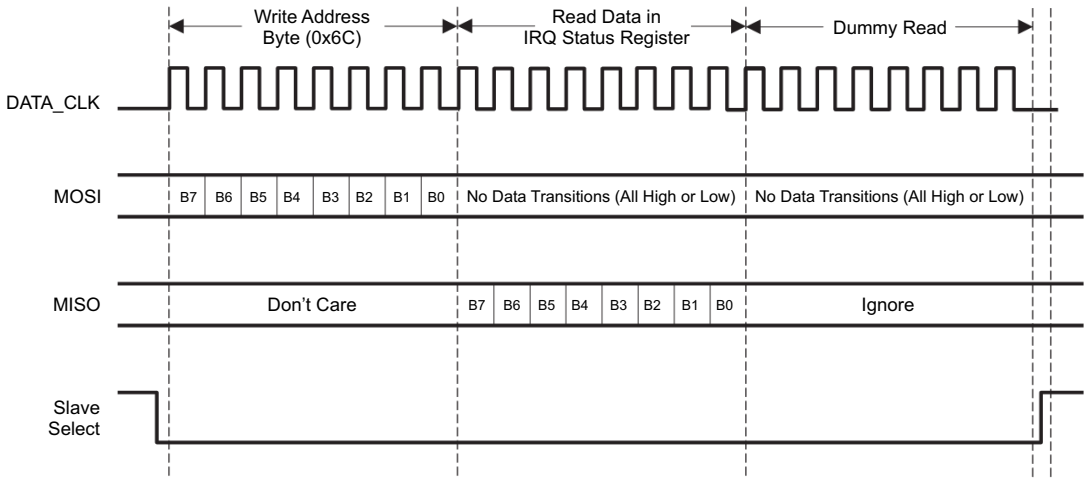


Figure 6-17. Procedure for Dummy Read

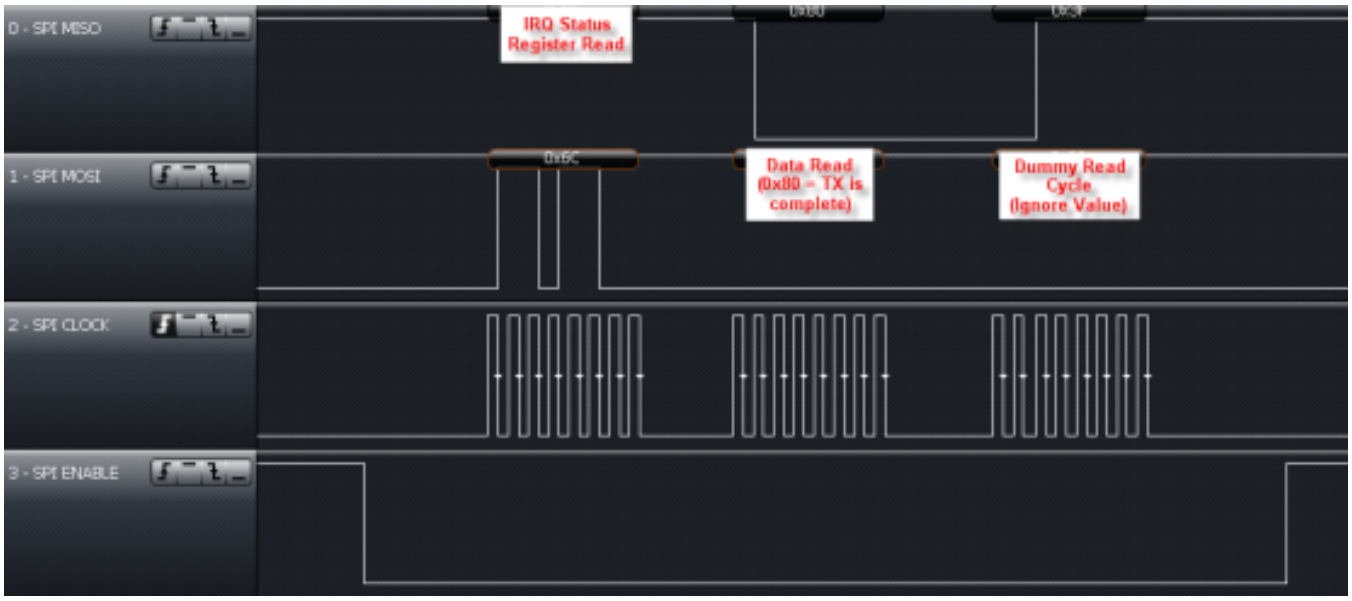


Figure 6-18. Example of Dummy Read Using SPI With SS

6.10.5.1 Serial Interface Mode With Slave Select (SS)

The serial interface is in reset while the Slave Select signal is high. Serial data in (MOSI) changes on the rising edge, and is validated in the reader on the falling edge, as shown in Figure 6-19. Communication is terminated when the Slave Select signal goes high.

All words must be 8 bits long with the MSB transmitted first.

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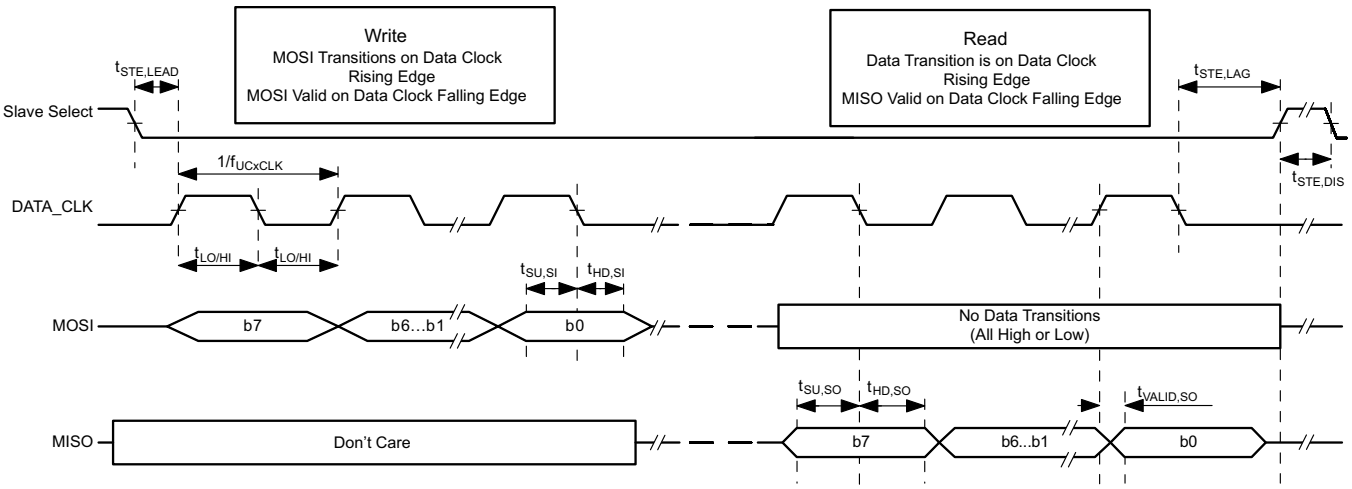


Figure 6-19. SPI With Slave Select Timing Diagram

The read command is sent out on the MOSI pin, MSB first, in the first eight clock cycles. MOSI data changes on the rising edge, and is validated in the reader on the falling edge, as shown in Figure 6-19. During the write cycle, the serial data out (MISO) is not valid. After the last read command bit (B0) is validated at the eighth falling edge of SCLK, valid data can be read on the MISO pin at the falling edge of SCLK. It takes eight clock edges to read out the full byte (MSB first). See Section 5.4 for electrical specifications related to Figure 6-19.

Figure 6-20 and Figure 6-21 show the continuous read operation.

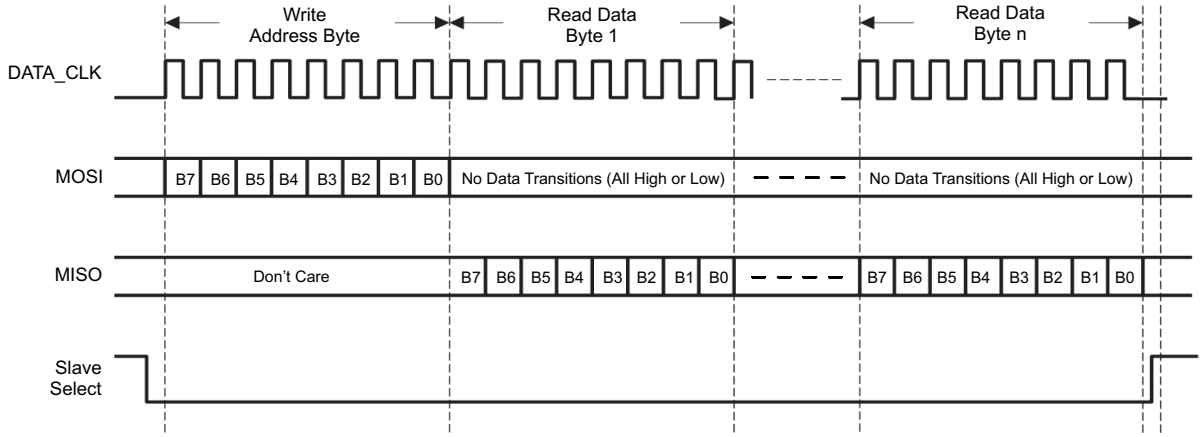


Figure 6-20. Continuous Read Operation Using SPI With Slave Select

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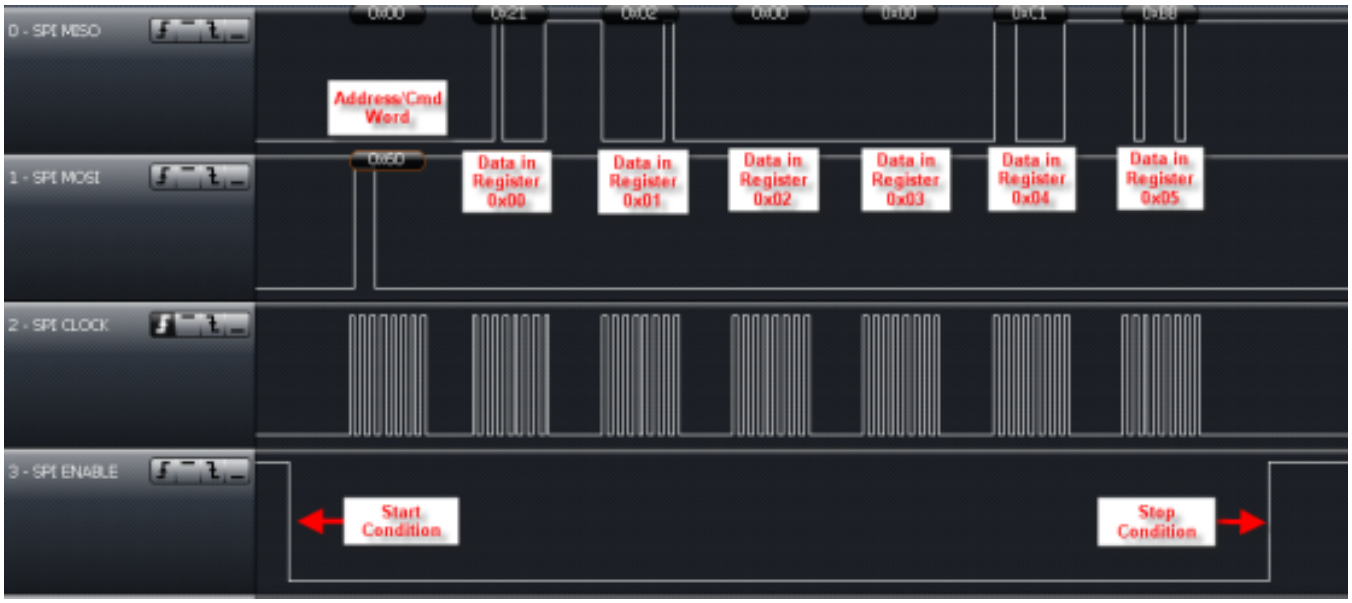


Figure 6-21. Continuous Read of Registers 0x00 to 0x05 Using SPI With SS

Figure 6-22 shows an example of performing a single slot inventory command. Reader registers (in this example) are configured for 5 VDC in and default operation.

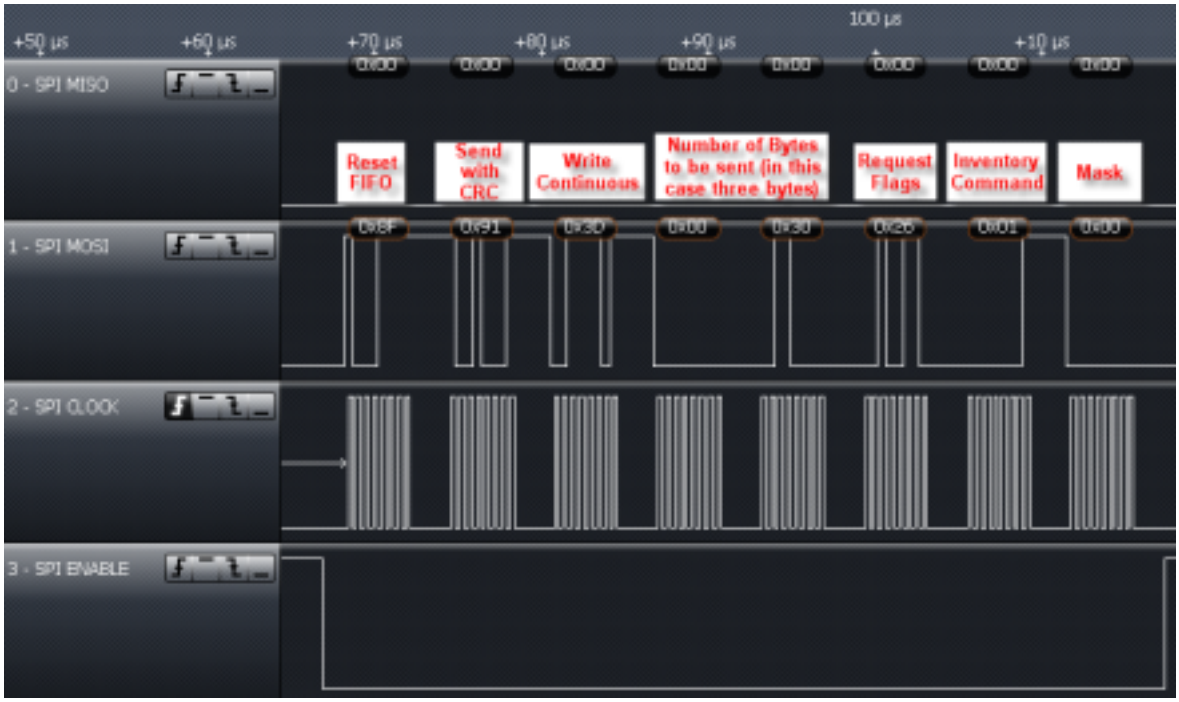


Figure 6-22. Inventory Command Sent From MCU to TRF7964A

The TRF7964A takes these bytes from the MCU and then send out Request Flags, Inventory Command, and Mask over the air to the ISO/IEC 15693 transponder. After these three bytes have been transmitted, an interrupt occurs to indicate back to the reader that the transmission has been completed. In the example in Figure 6-23, this IRQ occurs approximately 1.6 ms after the SS line goes high after the Inventory command is sent out.

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Figure 6-23. IRQ After Inventory Command

The IRQ status register read (0x6C) yields 0x80, which indicates that TX is indeed complete. This is followed by a dummy clock. Then, if a tag is in the field and no error is detected by the reader, a second interrupt is expected and occurs (in this example) approximately 4 ms after first IRQ is read and cleared.

In the continuation of the example (see Figure 6-24), the IRQ Status Register is read using method previously recommended, followed by a single read of the FIFO Status register, which indicates that there are 10 bytes to be read out.

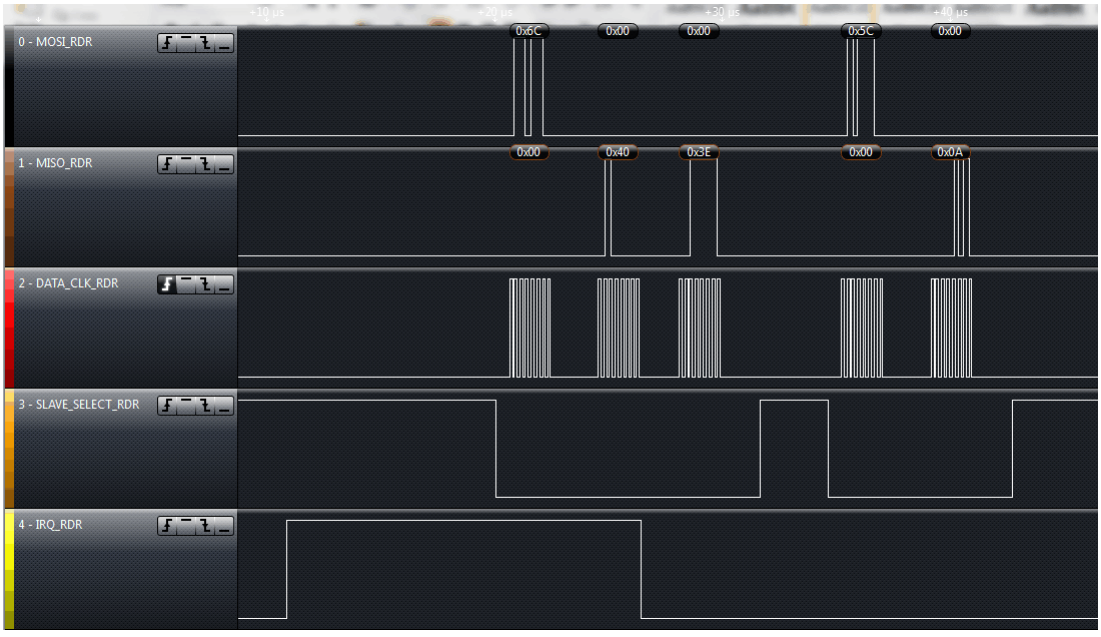


Figure 6-24. Read IRQ Status Register After Inventory Command

This is then followed by a continuous read of the FIFO (see Figure 6-25). The first byte is (and should be) 0x00 for no error. The next byte is the DSFID (usually shipped by manufacturer as 0x00), then the UID, shown here up to the next most significant byte, the MFG code [shown as 0x07 (TI silicon)].

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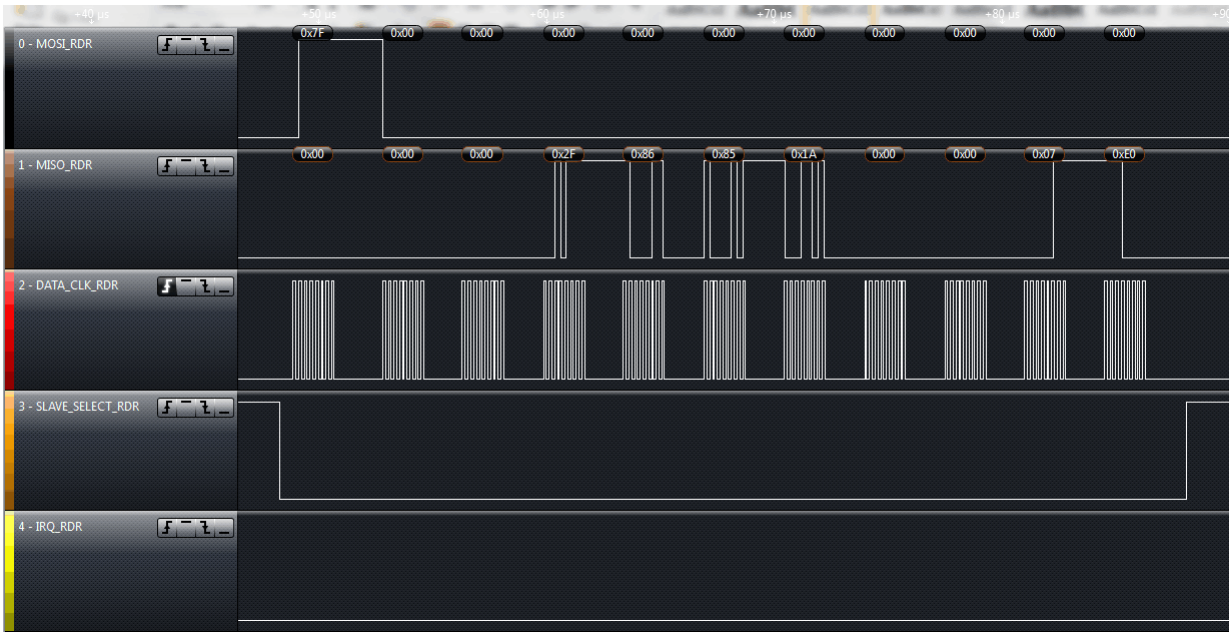


Figure 6-25. Continuous Read of FIFO After Inventory Command

TI recommends resetting the FIFO after receiving data. Additionally, the RSSI value of the tag can be read out at this point. In the example in Figure 6-26, the transponder is very close to the antenna, so value of 0x7F is recovered.



Figure 6-26. Reset FIFO and Read RSSI

6.10.6 Direct Mode

Direct mode allows the user to configure the reader in one of two ways. Direct mode 0 (bit 6 = 0, as defined in ISO Control register) allows the user to use only the front-end functions of the reader, bypassing the protocol implementation in the reader. For transmit functions, the user has direct access to the transmit modulator through the MOD pin (pin 14). On the receive side, the user has direct access to the subcarrier signal (digitized RF envelope signal) on I/O_6 (pin 23).

Direct mode 1 (bit 6 = 1, as defined in ISO Control register) uses the subcarrier signal decoder of the selected protocol (as defined in ISO Control register). This means that the receive output is not the subcarrier signal but the decoded serial bit stream and bit clock signals. The serial data is available on I/O_6 (pin 23) and the bit clock is available on I/O_5 (pin 22). The transmit side is identical; the user has direct control over the RF modulation through the MOD input. This mode is provided so that the user can implement a protocol that has the same bit coding as one of the protocols implemented in the reader, but needs a different framing format.

To select direct mode, the user must first choose which direct mode to enter by writing B6 in the ISO Control register. This bit determines if the receive output is the direct subcarrier signal (B6 = 0) or the serial data of the selected decoder. If B6 = 1, then the user must also define which protocol should be used for bit decoding by writing the appropriate setting in the ISO Control register.

The reader actually enters the direct mode when B6 (direct) is set to 1 in the chip status control register. Direct mode starts immediately. The write command should not be terminated with a stop condition (see communication protocol), because the stop condition terminates the direct mode and clears B6. This is necessary as the direct mode uses one or two I/O pins (I/O_6, I/O_5). Normal parallel communication is not possible in direct mode. Sending a stop condition terminates direct mode.

NOTE

An additional direct mode known as special direct mode can be used to communicate with certain tags not compliant with ISO standards. For full details on how to use this feature, see *Using Special Direct Mode With the TRF7970A*.

Figure 6-27 shows the different configurations available in direct mode.

- In mode 0, the reader is used as an AFE only, and protocol handling is bypassed.
- In mode 1, framing is not done, but SOF and EOF are present. This allows for a user-selectable framing level based on an existing ISO standard.
- In mode 2, data is ISO-standard formatted. SOF, EOF, and error checking are removed, so the microprocessor receives only bytes of raw data through a 127-byte FIFO.

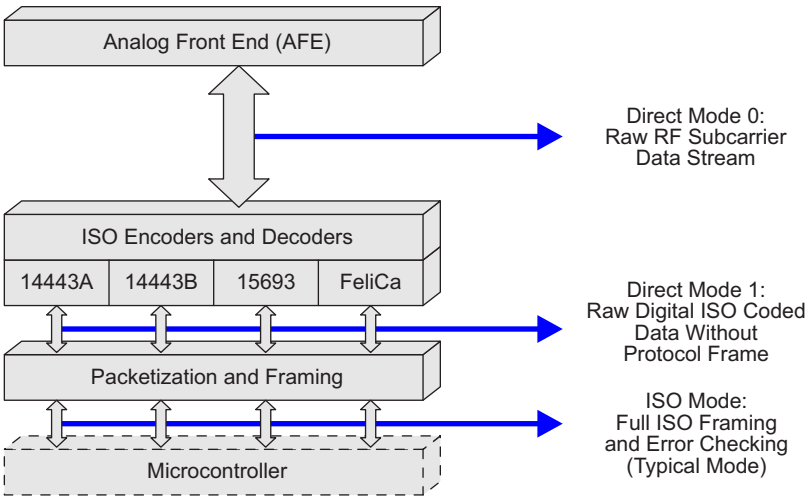


Figure 6-27. User-Configurable Modes

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The steps to enter direct mode are listed below, using SPI with SS communication method only as one example, as direct modes are also possible with parallel and SPI without SS. The must enter direct mode 0 to accommodate card type communications that are not compliant with ISO standards. Direct mode can be entered at any time, so if a card type started with ISO standard communications, then deviated from the standard after being identified and selected, the ability to go into direct mode 0 is very useful.

Step 1: Configure Pins I/O_0 to I/O_2 for SPI with SS

Step 2: Set Pin 12 of the TRF7964A (ASK/OOK pin) to 0 for ASK or 1 for OOK

Step 3: Program the TRF7964A registers

The following registers must be explicitly set before going into the direct mode.

1. ISO Control register (0x01) to the appropriate standard
   - 0x02 for ISO/IEC 15693 High Data Rate
   - 0x08 for ISO/IEC 14443 A (106 kbps)
   - 0x1A for FeliCa 212 kbps
   - 0x1B for FeliCa 424 kbps
2. Modulator and SYS_CLK register (0x09) to the appropriate clock speed and modulation
   - 0x21 for 6.78 MHz Clock and OOK (100%) modulation
   - 0x20 for 6.78 MHz Clock and ASK 10% modulation
   - 0x22 for 6.78 MHz Clock and ASK 7% modulation
   - 0x23 for 6.78 MHz Clock and ASK 8.5% modulation
   - 0x24 for 6.78 MHz Clock and ASK 13% modulation
   - 0x25 for 6.78 MHz Clock and ASK 16% modulation
     (See register 0x09 definition for all other possible values)

Example register setting for ISO/IEC 14443 A at 106 kbps:

- ISO Control register (0x01) to 0x08
- RX No Response Wait Time register (0x07) to 0x0E
- RX Wait Time register (0x08) to 0x07
- Modulator control register (0x09) to 0x21 (or any custom modulation)
- RX Special Settings register (0x0A) to 0x20

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Step 4: Entering Direct Mode 0

The following registers must be programmed to enter direct mode 0:

1. Set bit B6 of the Modulator and SYS_CLK Control register (0x09) to 1.
2. Set bit B6 of the ISO Control (Register 01) to 0 for direct mode 0 (default its 0)
3. Set bit B6 of the Chip Status Control register (0x00) to 1 to enter direct mode
4. Send extra eight clock cycles (see Figure 6-28, this step is TRF7964A specific)

NOTE

- It is important that the last write is not terminated with a stop condition. For SPI, this means that Slave Select (I/O_4) stays low.
- Sending a Stop condition terminates the direct mode and clears bit B6 in the Chip Status Control register (0x00).

NOTE

Access to Registers, FIFO, and IRQ is not available during direct mode 0.

The reader enters the direct mode 0 when bit 6 of the Chip Status Control register (0x00) is set to a 1 and stays in direct mode 0 until a stop condition is sent from the microcontroller.

NOTE

The write command should not be terminated with a stop condition (for example, in SPI mode this is done by bringing the Slave Select line high after the register write), because the stop condition terminates the direct mode and clears bit 6 of the Chip Status Control register (0x00), making it a 0.

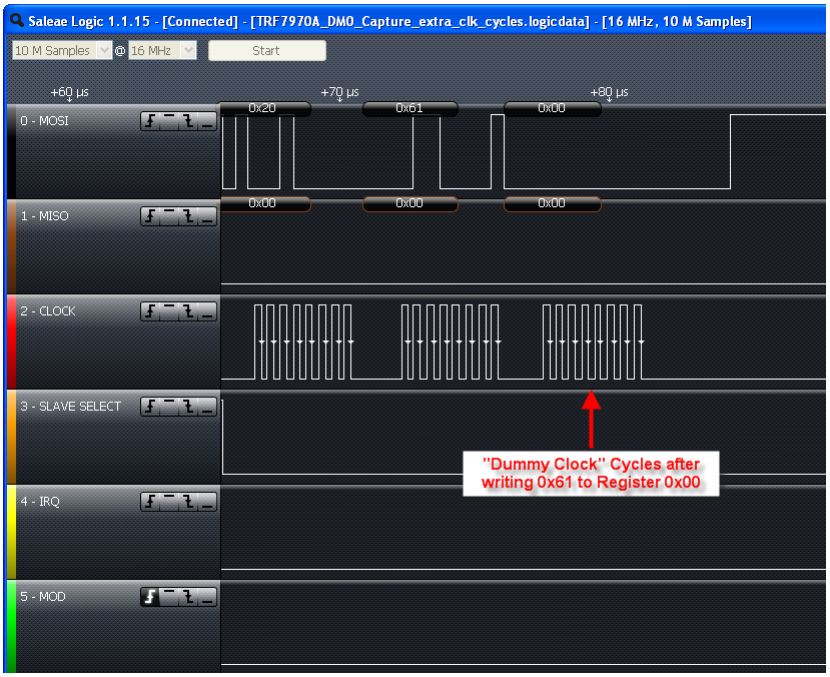


Figure 6-28. Entering Direct Mode 0

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Step 5: Transmit Data Using Direct Mode

The application now has direct control over the RF modulation through the MOD input (see Figure 6-29).

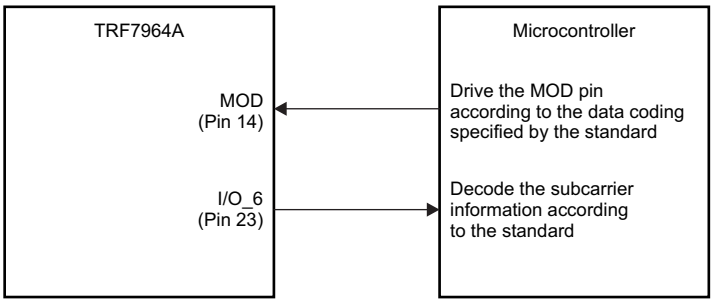


Figure 6-29. Direct Control Signals

The microcontroller is responsible for generating data according to the coding specified by the particular standard. The microcontroller must generate SOF, EOF, Data, and CRC. In direct mode, the FIFO is not used and no IRQs are generated. See the applicable ISO standard to understand bit and frame definitions. Figure 6-30 shows an example of what the developer sees when using DM0 in an actual application. This figure clearly shows the relationship between the MOD pin being controlled by the MCU and the resulting modulated 13.56-MHz carrier signal.

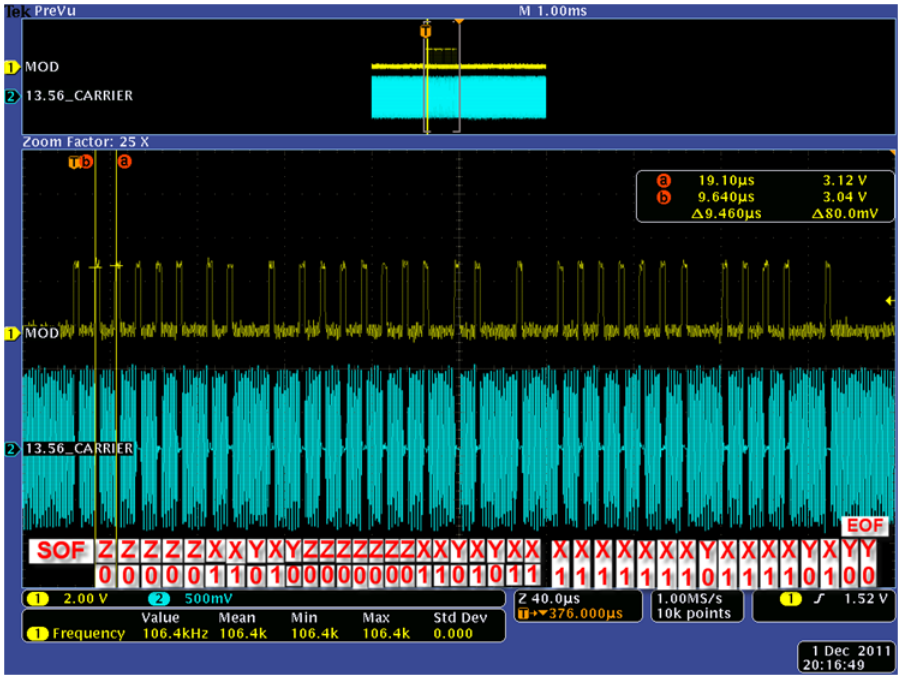


Figure 6-30. TX Sequence Out in DM0

Step 6: Receive Data Using Direct Mode

After the TX operation is complete, the tag responds to the request and the subcarrier data is available on pin I/O_6. The microcontroller needs to decode the subcarrier signal according to the standard. This includes decoding the SOF, data bits, CRC, and EOF. The CRC then needs to be checked to verify data integrity. The receive data bytes must be buffered locally.

As an example of the receive data bits and framing level according to the ISO/IEC 14443 A standard is shown in Figure 6-31 (taken from ISO/IEC 14443 specification and TRF7964A air interface).

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- 128/fc = 9.435 µs = t_b (106-kbps data rate)
- 64/fc = 4.719 µs = t_x time
- 32/fc = 2.359 µs = t_1 time

Table 7 — Parameters for sequences

Parameter	Bit rate			
	fc/128	fc/64	fc/32	fc/16
t_b	128/fc	64/fc	32/fc	16/fc
t_x	64/fc	32/fc	16/fc	8/fc
t_1	see t_1 of Table 3	see t_1 of Table 5		

Figure 10 together with the timing parameters in Table 7 illustrate sequences X, Y and Z.

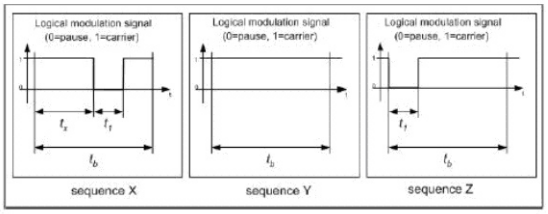


Figure 10 — Sequences for Type A communication PCD to PICC

The above sequences shall be used to code the following information:

— logic "1": sequence X,

— logic "0": sequence Y with the following two exceptions:

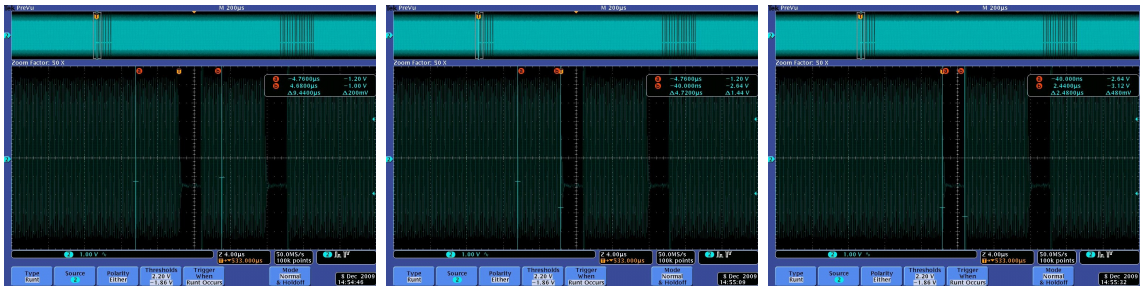
i) If there are two or more contiguous "0"s, sequence Z shall be used from the second "0" on,

ii) If the first bit after a "start of frame" is "0", sequence Z shall be used to represent this and any "0"s which follow directly thereafter.

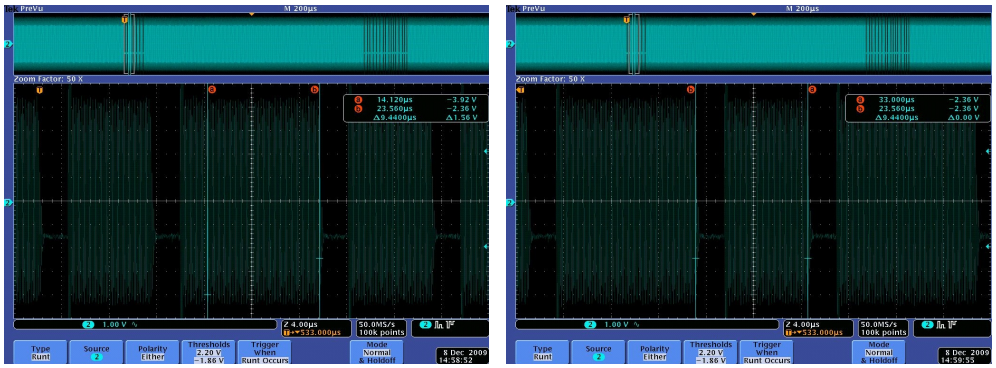
— start of communication: sequence Z,

— end of communication: logic "0" followed by sequence Y,

— no information: at least two sequences Y.



t_b = 9.44 µs | t_x = 4.72 µs | t_1 = 2.48 µs



Sequence Y = Carrier for 9.44 µs | Sequence Z = Pause for 2 to 3 µs, Carrier for Remainder of 9.44 µs

Figure 6-31. Receive Data Bits and Framing Level

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Figure 6-32 shows an example of what the developer should expect on the I/O_6 line during the RX process while in direct mode 0.

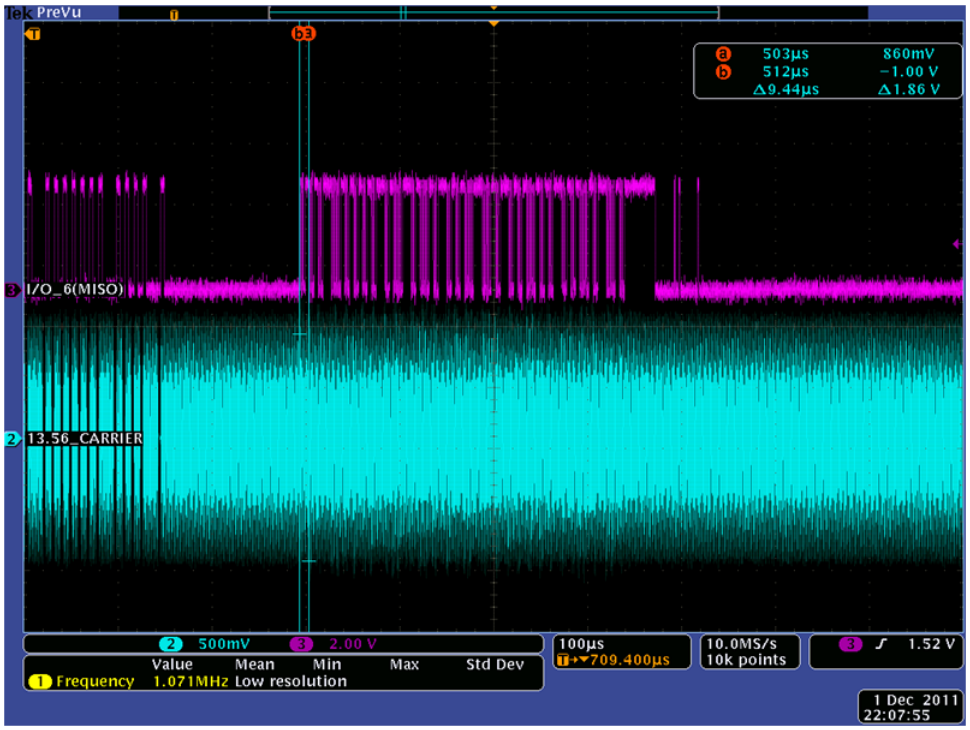


Figure 6-32. RX Sequence on I/O_6 in DM0 (Analog Capture)

Step 7: Terminating Direct Mode 0

After the EOF is received, data transmission is over, and direct mode 0 can be terminated by sending a Stop Condition (in the case of SPI, make the Slave Select go high). The TRF7964A is returned to default state.

6.11 TRF7964A Initialization

To properly initialize the TRF7964A, perform these steps:

1. Raise the EN, EN2, and SS lines at the correct intervals after power up (for timing diagrams, see Figure 6-3 and Figure 6-4).
2. Issue a Software Initialization direct command (0x03), followed by an Idle direct command (0x00) to soft reset the TRF7964A.

NOTE

Table 6-16 lists the initial register settings for the TRF7964A after the Software Initialization command.

3. Delay 1 ms to allow the TRF7964A to fully process the soft reset.
4. Issue a Reset FIFO direct command (0x0F).
5. Write the Modulator and SYS_CLK Control register (0x09) with the appropriate application-specific setting for the crystal and system clock settings.
6. Write the Regulator and I/O Control register (0x0B) with the appropriate application-specific setting.

6.12 Special Direct Mode for Improved MIFARE™ Compatibility

See *Using Special Direct Mode With the TRF7970A*.

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6.13 Direct Commands from MCU to Reader

6.13.1 Command Codes

Table 6-14 summarizes the command codes.

Table 6-14. Address and Command Word Bit Distribution

COMMAND CODE	COMMAND	COMMENTS
0x00	Idle	
0x03	Software initialization	Same as Power on Reset
0x0F	Reset FIFO	
0x10	Transmission without CRC	
0x11	Transmission with CRC	
0x12	Delayed transmission without CRC	
0x13	Delayed transmission with CRC	
0x14	End of frame and transmit next time slot	Used for ISO/IEC 15693 only
0x16	Block receiver	
0x17	Enable receiver	
0x18	Test internal RF (RSSI at RX input with TX off)	
0x19	Test external RF (RSSI at RX input with TX on)	

The command code values from Table 6-14 are substituted in Table 6-15, bits 0 through 4. Also, the most-significant bit (MSB) in Table 6-15 must be set to 1. (Table 6-15 is same as Table 6-10, shown here again for easy reference).

Table 6-15. Address and Command Word Bit Distribution

BIT	DESCRIPTION	BIT FUNCTION	ADDRESS	COMMAND
B7	Command control bit	0 = Address 1 = Command	0	1
B6	Read/Write	0 = Write 1 = Read	R/W	0
B5	Continuous address mode	1 = Continuous mode	R/W	0
B4	Address/Command bit 4		Adr 4	Cmd 4
B3	Address/Command bit 3		Adr 3	Cmd 3
B2	Address/Command bit 2		Adr 2	Cmd 2
B1	Address/Command bit 1		Adr 1	Cmd 1
B0	Address/Command bit 0		Adr 0	Cmd 0

The MSB determines if the word is to be used as a command or address. The last two columns of Table 6-15 show the function of each bit, depending on whether address or command is written. Command mode is used to enter a command resulting in reader action (initialize transmission, enable reader, and turn reader on or off).

6.13.1.1 Idle (0x00)

This command issues dummy clock cycles. In parallel mode, one cycle is issued. In SPI mode, eight cycles are issued. This command should be sent after a Software Initialization command to allow the command to finish operation.

6.13.1.2 Software Initialization (0x03)

This command starts a power-on reset. After sending this command, the register values change as shown in Table 6-16.

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Table 6-16. Register Values After Sending Software Initialization (0x03)

ADDRESS	REGISTER	VALUE
0x00	Chip status control	0x01
0x01	ISO control	0x21 (1)
0x02	ISO/IEC 14443 B TX options	0x00
0x03	ISO/IEC 14443 A high bit rate options	0x00
0x04	TX timer high byte control	0xC1 (1)
0x05	TX timer low byte control	0xC1 (1)
0x06	TX pulse length control	0x00
0x07	RX no response wait time	0x0E
0x08	RX wait time	0x07 (1)
0x09	Modulator and SYS_CLK control	0x91
0x0A	RX special setting	0x10 (1)
0x0B	Regulator and I/O control	0x87
0x0C	IRQ status	0x00
0x0D	Collision position and interrupt mask	0x3E
0x0E	Collision position	0x00
0x0F	RSSI levels and oscillator status	0x40
0x10	Special function	0x00
0x11	Special function	0x00
0x12	RAM	0x00
0x13	RAM	0x00
0x14	Adjustable FIFO IRQ levels	0x00
0x1A	Test	0x00
0x1B	Test	0x00
0x1C	FIFO status	0x00

(1) Differs from default at POR

6.13.1.3 Reset FIFO (0x0F)

The reset command clears the FIFO contents and FIFO Status register (0x1C). It also clears the register storing the collision error location (0x0E).

6.13.1.4 Transmission With CRC (0x11)

The transmission command must be sent first, followed by transmission length bytes, and FIFO data. The reader starts transmitting after the first byte is loaded into the FIFO. The CRC byte is included in the transmitted sequence.

6.13.1.5 Transmission Without CRC (0x10)

Same as Section 6.13.1.4 with CRC excluded.

6.13.1.6 Delayed Transmission With CRC (0x13)

The transmission command must be sent first, followed by the transmission length bytes, and FIFO data.

The reader transmission is triggered by the TX timer.

6.13.1.7 Delayed Transmission Without CRC (0x12)

Same as Section 6.13.1.6 with CRC excluded.

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6.13.1.8 Transmit Next Time Slot (0x14)

When this command is received, the reader transmits the next slot command. The next slot sign is defined by the protocol selection. This is used by the ISO/IEC 15693 protocol.

6.13.1.9 Block Receiver (0x16)

The block receiver command puts the digital part of receiver (bit decoder and framer) in reset mode. This is useful in an extremely noisy environment, where the noise level could otherwise cause a constant switching of the subcarrier input of the digital part of the receiver. The receiver (if not in reset) would try to catch a SOF signal, and if the noise pattern matched the SOF pattern, an interrupt would be generated, falsely signaling the start of an RX operation. A constant flow of interrupt requests can be a problem for the external system (MCU), so the external system can stop this by putting the receive decoders in reset mode. The reset mode can be terminated in two ways. The external system can send the enable receiver command. The reset mode is also automatically terminated at the end of a TX operation. The receiver can stay in reset after end of TX if the RX wait time register (0x08) is set. In this case, the receiver is enabled at the end of the wait time following the transmit operation.

6.13.1.10 Enable Receiver (0x17)

This command clears the reset mode in the digital part of the receiver if the reset mode was entered by the block receiver command.

6.13.1.11 Test Internal RF (RSSI at RX Input With TX ON) (0x18)

The level of the RF carrier at RF_IN1 and RF_IN2 inputs is measured. Operating range between 300 mV_P and 2.1 V_P (step size is 300 mV). The two values are displayed in the RSSI Levels and Oscillator Status register (0x0F). The command is intended for diagnostic purposes to set correct RF_IN levels. Optimum RFIN input level is approximately 1.6 V_P or code 5 to 6. The nominal relationship between the RF peak level and RSSI code is shown in Table 6-17 and in Section 6.5.1.1.

NOTE

If the command is executed immediately after power-up and before any communication with a tag is performed, the command must be preceded by Enable RX command. The Check RF commands require full operation, so the receiver must be activated by Enable RX or by a normal Tag communication for the Check RF command to work properly.

Table 6-17. Test Internal RF Peak Level to RSSI Codes

RF_IN1 [mV_{PP}]	300	600	900	1200	1500	1800	2100
Decimal Code	1	2	3	4	5	6	7
Binary Code	001	010	011	001	101	011	111

6.13.1.12 Test External RF (RSSI at RX Input with TX OFF) (0x19)

This command can be used in active mode when the RF receiver is switched on but RF output is switched off. This means bit B1 = 1 in Chip Status Control Register. The level of RF signal received on the antenna is measured and displayed in the RSSI Levels and Oscillator Status register (0x0F). The relation between the 3 bit code and the external RF field strength [A/m] must be determinate by calculation or by experiments for each antenna type as the antenna Q and connection to the RF input influence the result. The nominal relation between the RF peak to peak voltage in the RF_IN1 input and RSSI code is shown in Table 6-18 and in Section 6.5.1.2.

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NOTE

If the command is executed immediately after power-up and before any communication with a tag is performed, the command must be preceded by an Enable RX command. The Check RF commands require full operation, so the receiver must be activated by Enable RX or by a normal Tag communication for the Check RF command to work properly.

Table 6-18. Test External RF Peak Level to RSSI Codes

RF_IN1 [mV_{PP}]	40	60	80	100	140	180	300
Decimal Code	1	2	3	4	5	6	7
Binary Code	001	010	011	001	101	011	111

6.14 Register Description

6.14.1 Register Preset

After power up and the EN pin low-to-high transition, the reader is in the default mode. The default configuration is ISO/IEC 15693, single subcarrier, high data rate, 1-out-of-4 operation. The low-level option registers (0x02 to 0x0B) are automatically set to adapt the circuitry optimally to the appropriate protocol parameters. When entering another protocol (by writing to the ISO Control register 0x01), the low-level option registers (0x02 to 0x0B) are automatically configured to the new protocol parameters. After selecting the protocol, it is possible to change some low-level register contents if needed. However, changing to another protocol and then back, reloads the default settings, and so then the custom settings must be reloaded.

The Clo0 and Clo1 register (0x09) bits, which define the microcontroller frequency available on the SYS_CLK pin, are the only 2 bits in the configuration registers that are not cleared during protocol selection.

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6.14.2 Register Overview

Table 6-19 lists the registers.

Table 6-19. Register Definitions

ADDRESS	REGISTER	READ/WRITE	SECTION
Main Control Registers			
0x00	Chip status control	R/W	Section 6.14.3.1.1
0x01	ISO Control	R/W	Section 6.14.3.1.2
Protocol Subsetting Registers			
0x02	ISO/IEC 14443 B TX options	R/W	Section 6.14.3.2.1
0x03	ISO/IEC 14443 A high bit rate options	R/W	Section 6.14.3.2.2
0x04	TX timer high byte control	R/W	Section 6.14.3.2.3
0x05	TX timer low byte control	R/W	Section 6.14.3.2.4
0x06	TX pulse length control	R/W	Section 6.14.3.2.5
0x07	RX no response wait time	R/W	Section 6.14.3.2.6
0x08	RX wait time	R/W	Section 6.14.3.2.7
0x09	Modulator and SYS_CLK control	R/W	Section 6.14.3.2.8
0x0A	RX special setting	R/W	Section 6.14.3.2.9
0x0B	Regulator and I/O control	R/W	Section 6.14.3.2.10
0x10	Special function register (preset 0x00)	R/W	Section 6.14.3.3.4
0x11	Special function register (preset 0x00)	R/W	Section 6.14.3.3.5
0x14	Adjustable FIFO IRQ levels	R/W	Section 6.14.3.3.6
Status Registers			
0x0C	IRQ status	R	Section 6.14.3.3.1
0x0D	Collision position and interrupt mask register	R/W	Section 6.14.3.3.2
0x0E	Collision position	R	Section 6.14.3.3.2
0x0F	RSSI levels and oscillator status	R	Section 6.14.3.3.3
Test Registers			
0x1A	Test (preset 0x00)	R/W	Section 6.14.3.4.1
0x1B	Test (preset 0x00)	R/W	Section 6.14.3.4.2
FIFO Registers			
0x1C	FIFO status	R	Section 6.14.3.5.1
0x1D	TX length byte 1	R/W	Section 6.14.3.5.2
0x1E	TX length byte 2	R/W	Section 6.14.3.5.2
0x1F	FIFO I/O register	R/W	N/A

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6.14.3 Detailed Register Description

6.14.3.1 Main Configuration Registers

6.14.3.1.1 Chip Status Control Register (0x00)

Table 6-20 describes the Chip Status Control register.

Table 6-20. Chip Status Control Register (0x00)

Function: Control of Power mode, RF on or off, Active or Passive mode, Direct mode			
Default: 0x01, preset at EN = L or POR = H			
Bit	**Name**	**Function**	**Description**
B7	stby	1 = Standby mode	Standby mode keeps all supply regulators and the 13.56-MHz SYS_CLK oscillator running. (Typical start-up time to full operation is 100 µs.)
		0 = Active mode	Active mode (default)
B6	direct	1 = Direct mode 0 or 1	Provides user direct access to AFE (direct mode 0) or allows user to add custom framing (direct mode 1). Bit 6 of the ISO Control register must be set by user before entering direct mode 0 or 1.
		0 = Direct l 2 (default)	Uses SPI or parallel communication with automatic framing and ISO decoders
B5	rf_on	1 = RF output active	Transmitter on, receivers on
		0 = RF output not active	Transmitter off
B4	rf_pwr	1 = Half output power	TX_OUT (pin 5) = 8-Ω output impedance P = 100 mW (20 dBm) at 5 V, P = 33 mW (+15 dBm) at 3.3 V
		0 = Full output power	TX_OUT (pin 5) = 4-Ω output impedance P = 200 mW (+23 dBm) at 5 V, P = 70 mW (+18 dBm) at 3.3 V
B3	pm_on	1 = Selects aux RX input	RX_IN2 input is used
		0 = Selects main RX input	RX_IN1 input is used
B2	Reserved		
B1	rec_on	1 = Receiver activated for external field measurement	Forced enabling of receiver and TX oscillator. Used for external field measurement.
		0 = Automatic enable	Allows enable of the receiver by bit 5 of this register (0x00)
B0	vrs5_3	1 = 5-V operation 0 = 3-V operation	Selects the V_{IN} voltage range

6.14.3.1.2 ISO Control Register (0x01)

Table 6-21 describes the ISO Control register.

Table 6-21. ISO Control Register (0x01)

Function: Controls the selection of ISO standard protocol, direct mode and receive CRC			
Default: 0x02 (ISO/IEC 15693 high bit rate, one subcarrier, 1 out of 4); it is preset at EN = L or POR = H			
Bit	**Name**	**Function**	**Description**
B7	rx_crc_n	CRC Receive selection	0 = RX CRC (CRC is present in the response) 1 = no RX CRC (CRC is not present in the response)(1)
B6	dir_mode	Direct mode type selection	0 = Direct Mode 0 1 = Direct mode 1
B5	rfid	RFID / Reserved	0 = RFID mode 1 = Reserved (should be set to 0)
B4	iso_4	RFID	RFID: See Table 6-22 for B0:B4 settings based on ISO protocol in application
B3	iso_3	RFID	RFID: See Table 6-22 for B0:B4 settings based on ISO protocol in application
B2	iso_2	RFID	RFID: See Table 6-22 for B0:B4 settings based on ISO protocol in application
B1	iso_1	RFID	RFID: See Table 6-22 for B0:B4 settings based on ISO protocol in application

(1) Only applicable to ISO/IEC 14443 A and ISO/IEC 15693

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Table 6-21. ISO Control Register (0x01) (continued)

B0	iso_0	RFID	RFID: See Table 6-22 for B0:B4 settings based on ISO protocol in application

Table 6-22. ISO Control Register ISO_x Settings, RFID Mode

ISO_4	ISO_3	ISO_2	ISO_1	ISO_0	PROTOCOL	REMARKS
0	0	0	0	0	ISO/IEC 15693 low bit rate, 6.62 kbps, one subcarrier, 1 out of 4	
0	0	0	0	1	ISO/IEC 15693 low bit rate, 6.62 kbps, one subcarrier, 1 out of 256	
0	0	0	1	0	ISO/IEC 15693 high bit rate, 26.48 kbps, one subcarrier, 1 out of 4	Default for reader
0	0	0	1	1	ISO/IEC 15693 high bit rate, 26.48 kbps, one subcarrier, 1 out of 256	
0	0	1	0	0	ISO/IEC 15693 low bit rate, 6.67 kbps, double subcarrier, 1 out of 4	
0	0	1	0	1	ISO/IEC 15693 low bit rate, 6.67 kbps, double subcarrier, 1 out of 256	
0	0	1	1	0	ISO/IEC 15693 high bit rate, 26.69 kbps, double subcarrier, 1 out of 4	
0	0	1	1	1	ISO/IEC 15693 high bit rate, 26.69 kbps, double subcarrier, 1 out of 256	
0	1	0	0	0	ISO/IEC 14443 A RX bit rate, 106 kbps	RX bit rate (1)
0	1	0	0	1	ISO/IEC 14443 A RX high bit rate, 212 kbps	
0	1	0	1	0	ISO/IEC 14443 A RX high bit rate, 424 kbps	
0	1	0	1	1	ISO/IEC 14443 A RX high bit rate, 848 kbps	
0	1	1	0	0	ISO/IEC 14443 B RX bit rate, 106 kbps	RX bit rate (1)
0	1	1	0	1	ISO/IEC 14443 B RX high bit rate, 212 kbps	
0	1	1	1	0	ISO/IEC 14443 B RX high bit rate, 424 kbps	
0	1	1	1	1	ISO/IEC 14443 B RX high bit rate, 848 kbps	
1	0	0	1	1	Reserved	
1	0	1	0	0	Reserved	
1	1	0	1	0	FeliCa 212 kbps	
1	1	0	1	1	FeliCa 424 kbps	

(1) For ISO/IEC 14443 A or B, when bit rate of TX is different from RX, settings can be done in register 0x02 or 0x03.

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6.14.3.2 Control Registers – Sublevel Configuration Registers

6.14.3.2.1 ISO/IEC 14443 TX Options Register (0x02)

Table 6-23 describes the ISO/IEC 14443 TX Options register.

Table 6-23. ISO/IEC 14443 TX Options Register (0x02)

Function: Selects the ISO subsets for ISO/IEC 14443 – TX			
Default: 0x00 at POR = H or EN = L			
Bit	**Name**	**Function**	**Description**
B7	egt2	TX EGT time select MSB	Three bit code defines the number of etu (0-7) which separate two characters. ISO/IEC 14443 B TX only.
B6	egt1	TX EGT time select	
B5	egt0	TX EGT time select LSB	
B4	eof_l0	1 = EOF→ 0 length 11 etu 0 = EOF→ 0 length 10 etu	ISO/IEC 14443 B TX only
B3	sof_l1	1 = SOF→ 1 length 03 etu 0 = SOF→ 1 length 02 etu	
B2	sof _l0	1 = SOF→ 0 length 11 etu 0 = SOF→ 0 length 10 etu	
B1	l_egt	1 = EGT after each byte 0 = EGT after last byte is omitted	
B0	Reserved		

6.14.3.2.2 ISO/IEC 14443 High-Bit-Rate and Parity Options Register (0x03)

Table 6-24 describes the ISO/IEC 14443 High-Bit-Rate and Parity Options register.

Table 6-24. ISO/IEC 14443 High-Bit-Rate and Parity Options Register (0x03)

Function: Selects the ISO subsets for ISO/IEC 14443 – TX			
Default: 0x00 at POR = H or EN = L, and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	dif_tx_br	TX bit rate different from RX bit rate enable	Valid for ISO/IEC 14443 A or B high bit rate
B6	tx_br1	TX bit rate	tx_br1 = 0, tx_br = 0 → 106 kbps tx_br1 = 0, tx_br = 1 → 212 kbps tx_br1 = 1, tx_br = 0 → 424 kbps tx_br1 = 1, tx_br = 1 → 848 kbps
B5	tx_br0		
B4	parity-2tx	1 = parity odd except last byte which is even for TX	For ISO/IEC 14443 A high bit rate, coding and decoding
B3	parity-2rx	1 = parity odd except last byte which is even for RX	
B2			Unused
B1			Unused
B0			Unused

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6.14.3.2.3 TX Timer High Byte Control Register (0x04)

Table 6-25 describes the TX Timer High Byte Control register.

Table 6-25. TX Timer High Byte Control Register (0x04)

Function: For Timings			
Default: 0xC2 at POR = H or EN = L, and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	tm_st1	Timer Start Condition	tm_st1 = 0, tm_st0 = 0 → beginning of TX SOF tm_st1 = 0, tm_st0 = 1 → end of TX SOF tm_st1 = 1, tm_st0 = 0 → beginning of RX SOF tm_st1 = 1, tm_st0 = 1 → end of RX SOF
B6	tm_st0	Timer Start Condition	
B5	tm_lengthD	Timer Length MSB	
B4	tm_lengthC	Timer Length	
B3	tm_lengthB	Timer Length	
B2	tm_lengthA	Timer Length	
B1	tm_length9	Timer Length	
B0	tm_length8	Timer Length LSB	

6.14.3.2.4 TX Timer Low Byte Control Register (0x05)

Table 6-26 describes the TX Timer Low Byte Control register.

Table 6-26. TX Timer Low Byte Control Register (0x05)

Function: For Timings			
Default: 0x00 at POR = H or EN = L, and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	tm_length7	Timer Length MSB	Defines the time when delayed transmission is started. RX wait range is 590 ns to 9.76 ms (1 to 16383) Step size is 590 ns All bits low = timer disabled (0x00) Preset 0x00 for all other protocols
B6	tm_length6	Timer Length	
B5	tm_length5	Timer Length	
B4	tm_length4	Timer Length	
B3	tm_length3	Timer Length	
B2	tm_length2	Timer Length	
B1	tm_length1	Timer Length	
B0	tm_length0	Timer Length LSB	

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6.14.3.2.5 TX Pulse Length Control Register (0x06)

The length of the modulation pulse is defined by the protocol selected in the ISO Control register 0x01. With a high Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length can be corrected by using the TX Pulse Length Control register (0x06). If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 0x00, the pulse length is equal to the value of the register in 73.7-ns increments. This means the range of adjustment can be 73.7 ns to 18.8 µs.

Table 6-27 describes the TX Pulse Length Control register.

Table 6-27. TX Pulse Length Control Register (0x06)

Function: Controls the length of TX pulse			
Default: 0x00 at POR = H or EN = L and at each write to ISO Control register.			
Bit	**Name**	**Function**	**Description**
B7	Pul_p2	Pulse length MSB	The pulse range is 73.7 ns to 18.8 µs (1….255), step size 73.7 ns. All bits low (00): pulse length control is disabled. The following default timings are preset by the ISO Control register (0x01): 9.44 µs → ISO/IEC 15693 (TI Tag-It HF-I) 11 µs → Reserved 2.36 µs → ISO/IEC 14443 A at 106 kbps 1.4 µs → ISO/IEC 14443 A at 212 kbps 737 ns → ISO/IEC 14443 A at 424 kbps 442 ns → ISO/IEC 14443 A at 848 kbps; pulse length control disabled
B6	Pul_p1		
B5	Pul_p0		
B4	Pul_c4		
B3	Pul_c3		
B2	Pul_c2		
B1	Pul_c1		
B0	Pul_c0	Pulse length LSB	

6.14.3.2.6 RX No Response Wait Time Register (0x07)

The RX No Response timer is controlled by the RX NO Response Wait Time Register 0x07. This timer measures the time from the start of slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in IRQ status control register 0x0C. This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76 µs. This register is also preset, automatically, for every new protocol selection. Sending a Reset FIFO (0x0F) direct command after a TX Complete interrupt will disable this feature.

Table 6-28 describes the RX No Response Wait Time register.

Table 6-28. RX No Response Wait Time Register (0x07)

Function: Defines the time when "no response" interrupt is sent; only for ISO/IEC 15693			
Default: 0x0E at POR = H or EN = L and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	NoResp7	No response MSB	Defines the time when "no response" interrupt is sent. It starts from the end of TX EOF. RX no response wait range is 37.76 µs to 9628 µs (1 to 255), step size is: 37.76 µs. The following default timings are preset by the ISO Control register (0x01): 390 µs → Reserved 529 µs → for all protocols supported, but not listed here 604 µs → Reserved 755 µs → ISO/IEC 15693 high data rate (TI Tag-It HF-I) 1812 µs → ISO/IEC 15693 low data rate (TI Tag-It HF-I)
B6	NoResp6		
B5	NoResp5		
B4	NoResp4		
B3	NoResp3		
B2	NoResp2		
B1	NoResp1		
B0	NoResp0	No response LSB	

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6.14.3.2.7 RX Wait Time Register (0x08)

The RX-wait-time timer is controlled by the value in the RX wait time register 0x08. This timer defines the time after the end of the transmit operation in which the receive decoders are not active (held in reset state). This prevents incorrect detections resulting from transients following the transmit operation. The value of the RX wait time register defines this time in increments of 9.44 µs. This register is preset at every write to ISO Control register 0x01 according to the minimum tag response time defined by each standard.

Table 6-29 describes the RX Wait Time register.

Table 6-29. RX Wait Time Register (0x08)

Function: Defines the time after TX EOF when the RX input is disregarded for example, to block out electromagnetic disturbance generated by the responding card.			
Default: 0x1F at POR = H or EN = L and at each write to*ISO control* register.			
Bit	**Name**	**Function**	**Description**
B7	Rxw7	RX wait time	Defines the time after the TX EOF during which the RX input is ignored. Time starts from the end of TX EOF. RX wait range is 9.44 µs to 2407 µs (1 to 255), Step size 9.44 µs. The following default timings are preset by the ISO Control register (0x01): 9.44 µs → FeliCa 66 µs → ISO/IEC 14443 A and B 180 µs → Reserved 293 µs → ISO/IEC 15693 (TI Tag-It HF-I)
B6	Rxw6		
B5	Rxw5		
B4	Rxw4		
B3	Rxw3		
B2	Rxw2		
B1	Rxw1		
B1	Rxw0		

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6.14.3.2.8 Modulator and SYS_CLK Control Register (0x09)

The frequency of SYS_CLK (pin 27) is programmable by the bits B4 and B5 of this register. The frequency of the TRF7964A system clock oscillator is divided by 1, 2 or 4 resulting in available SYS_CLK frequencies of 13.56 MHz or 6.78 MHz or 3.39 MHz.

The ASK modulation depth is controlled by bits B0, B1 and B2. The range of ASK modulation is 7% to 30% or 100% (OOK). The selection between ASK and OOK (100%) modulation can also be done using direct input OOK (pin 12). The direct control of OOK/ASK using OOK pin is only possible if the function is enabled by setting B6 = 1 (en_ook_p) in this register (0x09) and the ISO Control Register (0x01, B6 = 1). When configured this way, the MOD (pin 14) is used as input for the modulation signal.

Table 6-30 describes the Modulator and SYS_CLK Control register.

Table 6-30. Modulator and SYS_CLK Control Register (0x09)

<table>
<tr><td colspan="6">Function: Controls the modulation input and depth, ASK / OOK control and clock output to external system (MCU)</td></tr>
<tr><td colspan="6">Default: 0x91 at POR = H or EN = L, and at each write to ISO control register, except Clo1 and Clo0.</td></tr>
<tr><th>Bit</th><th>Name</th><th>Function</th><th colspan="3">Description</th></tr>
<tr><td>B7</td><td>27MHz</td><td>Enables 27.12-MHz crystal</td><td colspan="3">Default = 1 (enabled)</td></tr>
<tr><td>B6</td><td>en_ook_p</td><td>1 = Enables external selection of ASK or OOK modulation
0 = Default operation as defined in B0 to B2 (0x09)</td><td colspan="3">Enable ASK/OOK pin (pin 12) for "on the fly change" between any preselected ASK modulation as defined by B0 to B2 and OOK modulation:
If B6 is 1, pin 12 is configured as follows:
1 = OOK modulation
0 = Modulation as defined in B0 to B2 (0x09)</td></tr>
<tr><td rowspan="5">B5</td><td rowspan="5">Clo1</td><td rowspan="5">SYS_CLK output frequency MSB</td><td>Clo1</td><td>Clo0</td><td>SYS_CLK Output (if 13.56-MHz crystal is used)</td><td>SYS_CLK Output (if 27.12-MHz crystal is used)</td></tr>
<tr><td>0</td><td>0</td><td>Disabled</td><td>Disabled</td></tr>
<tr><td>0</td><td>1</td><td>3.39 MHz</td><td>6.78 MHz</td></tr>
<tr><td>1</td><td>0</td><td>6.78 MHz</td><td>13.56 MHz</td></tr>
<tr><td>1</td><td>1</td><td>13.56 MHz</td><td>27.12 MHz</td></tr>
<tr><td>B4</td><td>Clo0</td><td>SYS_CLK output frequency LSB</td><td colspan="3"></td></tr>
<tr><td>B3</td><td>en_ana</td><td>1 = Sets pin 12 (ASK/OOK) as an analog output
0 = Default</td><td colspan="3">For test and measurement purpose. ASK/OOK pin 12 can be used to monitor the analog subcarrier signal before the digitizing with DC level equal to AGND.</td></tr>
<tr><td rowspan="9">B2</td><td rowspan="9">Pm2</td><td rowspan="9">Modulation depth MSB</td><td>Pm2</td><td>Pm1</td><td>Pm0</td><td>Mod Type and %</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>ASK 10%</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>OOK (100%)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ASK 7%</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>ASK 8.5%</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>ASK 13%</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>ASK 16%</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>ASK 22%</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>ASK 30%</td></tr>
<tr><td>B1</td><td>Pm1</td><td>Modulation depth</td><td colspan="3"></td></tr>
<tr><td>B0</td><td>Pm0</td><td>Modulation depth LSB</td><td colspan="3"></td></tr>
</table>

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6.14.3.2.9 RX Special Setting Register (0x0A)

Table 6-31 describes the RX Special Setting register.

Table 6-31. RX Special Setting Register (0x0A)

Function: Sets the gains and filters directly			
Default: 0x40 at POR = H or EN = L, and at each write to the ISO Control register 0x01. When bits B7, B6, B5 and B4 are all zero, the filters are set for ISO/IEC 14443 B (240 kHz to 1.4 MHz).			
Bit	**Name**	**Function**	**Description**
B7	C212	Band-pass 110 kHz to 570 kHz	Appropriate for 212-kHz subcarrier system (FeliCa)
B6	C424	Band-pass 200 kHz to 900 kHz	Appropriate for 424-kHz subcarrier used in ISO/IEC 15693
B5	M848	Band-pass 450 kHz to 1.5 MHz	Appropriate for Manchester-coded 848-kHz subcarrier used in ISO/IEC 14443 A and B
B4	hbt	Band-pass 100 kHz to 1.5 MHz Gain reduced for 18 dB	Appropriate for highest bit rate (848 kbps) used in high-bit-rate ISO/IEC 14443
B3	gd1	00 = Gain reduction 0 dB 01 = Gain reduction for 5 dB 10 = Gain reduction for 10 dB 11 = Gain reduction for 15 dB	Sets the RX gain reduction and reduces sensitivity
B2	gd2		
B1	Reserved		
B0	Reserved		

NOTE

The setting of bits B4, B5, B6 and B7 to 0 selects bandpass characteristic of 240 kHz to 1.4 MHz. This is appropriate for ISO/IEC 14443 B, FeliCa protocol, and ISO/IEC 14443 A higher bit rates of 212 kbps and 424 kbps.

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6.14.3.2.10 Regulator and I/O Control Register (0x0B)

Table 6-32 describes the Regulator and I/O Control register.

Table 6-32. Regulator and I/O Control Register (0x0B)

Function: Control the three voltage regulators			
Default: 0x87 at POR = H or EN = L			
Bit	**Name**	**Function**	**Description**
B7	auto_reg	0 = Manual settings; see B0 to B2 in Table 6-33 and Table 6-34 1 = Automatic setting (see Table 6-35 and Table 6-36)	Auto system sets V_{DD_RF} = V_{IN} – 250 mV and V_{DD_A} = V_{IN} – 250 mV and V_{DD_X}= V_{IN} – 250 mV, but not higher than 3.4 V.
B6	en_ext_pa	Support for external power amplifier	Internal peak detectors are disabled, receiver inputs (RX_IN1 and RX_IN2) accept externally demodulated subcarrier. At the same time ASK/OOK pin 12 becomes modulation output for external TX amplifier.
B5	io_low	1 = enable low peripheral communication voltage	When B5 = 1, maintains the output driving capabilities of the I/O pins connected to the level shifter under low voltage operation. Should be set 1 when $V_{DD_I/O}$ voltage is between 1.8 V to 2.7 V.
B4	Unused	No function	Default is 0.
B3	Unused	No function	Default is 0.
B2	vrs2	Voltage set MSB voltage set LSB	Vrs3_5 = L: V_{DD_RF}, V_{DD_A}, V_{DD_X} range 2.7 V to 3.4 V; see Table 6-33 and Table 6-34
B1	vrs1		
B0	vrs0		

Table 6-33. Supply-Regulator Setting – Manual 5-V System

REGISTER	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2	B1	B0	
00								1	5-V system
0B	0								Manual regulator setting
0B	0					1	1	1	V_{DD_RF} = 5 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					1	1	0	V_{DD_RF} = 4.9 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					1	0	1	V_{DD_RF} = 4.8 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					1	0	0	V_{DD_RF} = 4.7 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					0	1	1	V_{DD_RF} = 4.6 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					0	1	0	V_{DD_RF} = 4.5 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					0	0	1	V_{DD_RF} = 4.4 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					0	0	0	V_{DD_RF} = 4.3 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V

Table 6-34. Supply-Regulator Setting – Manual 3-V System

REGISTER	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2	B1	B0	
00								0	3-V system
0B	0								Manual regulator setting
0B	0					1	1	1	V_{DD_RF} = 3.4 V, V_{DD_A} and V_{DD_X} = 3.4 V
0B	0					1	1	0	V_{DD_RF} = 3.3 V, V_{DD_A} and V_{DD_X} = 3.3 V
0B	0					1	0	1	V_{DD_RF} = 3.2 V, V_{DD_A} and V_{DD_X} = 3.2 V
0B	0					1	0	0	V_{DD_RF} = 3.1 V, V_{DD_A} and V_{DD_X} = 3.1 V
0B	0					0	1	1	V_{DD_RF} = 3.0 V, V_{DD_A} and V_{DD_X} = 3.0 V
0B	0					0	1	0	V_{DD_RF} = 2.9 V, V_{DD_A} and V_{DD_X} = 2.9 V
0B	0					0	0	1	V_{DD_RF} = 2.8 V, V_{DD_A} and V_{DD_X} = 2.8 V
0B	0					0	0	0	V_{DD_RF} = 2.7 V, V_{DD_A} and V_{DD_X} = 2.7 V

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Table 6-35. Supply-Regulator Setting – Automatic 5-V System

REGISTER	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2	B1	B0	
00								1	5-V system
0B	1					x(1)	0	0	Automatic regulator setting 400-mV difference

(1) x = don't care

Table 6-36. Supply-Regulator Setting – Automatic 3-V System

REGISTER	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2	B1	B0	
00								0	3-V system
0B	1					x(1)	0	0	Automatic regulator setting 400-mV difference

(1) x = don't care

6.14.3.3 Status Registers

6.14.3.3.1 IRQ Status Register (0x0C)

Table 6-37 describes the IRQ Status register.

Table 6-37. IRQ Status Register (0x0C)

Function: Information available about TRF7964A IRQ and TX/RX status			
Default: 0x00 at POR = H or EN = L, and at each write to the ISO Control Register 0x01. It is also automatically reset at the end of a read phase. The reset also removes the IRQ flag.			
Bit	**Name**	**Function**	**Description**
B7	Irq_tx	IRQ set due to end of TX	Signals that TX is in progress. The flag is set at the start of TX but the interrupt request (IRQ = 1) is sent when TX is finished.
B6	Irg_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX but the interrupt request (IRQ = 1) is sent when RX is finished.
B5	Irq_fifo	Signals the FIFO level	Signals FIFO high or low as set in the Adjustable FIFO IRQ Levels (0x14) register
B4	Irq_err1	CRC error	Indicates receive CRC error only if B7 (no RX CRC) of ISO Control register is set to 0.
B3	Irq_err2	Parity error	Indicates parity error for ISO/IEC 14443 A
B2	Irq_err3	Byte framing or EOF error	Indicates framing error
B1	Irq_col	Collision error	Collision error for ISO/IEC 14443 A and ISO/IEC 15693 single subcarrier. Bit is set if more then 6 or 7 (as defined in register 0x10) are detected in 1 bit period of ISO/IEC 14443 A 106 kbps. Collision error bit can also be triggered by external noise.
B0	Irq_noresp	No response time interrupt	No response within the "No-response time" defined in RX No Response Wait Time register (0x07). Signals the MCU that the next slot command can be sent. Only for ISO/IEC 15693.

To reset (clear) the register 0x0C and the IRQ line, the register must be read. During Transmit the decoder is disabled, only bits B5 and B7 can be changed. During Receive only bit B6 can be changed, but does not trigger the IRQ line immediately. The IRQ signal is set at the end of Transmit and Receive phase.

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6.14.3.3.2 Interrupt Mask Register (0x0D) and Collision Position Register (0x0E)

Table 6-38 describes the Interrupt Mask register. Table 6-39 describes the Collision Position register.

Table 6-38. Interrupt Mask Register (0x0D)

Default: 0x3E at POR = H and EN = L. Collision bits reset automatically after read operation.			
Bit	**Name**	**Function**	**Description**
B7	Col9	Bit position of collision MSB	Supports ISO/IEC 14443 A
B6	Col8	Bit position of collision	
B5	En_irq_fifo	Interrupt enable for FIFO	Default = 1
B4	En_irq_err1	Interrupt enable for CRC	Default = 1
B3	En_irq_err2	Interrupt enable for Parity	Default = 1
B2	En_irq_err3	Interrupt enable for Framing error or EOF	Default = 1
B1	En_irq_col	Interrupt enable for collision error	Default = 1
B0	En_irq_noresp	Enables no-response interrupt	Default = 0

Table 6-39. Collision Position Register (0x0E)

Function: Displays the bit position of collision or error			
Default: 0x00 at POR = H and EN = L. Automatically reset after read operation.			
Bit	**Name**	**Function**	**Description**
B7	Col7	Bit position of collision MSB	ISO/IEC 14443 A mainly supported, in the other protocols this register shows the bit position of error. Frame, SOF, EOF, parity, or CRC error.
B6	Col6		
B5	Col5		
B4	Col4		
B3	Col3		
B2	Col2		
B1	Col1		
B0	Col0	Bit position of collision LSB	

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6.14.3.3.3 RSSI Levels and Oscillator Status Register (0x0F)

Table 6-40 describes the RSSI Levels and Oscillator Status register.

Table 6-40. RSSI Levels and Oscillator Status Register (0x0F)

Function: Displays the signal strength on both reception channels and RF amplitude during RF-off state. The RSSI values are valid from reception start till start of next transmission.			
Bit	**Name**	**Function**	**Description**
B7	Unused		
B6	osc_ok	Crystal oscillator stable indicator	13.56-MHz frequency stable (approximately 200 µs)
B5	rssi_x2	MSB RSSI value of auxiliary RX (RX_IN2)	Auxiliary channel is by default RX_IN2. The input can be swapped by B3 = 1 (Chip Status Control register 0x00). If "swapped", the Auxiliary channel is connected to RX_IN1 and, hence, the Auxiliary RSSI represents the signal level at RX_IN1.
B4	rssi_x1	Auxiliary channel RSSI	
B3	rssi_x0	MSB RSSI value of auxiliary RX (RX_IN2)	
B2	rssi_2	MSB RSSI value of main RX (RX_IN1)	Active channel is default and can be set with option bit B3 = 0 of Chip Status Control register 0x00.
B1	rssi_1	Main channel RSSI	
B0	rssi_0	LSB RSSI value of main RX (RX_IN1)	

RSSI measurement block is measuring the demodulated envelope signal (except in case of direct command for RF amplitude measurement described later in direct commands section). The measuring system is latching the peak value, so the RSSI level can be read after the end of receive packet. The RSSI value is reset during next transmit action of the reader, so the new tag response level can be measured. The RSSI levels calculated to the RF_IN1 and RF_IN2 are presented in Section 6.5.1.1 and Section 6.5.1.2. The RSSI has 7 steps (3 bits) with 4-dB increment. The input level is the peak-to-peak modulation level of RF signal measured on one side envelope (positive or negative).

6.14.3.3.4 Special Functions Register (0x10)

Table 6-41 describes the Special Functions register at address 0x10.

Table 6-41. Special Functions Register (0x10)

Function: User configurable options for ISO/IEC 14443 A specific operations			
Bit	**Name**	**Function**	**Description**
B7		Reserved	Reserved
B6		Reserved	Reserved
B5	par43	Disables parity checking for ISO/IEC 14443 A	
B4	next_slot_37us	0 = 18.88 µs 1 = 37.77 µs	Sets the time grid for next slot command in ISO/IEC 15693
B3	Sp_dir_mode	Bit stream transmit for MIFARE at 106 kbps	Enables direct mode for transmitting ISO/IEC 14443 A data, bypassing the FIFO and feeding the data bit stream directly onto the encoder.
B2	4_bit_RX	0 = normal receive 1 = 4-bit receive	Enable 4-bit replay for example, ACK, NACK used by some cards; for example, MIFARE Ultralight
B1	14_anticoll	0 = anticollision framing (0x93, 0x95, 0x97) 1 = normal framing (no broken bytes)	Disable anticollision frames for ISO/IEC 14443 A (this bit should be set to 1 after anticollision is finished)
B0	col_7_6	0 = 7 subcarrier pulses 1 = 6 subcarrier pulses	Selects the number of subcarrier pulses that trigger collision error in ISO/IEC 14443 A at 106 kbps

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6.14.3.3.5 Special Functions Register (0x11)

Table 6-42 describes the Special Functions register at address 0x11.

Table 6-42. Special Functions Register (0x11)

Function: Indicate IRQ status for RX operations.			
Bit	**Name**	**Function**	**Description**
B7	Reserved		Reserved
B6	Reserved		Reserved
B5	Reserved		Reserved
B4	Reserved		Reserved
B3	Reserved		Reserved
B2	Reserved		Reserved
B1	Reserved		Reserved
B0	irg_srx	Copy of the RX start signal (Bit 6) of the IRQ Status register (0x0C)	Signals the RX SOF was received and the RX is in progress. IRQ when RX is completed.

6.14.3.3.6 Adjustable FIFO IRQ Levels Register (0x14)

Table 6-43 describes the Adjustable FIFO IRQ Levels register.

Table 6-43. Adjustable FIFO IRQ Levels Register (0x14)

Function: Adjusts level at which FIFO indicates status by IRQ					
Default: 0x00 at POR = H and EN = L					
Bit	**Name**	**Function**	**Description**		
B7	Reserved		Reserved		
B6	Reserved		Reserved		
B5	Reserved		Reserved		
B4	Reserved		Reserved		
B3	Wlh_1	FIFO high IRQ level (during RX)	**Wlh_1** 0 0 1 1	**Wlh_0** 0 1 0 1	**IRQ Level** 124 120 112 96
B2	Wlh_0				
B1	Wll_1	FIFO low IRQ level (during TX)	**Wll_1** 0 0 1 1	**Wll_0** 0 1 0 1	**IRQ Level** 4 8 16 32
B0	Wll_0				

6.14.3.4 Test Registers

6.14.3.4.1 Test Register (0x1A)

Table 6-44 describes the Test register at address 0x1A.

Table 6-44. Test Register (0x1A) (for Test or Direct Use)

Default: 0x00 at POR = H and EN = L.			
Bit	**Name**	**Function**	**Description**
B7	OOK_Subc_In	Subcarrier input	OOK pin becomes decoder digital input
B6	MOD_Subc_Out	Subcarrier output	MOD pin becomes receiver digitized subcarrier output
B5	MOD_Direct	Direct TX modulation and RX reset	MOD pin becomes input for TX modulation control by the MCU
B4	o_sel	First stage output selection	o_sel = L: First stage output used for analog out and digitizing o_sel = H: Second Stage output used for analog out and digitizing
B3	low2	Second stage gain –6 dB, HP corner frequency / 2	
B2	low1	First stage gain –6 dB, HP corner frequency / 2	
B1	zun	Input followers test	
B0	Test_AGC	AGC test, AGC level is seen on rssi_210 bits	

6.14.3.4.2 Test Register (0x1B)

Table 6-45 describes the Test register at address 0x1B.

Table 6-45. Test Register (0x1B) (for Test or Direct Use)

Default: 0x00 at POR = H and EN = L. When a test_dec or test_io is set IC is switched to test mode. Test Mode persists until a stop condition arrives. At stop condition the test_dec and test_io bits are cleared.			
Bit	**Name**	**Function**	**Description**
B7	test_rf_level	RF level test	
B6			
B5			
B4			
B3	test_io1	I/O test	Not implemented
B2	test_io0		
B1	test_dec	Decoder test mode	
B0	clock_su	Coder clock 13.56 MHz	For faster test of coders

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6.14.3.5 FIFO Control Registers

Section 6.14.3.5.1 describes the FIFO Status register.

6.14.3.5.1 FIFO Status Register (0x1C)

Table 6-46. FIFO Status Register (0x1C)

Function: Number of bytes available to be read from FIFO (= N number of bytes, in hexadecimal)			
Bit	**Name**	**Function**	**Description**
B7	Foverflow	FIFO overflow error	Bit is set when FIFO has more than 127 bytes presented to it
B6	Fb6	FIFO bytes fb[6]	Bits B0:B6 indicate how many bytes are in the FIFO to be read out (= N number of bytes, in hex)
B5	Fb5	FIFO bytes fb[5]	
B4	Fb4	FIFO bytes fb[4]	
B3	Fb3	FIFO bytes fb[3]	
B2	Fb2	FIFO bytes fb[2]	
B1	Fb1	FIFO bytes fb[1]	
B0	Fb0	FIFO bytes fb[0]	

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6.14.3.5.2 TX Length Byte1 Register (0x1D), TX Length Byte2 Register (0x1E)

Table 6-47 describes the TX Length Byte1 register. Table 6-48 describes the TX Length Byte2 register.

Table 6-47. TX Length Byte1 Register (0x1D)

Function: High 2 nibbles of complete, intended bytes to be transferred through FIFO			
Register default is set to 0x00 at POR and EN = 0. It is also automatically reset at TX EOF			
Bit	**Name**	**Function**	**Description**
B7	TxI11	Number of complete byte bn[11]	High nibble of complete, intended bytes to be transmitted
B6	TxI10	Number of complete byte bn[10]	
B5	TxI9	Number of complete byte bn[9]	
B4	TxI8	Number of complete byte bn[8]	
B3	TxI7	Number of complete byte bn[7]	Middle nibble of complete, intended bytes to be transmitted
B2	TxI6	Number of complete byte bn[6]	
B1	TxI5	Number of complete byte bn[5]	
B0	TxI4	Number of complete byte bn[4]	

Table 6-48. TX Length Byte2 Register (0x1E)

Function: Low nibbles of complete bytes to be transferred through FIFO; Information about a broken byte and number of bits to be transferred from it			
Default: 0x00 at POR and EN = 0. It is also automatically reset at TX EOF			
Bit	**Name**	**Function**	**Description**
B7	TxI3	Number of complete byte bn[3]	Low nibble of complete, intended bytes to be transmitted
B6	TxI2	Number of complete byte bn[2]	
B5	TxI1	Number of complete byte bn[1]	
B4	TxI0	Number of complete byte bn[0]	
B3	Bb2	Broken byte number of bits bb[2]	Number of bits in the last broken byte to be transmitted. Valid only when broken byte flag is set.
B2	Bb1	Broken byte number of bits bb[1]	
B1	Bb0	Broken byte number of bits bb[0]	
B0	Bbf	Broken byte flag	B0 = 1 indicates that last byte is not complete 8 bits wide.

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7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 TRF7964A Reader System Using SPI With SS Mode

7.1.1 General Application Considerations

Figure 7-1 shows and application schematic optimized for all TRF7964A modes using the Serial Port Interface (SPI). Short SPI lines, proper isolation of radio frequency lines, and a proper ground area are essential to avoid interference. The recommended clock frequency on the DATA_CLK line is 2 MHz. This figure also shows matching to a 50-Ω port, which allows connecting to a properly matched 50-Ω antenna circuit or RF measurement equipment (for example, a spectrum analyzer or power meter).

7.1.2 Schematic

Figure 7-1 shows a sample application schematic for SPI with an SS mode MCU interface.

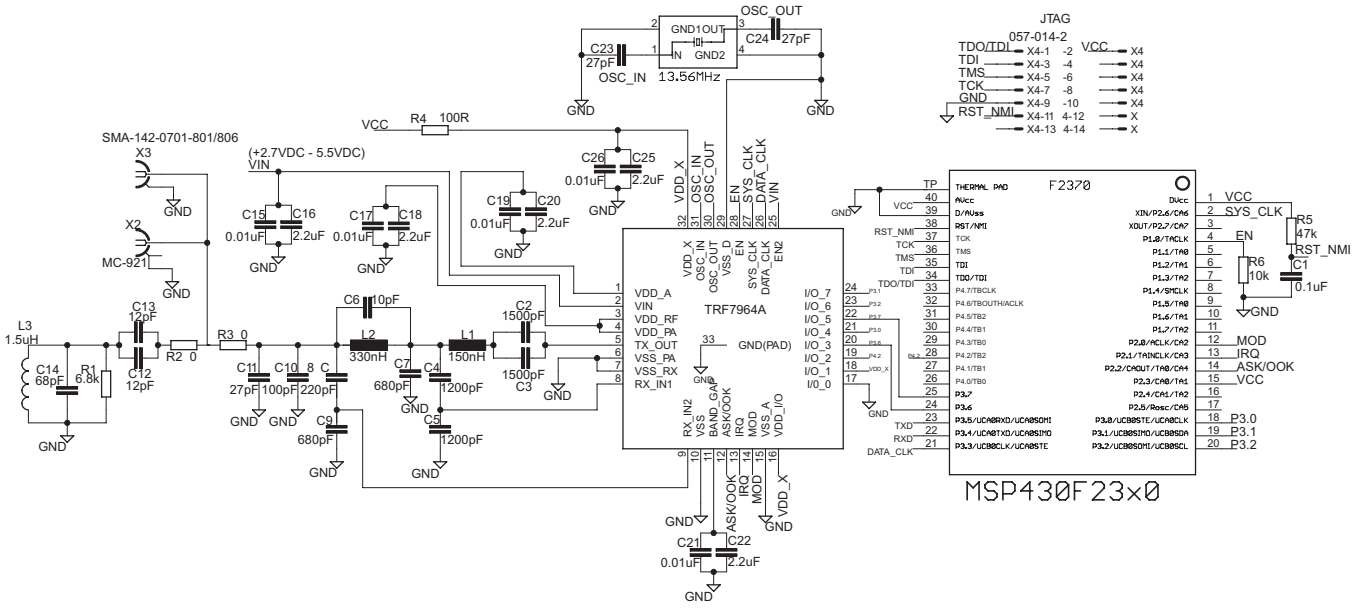


Figure 7-1. Application Schematic – SPI With SS Mode MCU Interface

Minimum MCU requirements depend on application requirements and coding style. If only one ISO protocol or a limited command set of a protocol needs to be supported, MCU Flash and RAM requirements can be significantly reduced. Recursive inventory and anticollision commands require more RAM than single slotted operations. For example, an ISO/IEC 15693-only application that supports anticollision needs approximately 7KB of flash memory and 500 bytes of RAM. In contrast, a full NFC stack that supports peer-to-peer, card emulation, and reader/writer modes needs 65KB of flash memory and 4KB of RAM. An MCU that can run its GPIOs at 13.56 MHz is required for direct mode 0 operations.

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7.2 Layout Considerations

Keep all decoupling capacitors as close to the IC as possible, with the high-frequency decoupling capacitors (10 nF) closer than the low-frequency decoupling capacitors (2.2 µF).

Place ground vias as close as possible to the ground side of the capacitors and reader IC pins to minimize possible ground loops.

TI recommends not using any inductor sizes smaller than 0603, as the output power can be compromised. If smaller inductors are necessary, output performance must be confirmed in the final application.

Pay close attention to the required load capacitance of the crystal, and adjust the two external shunt capacitors accordingly. Follow the recommendations of the crystal manufacturer for those values.

There should be a common ground plane for the digital and analog sections. The multiple ground sections or islands should have vias that tie the different sections of the planes together.

Ensure that the exposed thermal pad at the center of the reader IC is properly laid out. It should be tied to ground to help dissipate any heat from the package.

All trace line lengths should be made as short as possible, particularly the RF output path, crystal connections, and control lines from the reader to the microprocessor. Proper placement of the TRF7964A, microprocessor, crystal, and RF connection or connector help facilitate this.

Avoid crossing of digital lines under RF signal lines. Also, avoid crossing of digital lines with other digital lines when possible. If the crossings are unavoidable, 90° crossings should be used to minimize coupling of the lines.

Depending on the production test plan, consider possible implementations of test pads or test vias for use during testing. The necessary pads or vias should be placed in accordance with the proposed test plan to enable easy access to those test points.

If the system implementation is complex (for example, if the RFID reader module is a subsystem of a greater system with other modules (microprocessors and clocks), special considerations should be taken to ensure that there is no noise coupling into the supply lines. If needed, special filtering or regulator considerations should be used to minimize or eliminate noise in these systems.

For more information/details on layout considerations, see the *TRF796x HF-RFID Reader Layout Design Guide*.

7.3 Impedance Matching TX_Out (Pin 5) to 50 Ω

The output impedance of the TRF7964A when operated at full power out setting is nominally 4 + j0 (4 Ω real). This impedance must be matched to a resonant circuit and TI recommends matching circuit from 4 Ω to 50 Ω, as commercially available test equipment (for example, spectrum analyzers, power meters, and network analyzers) are 50-Ω systems. Figure 7-2 shows an impedance-matching reference circuit. Figure 7-3 shows a Smith chart simulation based on this circuit. This section explains how the values were calculated.

Starting with the 4-Ω source, the process of going from 4 Ω to 50 Ω can be represented on a Smith Chart simulator (available from http://www.fritz.dellsperger.net/). The elements are combined where appropriate (see Figure 7-2).

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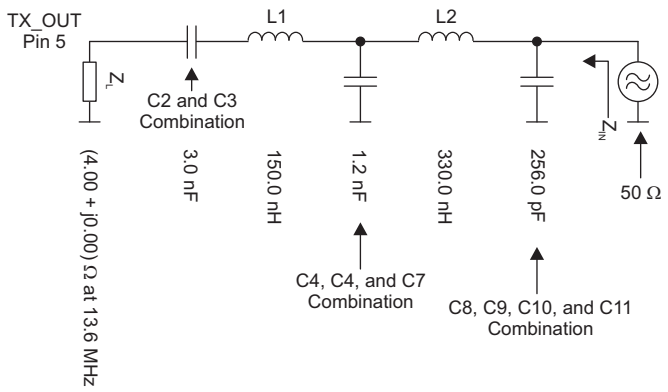


Figure 7-2. Impedance Matching Circuit

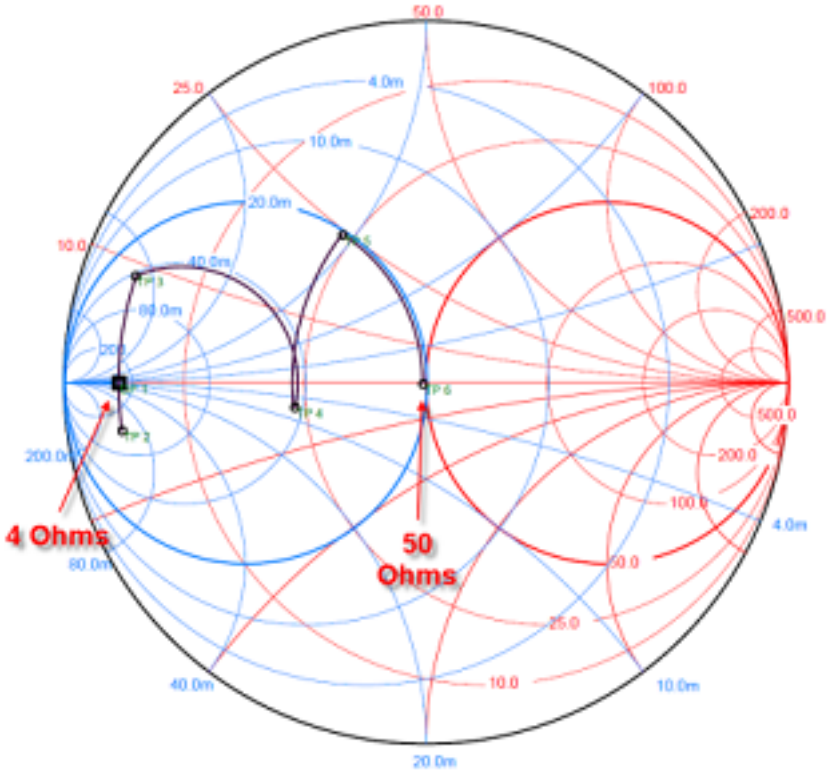


Figure 7-3. Smith Chart Simulation

Resulting power out can be measured with a power meter or spectrum analyzer with power meter function or other equipment capable of making a "hot" measurement. Observe maximum power input levels on test equipment and use attenuators whenever available to avoid damage to equipment. Expected output power levels under various operating conditions are shown in Table 6-20.

7.4 Reader Antenna Design Guidelines

For HF antenna design considerations using the TRF7964A, see these documents:

- Antenna Design Guide for the TRF79xxA

8 Device and Documentation Support

8.1 Getting Started and Next Steps

For more information on the TI NFC/RFID devices and the tools and software that are available to help with your development, visit Overview for NFC / RFID.

8.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of devices. Each commercial family member has one of three prefixes: x, p, or no prefix. These prefixes represent evolutionary stages of product development from engineering prototypes (with prefix x) through fully qualified production devices (with no prefix).

Device development evolutionary flow:

xTRF... – Experimental device that is not necessarily representative of the electrical specifications of the final device

pTRF... – Final device that conforms to the electrical specifications of the final product but has not completed quality and reliability verification

TRF... – Fully qualified production device

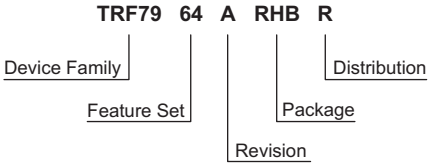
Devices with a prefix of **x** or **p** are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type and, optionally, the temperature range. Figure 8-1 provides a legend for reading the complete device name.



Device Family	TRF79 = NFC/RFID Transceiver
Feature Set	64 = Feature Set
Revision	A = Silicon Revision
Package	See Packaging Information or www.ti.com/package
Distribution	R = Large Reel T = Small Reel

Figure 8-1. Device Nomenclature

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8.3 Tools and Software

Design Kits and Evaluation Modules

NFC Transceiver Booster Pack Plug-in Module The third-party provider DLP Design NFC/RFID BoosterPack plug-in module (DLP-7970ABP) is an add-on board designed to fit all of TI's MCU LaunchPad development kits. This BoosterPack plug-in module lets the software application developer get familiar with the functionality of the TRF7970A multiprotocol fully integrated 13.56 MHz NFC and HF RFID IC on their TI embedded microcontroller platform of choice without having to worry about developing the RF section.

8.4 Documentation Support

The following documents describe the TRF7964A device. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for example, TRF7964A). In the upper-right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Application Notes

Minimizing TRF79xx Current Use During Power-Down Mode This application report provides recommendations on circuit and firmware design to reduce current consumption in power-down mode for the TRF79xx family of devices (TRF796x, TRF796xA, and TRF7970A). Various designs are considered, and they are analyzed based on their current consumption. This application report is particularly targeted for dual-voltage systems that are powered by battery.

NFC/HF RFID Reader/Writer Using the TRF7970A The near field communication (NFC) market is emerging into multiple fields including medical, consumer, retail, industrial, automotive, and smart grid. Reader/writer is one of the three operational modes supported by the TRF7970A. When using reader/writer mode, the user can configure the TRF7970A to read type 2, type 3, type 4A, type 4B, and type 5 tag platforms, also called transponders. The tags can store NFC data exchange format (NDEF) messages or proprietary defined data. This application report describes the fundamental concepts of reader/writer mode and how to properly configure the TRF7907A transceiver for each supported technology.

TRF7970A NFC Reader Antenna Multiplexing This application report describes the implementation of multiple reader antennas with a single TRF7970A NFC transceiver IC. For demonstration purposes, the MSP430F5529 LaunchPad development kit with TRF7970A BoosterPack plug-in module are used. The demo supports ISO/IEC 15693, and ISO/IEC 14443 A and B communication protocols.

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NFC/RFID Reader Ultra-Low-Power Card Presence Detect With MSP430 and TRF79xxA NFC and RFID reader battery-powered applications must have a defined and limited energy consumption budget as well as low cost for a product to be realized. Techniques and strategies have emerged over the years for the card presence detection that attempt to address both concerns. The intent of this application report is to contribute to these techniques and strategies by offering an advancement expressed by adding a simple circuit and small firmware control logic loop to an existing design, which offers dramatic improvement over previously identified card detection solutions.

8.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.6 Trademarks

E2E is a trademark of Texas Instruments.
MIFARE is a trademark of NXP Semiconductors.
FeliCa is a trademark of Sony Corporation.

8.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF7964ARHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	TRF 7964A	Samples
TRF7964ARHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	TRF 7964A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

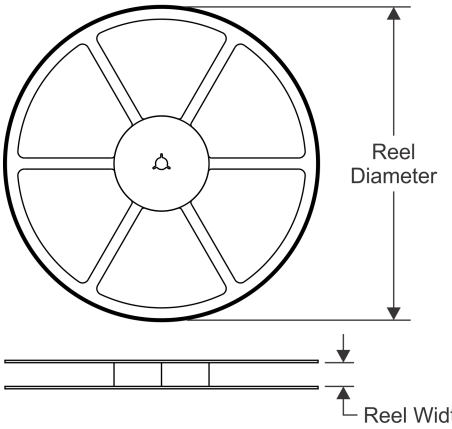
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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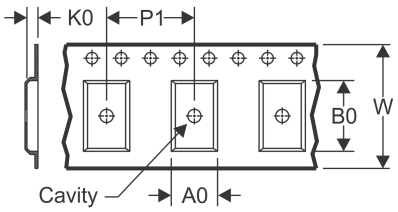
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

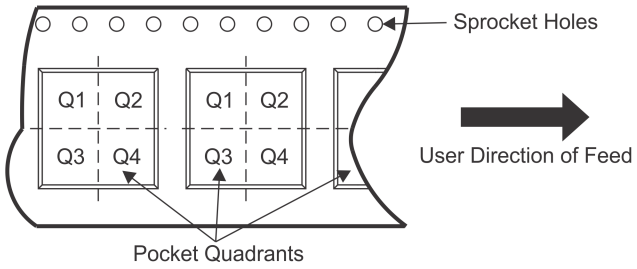


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

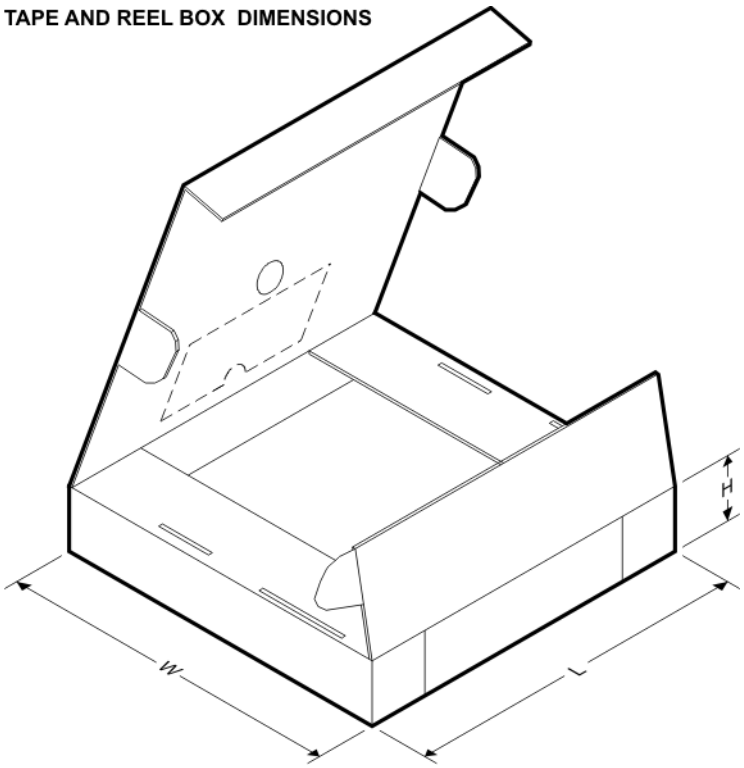
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF7964ARHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF7964ARHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF7964ARHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TRF7964ARHBT	VQFN	RHB	32	250	210.0	185.0	35.0

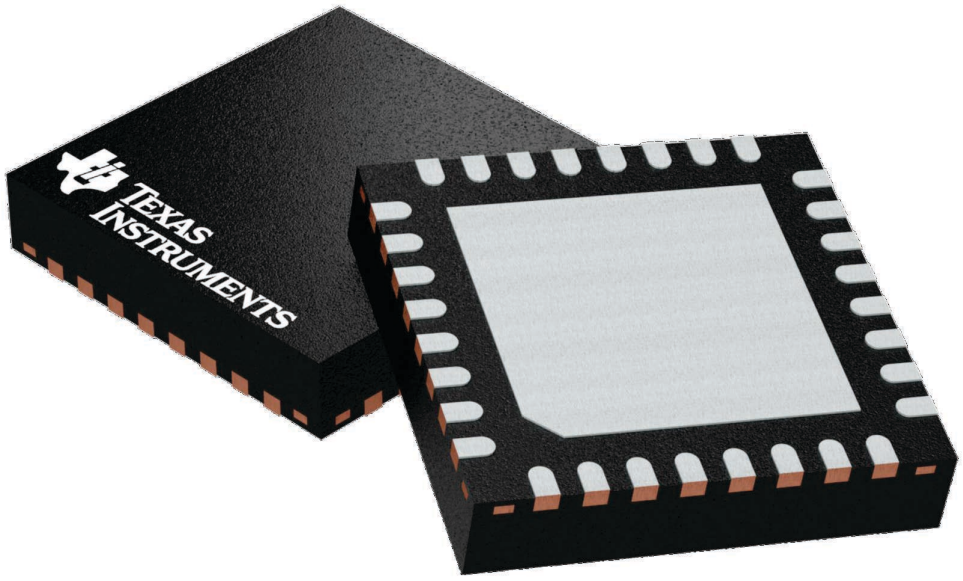
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

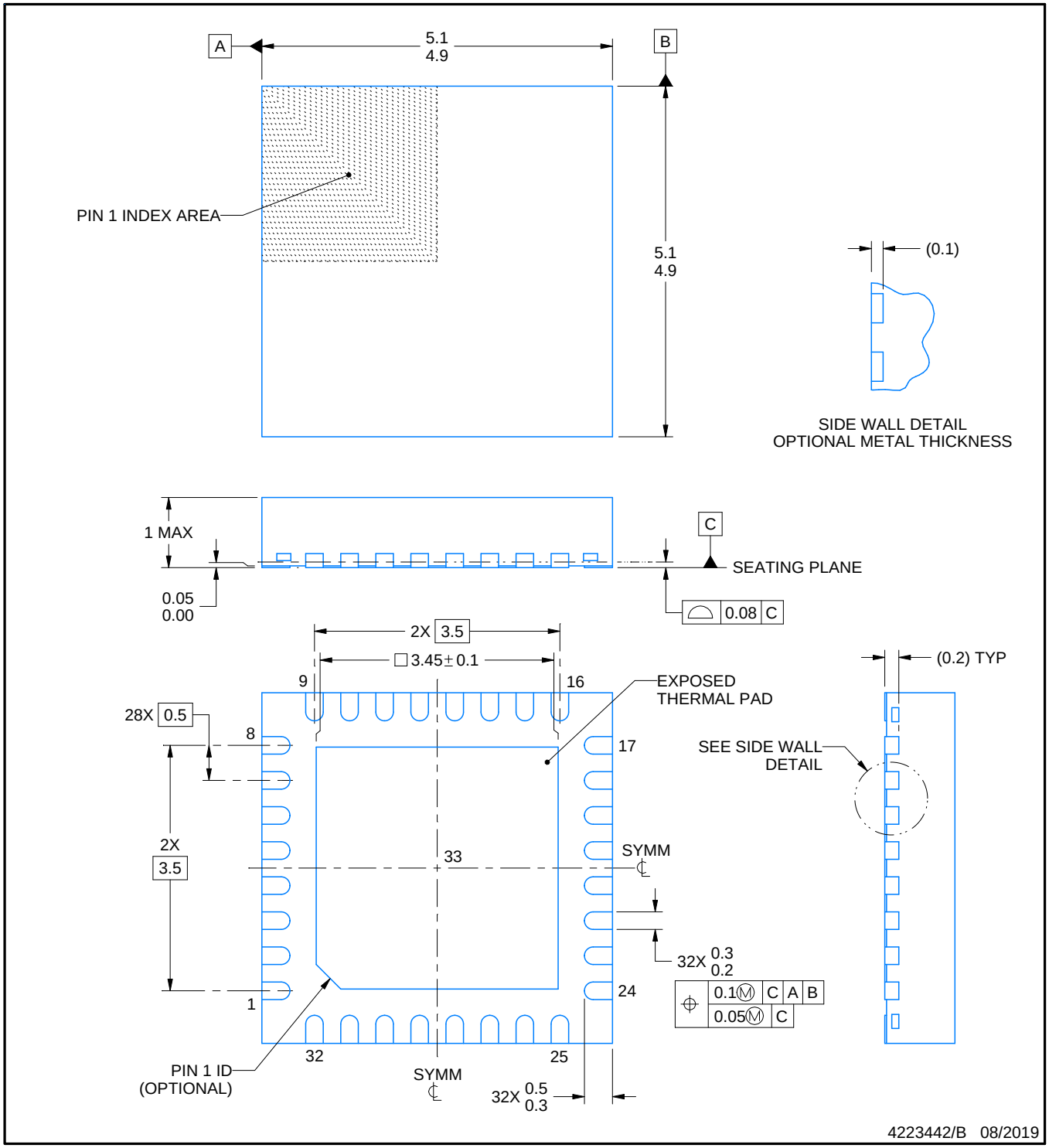
4224745/A

RHB0032E

PACKAGE OUTLINE

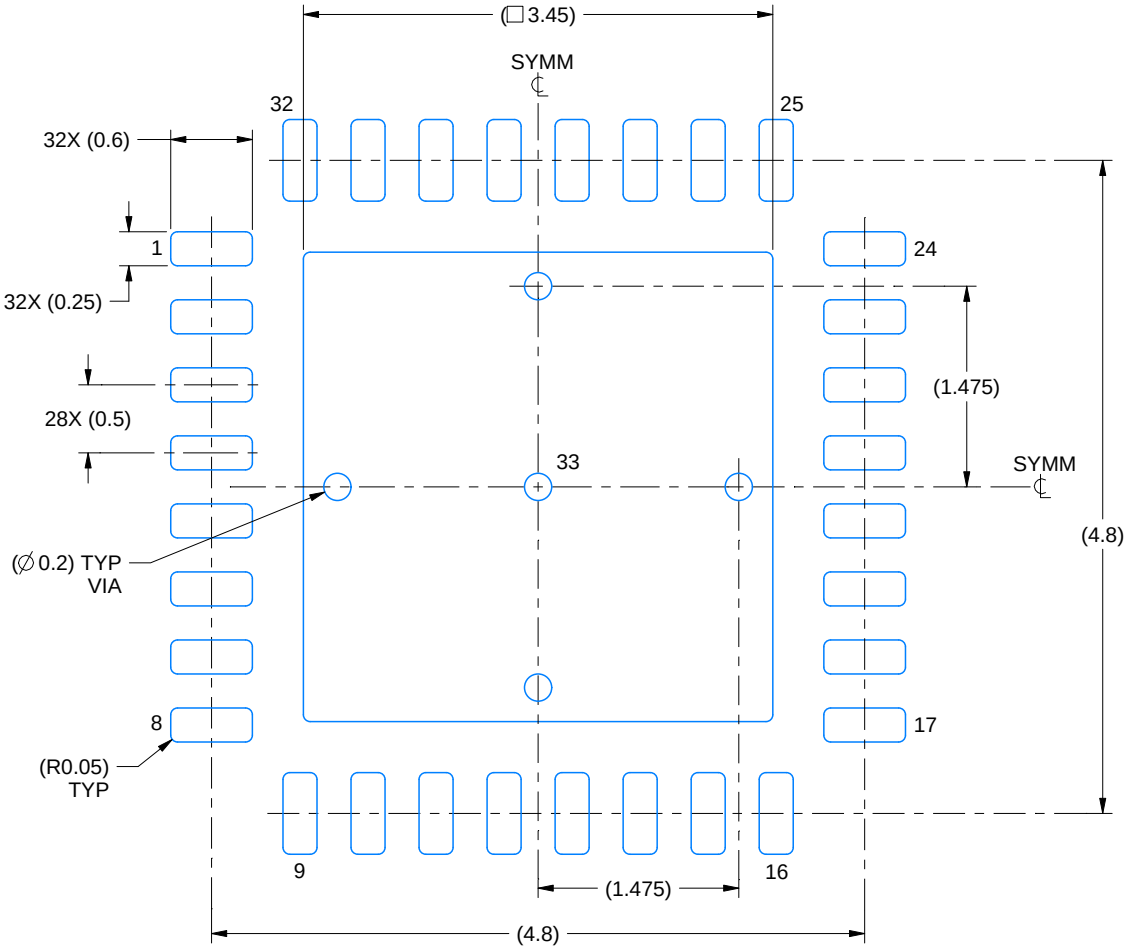
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

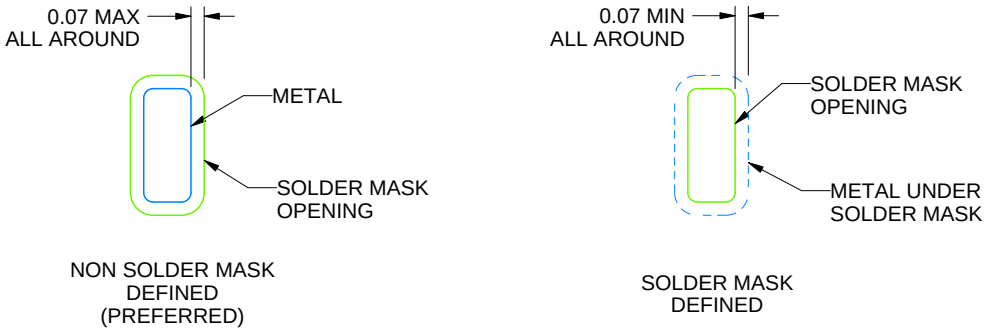


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

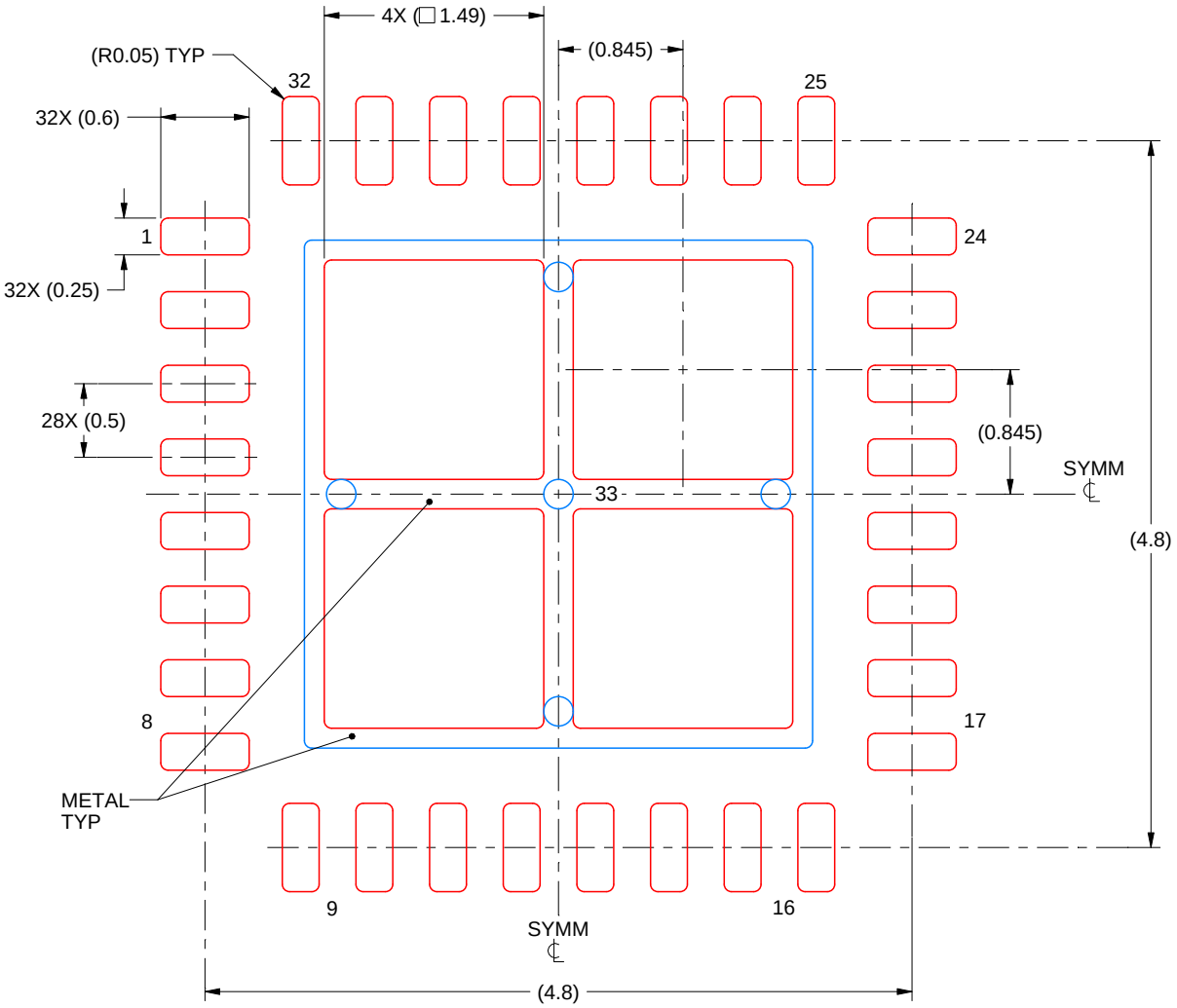


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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