# TRF37D73 1-6000 MHz RF Gain Block

## 1 Features

- 1 MHz – 6000 MHz
- Gain: 19.5 dB
- Noise Figure: 3.25 dB
- Output P1dB: 16.5 dBm at 2000 MHz
- Output IP3: 28 dBm at 2000 MHz
- Power Down Mode
- Single Supply: 3.3 V
- Stabilized Performance Over Temperature
- Unconditionally Stable
- Robust ESD: >1 kV HBM; >1 kV CDM

## 2 Applications

- General Purpose RF Gain Block
- Consumer
- Industrial
- Utility Meters
- Low-cost Radios
- Cellular Base Station
- Wireless Infrastructure
- RF Backhaul
- Radar
- Electronic Warfare
- Software-defined Radio
- Test and Measurement
- Point-to-Point/Multipoint Microwave
- Software Defined Radios
- RF Repeaters
- Distributed Antenna Systems
- LO and PA Driver Amplifier
- Wireless Data, Satellite, DBS, CATV
- IF Amplifier

## 3 Description

The TRF37D73 is packaged in a 2.00mm x 2.00mm WSON with a power down pin feature making it ideal for applications where space and low power modes are critical.

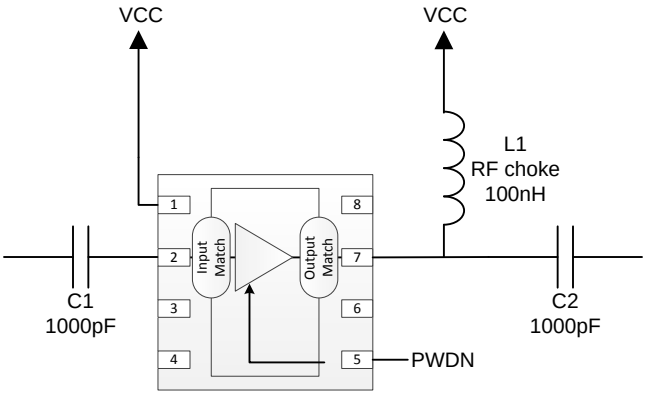
The TRF37D73 is designed for ease of use. For maximum flexibility, this family of parts uses a common 3.3 V supply and consumes 53 mA. In addition, this family was designed with an active bias circuit that provides a stable and predictable bias current over process, temperature and voltage variations. For gain and linearity budgets the device was designed to provide a flat gain response and excellent OIP3 out to 6000 MHz. For space constrained applications, this family is internally matched to 50 Ω, which simplifies ease of use and minimizes needed PCB area.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TRF37D73 | WSON (32) | 2.00mm x 2.00mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Schematic**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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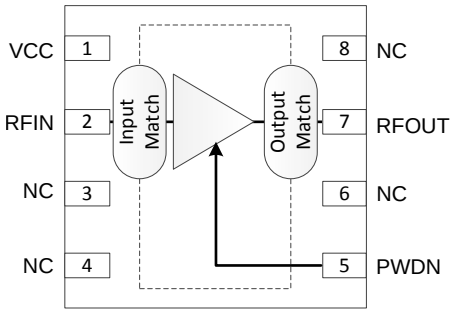
## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| May 2014 | * | Initial release. |


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# 5 Pin Configuration and Functions

**DSG PACKAGE**
**(TOP VIEW)**




**Pin Functions**

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| VCC | 1 | DC Bias. |
| RFIN | 2 | RF input. Connect to an RF source through a DC-blocking capacitor. Internally matched to 50 Ω. |
| NC | 3, 4, 6, 8 | No electrical connection. Connect pad to GND for board level reliability integrity. |
| PWDN | 5 | When high the device is in power down state. When LOW or NC the device is in active state. Internal pulldown resistor to GND. |
| RFOUT | 7 | RF Output and DC Bias ($V_{CC}$). Connect to DC supply through an RF choke inductor. Connect to output load through a DC-blocking capacitor. Internally matched to 50 Ω. |
| GND | PowerPAD™ | RF and DC GND. Connect to PCB ground plane. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply Input voltage | –0.3 | 3.6 | V |
| Input Power | | 10 | dBm |
| Operating virtual junction temperature range | –40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{ESD}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1) | –1 | 1 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2) | –1 | 1 | kV |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage, $V_{CC}$ | 3 | 3.3 | 3.45 | V |
| Operating junction temperature, $T_J$ | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | DSG | UNIT |
|---|---|---|---|
| | | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 79.3 | °C/W |
| $R_{\theta JCtop}$ | Junction-to-case (top) thermal resistance | 110 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 49.4 | |
| $R_{\theta JCbot}$ | Junction-to-case (bottom) thermal resistance | 19.2 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.


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## 6.5 Electrical Characteristics

$V_{CC}$ = 3V3, $T_A$ = 25°C, PWDN = Low, $L_{OUT}$ = 100 nH, C1 = C2 = 1000 pF, $Z_S$ = $Z_L$ = 50 Ω (unless otherwise noted)

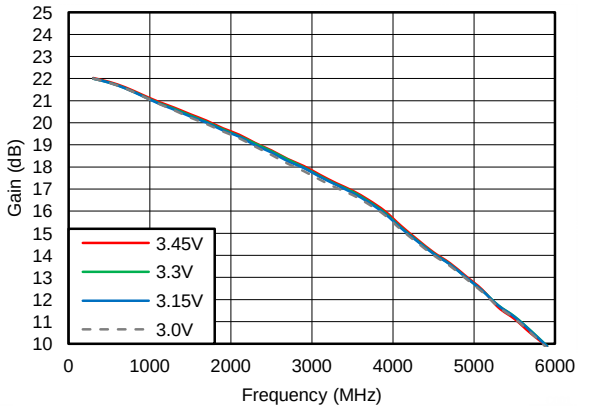
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC PARAMETERS** | | | | | | |
| $I_{CC}$ | Total supply current | | | 53 | 65 | mA |
| | Power down current | PWDN = High | | 125 | | µA |
| $P_{diss}$ | Power dissipation | | | 0.175 | | W |
| **RF REQUENCY RANGE** | | | | | | |
| | Frequency range | | 1 | | 6000 | MHz |
| G | Small signal gain | $f_{RF}$ = 400 MHz | | 22 | | dB |
| | | $f_{RF}$ = 2000 MHz | | 19.5 | | dB |
| | | $f_{RF}$ = 3000 MHz | | 18 | | dB |
| | | $f_{RF}$ = 4000 MHz | | 15.5 | | dB |
| | | $f_{RF}$ = 5000 MHz | | 13 | | dB |
| | | $f_{RF}$ = 6000 MHz | | 10 | | dB |
| OP1dB | Output 1dB compression point | At 2000 MHz | | 16.5 | | dBm |
| OIP3 | Output 3rd order intercept point | At 2000 MHz, 2-tone 10 MHz apart | | 27.5 | | dBm |
| NF | Noise figure | At 2000 MHz | | 3.25 | | dB |
| $R_{(LI)}$ | Input return loss | At 2000 MHz | | 20 | | dB |
| $R_{(LO)}$ | Output return loss | At 2000 MHz | | 12 | | dB |
| **PWDN PIN** | | | | | | |
| $V_{IH}$ | High level input level | | 2 | | | V |
| $V_{IL}$ | Low level input level | | | | 0.8 | V |
| $I_{IH}$ | High level input current | | | 30 | | µA |
| $I_{IL}$ | Low level input current | | | 1 | | µA |

## 6.6 Timing Requirements

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PWDN PIN** | | | | | | |
| $t_{ON}$ | Turn-on Time | 50% TTL to 90% $P_{OUT}$ | | 0.6 | | µs |
| $t_{OFF}$ | Turn-off Time | 50% TTL to 10% $P_{OUT}$ | | 1.4 | | µs |

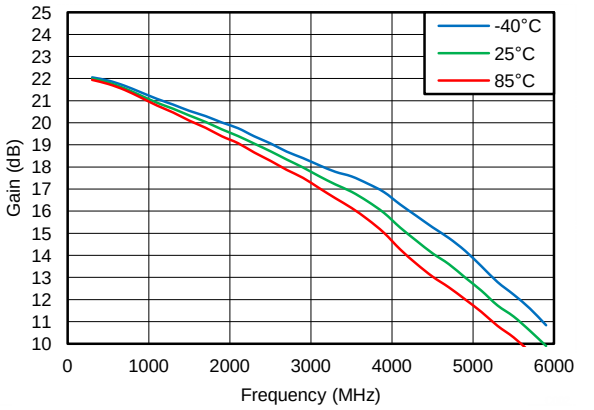
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## 6.7 Typical Characteristics



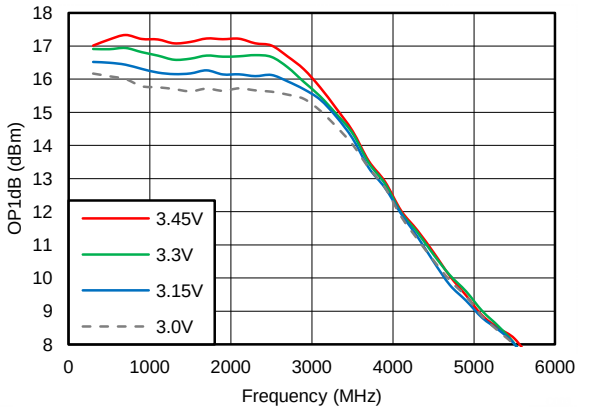

$V_{CC}$ curves Temp = 25°C Pin = –10 dBm

**Figure 1. Gain vs Frequency**



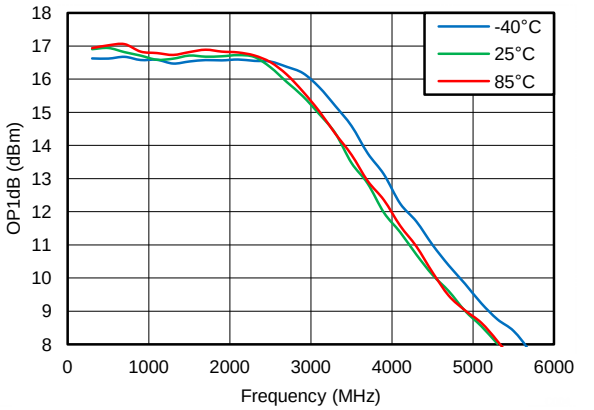

Temp curves $V_{CC}$ = 3.3 V Pin = –10 dBm

**Figure 2. Gain vs Frequency**



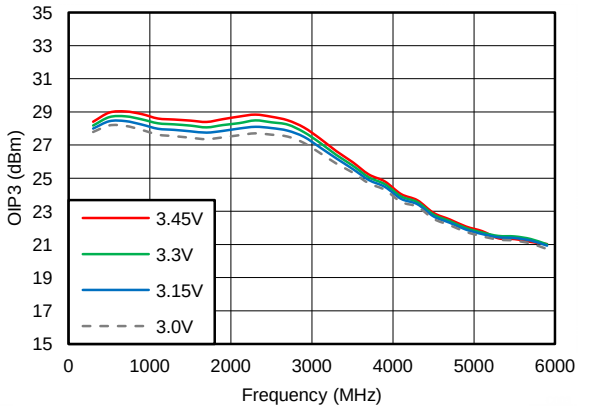

$V_{CC}$ curves Temp = 25°C

**Figure 3. OP1dB vs Frequency**



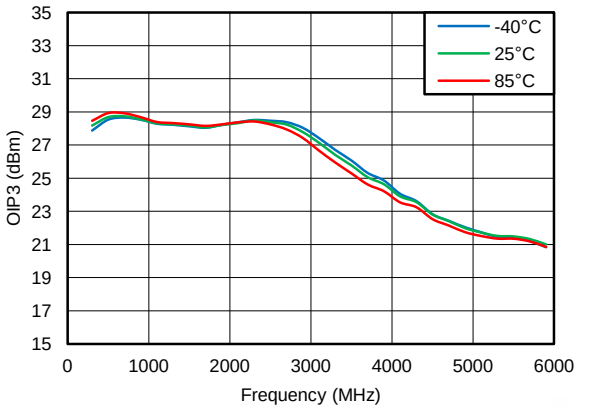

Temp curves $V_{CC}$ = 3.3 V

**Figure 4. OP1dB vs Frequency**




$V_{CC}$ curves Temp = 25°C Pin = –10 dBm/tone

**Figure 5. OIP3 vs Frequency**

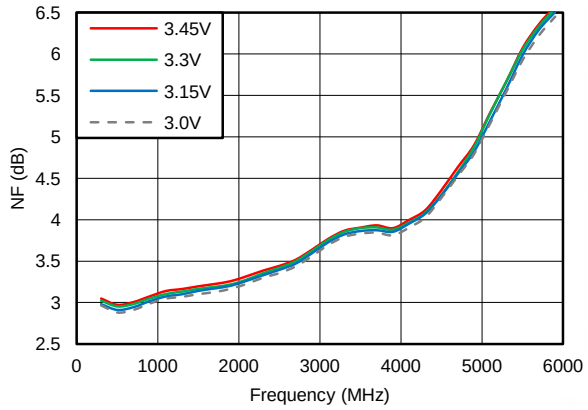



Temp curves $V_{CC}$ = 3.3 V Pin = –10 dBm/tone

**Figure 6. OIP3 vs Frequency**

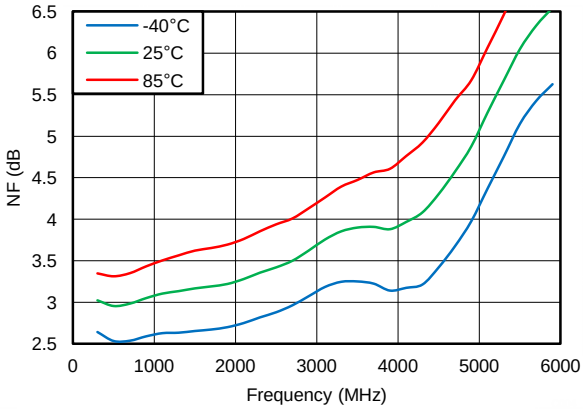

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## Typical Characteristics (continued)



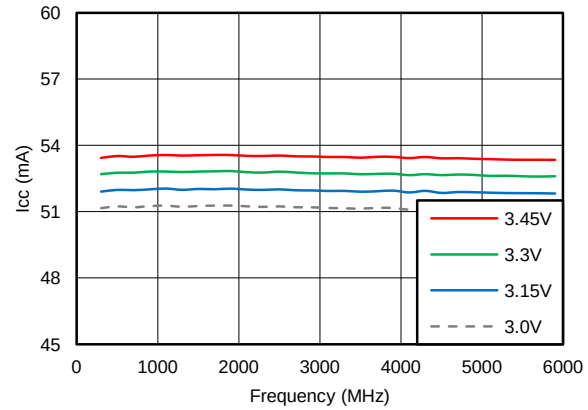

$V_{CC}$ curves Temp = 25°C

**Figure 7. NF vs Frequency**



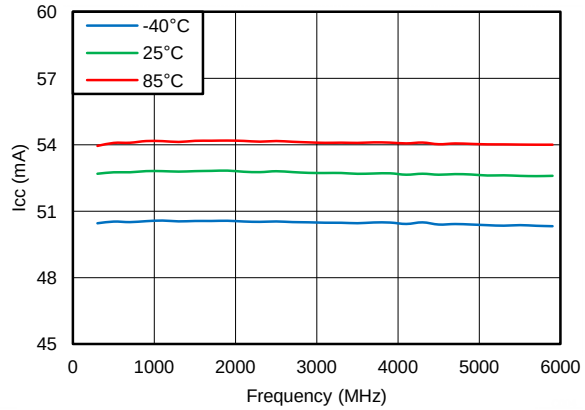

Temp curves $V_{CC}$ = 3.3 V

**Figure 8. NF vs Frequency**



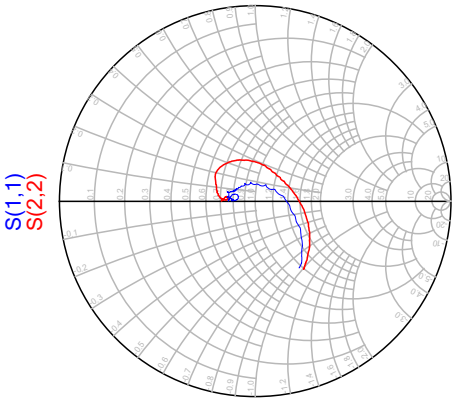

$V_{CC}$ curves Temp = 25°C

**Figure 9. $I_{CC}$ vs Frequency**




Temp curves $V_{CC}$ = 3.3 V

**Figure 10. $I_{CC}$ vs Frequency**

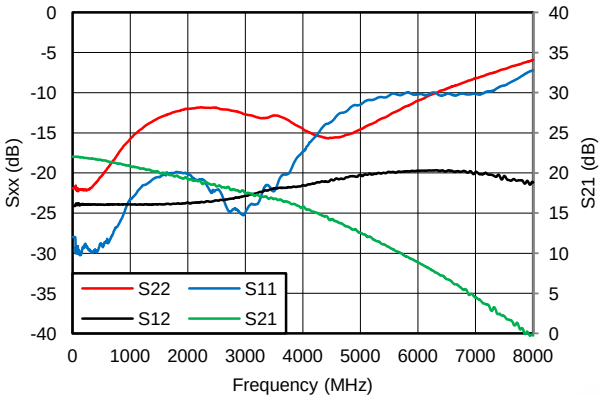



freq (1.000MHz to 8.000GHz)

$V_{CC}$ = 3.3 V Temp = 25°C 1 MHz to 8 GHz

Data Taken with EVM and Bias T, De-embedded to DUT pin

**Figure 11. Smith Chart – S11, S22**




$V_{CC}$ = 3.3 V Temp = 25°C 1 MHz to 8 GHz

Data Taken with EVM and Bias T, De-embedded to DUT pin

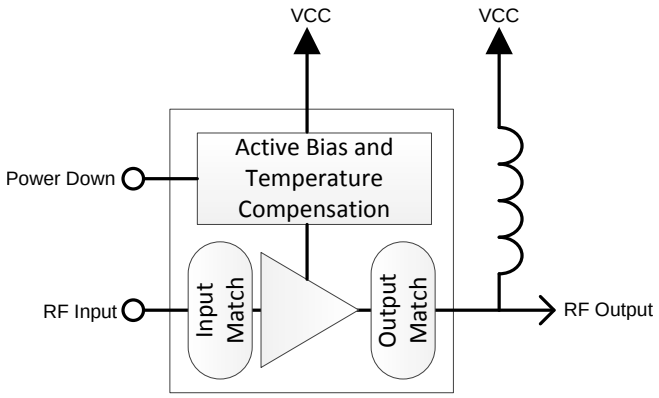
**Figure 12. S22, S11, S12, S21**

# 7 Detailed Description

## 7.1 Overview

The device is a 3.3 V general purpose RF gain block. It is a SiGe Darlington amplifier with integrated 50 Ω input and output matching. The device contains an active bias circuit to maintain performance over a wide temperature and voltage range. The included power down function allows the amplifier to shut down saving power when the amplifier is not needed. Fast shut down and start up enable the amplifier to be used in a host of time division duplex applications.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

The TRF37D73 is a fixed gain RF amplifier. It is internally matched to 50 Ω on both the input and output. It is a fully cascadable general purpose amplifier. The included active bias circuitry ensures the amplifier performance is optimized over the full operating temperature and voltage ranges.

## 7.4 Device Functional Modes

### 7.4.1 Power Down

The TRF37D73 PWDN pin can be left unconnected for normal operation or a logic-high for disable mode operation. For applications that use the power down mode, normal 5 V TLL levels are supported.


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# 8 Applications and Implementation

## 8.1 Application Information

The TRF37D73 is a wideband, high performance, general purpose RF amplifier. To maximize its performance, good RF layout and grounding techniques should be employed.

## 8.2 Typical Application

The TRF37D73 device is typically placed in a system as illustrated in Figure 13.

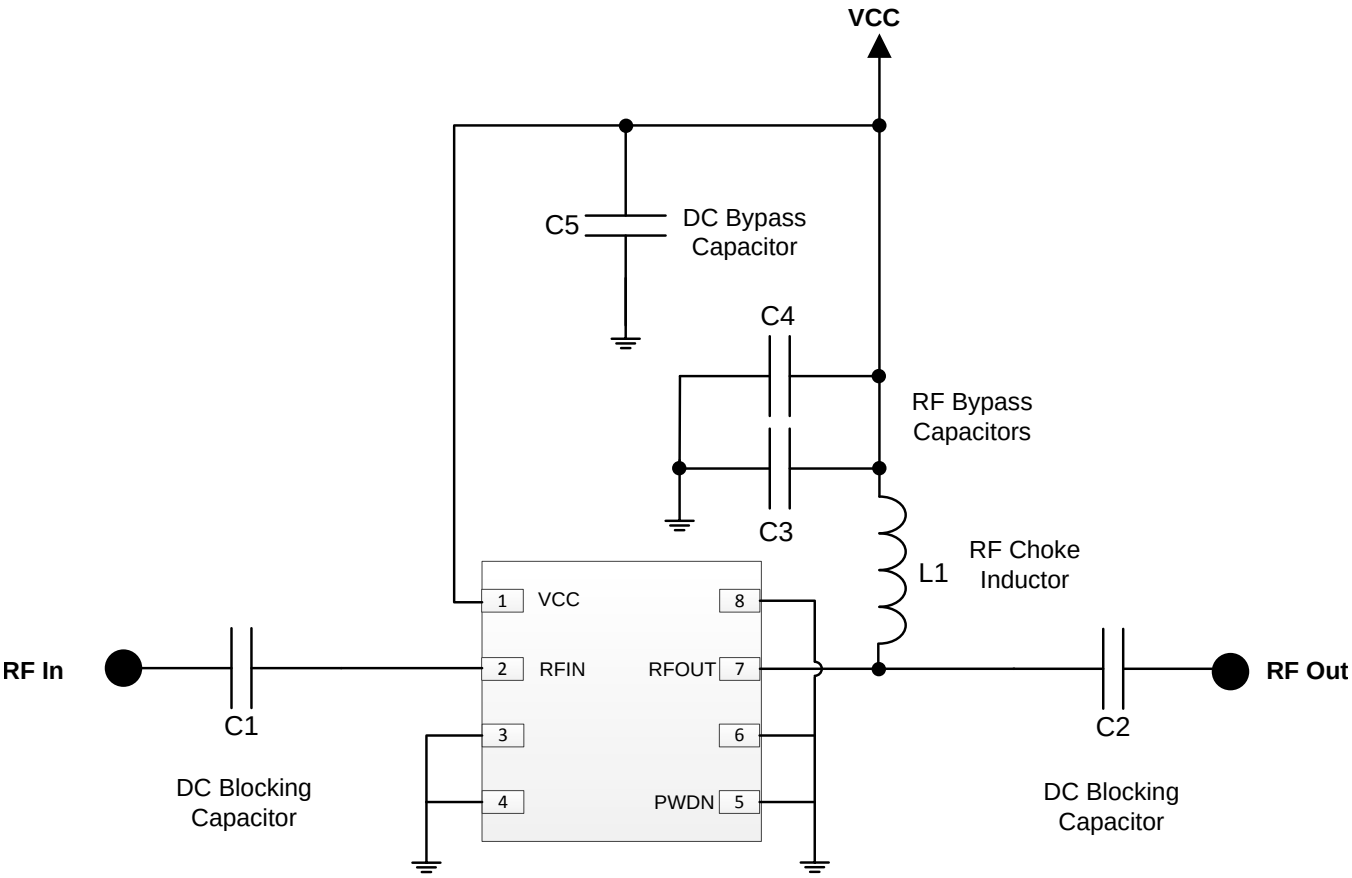



**Figure 13. Typical Application Schematic for TRF37D73**

### 8.2.1 Design Requirements

**Table 1. Design Parameters**

| PARAMETERS | EXAMPLE VALUES |
|---|---|
| Input power range | < 3 dBm |
| Output power | < 18 dBm |
| Operating frequency range | 1 — 6000 MHz |

### 8.2.2 Detailed Design Procedure

The TRF37D73 is a simple to use internally matched and cascadable RF amplifier. Following the recommended RF layout with good quality RF components and local DC bypass capacitors will ensure optimal performance is achieved. TI provides various support materials including S-Parameter and ADS models to allow the design to be optimized to the user's particular performance needs.

### 8.2.3 Application Curve

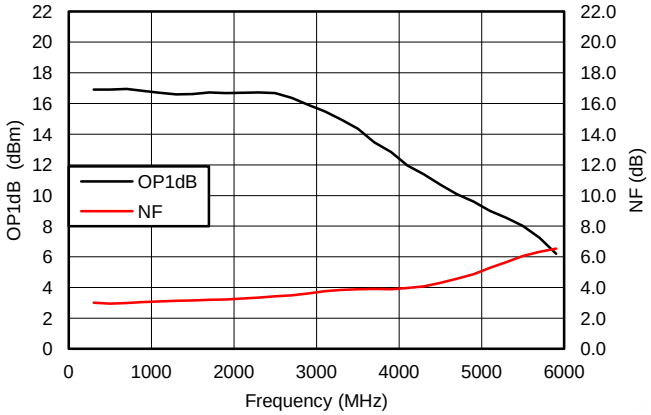



**Figure 14. OP1dB and NF vs Frequency**

## 9 Power Supply Recommendations

All supplies may be generated from a common nominal 3.3 V source but should be isolated through decoupling capacitors placed close to the device. The typical application schematic in Figure 13 is an excellent example. Select capacitors with self-resonant frequency near the application frequency. When multiple capacitors are used in parallel to create a broadband decoupling network, place the capacitor with the higher self-resonant frequency closer to the device. Expensive tantalum capacitors are not needed for optimal performance.


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# 10 Layout

## 10.1 Layout Guidelines

Good layout practice helps to enable excellent linearity and isolation performance. An example of good layout is shown in Figure 15. In the example, only the top signal layer and its adjacent ground reference plane are shown.

- Excellent electrical connection from the PowerPAD™ to the board ground is essential. Use the recommended footprint, solder the pad to the board, and do not include solder mask under the pad.
- Connect pad ground to device terminal ground on the top board layer.
- Verify that the return DC and RF current path have a low impedance ground plane directly under the package and RF signal traces into and out of the amplifier.
- Ensure that ground planes on the top and any internal layers are well stitched with vias.
- Do not route RF signal lines over breaks in the reference ground plane.
- Avoid routing clocks and digital control lines near RF signal lines.
- Do not route RF or DC signal lines over noisy power planes. Ground is the best reference, although clean power planes can serve where necessary.
- Place supply decoupling close to the device.

## 10.2 Layout Example

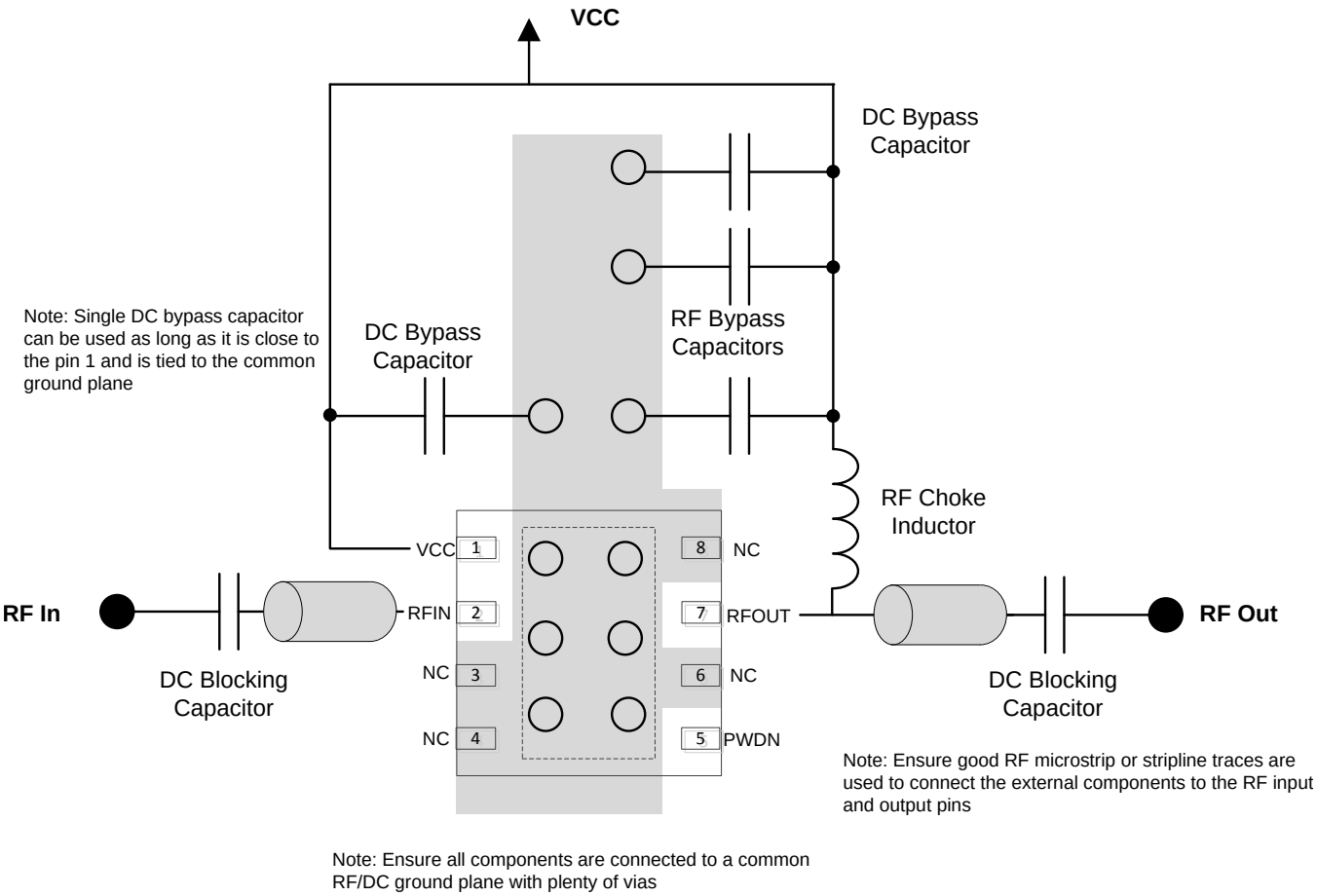



**Figure 15. Layout**

# 11 Device and Documentation Support

## 11.1 Trademarks

PowerPAD is a trademark of Texas Instruments.

## 11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TRF37D73IDSGR | ACTIVE | WSON | DSG | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | D73I | Samples |
| TRF37D73IDSGT | ACTIVE | WSON | DSG | 8 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | D73I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

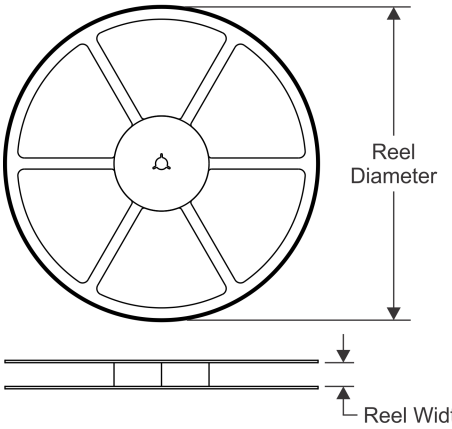
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

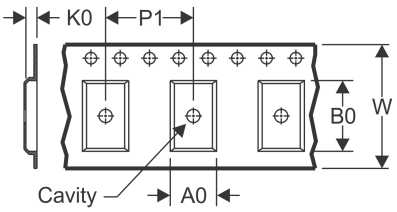
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

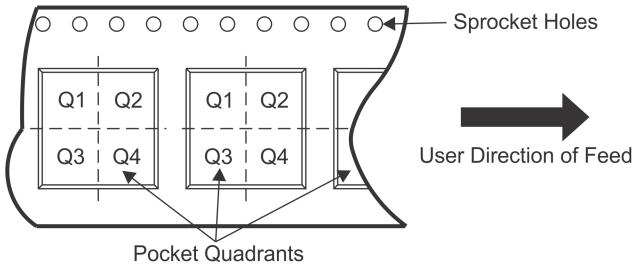



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

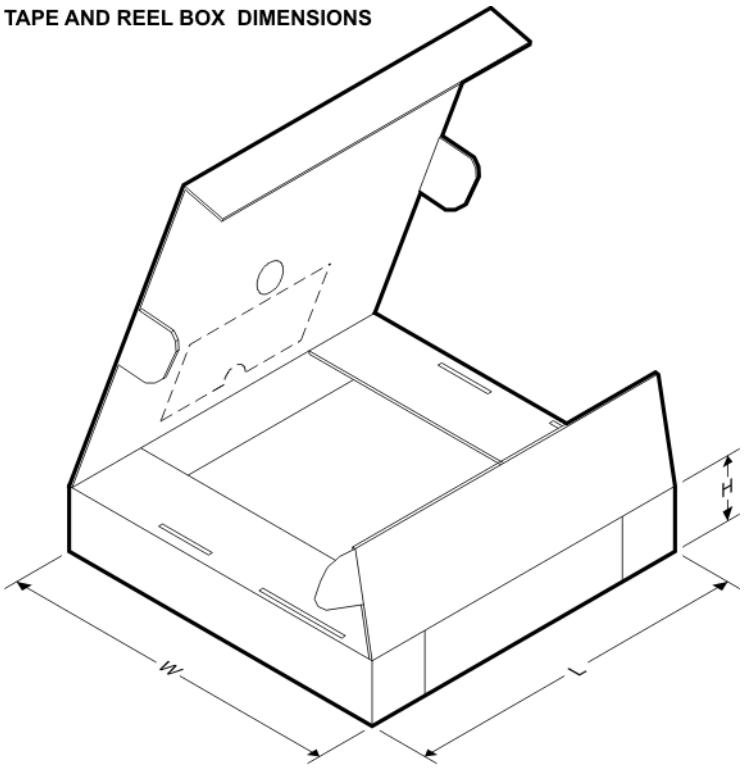
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRF37D73IDSGR | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TRF37D73IDSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TRF37D73IDSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TRF37D73IDSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |

# GENERIC PACKAGE VIEW

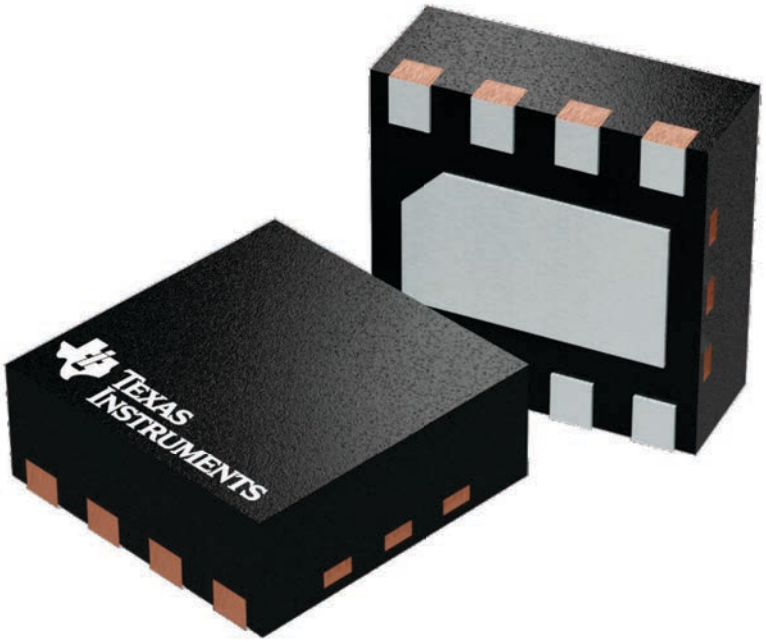
## DSG 8

## WSON - 0.8 mm max height

**2 x 2, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



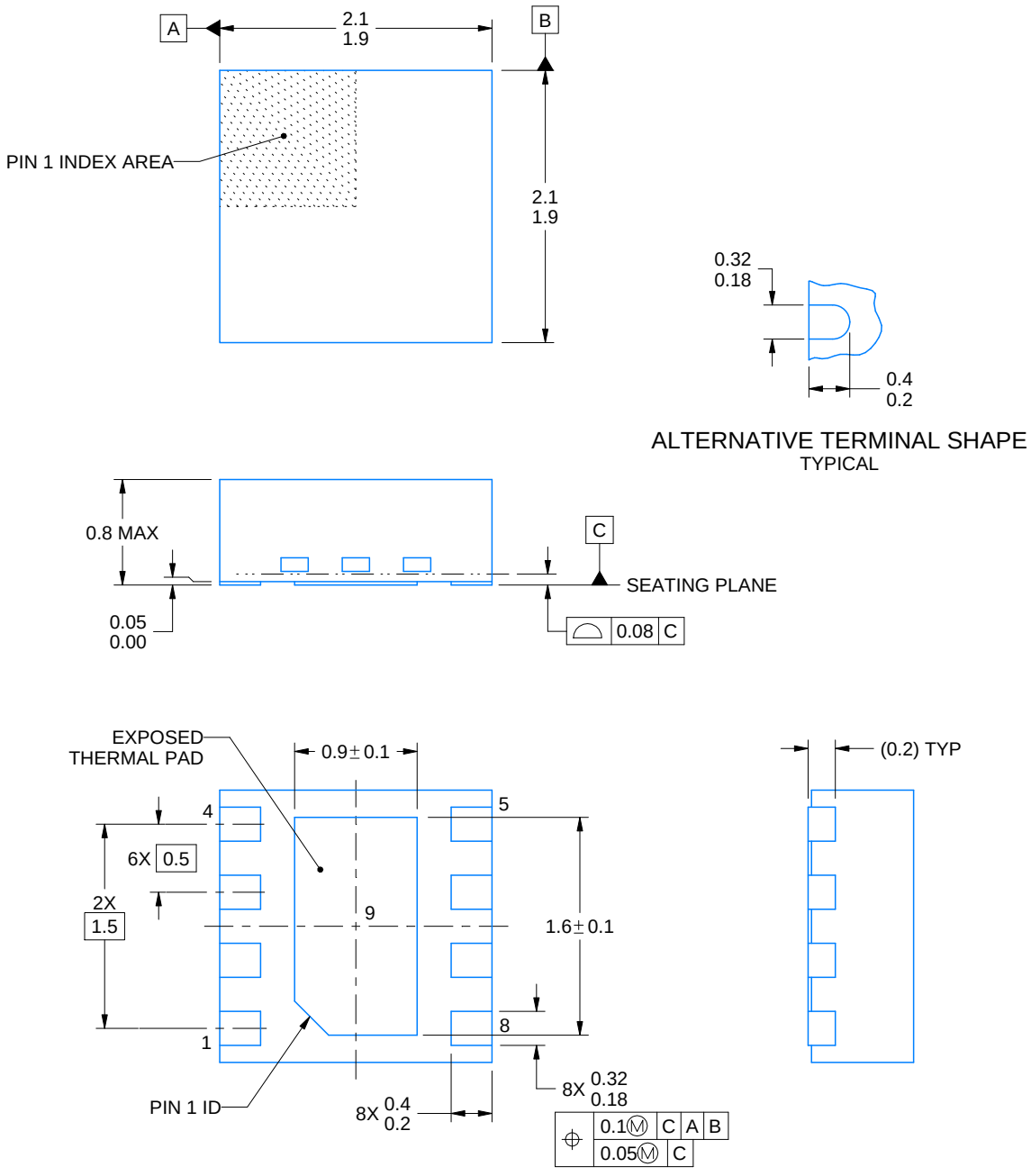

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# PACKAGE OUTLINE

## DSG0008A

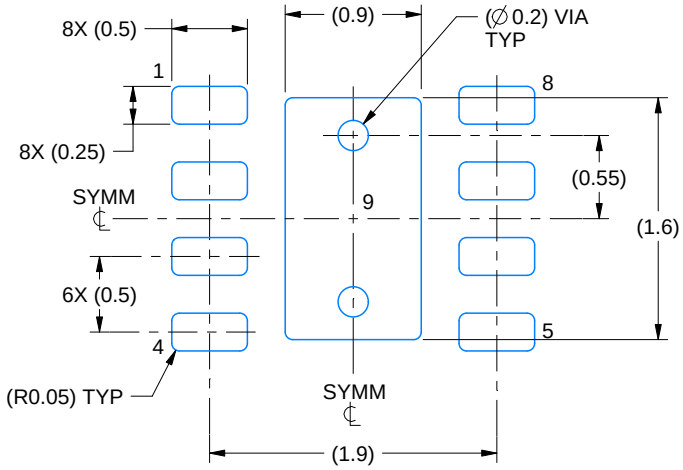
## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

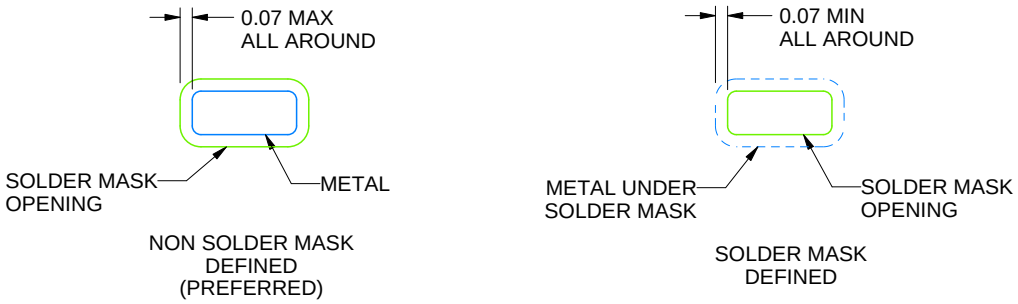



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X




SOLDER MASK DETAILS

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NOTES: (continued)

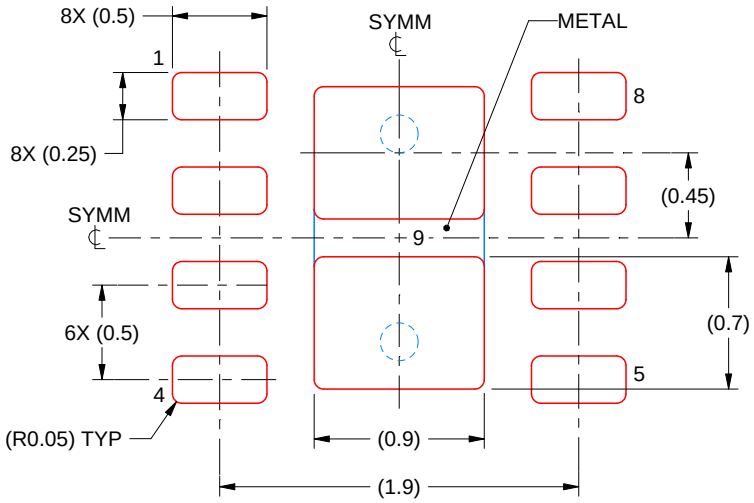
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DSG0008A

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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