TR7002

418.00 MHz Hybrid Transceiver

- ***Designed for Short-Range Wireless Data Communications***
- ***Supports RF Data Transmission Rates Up to 115.2 kbps***
- ***3 V, Low Current Operation plus Sleep Mode***
- ***Up to 10 mW Transmitter Power***
- ***Complies with Directive 2002/95/EC***

The TR7002 hybrid transceiver is ideal for short-range wireless data applications where robust operation, small size, low power consumption and low cost are required. The TR7002 employs RFM's amplifier-sequenced hybrid (ASH) architecture to achieve this unique blend of characteristics. All critical RF functions are contained in the hybrid, simplifying and speeding design-in. The receiver section of the TR7002 is sensitive and stable. A wide dynamic range log detector, in combination with digital AGC and a compound data slicer, provide robust performance in the presence of on-channel interference or noise. Two stages of SAW filtering provide excellent receiver out-of-band rejection. The transmitter includes provisions for both on-off keyed (OOK) and amplitude-shift keyed (ASK) modulation. The transmitter employs SAW filtering to suppress output harmonics, facilitating compliance with FCC/ETSI I-ETS 300 220 and similar regulations.



SM3-20H

Absolute Maximum Ratings

Rating	Value	Units
Power Supply and All Input/Output Pins	-0.3 to +4.0	V
Non-Operating Case Temperature	-50 to +100	°C
Soldering Temperature (10 seconds, 5 cycles maximum)	260	°C

Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency	f_o		417.80		418.20	MHz
Data Modulation Type				OOK/ASK		
OOK Data Rate					30	kb/s
ASK Data Rate					576	kb/s
Receiver Performance						
Sensitivity, 4.8 kbps, 10-3 BER, AM Test Method		1		-111		dBm
Sensitivity, 4.8 kbps, 10-3 BER, Pulse Test Method		1		-105		dBm
Current, 4.8 kbps				4.2		mA
Sensitivity, 19.2 kbps, 10-3 BER, AM Test Method		1		-107		dBm
Sensitivity, 19.2 kbps, 10-3 BER, Pulse Test Method		1		-101		dBm
Current, 19.2 kbps				4.25		mA
Sensitivity, 115.2 kbps, 10-3 BER, AM Test Method		1		-102		dBm
Sensitivity, 115.2 kbps, 10-3 BER, Pulse Test Method		1		-96		dBm
Current, 115.2 kbps				4.3		mA
Receiver Out-of-Band Rejection, ±5% fo	$R_{\pm 5\%}$	2		80		dB
Receiver Ultimate Rejection	R_{ULT}	2		100		dB

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Electrical Characteristics (typical values given for 3.0 Vdc power supply, 25 °C)

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Transmitter Performance						
Peak RF Output Power, 235 µA TXMOD Current	P_{OL}	2		10		dBm
Peak Current, 235 µA TXMOD Current	I_{TPL}	2		32		mA
2nd - 4th Harmonic Outputs		2			-40	dBm
5th - 10th Harmonic Outputs		2			-45	dBm
Non-harmonic Spurious Outputs		2			-40	dBm
OOK Turn On/Turn Off Times	t_{ON}/t_{OFF}	3			12/6	µs
ASK Output Rise/Fall Times	t_{TR}/t_{TF}	3			1.1/1.1	µs
Logic 0 Input Voltage			0		0.15 Vcc	V
Logic 1 Input Voltage			0.85 Vcc		Vcc	V
Logic 0 Output Voltage, 1 mA Sink			0		0.1 Vcc	V
Logic 1 Output Voltage, 1 mA Source			0.9 Vcc		Vcc	V
Sleep Mode Current	I_S			200		nA
Power Supply Voltage Range	V_{CC}		2.2		3.7	Vdc
Power Supply Voltage Ripple					10	mV_{P-P}
Ambient Operating Temperature	T_A		-40		85	°C

CAUTION: Electrostatic Sensitive Device. Observe precautions for handling.

Notes:

1. Typical sensitivity data is based on a 10^{-3} bit error rate (BER), using DC-balanced data. There are two test methods commonly used to measure OOK/ASK receiver sensitivity, the “100% AM” test method and the “Pulse” test method. Sensitivity data is given for both test methods. The application/test circuit and component values are shown on the next page.
2. Data is given with the ASH radio matched to a 50 ohm load. Matching component values are given on the next page.

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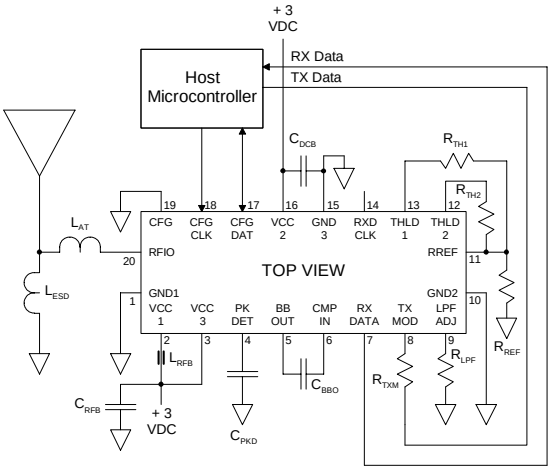
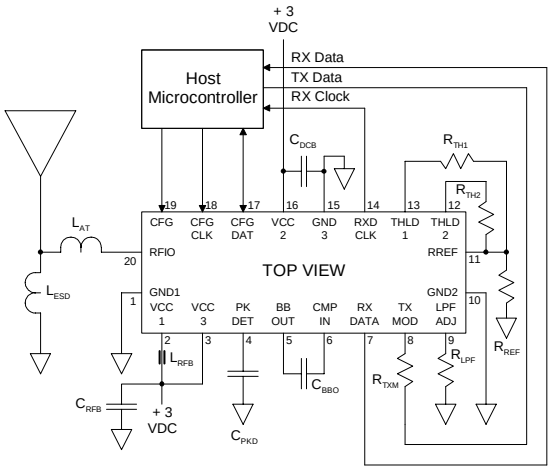
3G ASH Transceiver Application Circuit
2G Default OOK/ASK Configuration



3G ASH Transceiver Application Circuit
3G OOK/ASK Configuration



Tranceiver Set-Up, 3.0 Vdc, -40 to +85 °C

Item	Symbol	OOK	OOK	ASK	Units	Notes
Encoded Data Rate	DR_{NOM}	4.8	19.2	115.2	kb/s	see pages 1 & 2
Minimum Signal Pulse	SP_{MIN}	208.32	52.08	8.68	µs	single bit
Maximum Signal Pulse	SP_{MAX}	833.28	208.32	34.72	µs	4 bits of same value
PKDET Capacitor	C_{PKD}	0.022	0.0056	820 pF	µF	±10% ceramic
BBOUT Capacitor	C_{BBO}	0.01	0.0027	390 pF	µF	±10% ceramic
TXMOD Resistor	R_{TXM}	9.1	9.1	9.1	K	±5%, for 10 dBm output
LPFADJ Resistor	R_{LPF}	470	160	24	K	±5%
RREF Resistor	R_{REF}	100	100	100	K	±1%
THLD2 Resistor	R_{TH2}	-	-	100	K	±1%, typical values
THLD1 Resistor[1]	R_{TH1}	20	20	20	K	±1%, typical values
DC Bypass Capacitor	C_{DCB}	4.7	4.7	4.7	µF	tantalum
RF Bypass Capacitor	C_{RFB}	100	100	100	pF	±5% NPO
Series Tuning Inductor	L_{AT}	56	56	56	nH	50 ohm antenna
Shunt Tuning/ESD Inductor	L_{ESD}	220	220	220	nH	50 ohm antenna
RF Bypass Bead	L_{RFB}	Fair-Rite	Fair-Rite	Fair-Rite		2506033017YO or equivalent

1. When using internal data and clock recovery, a THLD1 value of 47K is recommended to minimize start vector “nuisance tripping” due to random noise.

CAUTION: Electrostatic Sensitive Device. Observe precautions for handling.

Notes:

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ASH Transceiver Theory of Operation

Introduction

RFM's amplifier-sequenced hybrid (ASH) transceiver technology is specifically designed for short-range wireless data communication applications. ASH transceivers provide robust operation, very small size, low power consumption and low implementation cost. All critical RF functions are contained in the hybrid, simplifying and speed-ing design-in. ASH transceivers can be readily configured to support a wide range of data rates and protocol requirements. These transceivers feature excellent suppression of transmitter harmonics and virtually no RF emissions when receiving, making them easy to certify to short-range (unlicensed) radio regulations.

Amplifier-Sequenced Receiver Operation

The ASH transceiver's unique feature set is made possible by its system architecture. The heart of the transceiver is the amplifier-sequenced receiver section, which provides more than 100 dB of stable RF and detector gain without any special shielding or decoupling requirements.

Figure 1 shows the basic block diagram and timing cycle for an amplifier sequenced receiver. Note that the bias to RF amplifiers RFA1 and RFA2 are independently controlled by a pulse generator, and that the two amplifiers are coupled by a surface acoustic wave (SAW) delay line, which has a typical delay of 0.5 µs.

An incoming RF signal is first filtered by a narrow-band SAW filter, and is then applied to RFA1. The pulse generator turns RFA1 ON for 0.814 µs. The amplified signal from RFA1 emerges from the SAW delay line at the input to RFA2. RFA1 is now switched OFF and RFA2 is switched ON for 0.814 µs, amplifying the RF signal further. The ON time for RFA1 and RFA2 is set by a 614 kHz internal pulse generator. As shown in the timing diagram, RFA1 and RFA2 are never on at the same time, assuring excellent receiver stability. Note that the narrow-band SAW filter eliminates sampling sideband responses outside of the receiver passband, and the SAW filter and delay line act together to provide very high receiver ultimate rejection.

ASH Transceiver Block Diagram

Figure 2 is the general block diagram of the ASH transceiver.

Please refer to Figure 2 for the following discussions.

Antenna Port

The only external RF components needed for the transceiver are the antenna and its matching components. Antennas presenting an impedance in the range of 35 to 72 ohms resistive can be satisfactorily matched to the RFIO pin with a series matching coil and a shunt matching/ESD protection coil. Other antenna impedances can be matched using two or three components. For some impedances, two inductors and a capacitor will be required. A DC path from RFIOto ground is required for ESD protection.

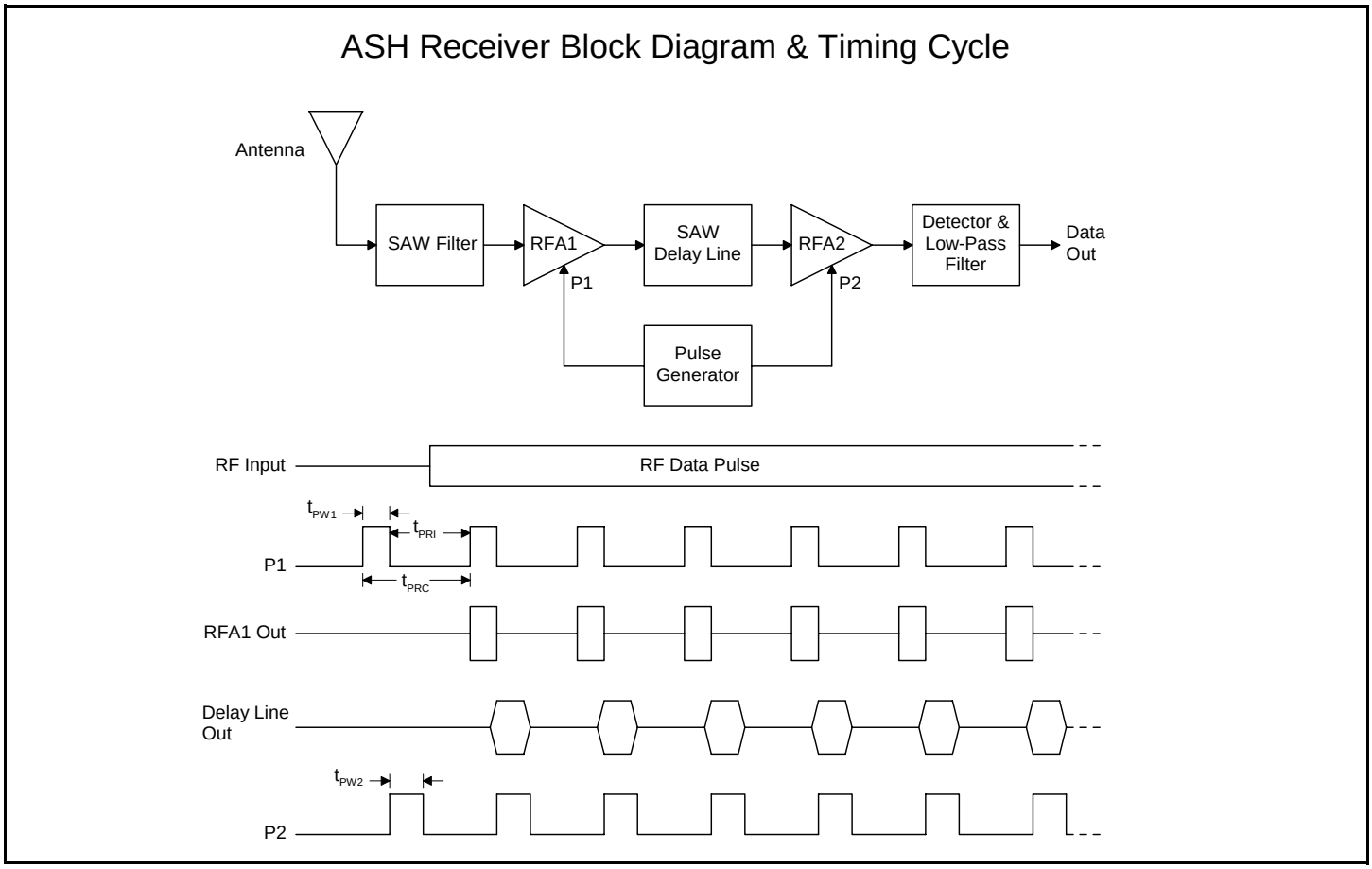

Figure 1

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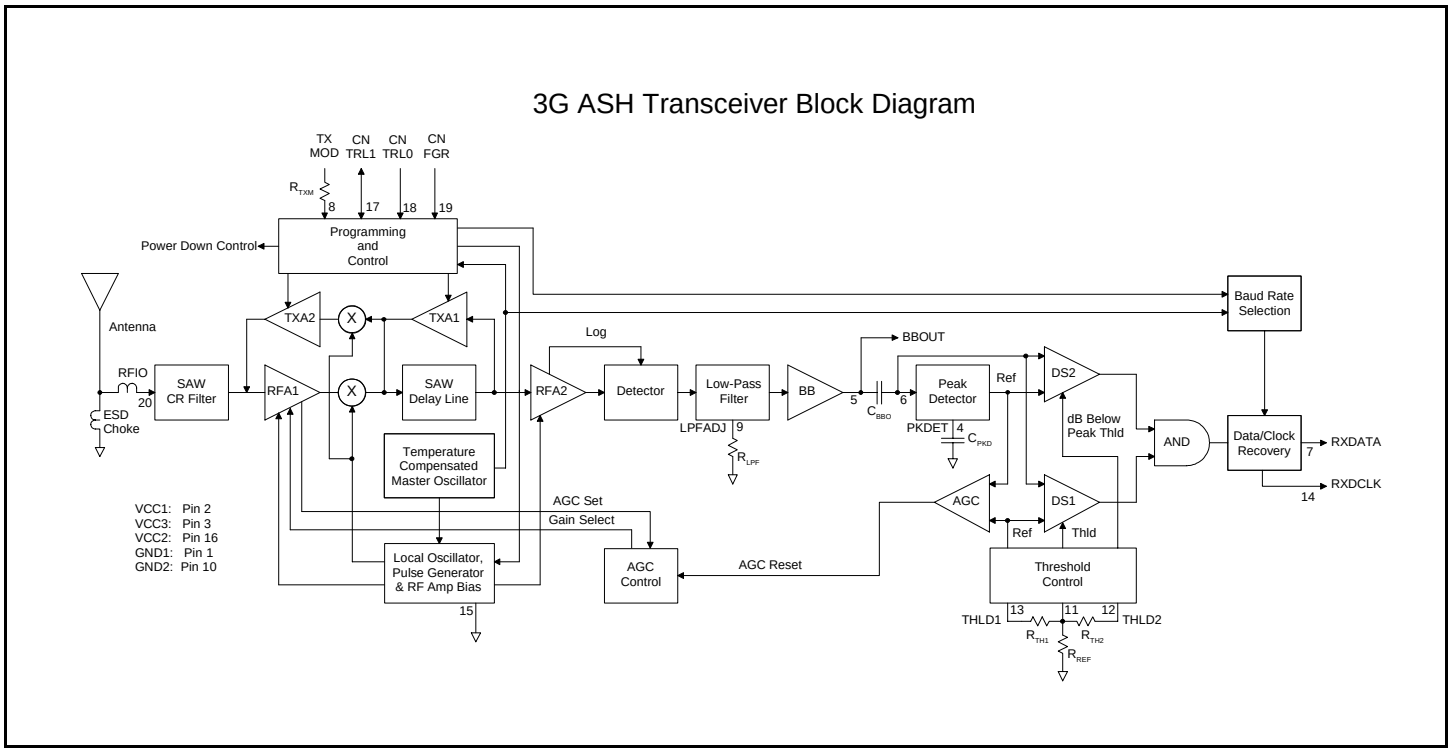

Figure 2

Receiver Chain

The output of the SAW filter drives amplifier RFA1. This amplifier includes provisions for detecting the onset of saturation (AGC Set), and for switching between 35 dB of gain and 5 dB of gain (Gain Select). AGC Set is an input to the AGC Control function, and Gain Select is the AGC Control function output. ON/OFF control to RFA1 (and RFA2) is generated by the Pulse Generator & RF Amp Bias function. The output of RFA1 drives the SAW delay line, which has a nominal delay of 0.5 µs.

The second amplifier, RFA2, provides 51 dB of gain below saturation. The output of RFA2 drives a full-wave detector with 19 dB of threshold gain. The onset of saturation in each section of RFA2 is detected and summed to provide a logarithmic response. This is added to the output of the full-wave detector to produce an overall detector response that is square law for low signal levels, and transitions into a log response for high signal levels. This combination provides excellent threshold sensitivity and more than 70 dB of detector dynamic range. In combination with the 30 dB of AGC range in RFA1, more than 100 dB of receiver dynamic range is achieved.

The detector output drives a gyrator filter. The filter provides a three-pole, 0.05 degree equiripple low-pass response with excellent group delay flatness and minimal pulse ringing. The 3 dB bandwidth of the filter can be set from 4.5 kHz to 1.8 MHz with an external resistor.

The filter is followed by a base-band amplifier which boosts the detected signal to the BBOUT pin. When the receiver RF amplifiers are operating at a 50%-50% duty cycle, the BBOUT signal changes about 10 mV/dB, with a peak-to-peak signal level of up to 450 mV. For lower duty cycles, the mV/dB slope and peak-to-peak signal level are proportionately less. The detected signal is riding on a 1.5 Vdc level that varies somewhat with supply voltage, temperature, etc. BBOUT is coupled to the CMPIN pin, or to an external data recovery process (DSP), by a series capacitor. The correct value of the series capacitor depends on data rate, data run length, and other factors as discussed in the *ASH Transceiver Designer's* Guide.

When an external data recovery process is used with AGC, BBOUT must be coupled to the external data recovery process and to CMPIN by separate series coupling capacitors. The AGC reset function is driven by the signal applied to CMPIN.

Data Slicers

The CMPIN pin drives two data slicers, which convert the analog signal from BBOUT back into a digital stream. The best data slicer configuration depends on the system operating parameters. Data slicer DS1 is a capacitively-coupled comparator with provisions for an adjustable threshold. DS1 provides the best performance at low signal-to-noise conditions. The threshold, or squelch, offsets the comparator's slicing level from 0 to 90 mV, and is set with a resistor between the RREF and THLD1 pins. This threshold allows a trade-off between receiver sensitivity and output noise density in the no-signal condition. For best sensitivity, the threshold is set to zero but a minimum R_{TH1} value of approximately 20 K Ohms should be used for proper AGC action. In this case, noise is output continuously when no signal is present. This, in turn, requires the circuit being driven by the RXDATA pin to be able to process noise (and signals) continuously.

This can be a problem if RXDATA is driving a circuit that must sleep when data is not present to conserve power, or when it its necessary to minimize false interrupts to a multitasking processor. In this case, noise can be greatly reduced by increasing the threshold level, but at the expense of sensitivity. In order to guarantee THLD1 to be the value calculated, the device should not be powered up in the receive mode. It should be powered up in either the sleep mode or the transmit mode and then switched to the recieve mode. The best 3 dB bandwidth for the low-pass filter

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is also affected by the threshold level setting of DS1. The bandwidth must be increased as the threshold is increased to minimize data pulse-width variations with signal amplitude.

DS2 is a “dB-below-peak” slicer. The peak detector charges rapidly to the peak value of each data pulse, and decays slowly in between data pulses (1:1000 ratio). The slicer trip point can be set from 0 to 120 mV below this peak value with a resistor between RREF and THLD2.

DS2 is best for ASK modulation where the transmitted waveform has been shaped to minimize signal bandwidth. However, DS2 is subject to being temporarily “blinded” by strong noise pulses, which can cause burst data errors. Note that DS1 is active when DS2 is used, as the compound data slicer output is the logical AND of the DS1 and DS2 outputs. DS2 can be disabled by leaving THLD2 disconnected. Note that a non-zero DS1 threshold is required for proper AGC operation.

Data and Clock Recovery

RXDATA is the receiver data output pin. The signal on this pin can come from one of two sources. The default source is directly from the output of the compound data slicer circuit. The alternate source is from the radio’s internal data and clock recovery circuit. When the internal data and clock recovery circuit is used (CFG0 Bit 0 high), the signal on RXDATA is switched from the output of the data slicer to the output of the data and clock recovery circuit when a packet start symbol is detected.

When the radio’s internal data and clock recovery circuit is not used, RXDCLK is a steady low value. When the internal data and clock recovery is used, RXDCLK is low until a start symbol is detected at the output of the data slicer. Each bit following the start symbol is output at RXDATA on the rising edge of a RXDCLK pulse, and is stable for reading on the falling edge of the RXDCLK pulse. Once RXDCLK is activated by the detection of a start symbol, it remains active until CFG0 Bit 0 is reset low. Normally RXDCLK is reset by the host processor as soon as a packet is received.

AGC Control

The output of the Peak Detector also provides an AGC Reset signal to the AGC Control function through the AGC comparator. The purpose of the AGC function is to extend the dynamic range of the receiver, so that two transceivers can operate close together when running ASK and/or high data rate modulation. The onset of saturation in the output stage of RFA1 is detected and generates the AGC Set signal to the AGC Control function. The AGC Control function then selects the 5 dB gain mode for RFA1. The AGC Comparator will send a reset signal when the Peak Detector output (multiplied by 0.8) falls below the threshold voltage for DS1.

Transmitter Chain

The transmitter chain consists of a SAW delay line oscillator followed by an OOK/ASK modulated buffer amplifier. The SAW filter suppresses transmitter harmonics to the antenna. Note that the same SAW devices used in the amplifier-sequenced receiver are reused in the transmit modes.

Transmitter operation supports two modulation formats, on-off keyed (OOK) modulation, and amplitude-shift keyed (ASK) modulation. When OOK modulation is chosen, the transmitter output turns completely off between “1” data pulses. When ASK modulation is chosen, a “1” pulse is represented by a higher transmitted power level, and a “0” is represented by a lower transmitted power level. OOK modulation provides compatibility with first-generation ASH technology, and provides for power conservation. ASK modulation must be used for high data rates (data pulses less than 30 µs). ASK modulation also reduces the effects of some types of interference and allows the transmitted pulses to be shaped to control modulation bandwidth.

When either modulation format is chosen, the receiver RF amplifiers are turned off. In the OOK mode, the delay line oscillator amplifier TXA1 and the buffer amplifier TXA2 are turned off when the voltage to the TXMOD input falls below 220 mV. In the OOK mode, the data rate is limited by the turn-on and turn-off times of the delay line oscillator, which are 12 and 6 µs respectively. In the ASK mode TXA1 is biased ON continuously, and the output of TXA2 is modulated by the TXMOD input current. Minimum output power occurs in the ASK mode when the modulation driver sinks about 10 µA of current from the TXMOD pin.

The transmitter RF output power is proportional to the input current to the TXMOD pin. A series resistor is used to adjust the peak transmitter output power. 10 dBm of output power requires about 235 µA of input current.

Configuration Control

The operating configuration of the TR7002 is controlled by three pins: Pin 17 (CFGDAT), Pin 18 (CFGCLK), and Pin 19 (CFG). When DC power is applied to the TR7002 with Pin 19 held low, the functions of Pins 17 and 18 default to the “2G ASH” TR3000 definition. This allows the TR7002 to be used with existing TR1000 PCB layouts and protocol software. The logic levels on Pins 17 and 18 control the default operation as shown below:

Pin 17	Pin 18	Mode
1	1	Receive
0	0	Sleep
0	1	Transmit OOK
1	0	Transmit ASK

Note that for default 2G operation, Pin 15 is grounded (zero ohm resistor) and Pin 14 is left unconnected.

When Pin 19 is first set to a logic 1 after DC power is applied, the functionality of Pins 17 and 18 change from direct mode control to serial control. This change persists until a DC power reset occurs.

After serial control is invoked, Pins 17, 18 and 19 are used to write data to and read from three 8-bit configuration control registers in the radio. To begin a write or read sequence, Pin 19 is set to logic 1. Data is then clocked into or out of Pin 17 on the rising edge of each clock pulse applied to Pin 18. Configuration data clocked into Pin 17 is transferred to a control register every eight bits. Bits clocked into Pin 17 when Pin 19 is a logic 0 are ignored. Also, if Pin 19 is reset to logic 0 before a complete group of eight data bits is received, the incomplete group is ignored.

Single-byte and multi-byte write and read sequences are detailed in Figures 4 and 5. The bits in the configuration registers are summarized in Figure 3.

CFG0 Bit 7 - When this bit is 0, the radio is operational. Setting this bit to 1 invokes the sleep mode. In the sleep mode most of the radio is powered down, reducing the radio’s current consumption to about 200 nA. The contents of the configuration registers are preserved during sleep mode. The power-on default value of this bit is 0. Note that once sleep mode is invoked, Pin 19 must be set to a logic 1 to return to active operation. In changing from sleep mode to active mode, Pin 19 should be high for at least one microsecond before attempting to clock data in or out of the control registers.

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Adress	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	CFG0	Sleep	TX/RX	ASK/OOK	-	Mode 1	Mode 0	-	SV En
1	CFG1	-	VCOlock	-	-	BR3	BR2	BR1	BR0
2	LoSyn	Test	LOSyn6	LOSyn5	LOSyn4	LOSyn3	LOSyn2	LOSyn1	LOSyn0

Figure 3

CFG0 Bit 6 - When this bit is 0, the radio is in the receive mode (provided CFG0 Bit 7 is 0). When this bit is 1, the radio is in one of the transmit modes. Note the radio will transmit using OOK or ASK modulation, depending on the value of CFG0 Bit 5. The power-on default value of this bit is 0.

CFG0 Bit 5 - When this bit is 0, the transmitter uses OOK modulation. When this bit is 1, the transmitter uses ASK modulation. The power-on default value of this bit is 0.

CFG0 Bit 4 - This bit should always be set to 0 in the TR7002. The power-on default value of this bit is 0.

CFG0 Bits 3, 2 - The states of these two bits set the basic operating mode of the radio as shown below. The power-on default value of these two bits is 0.

Bit 3	Bit 2	Mode
0	0	Single-channel Mode
0	1	Not Used
1	0	Not Used
1	1	Not Used

CFG0 Bit 1 - This bit should always be set to 0 in the TR7002. The power-on default value of this bit is 0.

CFG0 Bit 0 - Setting this bit to logic 1 enables the internal start symbol (vector) detection and the data and clock recovery circuit. When active, this function continuously tests for a 16-bit start symbol, 0xE2E2 (hex). Data clocking begins in the middle of the first bit following the 16-bit start symbol, and clocking continues until CFG0 Bit 0 is reset to a logic 0. *Note that CFG0 Bit 0 must be set to back to a* logic 1 to re-enable the start symbol detection and the data and *clock recovery circui*t. The common way to use this function is for the host processor to set this bit to a 1 when it is ready to receive a message. When a start symbol is detected, data clocking begins, and the host processor inputs the message bits. Once all of the bits in the message are received, the host processor resets this bit to 0 to end data clocking. After the current message has been processed, the host processor sets this bit to 1 again to enable detection of the next message. The power-on default value of this bit is 0.

The start symbol pattern is sent starting with the MSB. This start symbol pattern will not occur in a message that has been encoded for DC-balance using either Manchester encoding or 8-to-12 bit symbolization using the encoding table given below. Note that the table is given for 4-to-6 bit encoding, so each byte of the message is encoded starting with the high nibble and then the low nibble.

Nibble Hex Value	Symbol Hex Value (6 bits)
0	0D
1	0E
2	13
3	15
4	16
5	19
6	1A
7	1C
8	23
9	25
A	26
B	29
C	2A
D	2C
E	32
F	34

CFG1 Bit 7 - This bit is unused in the TR7002.

CFG1 Bit 6 - This bit is a Read Only bit. Writing has no effect. When performing a read and this bit is set, this indicates that the internal VCO is locked and ready to transmit or receive data.

CFG1 Bit 5 - This bit is unused in the TR7002.

CFG1 Bit 4 - This bit is unused in the TR7002.

CFG1 Bits 3, 2, 1, 0 - These bits select the internal data and clock recovery data (bit) rate as shown in the table below. The power-on default value of these bits is 0.

LOSyn Bit 7 - This bit is only used in product testing. It should always be set to 0 for normal operation. The power-on default value of this bit is 0.

LOSyn Bits 6, 5, 4, 3, 2, 1, 0 -These bits have no function in the TR7002 and can be written as either a logic 1 or a logic 0.

Note that data to/from the configuration registers is clocked in/out MSB first. See the Control Register Read/Write Detail and Control Register Read/Write Timing Drawings for additional details.

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Receiver Turn-On Timing

The maximum time t_{PR} required for the receive function to become operational at turn-on is influenced by two factors. All receiver circuitry will be operational 1 ms after the supply voltage reaches 2.2 Vdc. The BBOUT-CMPIN coupling-capacitor is then DC stabilized in 4 time constants ($4*t_{BBC}$). The total turn-on time to stable receiver operation for a 10 ms power supply rise time is:

$t_{PR} = 15\ ms + 4*t_{BBC}$

Data Rate (b/s)	CFG1 Bits 3-0
1200	0000
2400	0001
4800	0010
9600	0011
19200	0100
38400	0101
57600	0110
115200	0111
230400	1000

Receiver Wake-Up Timing

The maximum transition time t_{SR} from the sleep mode to the receive mode is $4*t_{BBC}$, where t_{BBC} is the BBOUT-CMPIN coupling-capacitor time constant. When the operating temperature is limited to 60°C, the time required to switch from sleep to receive is dramatically less for short sleep times, as less charge leaks away from the BBOUT-CMPIN coupling capacitor.

AGC Timing

The maximum AGC engage time tAGC is 5 µs after the reception of a -30 dBm RF signal with a 1 µs envelope rise time.

Peak Detector Timing

The Peak Detector attack time constant is set by the value of the capacitor at the PKDET pin. The attack time $t_{PKA} = C_{PKD}/4167$, where t_{PKA} is in µs and C_{PKD} is in pF. The Peak Detector decay time constant $t_{PKD} = 1000*t_{PKA}$.

Pin Descriptions

Pin	Name	Description
1	GND1	GND1 is the RF ground pin.
2	VCC1	VCC1 is a positive supply voltage pin. VCC1 is decoupled with a ferrite bead and bypassed by an RF capacitor.
3	VCC3	VCC3 is a positive supply voltage pin. VCC3 is bypassed by an RF capacitor.
4	PKDET	This pin controls the peak detector operation. A capacitor between this pin and ground sets the peak detector attack and decay times, which have a fixed 1:1000 ratio. For most applications, these time constants should be coordinated with the base-band time constant. For a given base-band capacitor C_{BBO} , the capacitor value C_{PKD} is: $C_{PKD} = 2.0* C_{BBO}$, where C_{BBO} and C_{PKD} are in pF A ±10% ceramic capacitor should be used at this pin. This time constant will vary between t_{PKA} and $1.5* t_{PKA}$ with variations in supply voltage, temperature, etc. The capacitor is driven from a 200 ohm “attack” source, and decays through a 200 K load. The peak detector is used to drive the “dB-below-peak” data slicer and the AGC release function. The peak detector capacitor is discharged in the receiver power-down (sleep) mode and in the transmit modes.
5	BBOUT	BBOUT is the receiver base-band output pin. This pin drives the CMPIN pin through a coupling capacitor C_{BBO} for internal data slicer operation. The time constant t_{BBC} for this connection is: $t_{BBC} = 0.1C_{BBO}$, where t_{BBC} is in µs and C_{BBO} is in pF A ±10% ceramic capacitor should be used between BBOUT and CMPIN. The time constant can vary between t_{BBC} and $1.8*t_{BBC}$ with variations in supply voltage, temperature, etc. The optimum time constant in a given circumstance will depend on the data rate, data run length, and other factors as discussed in the ASH Transceiver Designer’s Guide. $C_{BBO} = 11.2*SP_{MAX}$, where SP_{MAX} is the maximum signal pulse width in µs and C_{BBO} is in pF The output from this pin can also be used to drive an external data recovery process (DSP, etc.). The nominal output impedance of this pin is 1 K. When the receiver RF amplifiers are operating at a 50%-50% duty cycle, the BBOUT signal changes about 10 mV/dB, with a peak-to-peak signal level of up to 450 mV. The signal at BBOUT is riding on a 1.5 Vdc value that varies somewhat with supply voltage and temperature, so it should be coupled through a capacitor to an external load. A load impedance of 50 K to 500 K in parallel with no more than 10 pF is recommended. When an external data recovery process is used with AGC, BBOUT must be coupled to the external data recovery process and CMPIN by separate series coupling capacitors. The AGC reset function is driven by the signal applied to CMPIN. When the transceiver is in power-down (sleep) or in a transmit mode, the output impedance of this pin becomes very high, preserving the charge on the coupling capacitor.
6	CMPIN	This pin is the input to the internal data slicers. It is driven from BBOUT through a coupling capacitor. The input impedance of this pin is 100 K.

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Pin	Name	Description
7	RXDATA	RXDATA is the receiver data output pin. It is a CMOS output. The signal on this pin can come from one of two sources. The default source is directly from the output of the data slicer circuit. The alternate source is from the radio's internal data and clock recovery circuit. When the internal data and clock recovery circuit is used, the signal on RXDATA is switched from the output of the data slicer to the output of the data and clock recovery circuit when a packet start symbol is detected. Each recovered data bit is then output on the rising edge of a RXDCLK pulse (Pin 14), and is stable for reading on the falling edge of the RXDCLK pulse.
8	TXMOD	The transmitter RF output voltage is proportional to the input current to this pin. A resistor in series with the TXMOD input is normally used to adjust the peak transmitter output. Full transmitter power (10 mW) requires about 235 µA of drive current. The transmitter output power P_O for a 3 Vdc supply voltage is approximately: $PO = 180*(I_{TXM})^2$, where PO is in mW and the modulation current I_{TXM} is in mA The practical power control range is 10 to -50 dBm. A ±5% TXMOD resistor value is recommended. Internally, this pin is connected to the base of a bipolar transistor with a small emitter resistor. The voltage at the TXMOD input pin is about 0.85 volt with 235 uA of drive current. This pin accepts analog modulation and can be driven with either logic level data pulses (unshaped) or shaped data pulses.
9	LPFADJ	This pin is the receiver low-pass filter bandwidth adjust. The filter bandwidth is set by a resistor R_{LPF} between this pin and ground. The resistor value can range from 510 K to 3 K, providing a filter 3 dB bandwidth f_{LPF} from 5 to 600 kHz. The resistor value is determined by: $R_{LPF} = (0.0006*f_{LPF})^{-1.069}$ where R_{LPF} is in kilohms, and f_{LPF} is in kHz A ±5% resistor should be used to set the filter bandwidth. This will provide a 3 dBfilter bandwidth between f_{LPF} and $1.3* f_{LPF}$ with variations in supply voltage, temperature, etc. The filter provides a three-pole, 0.05 degree equiripple phase response.D input is normally used to
10	GND2	GND2 is an IC ground pin.
11	RREF	RREF is the external reference resistor pin. A 100 K reference resistor is connected between this pin and ground. A ±1% resistor tolerance is recommended. It is important to keep the total capacitance between ground, Vcc and this node to less than 5 pF to maintain current source stability. If THLD1 and/or THDL2 are connected to RREF through resistor values less that 1.5 K, their node capacitance must be added to the RREF node capacitance and the total should not exceed 5 pF.
12	THLD2	THLD2 is the "dB-below-peak" data slicer (DS2) threshold adjust pin. The threshold is set by a 0 to 200 Kresistor R_{TH2} between this pin and RREF. Increasing the value of the resistor decreases the threshold below the peak detector value (increases difference) from 0 to 120 mV. For most applications, this threshold should be set at 6 dB below peak. The THLD2 resistor value is given by: $R_{TH2} = 1.5*V$, where R_{TH2} is in kilohms and the threshold V is in mV A ±1% resistor tolerance is recommended for the THLD2 resistor. Leaving the THLD2 pin open disables the dB-below-peak data slicer operation.
13	THLD1	The THLD1 pin sets the threshold for the standard data slicer (DS1) through a resistor R_{TH1} to RREF. The threshold is increased by increasing the resistor value. Connecting this pin directly to RREF provides zero theshold. The value of the resistor depends on whether THLD2 is used. For the case that THLD2 is not used, the acceptable range for the resistor is 0 to 200K, providing a THLD1 range of 0 to 112 mV. The resistor value is given by: For thresholds $0 \le V \le 30mV$: $R_{TH1} = 3.81*V - 14.28$, where R_{TH1} is in kilohms and the threshold V is in mV. For thresholds $31mV \le V \le 112mV$: $R_{TH1} = 1.22*V + 63.36$, where R_{TH1} is in kilohms and the threshold V is in mV. For the case that THLD2 is used, the acceptable range for the THLD1 resistor is 0 to 100K. The resistor value is given by: $R_{TH1} = 2.22*V$, where R_{TH1} is in kilohms and the threshold V is in mV A ±1% resistor tolerance is recommended for the THLD1 resistor. Note that a non-zero DS1 threshold is required for proper AGC operation. The minimum value recommended is 20K.
14	RXCLK	RXDCLK is the clock output from the data and clock recovery circuit. RXDCLK is a CMOS output. When the radio's internal data and clock recovery circuit is not used, RXDCLK is a steady low value. When the internal data and clock recovery is used, RXDCLK is low until a packet start symbol is detected at the output of the data slicer. Each bit following the start symbol is output at RXDATA on the rising edge of a RXDCLK pulse, and is stable for reading on the falling edge of the RXDCLK pulse. Once RXDCLK is activated by the detection of a start symbol, it remains active until CFG0 Bit 0 is set to 0. Normally RXDCLK is reset by the host processor as soon as a packet is received.
15	GND3	GND3 is an IC ground pin.
16	VCC2	VCC2 is a positive supply voltage pin. Pin 16 must be bypassed with an RF capacitor, and must also be by passed with a 1 µF tantalum or electrolytic capacitor.

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Pin	Name	Description
17	CFGDAT	In 3G control mode, CFGDAT is a bi-directional CMOS logic pin. When CFG (Pin 19) is set to a logic 1, configuration data can be clocked into or out of the radio's configuration registers through CFGDAT using CFGCLK (Pin 18). Data clocked into CFGDAT is transferred to a control register each time a group of 8 bits is received (see Figure 4). Pulses on CFGCLK are used to clock configuration data into and out of the radio through CFGDAT (Pin 17). When writing through CFGDAT, a data bit is clocked into the radio on the rising edge of a CFGCLK pulse. When reading through CFGDAT, data is output on the rising edge of the CFGCLK pulse and is stable for reading on the falling edge of the CFGCLK. CFGCLK is inactive when the CFG (Pin 19) is set at a logic 0. See Page 6 for details of 2G default control mode operation of this pin.
18	CFGCLK	In 3G control mode, pulses on CFGCLK are used to clock configuration data into and out of the radio through CFGDAT (Pin 17). When writing through CFGDAT, a data bit is clocked into the radio on the rising edge of a CFGCLK pulse. When reading through CFGDAT, data is output on the rising edge of the CFGCLK pulse and is stable for reading on the falling edge of the CFGCLK. CFGCLK is inactive when the CFG (Pin 19) is set to logic 0. See Page 6 for details of 2G default control mode operation of this pin. eac
19	CFG	CFG controls the operation of the CFGDAT (Pin 17) and CFGCLK (Pin 18) pins. If CFG is held at logic 0 when the radio is powered on, radio operation defaults to 2G control mode as explained on Page 6. Radio operation is switched to 3G serial control mode the first time CFG is set to logic 1. CFG must be set to a logic 1 before data can be clocked into or out of CFGDAT by CFGCLK. CFGDAT is inactive when the CFG (Pin 19) is set to logic 0. Setting CFG to a logic 1 will also switch the radio from sleep mode to active mode.
20	RFIO	RFIO is the RF input/output pin. This pin is connected directly to the SAW filter transducer. Antennas presenting an impedance in the range of 35 to 72 ohms resistive can be satisfactorily matched to this pin with a series matching coil and a shunt matching/ESD protection coil. Other antenna impedances can be matched using two or three components. For some impedances, two inductors and a capacitor will be required. A DC path from RFIO to ground is required for ESD protection.

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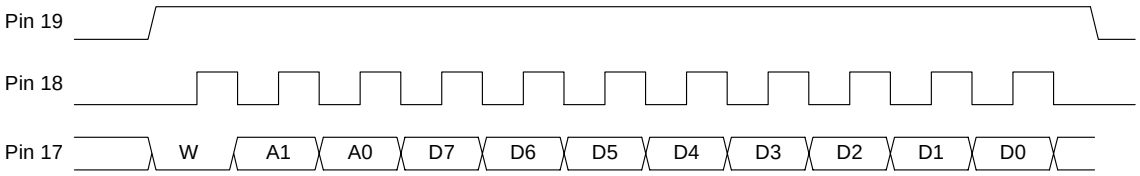
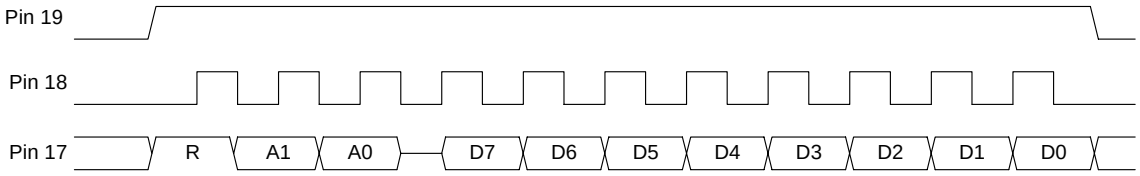
Control Register Read/Write Detail

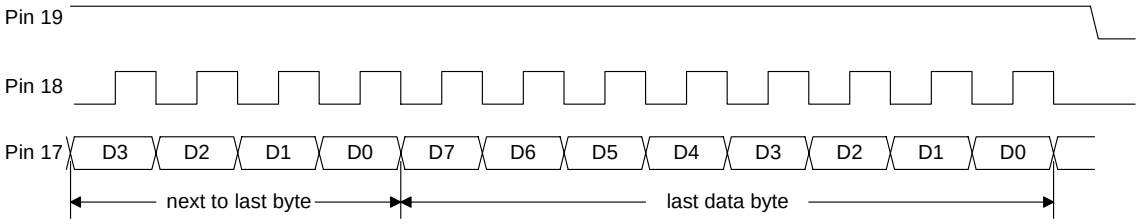
Single Byte Write Sequence
The write, address and data bits are clocked into the radio (left to right) on the rising edge of the clock input to Pin 18.



Single Byte Read Sequence
The read and address bits and are clocked into the radio on the rising edge of the clock input to Pin 18;
data is output on the rising edge of the clock and should be read into the host on the falling edge of the clock.



Multi-byte Write Sequence
Address increments automatically and rolls over from address 2 to address 0.



Multi-byte Read Sequence
Address increments automatically and rolls over from address 2 to address 0.

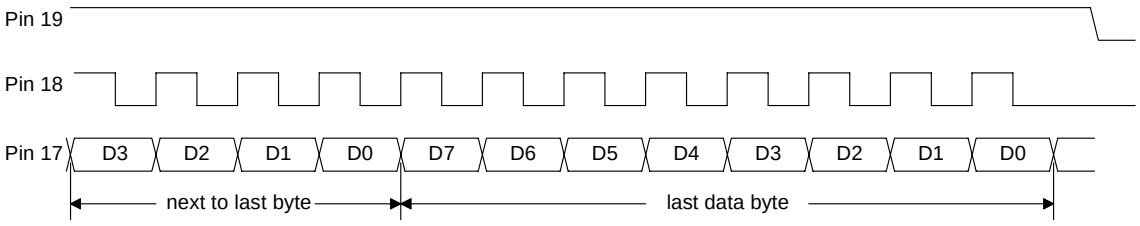


Figure 4

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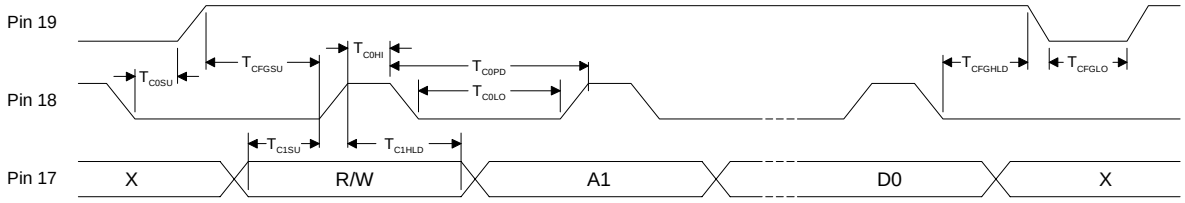
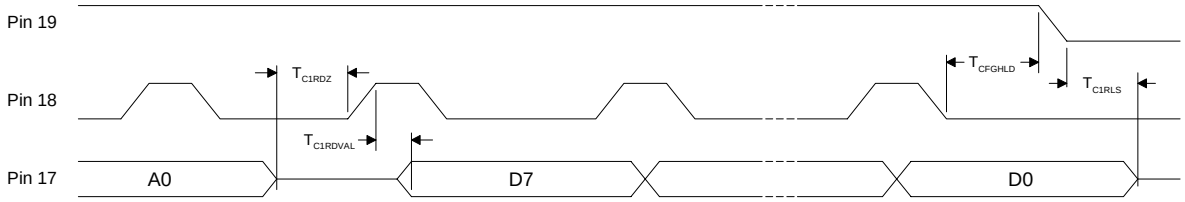
Control Register Read/Write Timing

Write Cycle Timing



Read Cycle Timing



Tranceiver Set-Up, 3.0 Vdc, -40 to +85 °C

Symbol	Characteristic	Min	Typ	Max	Units	Conditions
T_{C0SU}	CFGCLK (18) low setup time to CFG (19) rising edge	45			ns	
T_{C0HI}	CFGCLK (18) high time	90			ns	
T_{C0LO}	CFGCLK (18) low time	90			ns	
T_{C0PD}	CFGCLK (18) period - rising edge to rising edge	190			ns	
T_{CFGSU}	CFG (19) setup time - active modes	90			ns	all modes except sleep
T_{CFGSU}	CFG (19) setup time - sleep mode	1000			ns	sleep mode
T_{C1SU}	CFGDAT (17) setup time to CFGCLK (18) rising edge	45			ns	
T_{C1HLD}	CFGDAT (17) hold time to CFGCLK (18) rising edge	90			ns	
T_{CFGLO}	CFG (19) low time between transfers	90			ns	
T_{C1RDZ}	CFGDAT (17) high impedance setup time on data read	20			ns	
$T_{C1RDVAL}$	CFGDAT (17) time to valid data output on read			90	ns	
T_{C1RLS}	CFGDAT (17) time to high impedance on end of transfer			20	ns	

Tranceiver Set-Up, 3.0 Vdc, -40 to +85 °C

Command	R/W	Address	CFG0	CFG1
Receive OOK using external data and clock recovery	0	00	0000 0000	0000 0000
Receive OOK using internal 19.2 kb/s data and clock recovery	0	00	0000 0001	0000 0100
Transmit OOK	0	00	0100 0000	0010 0000
Sleep	0	00	1000 0000	0000 0000

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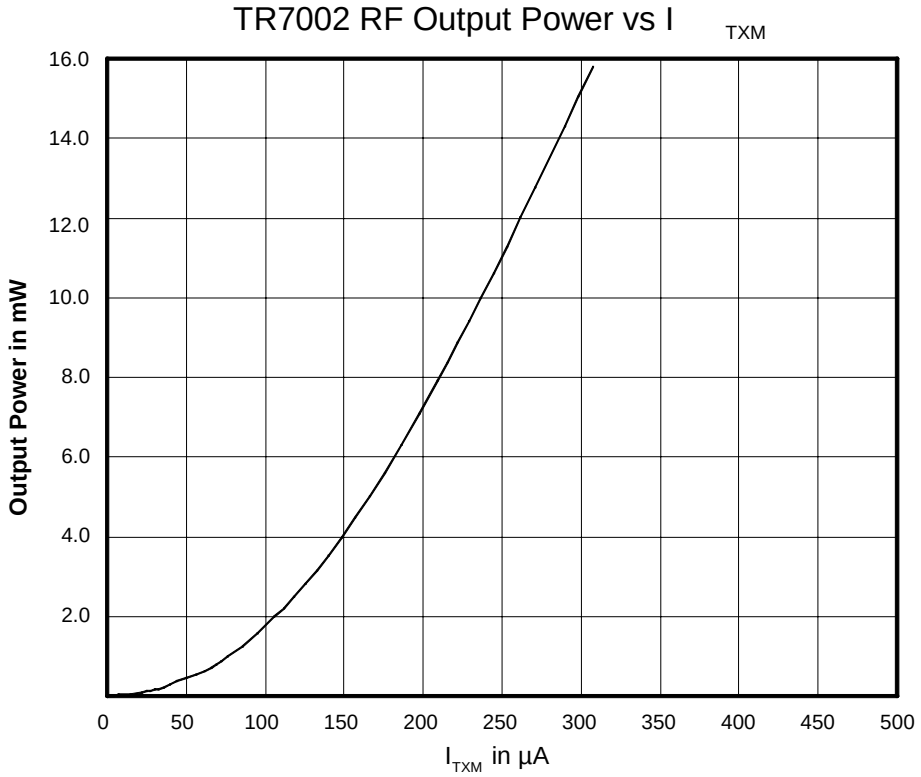

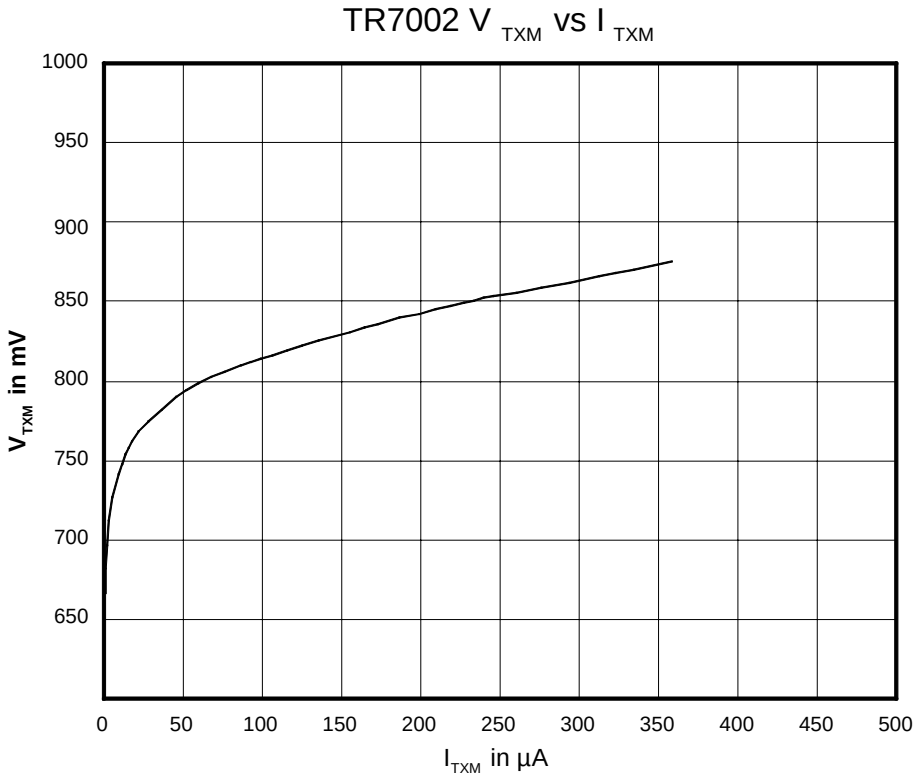

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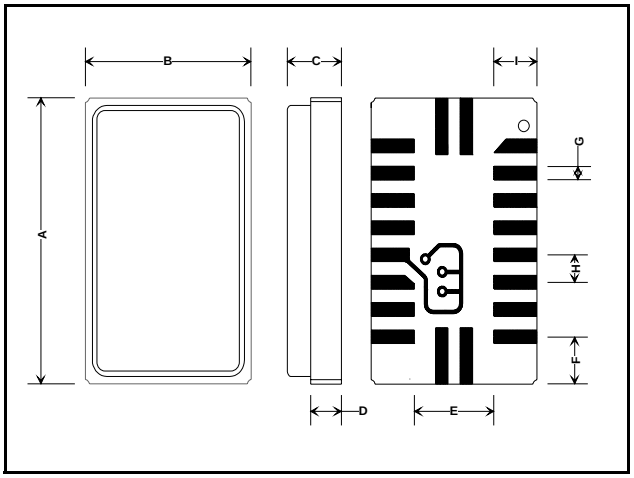
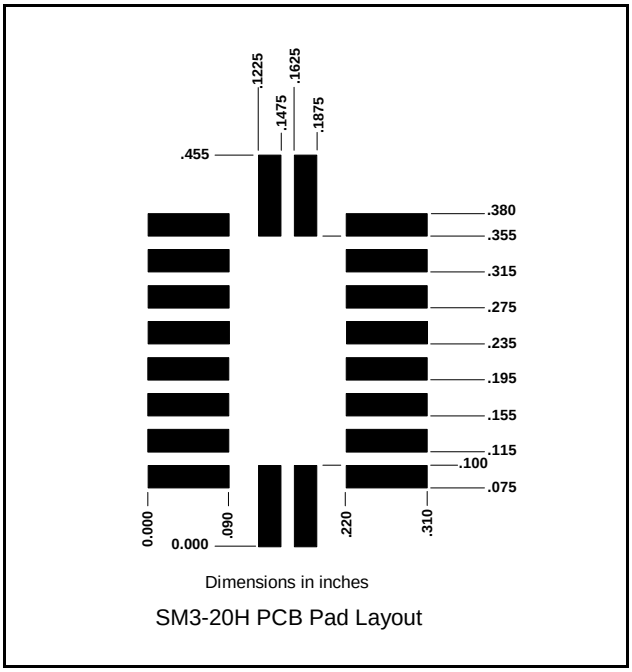


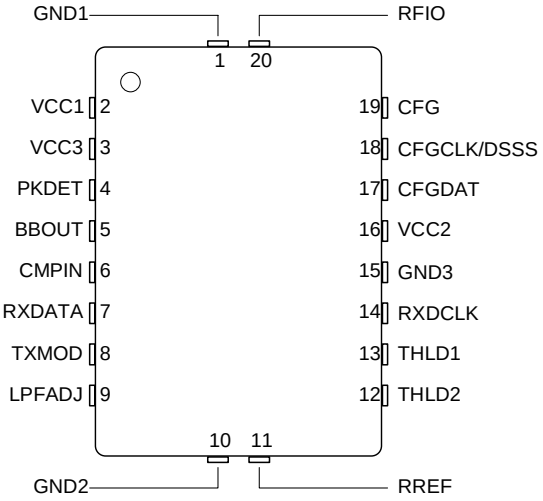
Dimension	mm			Inches		
	Min	Nom	Max	Min	Nom	Max
A	10.6	10.7	10.9	0.417	0.423	0.429
B	6.7	6.8	7.0	0.264	0.270	0.276
C	1.5	1.8	2.0	0.061	0.070	0.079
D	1.4	1.7	1.9	0.058	0.066	0.074
E	3.2	3.3	3.4	0.125	0.130	0.135
F	1.8	1.9	2.0	0.069	0.074	0.079
G	0.4	0.6	0.6	0.015	0.020	0.025
H	0.9	1.0	1.1	0.035	0.040	0.045
I	1.7	1.8	1.9	0.065	0.070	0.075



Dimensions in inches

SM3-20H PCB Pad Layout

Pin Out



Note: Specifications subject to change without notice.

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Rev	Date	Comments
-	08/25/2008	Initial Release

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