TQP3M9035

High Linearity LNA Gain Block

General Description

The TQP3M9035 is a high-linearity, low noise gain block amplifier in a low-cost surface-mount package. At 1900 MHz, the amplifier typically provides 16.5 dB gain, +37 dBm OIP3, and 0.65 dB Noise Figure. The LNA is also designed to be broadband without the requirement for external matching. The device is housed in a lead-free/green/RoHS-compliant industry-standard 2x2 mm package.

The TQP3M9035 has the benefit of having high linearity while also providing very low noise across a broad range of frequencies. This allows the device to be used in both receive and transmit chains for high performance systems. The amplifier is internally matched using a high performance E-pHEMT process and only requires an external RF choke and blocking/bypass capacitors for operation from a single +5V supply. The low noise amplifier integrates a shut-down biasing capability to allow for operation for TDD applications.

The TQP3M9035 covers the 50−6000 MHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

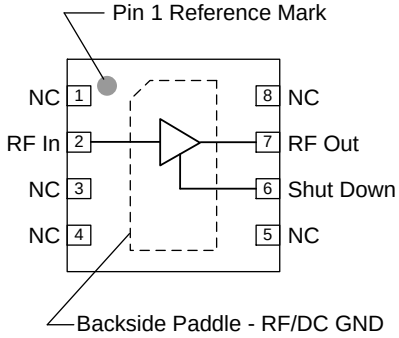


8 Pin 2X2 mm DFN Package

Product Features

- 50−6000 MHz Operating Range
- 0.65 dB Noise Figure @ 1900 MHz
- 16.5 dB Gain @ 1900 MHz
- +37 dBm Output IP3
- +22.5 dBm P1dB
- Shut-down capability
- Unconditionally stable
- 50 Ohm Cascadable Gain Block
- +5V Single Supply, 115 mA Current
- 2x2 mm 8 Pin DFN plastic package

Functional Block Diagram



Top View

Applications

- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

Ordering Information

Part No.	Description
TQP3M9035	High Linearity LNA Gain Block
TQP3M9035-PCB	500−6000 MHz Eval. Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150°C
Supply Voltage (V_{DD})	+6 V
RF Input Power, CW, 50Ω,T = 25°C	+23 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+3.3	+5.0	+5.25	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} =+5V, Temp=+25°C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		50		6000	MHz
Test Frequency			1900		MHz
Gain		15	16.5	18	dB
Input Return Loss			13		dB
Output Return Loss			10		dB
Output P1dB		+20	+23		dBm
Output IP3	Pout=+4 dBm/tone, Δf=1 MHz	+32.5	+37		dBm
Noise Figure (1)			0.65	1.0	dB
Switching Speed	Rise Time (10%-90%)		165		ns
	Fall Tine (90%-10%)		255		ns
Power Shutdown Control (2)	On state	0		0.8	V
	Off state (Power down)	3		V_{DD}	V
Current, I_{DD}	On state		115	150	mA
	Off state (Power down)		3		mA
Shutdown pin current, I_{SD}	V_{PD} ≥ 3 V		100		µA
Thermal Resistance, θ_{jc}	channel to case			50	°C/W

Notes:
1. Noise figure data has input trace loss de-embedded.
2. Voltage referred to J5 turret on evaluation board (pg.4).

S-Parameters

Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=115 mA (typ.), Temp=+25°C, 50 Ohm system

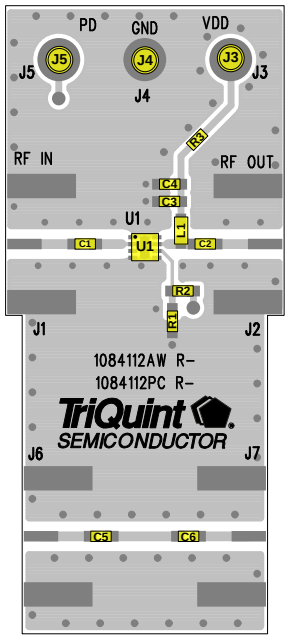
Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-11.5	-43.9	28.8	165.0	-31.8	13.5	-22.0	-106.8
100	-13.8	-43.3	28.2	161.3	-31.5	8.5	-26.5	172.1
200	-14.8	-50.7	27.6	151.4	-31.4	6.5	-20.1	99.9
400	-15.0	-74.6	26.1	132.1	-31.4	9.2	-14.9	57.7
600	-15.0	-93.2	24.5	116.9	-31.3	13.3	-13.1	35.6
800	-14.9	-106.9	23.0	104.8	-30.9	17.6	-12.2	19.5
1000	-15.0	-117.2	21.6	94.8	-30.3	21.5	-11.8	6.5
1200	-15.0	-125.4	20.4	86.1	-29.7	23.5	-11.6	-5.1
1400	-15.1	-131.8	19.4	78.2	-29.0	25.1	-11.4	-16.0
1600	-15.2	-137.5	18.5	71.0	-28.3	25.8	-11.2	-26.4
1800	-15.4	-142.3	17.6	64.2	-27.6	25.5	-11.0	-36.2
2000	-15.6	-147.1	16.9	57.7	-27.0	25.1	-10.7	-45.5
2200	-15.8	-151.7	16.2	51.4	-26.4	24.4	-10.4	-54.5
2400	-15.9	-156.6	15.6	45.4	-25.9	22.8	-10.1	-62.8
2600	-16.1	-161.5	15.0	39.5	-25.4	21.2	-9.7	-70.6
2800	-16.1	-166.5	14.5	33.6	-25.0	19.3	-9.3	-77.8
3000	-16.5	-174.6	14.0	27.9	-24.6	17.4	-8.7	-82.9
3200	-16.4	179.5	13.6	22.3	-24.2	15.1	-8.3	-88.4
3400	-16.0	176.3	13.2	16.8	-23.8	12.8	-8.0	-94.5
3600	-15.4	173.5	12.8	11.2	-23.5	10.3	-7.8	-100.7
3800	-14.8	170.9	12.5	5.6	-23.2	7.9	-7.6	-106.8
4000	-14.2	169.0	12.2	-0.1	-22.9	4.7	-7.4	-113.2
4200	-14.4	-174.7	11.7	-7.3	-22.7	-2.9	-8.3	-124.1
4400	-14.2	-178.1	11.4	-14.2	-22.6	-6.7	-8.0	-134.6
4600	-14.2	178.5	11.0	-21.3	-22.5	-11.6	-7.6	-145.4
4800	-13.9	176.9	10.6	-28.2	-22.4	-16.2	-7.1	-155.6
5000	-13.5	177.2	10.2	-35.3	-22.4	-21.0	-6.5	-164.7
5200	-13.0	177.4	9.8	-42.2	-22.5	-25.2	-5.9	-173.2
5400	-12.2	176.6	9.3	-49.2	-22.6	-30.3	-5.3	179.4
5600	-11.4	178.1	8.8	-55.7	-23.0	-34.5	-4.7	173.3
5800	-10.5	177.9	8.2	-62.3	-23.3	-38.2	-4.2	168.1
6000	-9.4	177.1	7.7	-68.7	-23.7	-41.3	-3.8	163.9

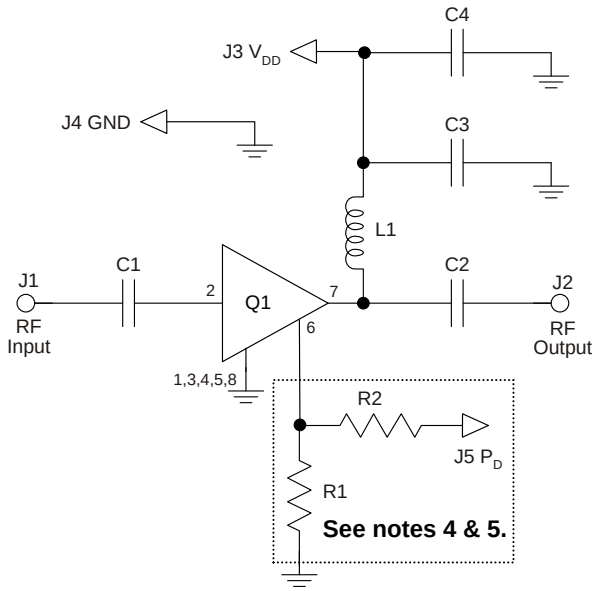
Noise Parameters

Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=115 mA (typ.), Temp=+25°C, 50 Ohm system

Freq (MHz)	NF_{min} (dB)	MagOpt (mag)	AngOpt (deg)	Rn (Ω)
700	0.41	0.100	118	0.046
1100	0.50	0.127	140	0.048
1500	0.59	0.113	165	0.060
1900	0.49	0.229	166	0.045
2300	0.59	0.267	179	0.048
2700	0.74	0.300	-166	0.051

TQP3M9035 – PCB Evaluation Board





Notes:
1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. C1, C2, and C3 are non-critical values. The reactive impedance should be as low as possible at the frequency of operation for optimal performance.
5. The L1 value is non-critical and needs to provide high reactive impedance at the frequency of operation.
6. R1 and R2 are optional and do not need to be loaded if the shut-down functionality is not needed; i.e. FDD applications. If R1 and R2 are not loaded, the LNA will operate in its standard “ON” state.
7. A through line is included on the evaluation board to de-embed the board losses.

Bill of Material – TQP3M9035 Evaluation Board

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	1084112
U1	n/a	High Linearity LNA Gain Block	Qorvo	TQP3M9035
R1	10K Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
R2	33K Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
L1(1)	68 nH	Inductor, 0603, 5%, Ceramic	various	various
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	various
C1, C2, C3, C5, C6(1)	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various	various
J3, J4, J5	n/a	Solder Turret	various	various

Notes:
1. For 50-500 MHz operation set L1=82 nH and C1, C2, C5, C6=1000 pF.

Typical Performance TQP3M9035-PCB V_{DD} = +5 V

Test conditions unless otherwise noted: I_{DD}=115 mA (typ.), Temp=+25°C

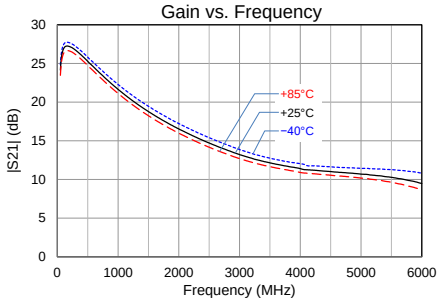
Parameter	Conditions	Typical Value				Units
Frequency		900	1900	2600	3500	MHz
Gain		22.0	16.5	14.0	12.0	dB
Input Return Loss		14	14	14	14	dB
Output Return Loss		13	10	8	7	dB
Output P1dB		+23	+23	+23		dBm
Output IP3	Pout= +4 dBm/tone, Δf=1 MHz	+37.2	+37.0	+37.3		dBm
Noise figure (1)		0.55	0.65	1.0	1.4	dB

Notes:
1. Noise figure data shown in the table above is de-embedded from the eval board loss.

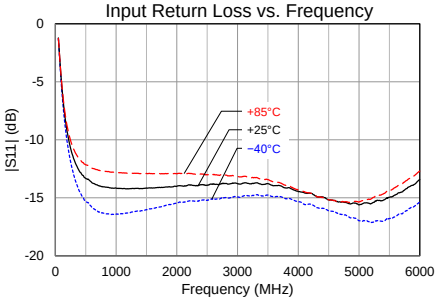
Performance Plots - TQP3M9035-PCB V_{DD} = +5 V

Test conditions unless otherwise noted: I_{DD}=115 mA (typ.), Temp=+25°C

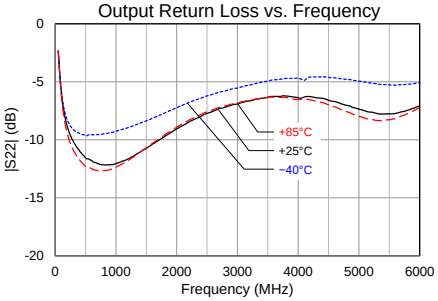
Gain vs. Frequency



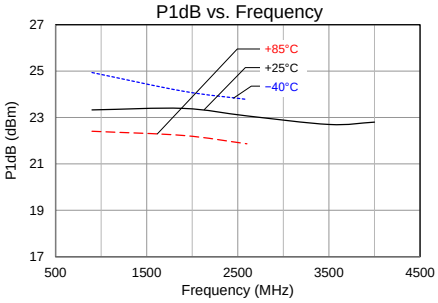
Input Return Loss vs. Frequency



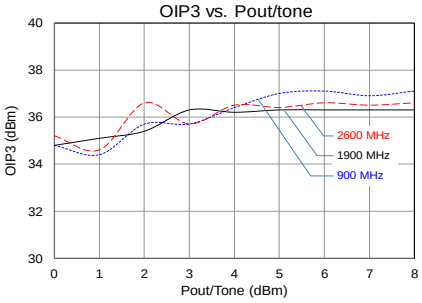
Output Return Loss vs. Frequency



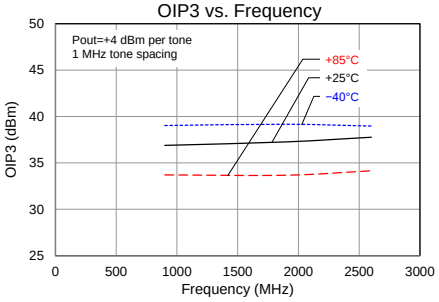
P1dB vs. Frequency



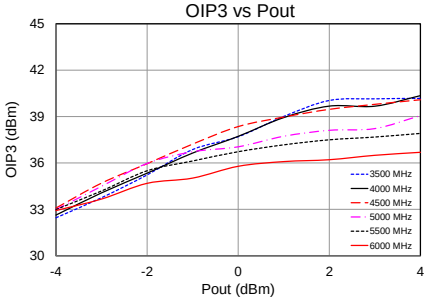
OIP3 vs. Pout/tone



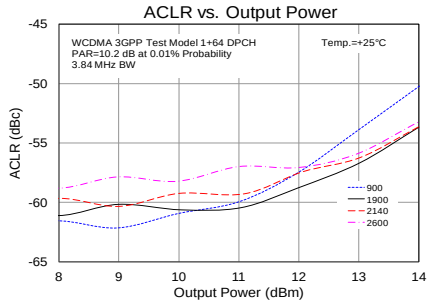
OIP3 vs. Frequency



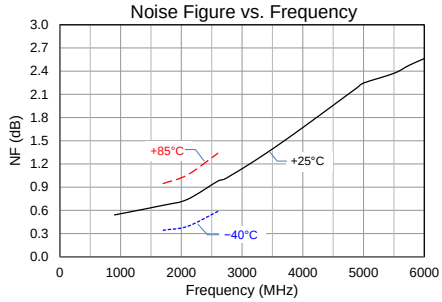
OIP3 vs Pout



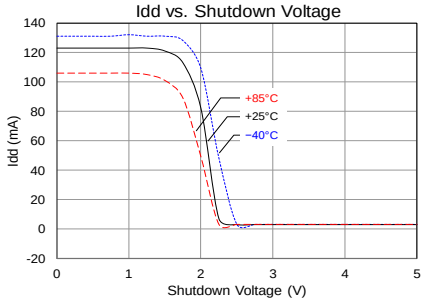
ACLR vs. Output Power



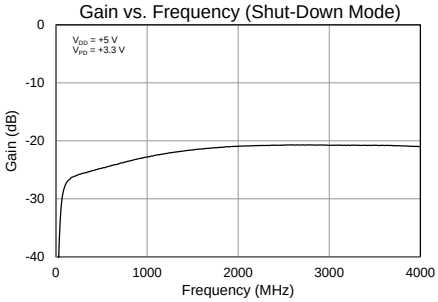
Noise Figure vs. Frequency



Idd vs. Shutdown Voltage



Gain vs. Frequency (Shut-Down Mode)



Typical Performance – TQP3M9035-PCB V_{DD} = +3.3 V

Test conditions unless otherwise noted: I_{DD}=67 mA (typ.), Temp=+25°C

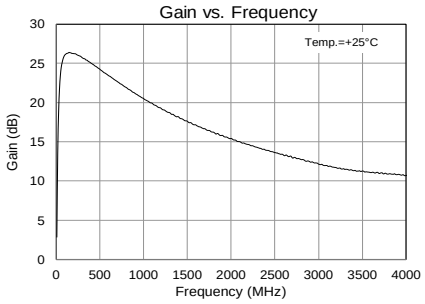
Parameter	Conditions	Typical Value		Units
Frequency		900	1900	MHz
Gain		21.2	15.8	dB
Input Return Loss		11.4	11.9	dB
Output Return Loss		15.6	10.6	dB
Output P1dB		+19	+18.8	dBm
Output IP3	Pout= +5 dBm/tone, Δf=1 MHz	+32.7	+33	dBm
Noise figure (1)		0.55	0.65	dB

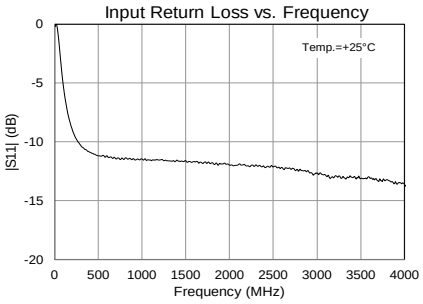
Notes:

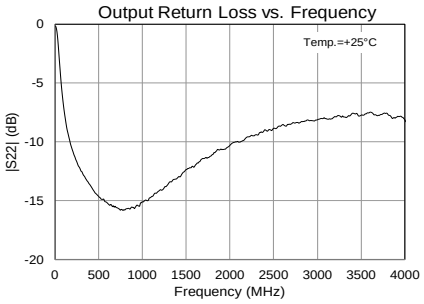
1. Noise figure data shown in the table above is de-embedded from the eval board loss.

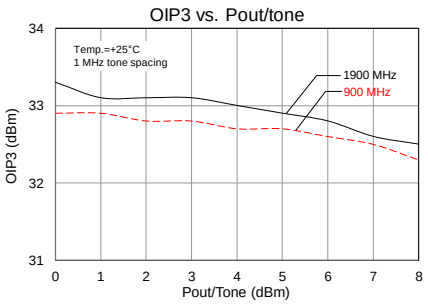
Performance Plots - TQP3M9035-PCB V_{DD} = +3.3 V

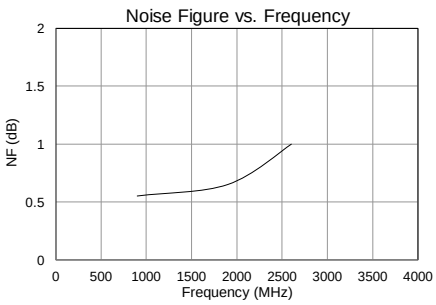
Test conditions unless otherwise noted: I_{DD} = 67 mA, T_{CASE} = +25°C, 50 Ω system











50 to 500 MHz IF Reference Design

TQP3M9035 performance may be optimized for IF operation below 500 MHz by making suitable adjustments to the value of the bias inductor L1 and the DC blocking capacitors C1 and C2. When using the TriQuint evaluation board be sure to match the value of C5 and C6 to that of C1 and C2 for accurate loss de-embedding.

Typical Performance – 50 to 500 MHz

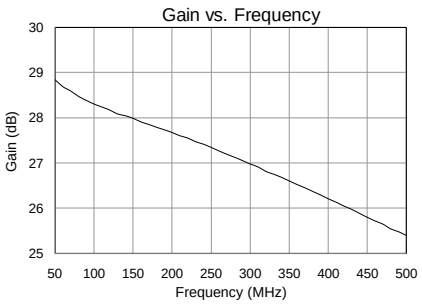
Test conditions unless otherwise noted: L1=82 nH, C1-C2, C5-C6=1000 pF, V_{DD}=+5V, I_{DD}=115 mA (typ.), Temp=+25°C

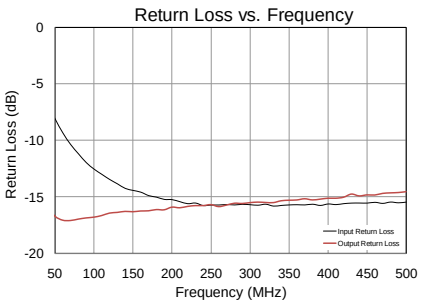
Parameter	Conditions	Typical Value				Units
Frequency		50	100	200	500	MHz
Gain		28.8	28.3	27.7	25.4	dB
Input Return Loss		8	12.5	15.2	15.4	dB
Output Return Loss		16.7	16.8	15.9	14.5	dB
Output P1dB		+17.7	+21.3	+23	+23.1	dBm
Output IP3	Pout= +5 dBm/tone, Δf=1 MHz	+32.9	+40.3	+38.8	+38.9	dBm
Noise figure (1)		0.64	0.52	0.56	0.56	dB

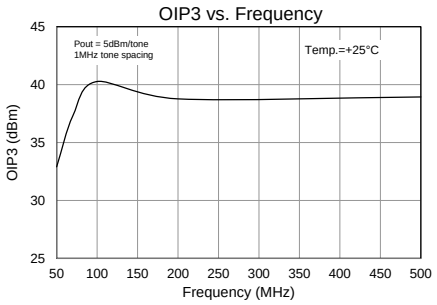
Notes:
1. Noise figure data shown in the table above is de-embedded from the eval board loss.

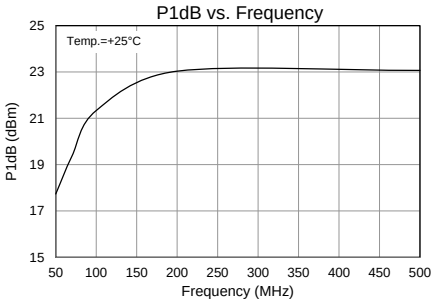
Performance Plots – 50-500 MHz

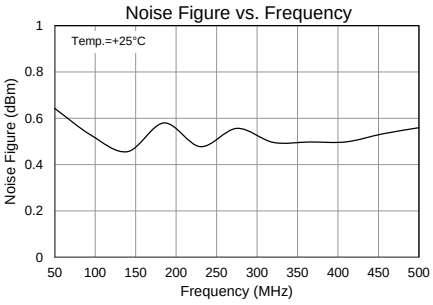
Test conditions unless otherwise noted: : L1=82 nH, C1-C2, C5-C6=1000 pF, V_{DD}=+5V, I_{DD}=115 mA (typ.), Temp=+25°C



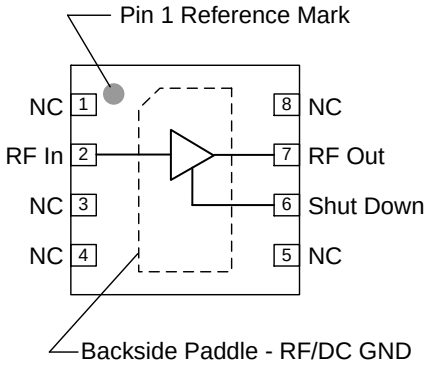








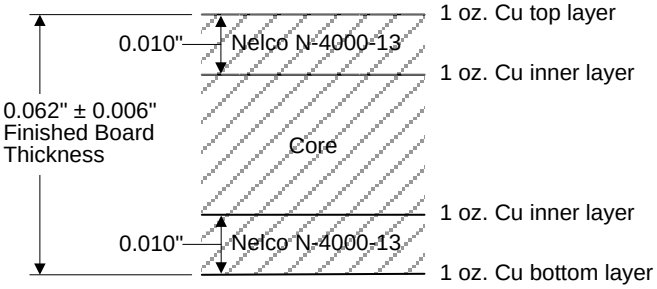
Pin Configuration and Description



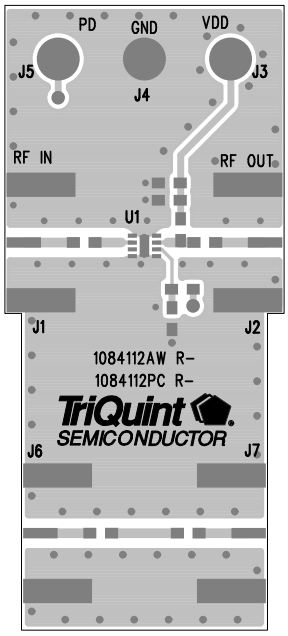
Pin No.	Label	Description
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	High Voltage (0.5 to 1.1V) turns OFF the device and Low Voltage (0 to 0.2V) turns ON the device.
7	RF Out / DCBias	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
1, 3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

Qorvo PCB 1084112 Material and Stack-up



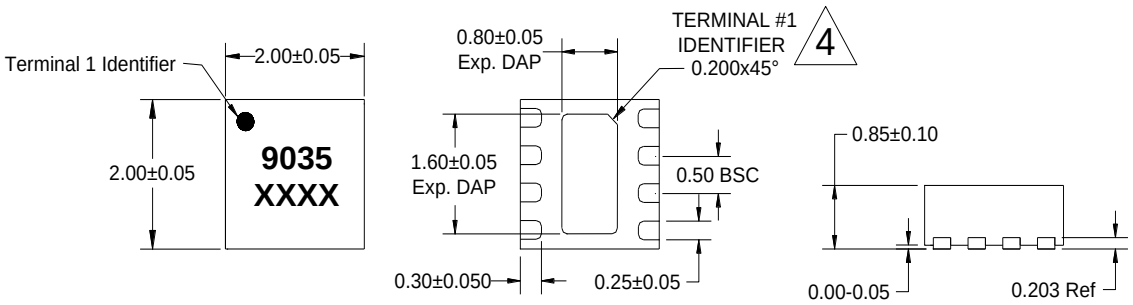
50 ohm line dimensions: width = .031”, spacing = .035”



Mechanical Information

Package Marking and Dimensions

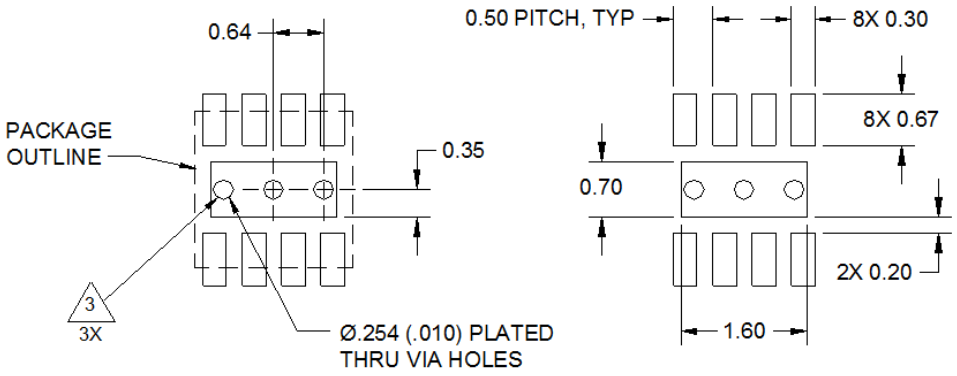
Marking: Part number – 9035
Lot Code – XXXX



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

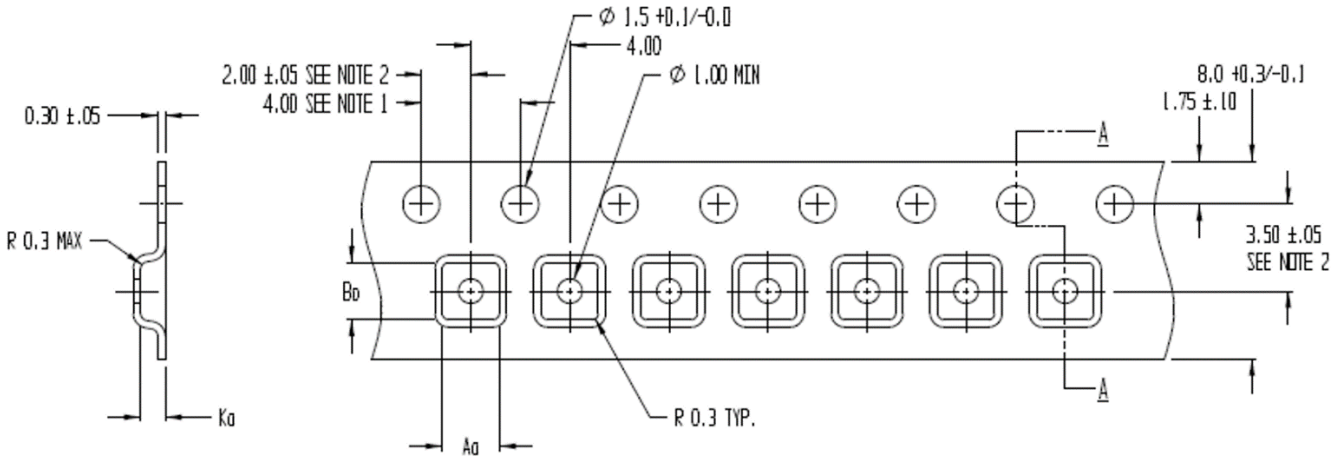
PCB Mounting Pattern



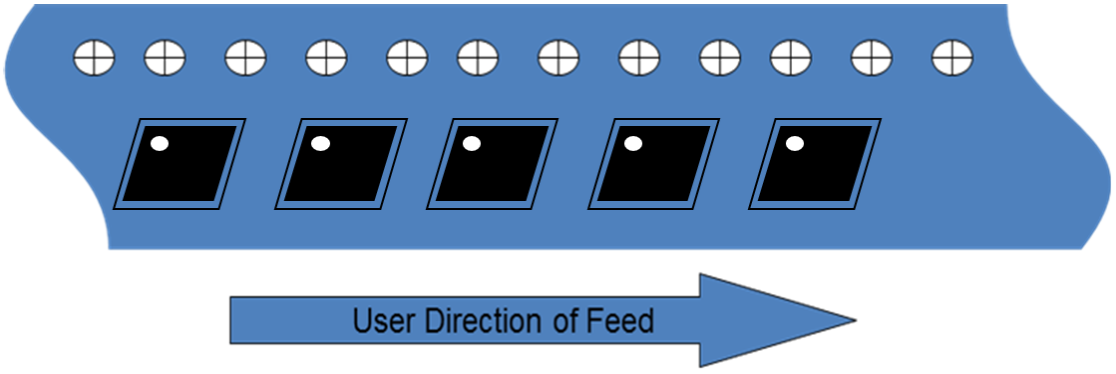
Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions

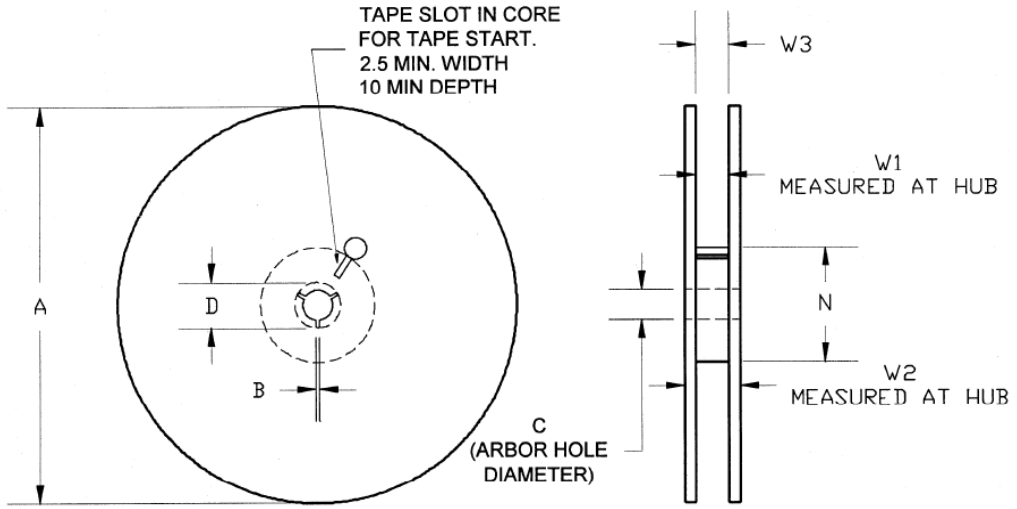


Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.039	1.00
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00



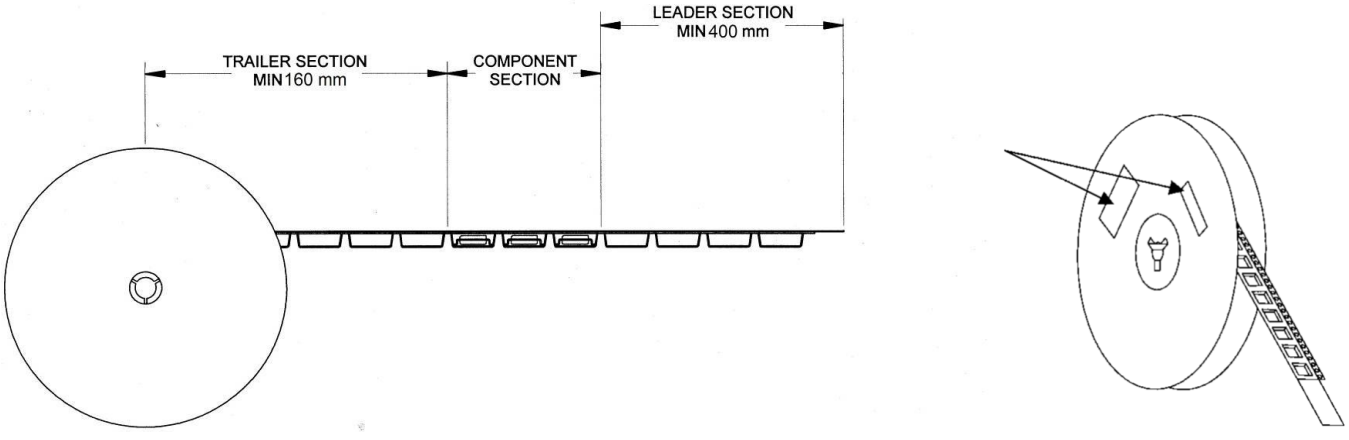
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	C3	ESDA / JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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