TPS99000-Q1 System Management and Illumination Controller

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Automotive System Management Device for DLP® Products:
  - Advanced Power Monitoring, Sequencing, and Protection Circuits
  - Two Die Temperature Monitors, MCU External Watchdog Timer, Clock Frequency Monitor
  - System Over-Brightness Detection
  - SPI Port With Parity, Checksum, and Password Register Protection
  - Second SPI Port for Independent System Monitoring
- On-Chip DMD Mirror Voltage Regulators
  - Generates +16 V, +8.5 V and –10 V DMD Control Voltages
- High Dynamic Range Dimming and Color Control, Enabling > 5000:1 Dimming Range With High Bit Depth and White Color Balance:
  - Two Transimpedance Amplifiers (TIA) With Wide Dynamic Range Supporting Numerous Optical Designs
  - 12-bit ADC With up to 63 Time Sequence Samples per Frame
  - DAC and Comparator Functions for Color and Pulse Control
  - FET Drivers for LED and Shunt Control

2 Applications

- Wide Field of View and Augmented Reality Head-Up Display (HUD) Systems
- Automotive Advanced Lighting Applications (High Resolution Headlight)
- Adaptive Driving Beam (ADB)

3 Description

The TPS99000-Q1 system management and illumination controller is part of the DLP553x-Q1 chipset, which also includes the DLPC230-Q1 DMD display controller. The chipset provides all functions needed to support and exceed typical 5000:1 display dimming requirements for Head-Up Display (HUD) applications, with typical requirements of 3 to 15,000 nits brightness range and tight color point control.

An integrated DMD high-voltage regulator supplies DMD mirror reference voltages, meeting the required tight tolerances. The power supply sequencer and monitor provide robust coordination of power-up and power-down events for the entire chipset.

The TPS99000-Q1 illumination controller integrates a 12-bit ADC, two DACs (12-bit and 10-bit), and two high-performance photodiode signal conditioning transimpedance amplifiers (TIAs) as the core components of the illumination control system. The ADC is capable of automatic sampling up to 63 events per video frame.

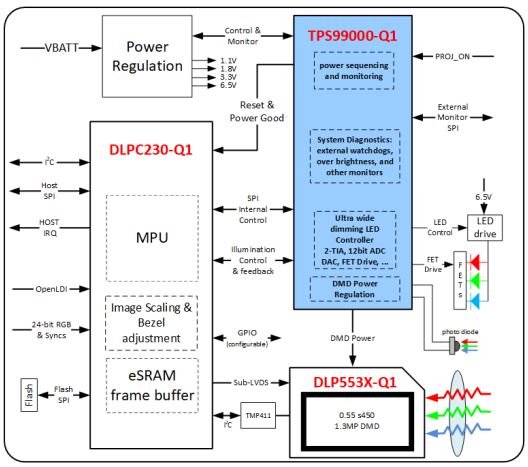
Advanced system status monitoring circuits provide real-time visibility into display sub-system operational condition, including two processor watchdog circuits, two die temperature monitors, comprehensive supply monitoring for overvoltage and undervoltage detection, checksum and password register protection with byte-level parity on SPI bus transactions, an excessive brightness monitor circuit, and other built-in test functions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS99000-Q1	HTQFP (100)	14.00 mm × 14.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Standalone System



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision D (May 2018) to Revision E **Page**

- Changed device status from *Advance Information* to *Production Data* ... 1

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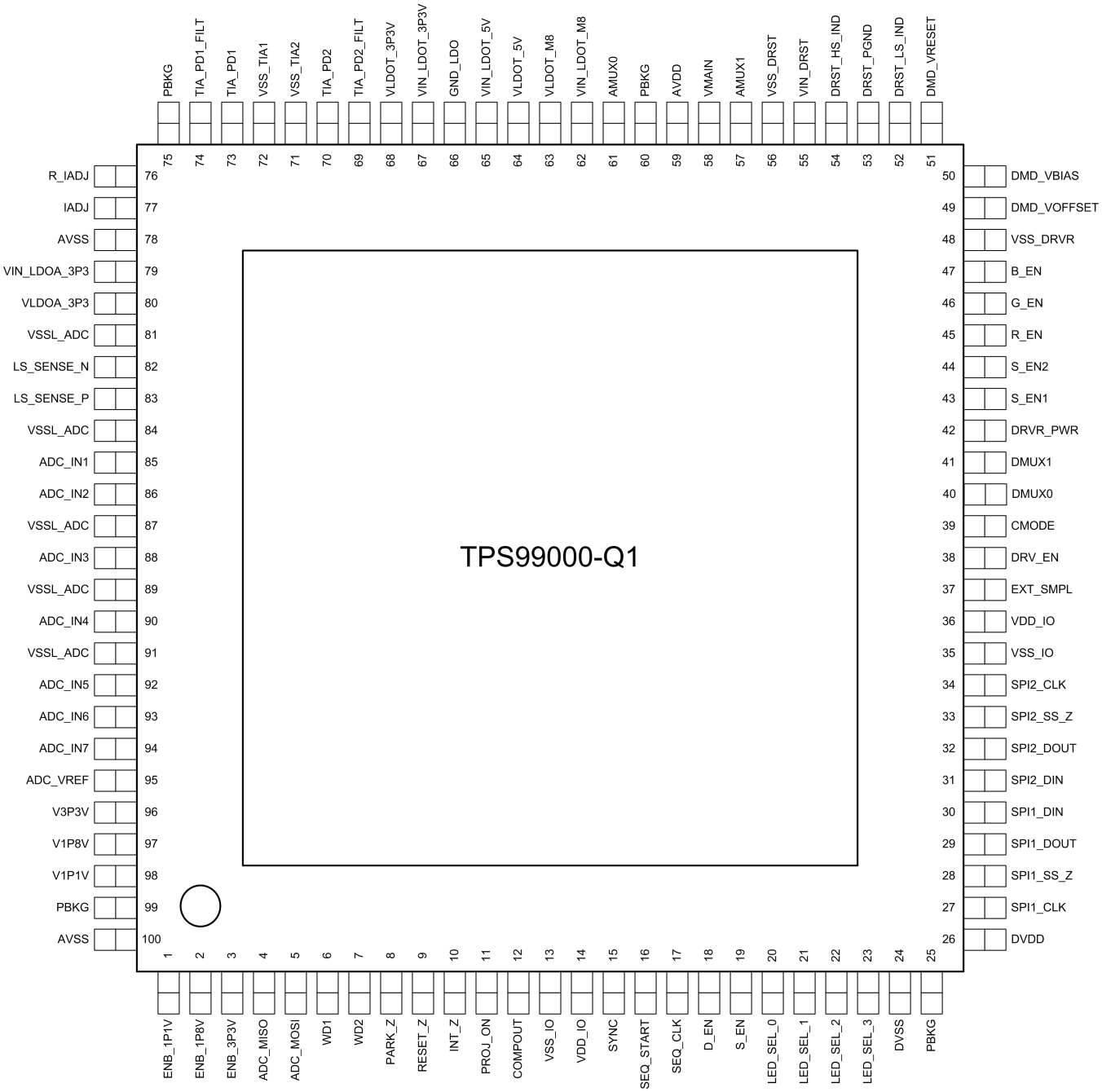
5 Pin Configuration and Functions

PZP Package
100-Pin HTQFP
Top View



Pin Functions - Initialization, Clock, and Diagnostics

PIN		TYPE	DESCRIPTION
NO.	NAME		
6	WD1	I	Watch Dog Interrupt Channel 1
7	WD2	I	Watch Dog Interrupt Channel 2
8	PARK_Z	O	DMD Mirror Parking Signal (active low)
9	RESET_Z	O	Reset output to the DLPC230-Q1. TPS99000-Q1 controlled.
10	INT_Z	O	Interrupt output signal to DLPC230-Q1 (open drain). Recommended to pull up to the DLPC230-Q1 3.3 V rail controlled by the TPS99000-Q1's ENB_3P3V signal.
11	PROJ_ON	I	Input signal to enable/disable the IC and DLP projector
16	SEQ_START	I	PWM Shadow Latch Control; indicates a Start of Sequence
17	SEQ_CLK	I	Sequencer Clock
40	DMUX0	O	Digital test point output
41	DMUX1	O	Digital test point output
57	AMUX1	O	Analog Test Mux Output 1
61	AMUX0	O	Analog Test Mux Output 0

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Pin Functions - Power and Ground

PIN		TYPE	DESCRIPTION
NO.	NAME		
13, 35	VSS_IO	GND	Ground Connection for Digital IO Interface
14, 36	VDD_IO	POWER	3.3 V power input for IO rail supply
24	DVSS	GND	Digital Core Ground Return
25, 60, 75, 99	PBKG	GND	Substrate Tie and ESD Ground Return
26	DVDD	POWER	3.3 V power input for digital core supply
42	DRVR_PWR	POWER	6 V or 3.3 V power input for FET driver power. Supply for S_EN1, S_EN2, R_EN, G_EN, & B_EN outputs
48	VSS_DRVR	GND	Ground Connection for FET driver power
49	DMD_VOFFSET	POWER	VOFFSET output rail. Connect a 1μF ceramic capacitor to ground
50	DMD_VBIAS	POWER	VBIAS output rail. Connect a 0.47μF ceramic capacitor to ground
51	DMD_VRESET	POWER	VRESET output rail. Connect a 1μF ceramic capacitor to ground. Connect to DRST_HS_IND through external diode. Connect anode of diode to DMD_VRESET.
53	DRST_PGND	GND	Power ground for DMD power supply. Connect to ground plane
55	VIN_DRST	POWER	6 V input for DMD power supply
56	VSS_DRST	GND	Ground Supply for DMD power supply
59	AVDD	POWER	3.3 V power supply input for analog circuit
63	VLDOT_M8	POWER	Dedicated TIA Interface –8 V LDO output
64	VLDOT_5V	POWER	Filter Cap Interface for 5 V TIA LDO
65	VIN_LDOT_5V	POWER	6 V power input for 5 V TIA LDO
66	GND_LDO	GND	Power ground return for LDO
67	VIN_LDOT_3P3V	POWER	6 V power input for 3.3 V TIA LDO
68	VLDOT_3P3V	POWER	Filter Cap Interface for 3.3 V TIA LDO
71	VSS_TIA2	GND	TIA2 Dedicated Ground
72	VSS_TIA1	GND	TIA1 Dedicated Ground
78, 100	AVSS	GND	Analog Ground
79	VIN_LDOA_3P3	POWER	6 V power input for dedicated ADC interface 3.3 V LDO supply
80	VLDOA_3P3	POWER	Dedicated ADC Interface 3.3 V LDO Filter Cap Output
81, 84, 87, 89, 91	VSSL_ADC	GND	External ADC Channel Bondwire and Lead Frame Isolation Ground
95	ADC_VREF	POWER	ADC Reference voltage output

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Pin Functions - Power Supply Management

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	ENB_1P1V	O	External 1.1 V Buck Enable. 3.3 V Output
2	ENB_1P8V	O	External 1.8 V Buck Enable. 3.3 V Output
3	ENB_3P3V	O	External 3.3 V Buck Enable. 3.3 V Output
52	DRST_LS_IND	ANA	Connection for the DMD power supply inductor (10μH). Connect a 330pF 50 V capacitor to ground. X7R recommended
54	DRST_HS_IND	ANA	Connection for the DMD power supply inductor (10μH)
58	VMAIN	I	Main intermediate voltage monitor input. Use external resistor divider to set voltage input for brownout monitoring
62	VIN_LDOT_M8	O	Dedicated TIA Interface –8 V LDO external regulation FET drive signal
96	V3P3V	I	External 3.3 V Buck Voltage Monitor Input
97	V1P8V	I	External 1.8 V Buck Voltage Monitor Input
98	V1P1V	I	External 1.1 V Buck Voltage Monitor Input

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Pin Functions - Illumination Control

PIN		TYPE	DESCRIPTION
NO.	NAME		
12	COMPOUT	O	Photodiode (PD) Interface High-speed comparator output
15	SYNC	O	External LED buck driver sync strobe output
18	D_EN	I	LED Interface; Buck High-Side FET Drive Enable
19	S_EN	I	LED Bypass Shunt Strobe Input
20	LED_SEL_0	I	LED Enable Strobe 0 Input
21	LED_SEL_1	I	LED Enable Strobe 1 Input
22	LED_SEL_2	I	LED Enable Strobe 2 Input
23	LED_SEL_3	I	LED Enable Strobe 3 Input
37	EXT_SMPL	I	Reserved. Connect to ground
38	DRV_EN	O	Drive enable for LM3409
39	CMODE	O	Capacitor selection output (allows for a smaller capacitance to be used in CM mode for less over/under shoot). Open drain
43	S_EN1	O	Low resistance shunt NFET drive enable [High means shunt active]
44	S_EN2	O	High resistance shunt NFET drive enable [High means shunt active]
45	R_EN	O	Red channel select. Drive for low side NFET
46	G_EN	O	Green channel select. Drive for low side NFET
47	B_EN	O	Blue channel select. Drive for low side NFET
69	TIA_PD2_FILT	O	TIA2 External Filter Cap - Low Bandwidth Sampling
70	TIA_PD2	I	TIA2 Photodiode Cathode Driver
73	TIA_PD1	I	TIA1 Photodiode Cathode Driver
74	TIA_PD1_FILT	O	TIA1 External Filter Cap - Low Bandwidth Sampling
76	R_IADJ	ANA	External resistance for IADJ voltage to current transformation
77	IADJ	ANA	Current output used to adjust external LED controller drive current set point

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Pin Functions - Serial Peripheral Interfaces

PIN		TYPE	DESCRIPTION
NO.	NAME		
27	SPI1_CLK	I	SPI Control interface (DLPC230-Q1 Master, TPS99000-Q1 slave), clock input
28	SPI1_SS_Z	I	SPI Control interface (DLPC230-Q1 Master, TPS99000-Q1 slave), chip select (active low)
29	SPI1_DOUT	O	SPI Control interface (DLPC230-Q1 Master, TPS99000-Q1 slave), Transmit data output
30	SPI1_DIN	I	SPI Control interface (DLPC230-Q1 Master, TPS99000-Q1 slave), Receive data input
31	SPI2_DIN	I	SPI Diagnostic Port (slave), Receive data input. For read-only monitoring
32	SPI2_DOUT	O	SPI Diagnostic Port (slave), Transmit data output. For read-only monitoring
33	SPI2_SS_Z	I	SPI Diagnostic Port (slave), chip select (active low). For read-only monitoring
34	SPI2_CLK	I	SPI Diagnostic Port (slave), clock input. For read-only monitoring

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Pin Functions - Analog to Digital Converter

PIN		TYPE	DESCRIPTION
NO.	NAME		
4	ADC_MISO	O	ADC 2-wire Interface - data Output. DLPC230-Q1 master, TPS99000-Q1 slave.
5	ADC_MOSI	I	ADC 2-wire Interface - data Input. DLPC230-Q1 master, TPS99000-Q1 slave.
82	LS_SENSE_N	I	Low side current sense ADC negative input, see Table 2
83	LS_SENSE_P	I	Low side current sense ADC positive input, see Table 2
85	ADC_IN1	I	External ADC Channel 1, see Table 2
86	ADC_IN2	I	External ADC Channel 2, see Table 2
88	ADC_IN3	I	External ADC Channel 3, see Table 2
90	ADC_IN4	I	External ADC Channel 4, see Table 2
92	ADC_IN5	I	External ADC Channel 5, see Table 2
93	ADC_IN6	I	External ADC Channel 6, see Table 2
94	ADC_IN7	I	External ADC Channel 7, see Table 2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VDD_IO to VSS_IO	–0.3	4	V
	DVDD to DVSS	–0.3	4	
	AVDD to DVSS	–0.3	4	
	All "VSS" to other "VSS" (grounds)	–0.1	0.1	
	All digital input signals to ground (WD1, WD2, ADC_MOSI, PROJ_ON, SEQ_START, SEQ_CLK, SPI1_CLK, SPI1_DIN, SPI1_SS, SPI2_DIN, SPI2_CLK, SPI2_SS, EXT_SMPL)	–0.3	3.6	
	DRVR_PWR to ground	–0.3	7.5	
	VIN_LDO_5V	–0.3	7.5	
	V3P3V to ground	–0.3	5	
	V1P8V to ground	–0.3	5	
	V1P1V to ground	–0.3	5	
	VIN_LDOA_3P3 to ground	–0.3	7.5	
	VIN_LDOT_3P3 to ground	–0.3	7.5	
	ADC_IN(7:1) to ground	–0.3	3.6	
	IADJ to ground	–0.3	18	
	R_IADJ to ground	–0.3	5	
	VIN_LDOT_M8 to ground	–18	0.3	
	DRST_LS_IND to DRST_PGND	–0.3	27	
	VIN_DRST to ground	–0.3	7.5	
	VMAIN	–0.3	7.5	
Outputs	INT_Z	–0.3	7.5	V
Operating junction temperature, T_J		–40	130	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
	Charged-device model (CDM), per AEC Q100-011	All pins	±500	
		Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
TEMPERATURE					
T_A	Operating ambient temperature[1]	–40		105	°C
T_J	Operating junction temperature	–40		125	°C
VOLTAGE					
VDD_IO	IO 3.3 V Voltage Supply	3	3.3	3.6	V
DVDD	Digital 3.3 V Supply	3	3.3	3.6	V
AVDD	Analog 3.3 V Supply	3	3.3	3.6	V
ADC	ADC(7:1) Inputs	0.1		1.6	V
VIN_DRST	DMD Reset Regulator Input	5.5	6	7	V
VIN_LDOT_5V	Power supply input to 5 V TIA LDO	5.5	6	7	V
VIN_LDOA_3P3V	Power supply input to 3.3 V ADC LDO	5.5	6	7	V
VIN_LDOT_3P3V	Power supply input to 3.3 V TIA LDO	5.5	6	7	V
DRVR_PWR	Gate driver power supply	3	6	7	V

(1) –40°C to 105°C ambient, free air convection, AEC Q100 grade 2.

6.4 Thermal Information

THERMAL METRIC[1][2]		TPS99000-Q1 PZP (HTQFP) 100 PINS	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) Operating ambient temperature is dependent on system thermal design. Operating junction temperature may not exceed its specified range across ambient temperature conditions.

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6.5 Electrical Characteristics - Transimpedance Amplifier Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIA1 AND TIA2						
I_{IN_TOT}	TIA1 and TIA2 Combined Input Current		0		7(1)	mA
TRANSIMPEDANCE AMPLIFIER #1 (TIA1)						
I_{IN}	TIA Input Current	RGB trim <= 0.5x(2)	0	0.6	4.8	mA
V_{SAT}	TIA DC Saturation Voltage			2.5		V
C_{IN}	Total Input Capacitance(3)	Allowable input capacitances from board, connectors, photo diode, and cables	10	50	140	pF
$TRIM_{RGB}$	RGB Trim, normal flux system		0.2	0.5	1	V/V
$GAINTOL_{ABS}$	TIA Gain Tolerance (absolute)	Tolerance to specified gain target per setting	–20%		20%	
$GAINTOL_{REL}$	TIA Gain Tolerance (relative)	Tolerance as a ratio to other settings		3%		
TIA1 SLEW RATE						
TIA_{SLEW1}	Low Gain Slew Rate, Output Referred	<= 96 kV/A gain	12			V/µs
TIA_{SLEW2}	High Gain Slew Rate, Output Referred	> 96 kV/A gain	5			V/µs
TIA_{DELAY}	TIA Pad to COMPOUT Pad Delay, DM min, Falling Edge	max slew rate input, 20 pF load, 100 mV minimum over trip point		40	64	ns
$TIA_{DELAYCM}$	TIA Pad to COMPOUT Delay. CM	CM max current			100	ns
TIA1 EFFECTIVE GAIN						
	Gain Setting 0	Trim set to 1.0	0.6	0.75	0.9	kV/A
	Gain Setting 1	Trim set to 1.0	1.2	1.5	1.8	kV/A
	Gain Setting 2	Trim set to 1.0	2.4	3	3.6	kV/A
	Gain Setting 3	Trim set to 1.0	4.8	6	7.2	kV/A
	Gain Setting 4	Trim set to 1.0	7.2	9	10.8	kV/A
	Gain Setting 5	Trim set to 1.0	9.6	12	14.4	kV/A
	Gain Setting 6	Trim set to 1.0	14.4	18	21.6	kV/A
	Gain Setting 7	Trim set to 1.0	19.2	24	28.8	kV/A
	Gain Setting 8	Trim set to 1.0	28.8	36	43.2	kV/A
	Gain Setting 9	Trim set to 1.0	38.4	48	57.6	kV/A
	Gain Setting 10	Trim set to 1.0	57.6	72	86.4	kV/A
	Gain Setting 11	Trim set to 1.0	76.8	96	115.2	kV/A
	Gain Setting 12	Trim set to 1.0	115.2	144	172.8	kV/A
	Gain Setting 13	Trim set to 1.0	230.4	288	345.6	kV/A

(1) For applications requiring greater than 7 mA combined TIA current, contact TI for details.
(2) Maximum input current decreases linearly in proportion to the selected trim value, with a lower maximum value of 2.4 mA occurring when the trim is 1.0×.
(3) Large capacitive loads could impact system performance.

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Electrical Characteristics - Transimpedance Amplifier Parameters (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSIMPEDANCE AMPLIFIER #2 (TIA2)						
I_{IN}	TIA Input Current	RGB trim <= 0.5x[2]	0		4.8	mA
V_{SAT}	TIA DC Saturation Voltage			2.5		V
$TRIM_{RGB}$	RGB Trim, normal flux system		0.2		1	V/V
TIA2 SLEW RATE						
$TIA2_{SLEW}$	Slew Rate, Output Referred	All gains	1			V/µs
TIA2 EFFECTIVE GAIN						
	Gain Setting 0	Trim set to 1.0	0.6	0.75	0.9	kV/A
	Gain Setting 1	Trim set to 1.0	1.2	1.5	1.8	kV/A
	Gain Setting 2	Trim set to 1.0	2.4	3	3.6	kV/A
	Gain Setting 3	Trim set to 1.0	4.8	6	7.2	kV/A
	Gain Setting 4	Trim set to 1.0	7.2	9	10.8	kV/A
	Gain Setting 5	Trim set to 1.0	9.6	12	14.4	kV/A
	Gain Setting 6	Trim set to 1.0	14.4	18	21.6	kV/A
	Gain Setting 7	Trim set to 1.0	19.2	24	28.8	kV/A
	Gain Setting 8	Trim set to 1.0	28.8	36	43.2	kV/A
	Gain Setting 9	Trim set to 1.0	38.4	48	57.6	kV/A
	Gain Setting 10	Trim set to 1.0	57.6	72	86.4	kV/A
	Gain Setting 11	Trim set to 1.0	76.8	96	115.2	kV/A
	Gain Setting 12	Trim set to 1.0	115.2	144	172.8	kV/A
	Gain Setting 13	Trim set to 1.0	230.4	288	345.6	kV/A

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6.6 Electrical Characteristics - Digital to Analog Converters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PHOTO FEEDBACK 12 BIT DAC						
$V_{OUTDAC\ Max}$	Output Range max		1.96	2	2.04	V
$V_{OUTDAC\ Min}$	Output Range min		–0.1	0	0.1	V
t_{SET}	Settling Time	Full-range step response, To within ±2%	0		500	ns
T_{SLEW}	Slew Rate			5		V/µs
INL	Integral Non-Linearity		–3.5		3.5	LSB
DNL	Differential Non-Linearity		–3.5		3.5	LSB
VOFF	Offset Error		–100		100	mV
$ZERO_{ERR}$	Zero-scale Error		–100		100	mV
$GAIN_{ERR}$	Gain Error		–5		5	%V/code
FS_{ERR}	Full-scale Error		–2		2	%FSR
$ZERO_{ERRDFT}$	Zero-scale Error Drift		–50	20	50	µV/°C
$GAIN_{TEMP}$	Gain Temperature Coefficient		–52	0	52	ppm FSR/°C
CURRENT CONTROL 10 BIT DAC						
$V_{OUTDAC\ Max}$	Output Range max		1.96	2	2.04	V
$V_{OUTDAC\ Min}$	Output Range min		–0.1	0	0.1	V
t_{SET}	Settling Time	Full-range step response to within ±2%	0		1000	ns
T_{SLEW}	Slew Rate			5		V/µs
INL	Integral Non-Linearity		–2		2	LSB
DNL	Differential Non-Linearity		–2		2	LSB
V_{OFF}	Offset Error		–100		100	mV
$ZERO_{ERR}$	Zero-scale Error		–100		100	mV
$GAIN_{ERR}$	Gain Error		–5		5	%V/code
FS_{ERR}	Full-scale Error		–2		2	%FSR
$ZERO_{ERRDFT}$	Zero-scale Error Drift		–50	20	50	µV/°C
$GAIN_{TEMP}$	Gain Temperature Coefficient		–-52	0	52	ppm FSR/°C
OVERBRIGHTNESS DETECTOR 8 BIT DAC						
$V_{OUTDAC\ max}$	Output Range max		1.95	2	2.05	V
$V_{OUTDAC\ min}$	Output Range min		–0.1	0	0.1	V
t_{OBDAC}	Over-brightness DAC Adjustment Time	From input code mux input change to 90/10 settling at analog output			1000	µs
INL	Integral Non-Linearity		–1		1	LSB
DNL	Differential Non-Linearity		–0.5		0.5	LSB
V_{OFF}	Offset Error		–100		100	mV
$ZERO_{ERR}$	Zero-scale Error		–100		100	mV
$GAIN_{ERR}$	Gain Error		–5		5	%V/code
FS_{ERR}	Full-scale Error		–3		3	%FSR
$ZERO_{ERRDFT}$	Zero-scale Error Drift		–50	20	50	µV/°C
$GAIN_{TEMP}$	Gain Temperature Coefficient		–52	0	52	ppm FSR/°C

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6.7 Electrical Characteristics - Analog to Digital Converter

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
12 BIT ADC(1)						
V_{INPUT}	Input Range(2)		0.1		1.6	V
INL	Integral Non-Linearity	Over valid input range VINPUT	–4		4	LSB
DNL	Differential Non-Linearity		–2.5		2.5	LSB
ENOB	Effective Number Of Bits		10	12		bits
t_{SAMPLE}	S/H Sampling Period		0.4	5.2	12.8	µs
t_{DELAY}	S/H Delay before conversion starts		0.4		2.8	µs
t_{SHOLD}	S/H Holding Period			102.4	245	µs
t_{CONV}	Conversion Period			102.4		µs
V_{REF}	Measurement Reference	ADC reference voltage is doubled to 1.6 V	0.784	0.8	0.816	V
V_{OFFS}	Offset		–20		20	LSB
	Gain Error	"ADC_IN(7:1) Inputs	2		2	%FSR

(1) ADC specifications refer to ADC core behavior, presume ideal clocks and IC input power conditions, unless otherwise noted.
(2) Results in invalid ADC codes below 256.

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6.8 Electrical Characteristics - FET Gate Drivers

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LED CONTROL SIGNAL FET GATE DRIVERS						
Q_{SEN}	S_EN1/2 Load Gate Charge			12	16.5	nC
Z_{SEN}	S_EN1/2 Pull-up Gate Drive Output Impedance	3.3 V domain(1)		12.3		Ω
		6 V domain(2)		10.7		Ω
Z_{SEN}	S_EN1/2 Pull-down Gate Drive Output Impedance	3.3 V domain(1)		4.85		Ω
		6 V domain(2)		4.6		Ω
T_{SEN}	S_EN1/2 Pull-up Transition Time	3.3 V domain, with max total gate charge load of 2.5 nF(1)	49.5	66	82.5	ns
		6 V domain, with max total gate charge load of 2.5 nF(2)	45	60	75	ns
T_{SEN}	S_EN1/2 Pull-down Transition Time	3.3 V domain, with max total gate charge load of 2.5 nF(1)	20.25	27	33.75	ns
		6 V domain, with max total gate charge load of 2.5 nF(2)	18.75	25	31.25	ns
Z_{RGB}	RGB_EN Pull-up Output Impedance	3.3 V domain(1)		50.8		Ω
		6 V domain(2)		43.6		Ω
Z_{RGB}	RGB_EN Pull-down Output Impedance	3.3 V domain(1)		4.85		Ω
		6 V domain(2)		4.6		Ω
T_{RGB}	RGB_EN Pull-up Falling Transition Time	3.3 V domain, with max total gate charge load of 2.5 nF(1)	198.75	265	331.25	ns
		6 V domain, with max total gate charge load of 2.5 nF(2)	180	240	300	ns
T_{RGB}	RGB_EN Pull-down Falling Transition Time	3.3 V domain, with max total gate charge load of 2.5 nF(1)	20.25	27	33.75	ns
		6 V domain, with max total gate charge load of 2.5 nF(2)	18.75	25	31.25	ns

(1) DRVR_PWR Supply Voltage is between 3 V and 3.6 V.
(2) DRVR_PWR Supply Voltage is between 5.5 V and 7.5 V.

6.9 Electrical Characteristics - Photo Comparator

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PHOTO FEEDBACK COMPARATOR						
V_{OFF}	Offset Voltage		–10		10	mV
T_{HYST}	Hysteresis		10	20		mV

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6.10 Electrical Characteristics - Voltage Regulators

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOFFSET REGULATOR						
V_{OUT}	Output Voltage	Across load conditions	8.25	8.5	8.75	V
I_{OUT}	Output Current (1)		0.1 (2)		16.3	mA
$V_{PGTHRESHR}$	Powergood Threshold, VOUT Rising			86%		
$V_{PGTHRESHF}$	Powergood Threshold, VOUT Falling			66%		
C_{OUT}	Output Capacitor			1		µF
T_{DISC}	Discharge Time	C_{OUT} = 1 µF			260	µs
VBIAS REGULATOR						
V_{OUT}	Output Voltage		15.5	16	16.5	V
I_{OUT}	Output Current (1)		0.1 (2)		1.5	mA
$V_{PGTHRESHR}$	Powergood Threshold, VOUT Rising			86%		
$V_{PGTHRESHF}$	Powergood Threshold, VOUT Falling			66%		
C_{OUT}	Output Capacitor			0.47		µF
T_{DISC}	Discharge Time	C_{OUT} = 0.47 µF			260	µs
VRESET REGULATOR						
V_{OUT}	Output Voltage		–10.5	–10	–9.5	V
I_{OUT}	Output Current (3) (1)		–17.6		–0.1 (2)	mA
$V_{PGTHRESHR}$	Powergood Threshold			80%		
C_{OUT}	Output Capacitor			1		µF
T_{DISC}	Discharge Time	C_{OUT} = 1 µF			260	µs
NEGATIVE 8 V PHOTO DIODE LDO						
V_{IN}	Input Voltage			–10		V
V_{OUT}	Output Voltage	Unloaded	–8.5	–8	–7.5	V
I_{OUT}	Output Current		–6			mA
$V_{IRIPPLE}$	Input Ripple				100	mVpp

(1) VOFFSET, VBIAS, and VRESET are designed to supply the DMD and Negative 8 V LDO only, and should not be connected to additional loads.
(2) Pull down resistors required to meet minimum current requirement.
(3) VRESET current supplies both DMD and Negative 8 V LDO

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6.11 Electrical Characteristics - Temperature and Voltage Monitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE MONITOR						
$TEMP_{WARN}$	Thermal Warning Threshold	Junction Temperature		135		°C
$TEMP_{EMRG}$	Thermal Emergency Threshold	Junction Temperature		150		°C
1.1 V SUPPLY MONITOR						
V_{TRIPN}	Negative Trip Threshold	Negative going only	0.95	0.98	1.01	V
$V_{TRIPHYST}$	Hysteresis	Positive going threshold, amount higher than negative trip voltage		2%		
t_{GLITCH}	Glitch Suppression	Size of glitch ignored (no reset) with 2% overdrive	20		1000	µs
1.8 V SUPPLY MONITOR						
V_{TRIPN}	Negative Trip Threshold	Negative going only	1.552	1.6	1.648	V
$V_{TRIPHYST}$	Hysteresis	Positive going threshold, amount higher than negative trip voltage		2%		
t_{GLITCH}	Glitch Suppression	Size of glitch ignored (no reset) with 2% overdrive	20		1000	µs
3.3 V SUPPLY MONITOR						
V_{TRIPN}	Negative Trip Threshold	Negative going only	2.852	2.93	3.03	V
$V_{TRIPHYST}$	Hysteresis	Positive going threshold, amount higher than negative trip voltage		2%		
t_{GLITCH}	Glitch Suppression	Size of glitch ignored (no reset) with 2% overdrive	20		1000	µs
VMAIN SYSTEM INPUT SUPPLY MONITOR						
$V_{MAINTHRSH}$	VMAIN Threshold	External resistor divider used to translate VMAIN	1.2125	1.25	1.2875	V
$t_{MAINGLITCH}$	VMAIN Glitch Suppression	At 2% overdrive	20		1000	µs

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6.12 Electrical Characteristics - Current Consumption

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
SUM OF 3.3 V SUPPLY PINS: DVDD, VDD_IO, AND AVDD					
System off	PROJ_ON Low		1.5	2	mA
System on	Display On state, no TIAs enabled		3.5	4	mA
TIA #1	Additional current from enabling TIA #1		1	1	mA
TIA #2	Additional current from enabling TIA #2		1	1	mA
SUM OF 6 V SUPPLY PINS: DRVR_PWR, VIN_DRST, VIN_LDOT_5V, VIN_LDOT_3P3V, AND VIN_LDOA_3P3V					
System off	PROJ_ON Low		1	2	mA
System on(3)	Display On state, no TIAs enabled		98	119	mA
TIA #1	Additional current from enabling TIA #1		20	25	mA
TIA #2	Additional current from enabling TIA #2		20	25	mA

(1) Typical measurements performed at 25°C and nominal voltage.
(2) Measurements taken at –40°C, 25°C, and 105°C. 3.3 V inputs measured at 3 V, 3.3 V, 3.6 V. 6 V inputs measured at 5.5 V, 6 V, and 7 V. The maximum current draw of all these conditions is shown.
(3) This number represents the current at the input to the TPS99000-Q1 when the DMD voltage rails output the maximum current as listed in the respective sections of this datasheet. This number is the combination of the measured current when the DMD voltage regulator is unloaded (35 mA typical, 56 mA max) and the estimated current draw on the 6 V supply when the DMD voltage regulator outputs the maximum current (63 mA). The estimated current draw is calculated by the equation $I_{6V}=[(16/6)*I_{VBIAS}+(8.5/6)*I_{VOFFSET}+(-10/6)*I_{VRESET}]/\eta$ where η = 0.9. In order to calculate the power dissipation of the TPS99000-Q1 in this condition, multiply the current from the unloaded condition by the input voltage, and add the current from the DMD voltage regulator multiplied by the input voltage multiplied by (1-η).

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6.13 Power-Up Timing Requirements

			TYP	UNIT
t_{en_dly}	PROJ_ON to 1.1 V enable. This includes PROJ_ON t_{glitch} time.	Rising edge of PROJ_ON to rising edge of 1.1 V enable.	11	ms
t_{mon1} (1)(2)	Maximum time for 1.1 V rail to reach voltage threshold after enable has been asserted. This delay length will occur even if 1.1 V meets threshold earlier.	Rising edge of ENB_1P1V to internal 1.1 V monitor test.	10	ms
t_{mon2} (1)(2)	Maximum time for 1.8 V rail to reach voltage threshold after enable has been asserted. This delay length will occur even if 1.8 V meets threshold earlier.	Rising edge of ENB_1P8V to internal 1.8 V monitor test.	10	ms
t_{mon3} (1)(2)	Maximum time for 3.3 V rail to reach voltage threshold after enable has been asserted. This delay length will occur even if 3.3 V meets threshold earlier.	Rising edge of ENB_3P3V to internal 3.3 V monitor test.	10	ms
t_{w1}	RESETZ delay after voltage testing completion.	Completion of 3.3 V monitor test to RESETZ rising edge.	10	ms

(1) V1P1V, V1P8V, and V3P3V rails can be enabled prior to the TPS99000-Q1 assertion of their respective enable signal if required for system power design. If necessary, ENB_1P1V may be connected to the 1.1 V, 1.8 V, and 3.3 V external supply enables.
(2) If any voltage threshold is not met within the specified time, the TPS99000-Q1 will not de-assert RESETZ. The power-up procedure must be fully restarted in this situation.

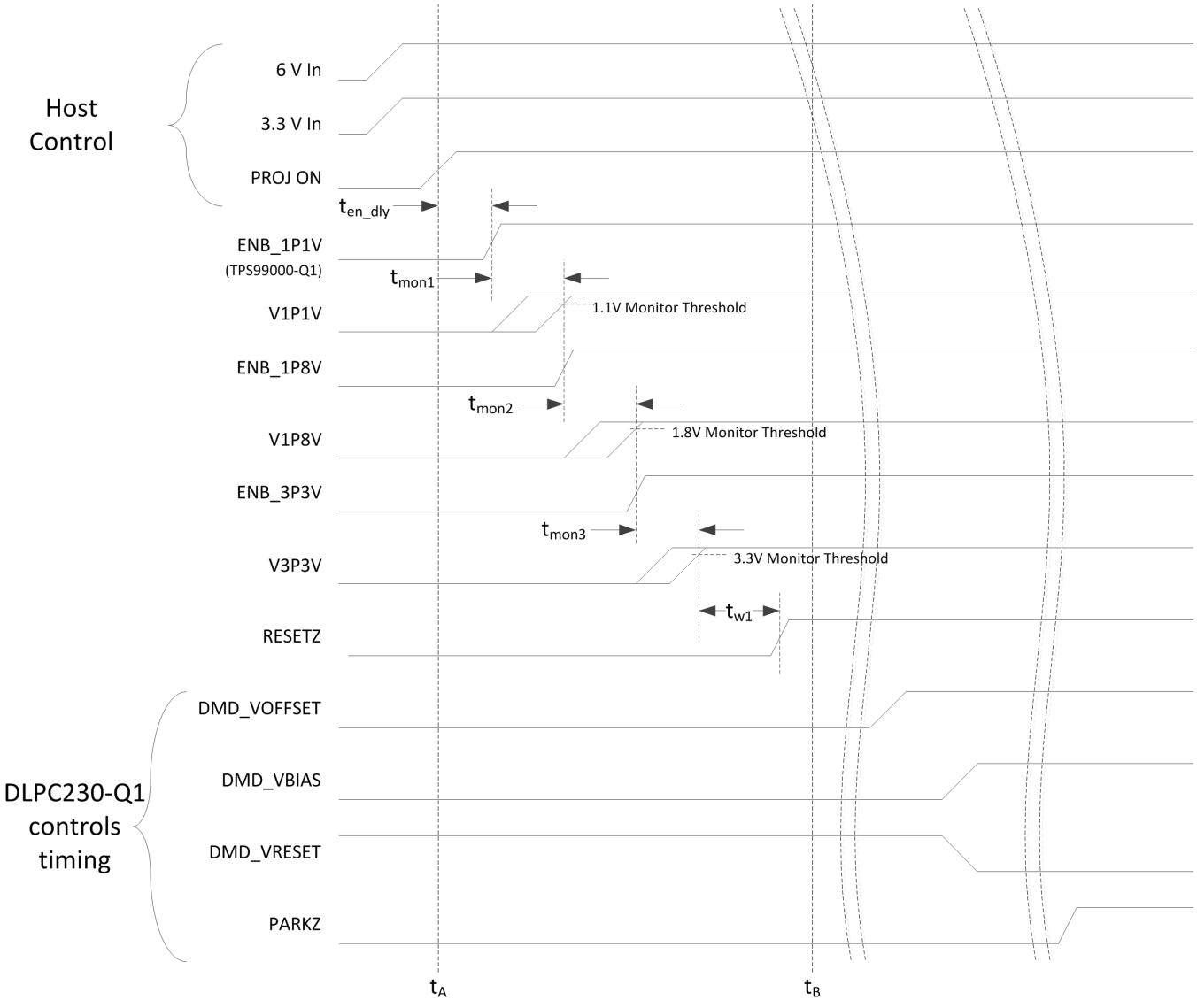

Figure 1. Power Up Timing

6.14 Power-Down Timing Requirements(1)

			MIN	MAX	UNIT
t_{vhold1}	Host voltage hold time after VMAIN minimum threshold reached. $t_{mon4}(max) + t_{park}(max) + t_{w2}(max)$	VMAIN threshold to 6 V and 3.3 V power loss.(2)(3)	900		µs
t_{vhold2}	Host voltage hold time after PROJ_ON de-asserted. $t_{mon5}(max) + t_{park}(max) + t_{w2}(max)$	VMAIN threshold to 6 V and 3.3 V power loss.(2)(3)	1.78		ms
t_{mon4}	VMAIN monitoring time.	Minimum voltage trip threshold to PARKZ falling edge.	52	120	µs
t_{mon5}	PROJ_ON de-assertion reaction time.	Falling edge of PROJ_ON to PARKZ falling edge.		1	ms
t_{park}	DMD Park time.	PARKZ falling edge to start DMD_VOFFSET discharge.		280	µs
$t_{discharge}$ (4)	DMD voltage rail discharge time.	VOFFSET C_{out}= 1 µF VRESET C_{out}= 1 µF VBIAS C_{out}= 0.47 µF		260	µs
t_{w2}	DMD voltage disable to RESETZ de-assertion.	Start of DMD voltage rail discharge to RESETZ falling edge.		500	µs

(1) There are two methods for initiating the power down sequence:
(a) VMAIN voltage decreases below its minimum threshold. This is typical if the TPS99000-Q1 is expected to initiate the power down sequence when main power is removed from the system. Note that the 6 V and 3.3 V input rails must remain within operating range for a specified period of time after the power-down sequence begins.
(b) PROJ_ON low. This is allows a host controller to initiate power down through a digital input to the TPS99000-Q1.
(2) 6 V input rails include DRVR_PWR, VIN_DRST, VIN_LDOT_5V, VIN_LDOA_3P3V, VIN_LDOT3P3V.
(3) 3.3 V input rails include VDD_IO, DVDD, AVDD.
(4) The DMD specifies a maximum absolute voltage difference between VBIAS and VOFFSET. In order to remain below this maximum voltage difference, VBIAS must discharge faster than VOFFSET. This is accomplished by using a smaller C_{out} capacitance for VBIAS in order to allow it to discharge quicker than VOFFSET.

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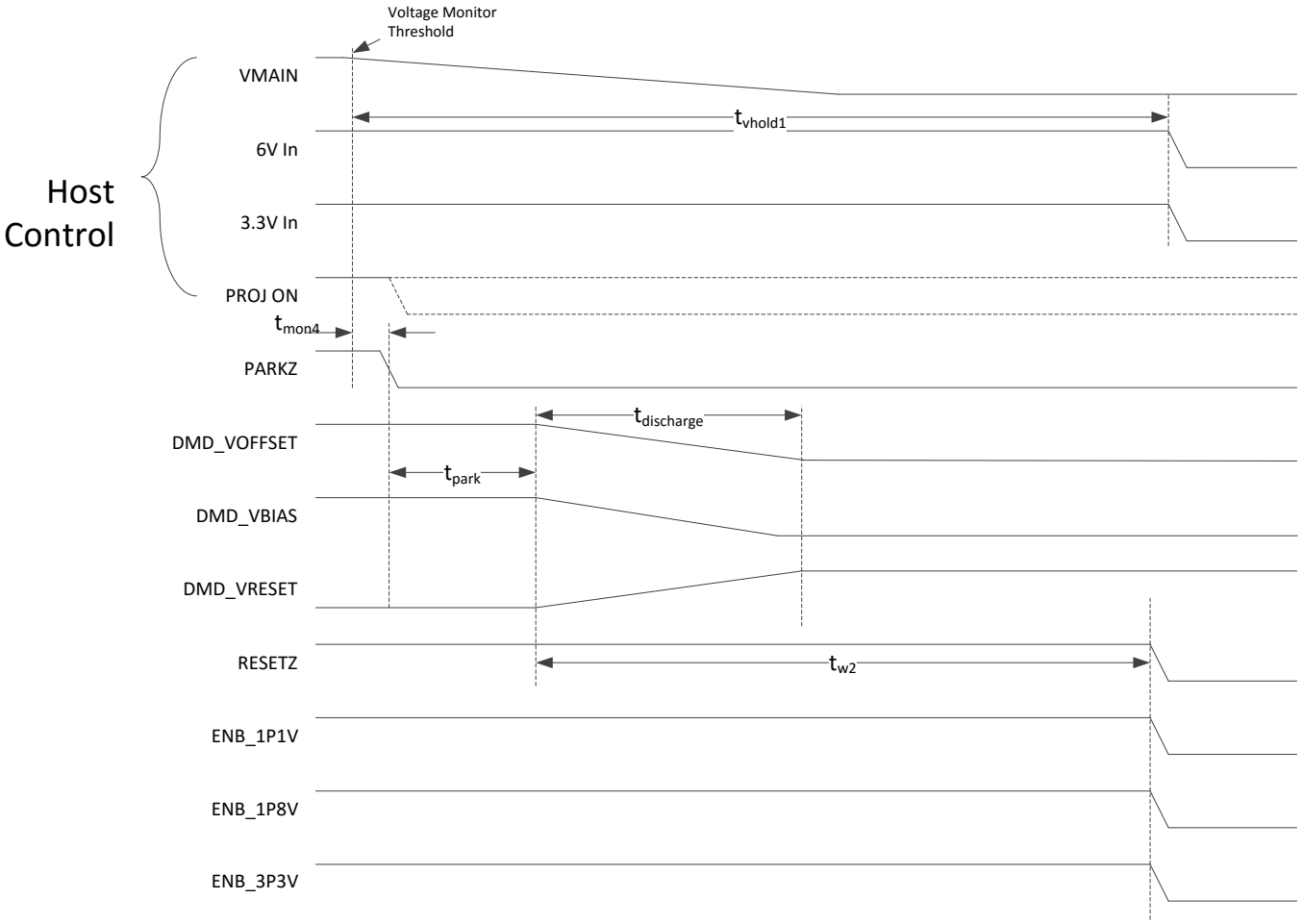

Figure 2. Power Down Timing - VMAIN Trigger

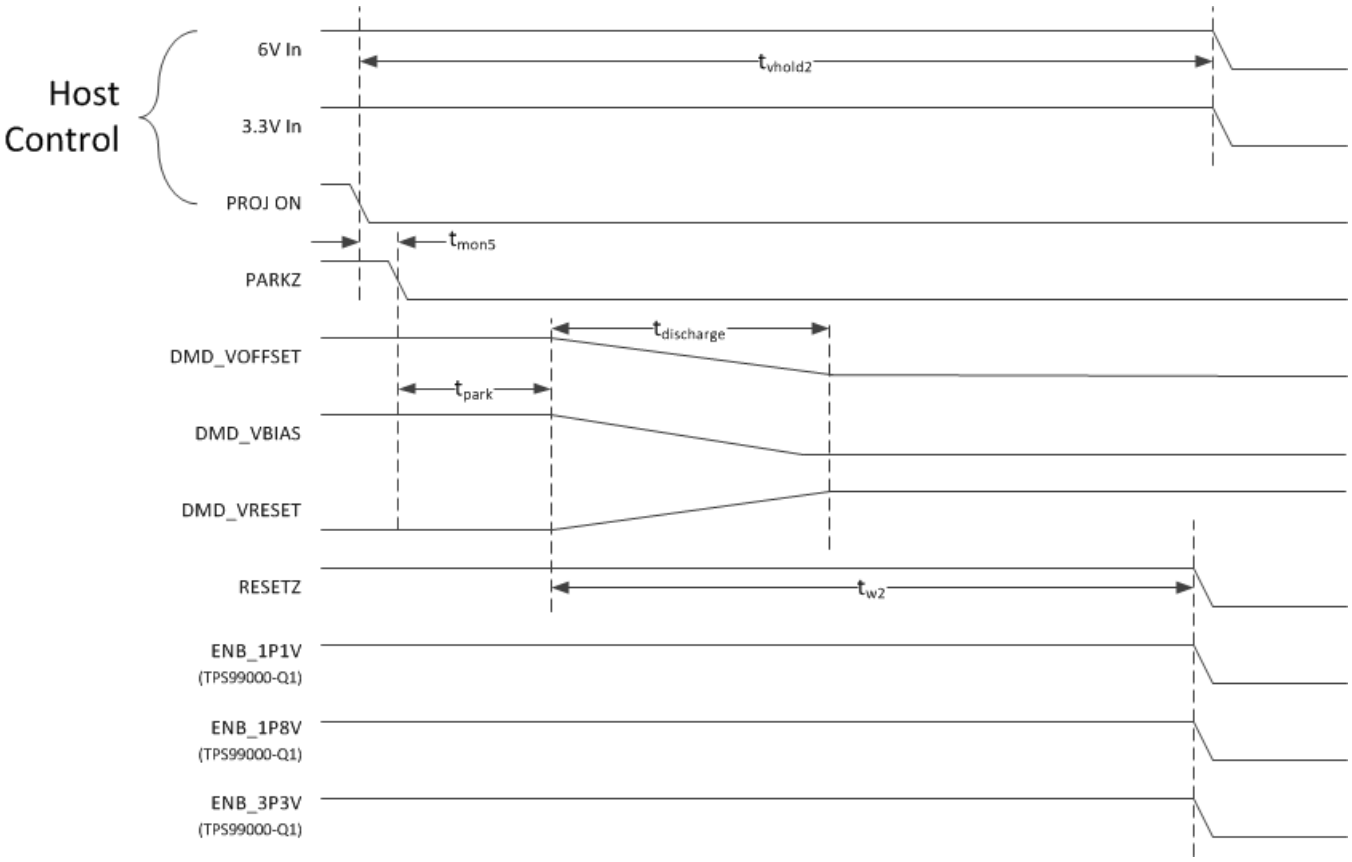

Figure 3. Power Down Timing - PROJ_ON Trigger

6.15 Timing Requirements - Sequencer Clock

		MIN	NOM	MAX	UNIT
f_{SEQ_CLK}	SEQ_CLK Frequency		30.00		MHz
t_{JPP}	SEQ_CLK Jitter (peak to peak)	–3%		3%	
f_{SS}	SEQ_CLK allowable spread spectrum	–2%		0%	
f_{SSMOD}	SEQ_CLK Spread Spectrum Modulation Frequency	25		100	kHz
$f_{SSSTEPS}$	SEQ_CLK Spread Spectrum Modulation Frequency Steps		50		steps

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6.16 Timing Requirements - Host / Diagnostic Port SPI Interface

		MIN	NOM	MAX	UNIT
$t_{SPICPER}$	SPI CLK Cycle Time	31	33		ns
$t_{SPICHIGH}$	SPI CLK High Time	10			ns
$t_{SPICLOW}$	SPI CLK Low Time	10			ns
$t_{SPIDOUT}$	CLK Falling to DOUT	0		15	ns
$t_{SSSETUP}$	SPI SS_Z to CLK Rising Setup Time	5			ns
t_{SSHOLD}	SPI CLK Rising to SS_Z Hold Time	5			ns
$t_{DINSETUP}$	SPI DIN to CLK Rising Setup Time	5			ns
$t_{DINHOLD}$	SPI CLK Rising to DIN Hold Time	5			ns

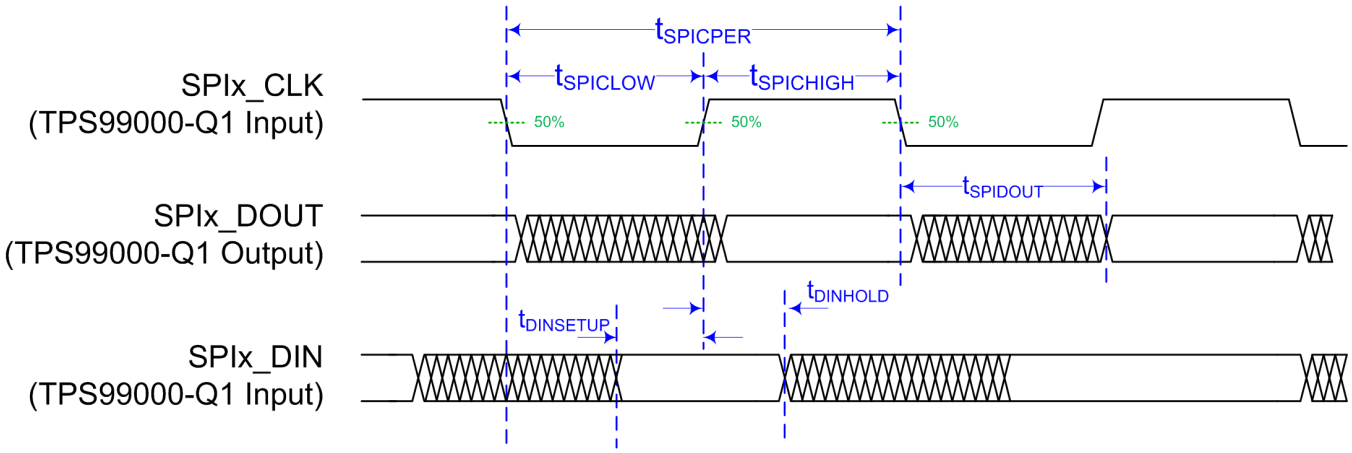

Figure 4. DLPC230-Q1 Diagnostic Interface Timing

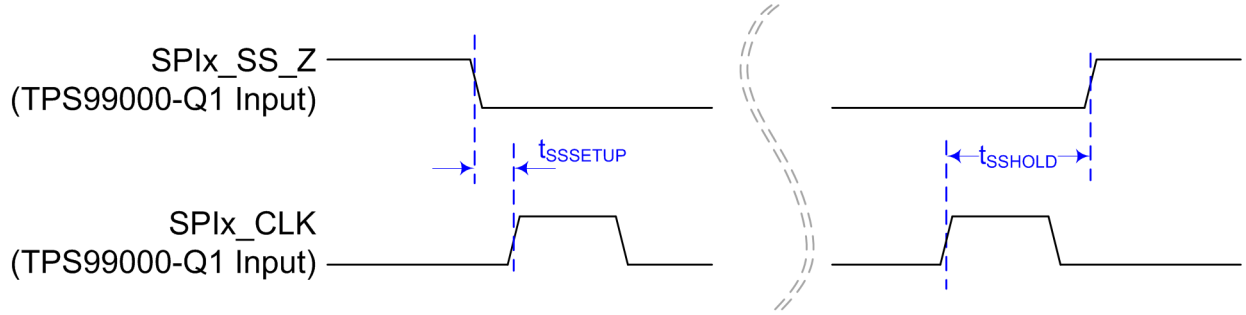

Figure 5. Chip Select Setup and Hold Timing

6.17 Timing Requirements - ADC Interface

		MIN	NOM	MAX	UNIT
$t_{ADCDINSETUP}$	ADC DIN to CLK Rising Setup Time	5			ns
$t_{ADCDINHOLD}$	ADC CLK Rising to DIN Hold Time	5			ns
$t_{ADCDOUT}$	CLK Rising to DOUT	0		15	ns

6.18 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL CLOCK						
f_{OSC}	Internal Oscillator Frequency		1.76	2	2.24	MHz

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7 Detailed Description

7.1 Overview

The TPS99000-Q1 is an integral component of the DLP553x-Q1 chipset, which also includes the DLPC230-Q1 DMD display controller. It provides features to support ultra-wide dimming requirements, which are unique to automotive. The TPS99000-Q1 also provides a high-voltage, high-precision, three-rail regulator to cost-effectively create DMD mirror control voltages (16 V, 8.5 V, –10 V). A complete system power monitor and DMD mirror parking solution is included to increase system robustness and reduce cost. In addition, the TPS99000-Q1 includes numerous system monitoring and diagnostic features, such as configurable ADCs, TIAs, and watchdogs.

An integrated 12-bit ADC supports the illumination system control, and provides useful information about the operating condition of the system. Several external ADC channels are included for general usage (LED temperature measurement, etc). One of the external ADC channels includes a differential input amplifier and is dedicated to LED current measurement. The DLPC230-Q1 and TPS99000-Q1 ADC control blocks support up to 63 samples per video frame, with precise hardware alignment of samples to the DMD sequence timeline. This information is available to the color control software in the DLPC230-Q1 where it can be used to counteract effects of temperature and LED aging to maintain brightness and white point targets.

Two SPI buses are included. The first bus is intended for command and control, and the second is a read-only bus for optional redundant system condition monitoring. The SPI ports include support for byte-level parity checking.

Two transimpedance amplifiers are included. The first TIA is dedicated to illumination control, and the second is available and reconfigurable for general usage, such as redundancy, ambient light detection, and output light validation. An over-brightness detector is included to provide a hardware redundant check of LED brightness.

Two windowed watchdog circuits are included to provide validation of DLPC230-Q1 microprocessor operation and monitoring of DMD sequencer activity. The TPS99000-Q1 also includes on-die temperature threshold monitoring and a monitor circuit to validate the external clock ratio (of the SEQ_CLK) against an internal oscillator.

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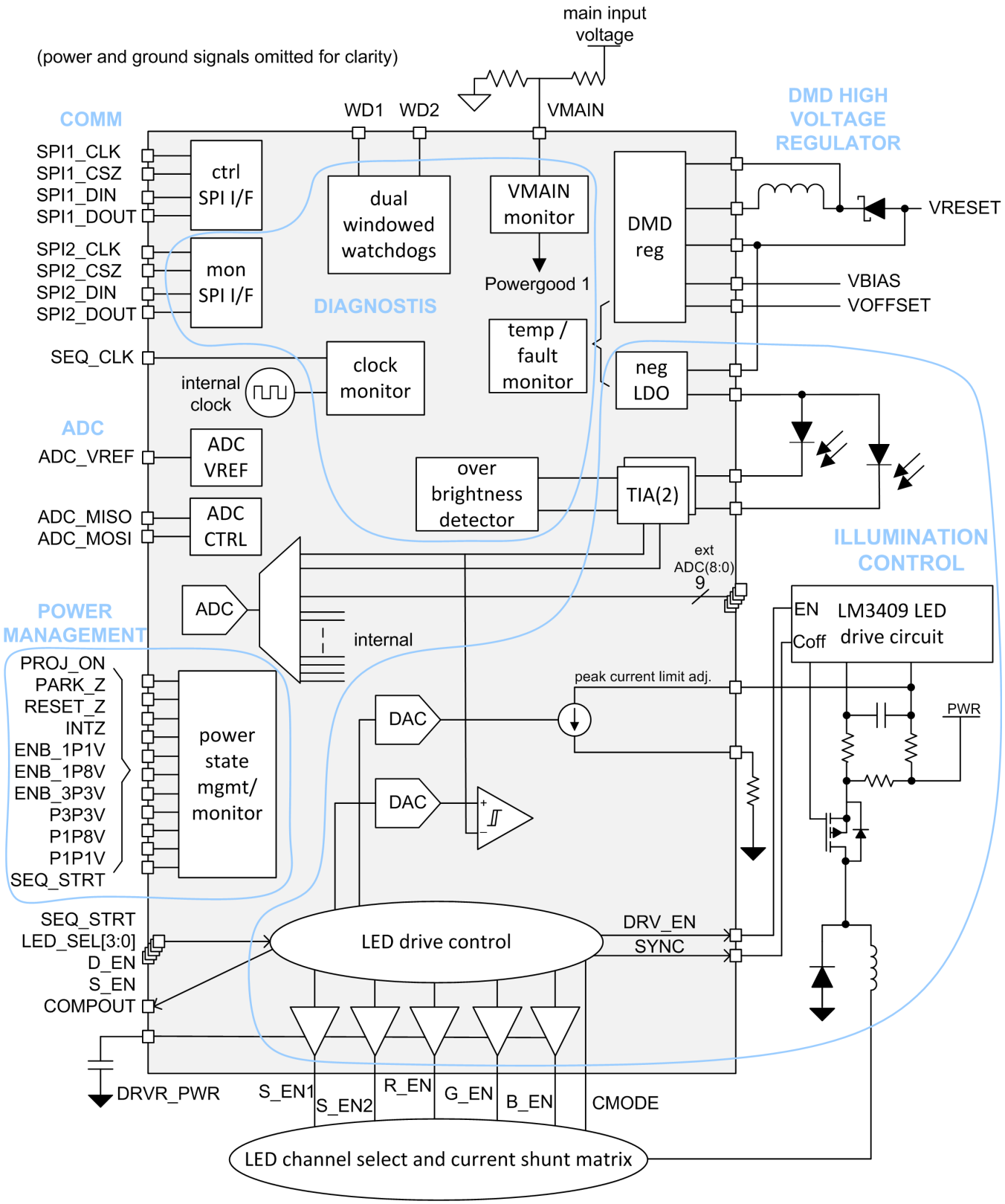
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Illumination Control

The illumination control function includes all blocks needed to generate light for the DLP subsystem. The system is designed to support automotive applications requiring precise control of color and brightness over a wide dimming range. The complete dimming solution consists of hardware features included in both the DLPC230-Q1 and TPS99000-Q1 along with DMD sequence data stored in the DLPC230-Q1. These elements work together to provide a usable system dimming range of over 5000:1, with up to 8 bits per color supported.

The illumination control function operates in two distinct modes to cover the full dimming range. These modes are referred to as continuous mode (CM) and discontinuous mode (DM).

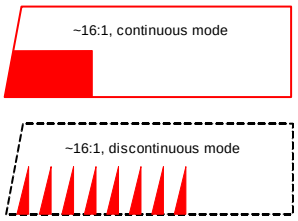


Figure 6. Comparison of Continuous and Discontinuous Mode Operation

Continuous mode features:

- High- to mid-brightness levels
- Rectangular light pulses created for each color
- Pulse amplitude and pulse width varied to adjust brightness level

Discontinuous mode features:

- Mid- to low-brightness levels
- A series of small triangular light pulses created for each color
- Number of pulses, pulse height, and LED current varied to adjust brightness level

The illumination control loop regulates current supplied to the LEDs through a real-time photo feedback control loop. A broadband photodiode is placed in the illumination path of the DLP subsystem in a location that receives light from all three red/green/blue LEDs. For continuous mode operation, photo feedback is used to create a real-time hysteretic control loop to set the brightness levels for each LED. In discontinuous mode, photo feedback is used to set a peak brightness threshold for each light pulse.

To support illumination control, the TPS99000-Q1 includes numerous high performance analog and mixed signal blocks. These blocks include:

- A high performance, ultra-wide dynamic range transimpedance amplifier (TIA) to convert photodiode current to a voltage, representing real-time LED brightness
- A high-speed comparator for photo feedback control
- A 12-bit DAC for photo feedback reference
- A 10-bit DAC for peak current limit adjustment
- Sync and drive enable outputs for synchronizing an external high-side PFET buck controller (LM3409)
- External FET drivers and control logic for selection of LEDs (FETs are external, but the drivers are internal)
- Two current *shunt* (by-pass) path FET controls, used to pre-regulate inductor current while light is disabled between colors, and to enable discontinuous mode operation
- A multi-purpose 12-bit ADC block with a dedicated two wire *Kelvin* input channel specifically for measuring LED current
- Hardware sample timer block that works in conjunction with DLPC230-Q1 to provide configurable hardware timed samples of LED current and voltage, temperature, etc.
- RGB specific multiplexed settings for most parameters, enabling independent control parameter optimization per color

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Feature Description (continued)

7.3.1.1 Illumination System High Dynamic Range Dimming Overview

This section provides a generalized overview, describing the concepts to provide a framework for understanding how the functions within the TPS99000-Q1 support the high dynamic dimming scheme of the full chipset and software.

A Head-Up Display (HUD) system must typically meet a target white point requirement over a wide range of brightness. Covering a wide brightness range requires a combination of continuous and discontinuous modes. Continuous mode will utilize different combinations of RGB sequence duty cycles, time attenuation, and amplitude attenuation. Discontinuous mode will utilize different combinations of the number of discrete pulses of light, photo feedback (TIA) gain, peak current limit settings, and light amplitude DAC settings. These adjustments can be categorized as coarse adjustments and fine adjustments.

Coarse adjustments include:

- **Illumination Bin** – Selects the DMD duty cycle, LED duty cycle, and the number of pulses (DM only).
- **LED Current Limits** – In CM, this specifies the maximum current each LED can operate with. Used to prevent damage to the LED. In DM, specifies pre-charge inductor current used to generate pulses. Determines shape/overshoot of pulse.
- **TIA Gain** – The TIA design supports a wide range of gain settings—14 in total—to cover a wide range of photodiode current levels. Higher gain settings result in lower LED output for a given feedback voltage.

Fine adjustments include:

- **Photo Feedback DAC Settings** – This function is implemented with a high speed 12-bit DAC. Sets the LED target amplitude.

7.3.1.2 Illumination Control Loop

Figure 7 shows the illumination control loop. This loop consists of the following features:

- An external buck controller (LM3409) and related discrete components which control the main LED drive PFET and controls and limits peak current using a high side sense circuit. This circuit creates a controlled current source that drives the LED high side connection (LED_ANODE).
- A 10-bit peak current limit (ILIM) adjustment DAC included in the TPS99000-Q1.
- Synchronization logic for external LED drive buck. SYNC pin to override the *controlled off time* pin of external device, and DRV_EN to control enable of external device.
- High speed comparator, used to compare photo feedback signal to programmable reference.
- 12-bit photo feedback comparison DAC. Sets reference for LED light pulse peak threshold in both continuous and discontinuous operating modes.
- A high speed, low noise, wide dynamic range transimpedance amplifier (TIA1) used for real time photo feedback. Includes support for 0.75 V to 288 V/mA gains, with 14 discrete gain steps and additional RGB specific trim of 1.0 to 0.2 gain. (Two TIAs included. TIA1 is dedicated to illumination control function).
- Negative LDO for cost effective reverse bias of photodiodes.
- 12-bit ADC, with differential input dedicated to low side current measurements.
- External FET gate drivers for RGB channel selection and two *shunt* path selections. Shunt paths provide a conduction path around the LEDs. These paths are used to control inductor current while LEDs are not emitting light. Control logic and firmware establishes appropriate current levels in inductor prior to enabling of LED during gaps between light pulses.

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Feature Description (continued)

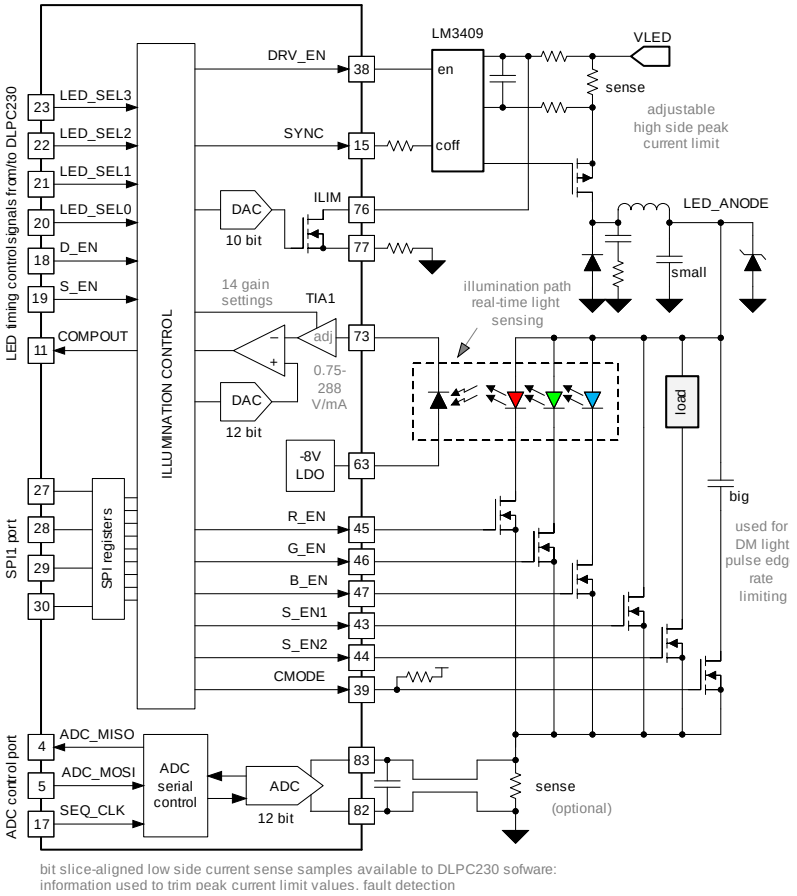

Figure 7. Illumination Control Loop

7.3.1.3 Continuous Mode Operation

When operating in continuous mode (continuous light output mode) a hysteretic control scheme is utilized. Real-time analog light amplitude measurements are used in the photo feedback loop to maintain a target light level. Figure 8 highlights the photo feedback control loop path in the driver for continuous mode.

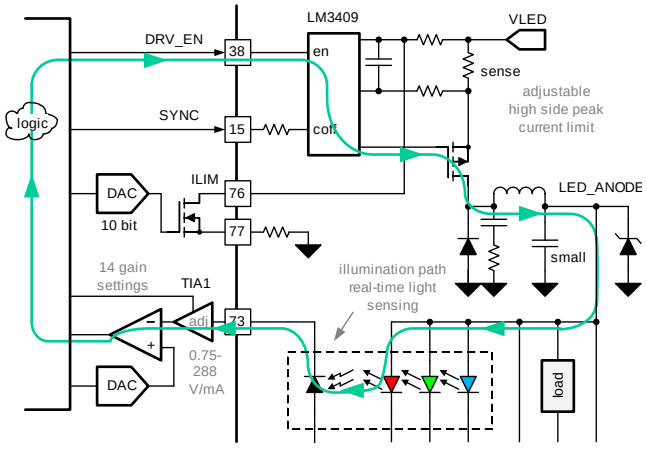

Figure 8. Continuous Mode Photo Feedback Path

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Feature Description (continued)

The on-chip analog comparator of the TPS99000-Q1 is used to compare desired target LED light amplitude to actual LED light output voltage from the photodiode TIA circuit. When the light output is below the threshold (set by the 12-bit photo feedback DAC output), the comparator will output a high level, causing DRV_EN to go high, which creates a connection from the power rail to the LED drive inductor to be made through the LED drive PFET. This connection will cause current flow to increase through the inductor. This current flows through an LED when its FET is enabled. When the light value goes above the threshold, DRV_EN goes low and the PFET is turned off, breaking the connection to the power rail with very little delay. Once the light level drops back below the threshold, DRV_EN goes high again and the PFET is turned back on, delivering more power to the LED. This process repeats as long as the LED circuit is enabled.

Hysteretic control results in ripple in the LED current. The amplitude and frequency of this ripple is a function of inductor inductance, input voltage, comparator hysteresis, and loop latency. An advantage of this hysteretic control approach is unconditional stability of the control loop.

Figure 9 shows the continuous mode signals and light output for a red, green, and blue bit slice. The signals, including LED_SEL(3:0), D_EN, S_EN1, and S_EN2, are sent from the DLPC230-Q1.

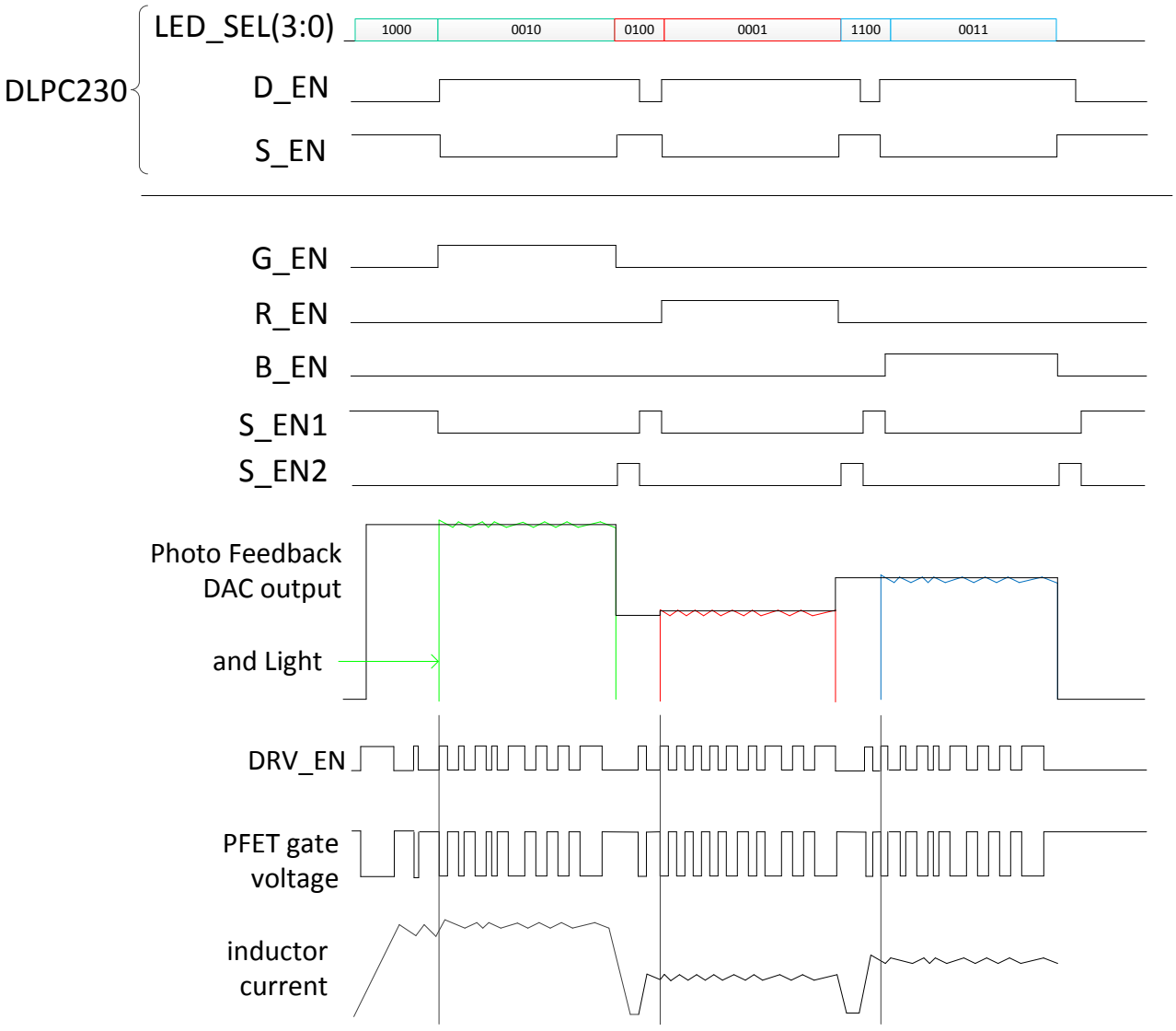

Figure 9. Continuous Mode Signal Example

Feature Description (continued)

In continuous mode, dimming is accomplished through a combination of amplitude/flux dimming and pulse time attenuation. Amplitude dimming is done by adjusting the photo feedback DAC output and TIA feedback gain. Time attenuation is accomplished by adjusting the length of shunt enable (S_EN from DLPC230-Q1) and drive enable (D_EN from DLPC230-Q1) (see Figure 10). Figure 10 shows an example with a 100% bit and a bit with time and amplitude attenuation to achieve 32:1 dimming. Figure 11 is a more generic example showing how many different dimming levels can be achieved with combinations of time and amplitude dimming.

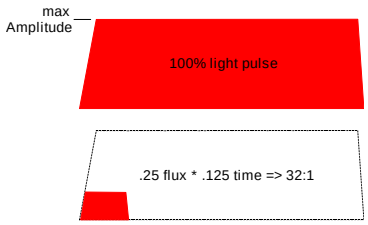

Figure 10. Continuous Mode Dimming Illustration 1

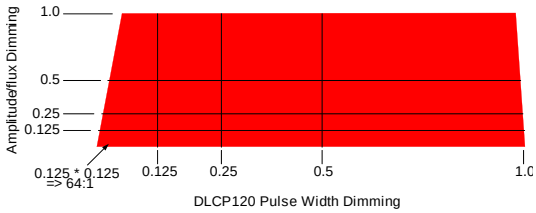

Figure 11. Continuous Mode Dimming Illustration 2

7.3.1.3.1 Output Capacitance in Continuous Mode

In continuous mode the CMODE signal from the TPS99000-Q1 is set low so the FET controlling the *big* (~1 µF) capacitor is turned off leaving only a small (~ 0.1 µF) high frequency decoupling capacitance in parallel with the LEDs and shunt FET paths (refer to Figure 7). Using a lower capacitance in continuous mode allows the voltage across the capacitor and LED to charge up faster so that the current in the inductor does not overshoot the desired current level before the LED light emission threshold is reached. This prevents the light pulse from overshooting at the beginning of bit slices. (Discontinuous pulse mode requires a larger, ~1 µF capacitance as will be discussed later in this document. CMODE pin is set high in discontinuous mode to enable higher capacitance in parallel with LEDs).

7.3.1.3.2 Continuous Mode Driver Distortion and Blanking Current

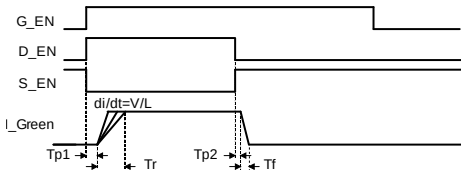

Figure 12. First Generation/Legacy System Pulse Distortion Example

As seen in Figure 12, the actual LED current pulse is distorted due to the rising (Tr) and falling (Tf) edges rates not being equal, and/or the turn-on (Tp1) and turn-off (Tp2) propagation delays not being equal. The rising edge turn-on time of the current pulse is primarily a function of the voltage across the inductor and the desired current, plus the inductor current initial condition. This distortion causes both the time attenuation and amplitude attenuation of the pulse to become non-linear functions of the control settings. This can lead to image artifacts.

Blanking time is the period of no light output in between two LED segments. The inductor current during this time is called blanking current. This current is controlled to provide an optimized Tr and Tf.

Blanking current control reduces image artifacts by preventing light overshoot and undershoot.

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Feature Description (continued)

The blanking current time periods are split into two parts. The first is a dissipation phase where the residual current in the inductor from the previous light pulse is reduced using a dissipative shunt. The second phase is a non-dissipative (low series resistance) shunt phase, where the inductor is charged up to the appropriate current for the next light pulse before current is applied to the LED. This process is illustrated in Figure 13.

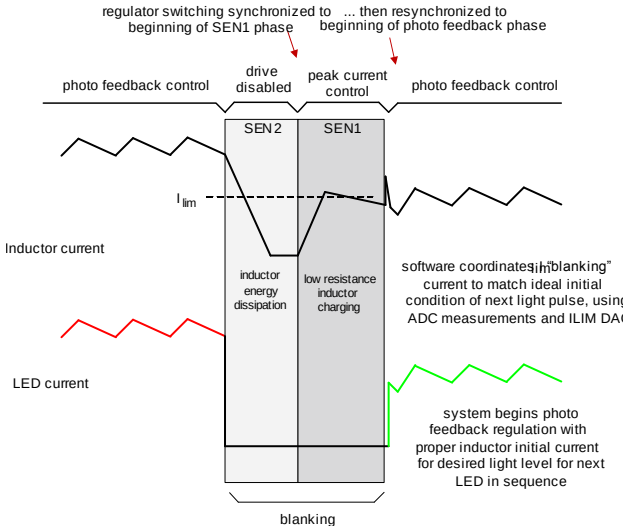

Figure 13. Blanking Current Discharge/Charge Cycles

During the first phase of the blanking time, shunt 2 (S_EN2) is enabled while the LEDs are disconnected. This places a load with a higher effective resistance in place of the LEDs. The residual energy in the inductor is dissipated into this load and the inductor current decreases rapidly. Without this feature, a high current in one pulse could cause excessive brightness in the next pulse.

During the second phase of the blanking time, the LED driver charges the inductor through a short circuit shunt (S_EN1). Charging continues until the peak current limit is reached. The peak current limit is set by the ILIM DAC. The peak current limit setting is coordinated by DLPC230-Q1 software to match the expected operating current during photo feedback operation. (The expected current level is determined from ADC measurements of LED current during prior frames.) When the blanking current time period is over, the S_EN1 short circuit shunt is turned off, the next LED is enabled, the DRV_EN signal is toggled, and the system reverts to photo feedback, hysteretic operation. Because the inductor is pre-charged to the ideal current and the system capacitance is low, light output rising edge is extremely fast, and the transition to stable hysteretic control is nearly immediate. This results in a more rectangular pulse. An illustration of the current paths is shown in Figure 14.

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Feature Description (continued)

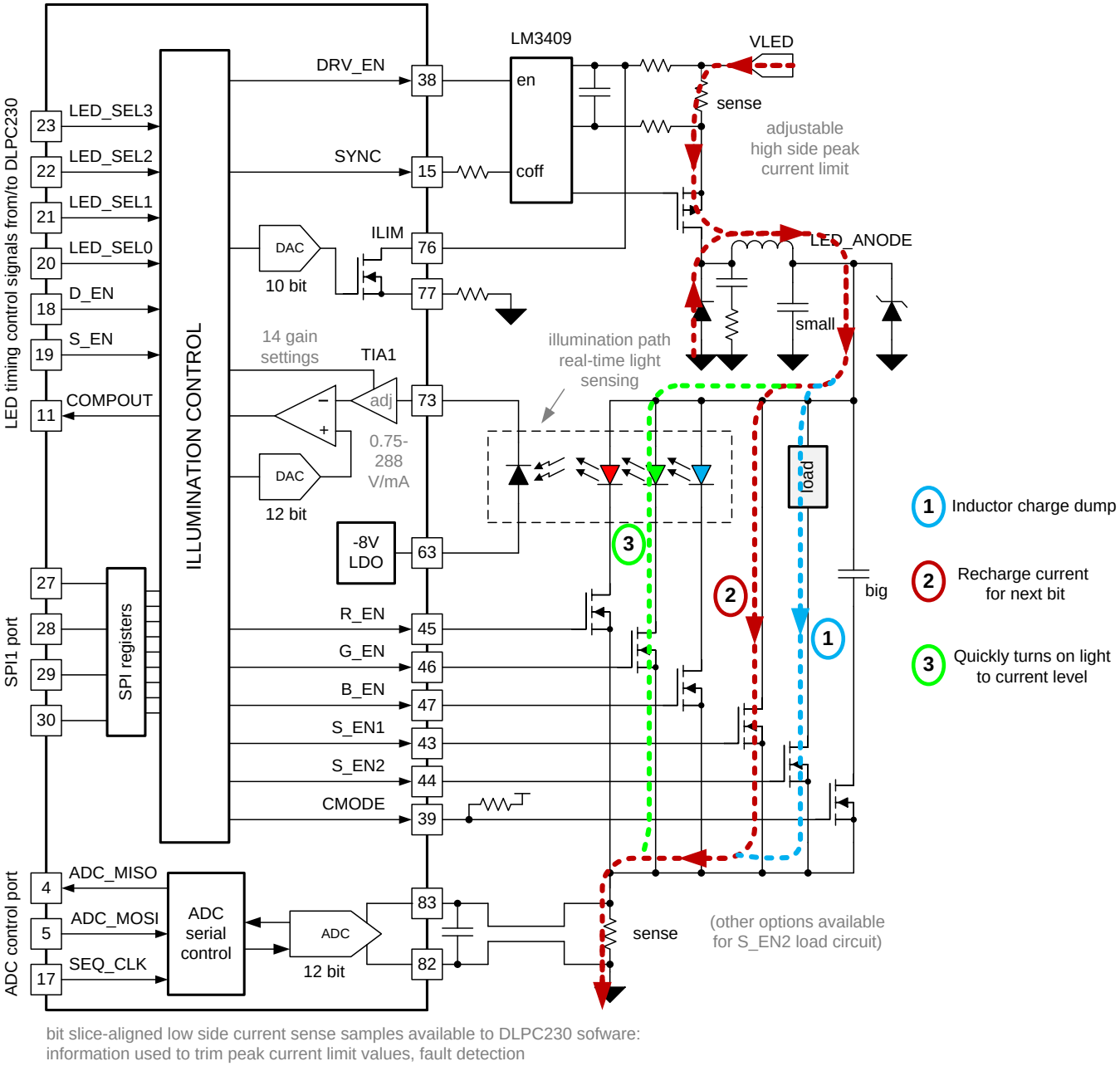

Figure 14. Blanking Current Paths

Precise control of the LED pulse shape results in greater dimming range, more display bit depth, and better color and gray ramp accuracy.

7.3.1.3.3 Continuous Mode S_EN2 Dissipative Load Shunt Options

The dissipative shunt, enabled by S_EN2 high, can be implemented with a variety of circuit types.

The circuit type selected for the shunt must be able to discharge the inductor used in the LED drive circuit, as well as protect against over voltage conditions on the LED anode voltage.

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Feature Description (continued)

The recommended option is to combine the open circuit protection Zener diode with the S_EN2 dissipative shunt functionality, as shown in Figure 15. This particular option does not connect the S_EN2 pin but still implements the same functionality as the alternate circuits in Figure 14 and Figure 16 which do connect the S_EN2 pin.

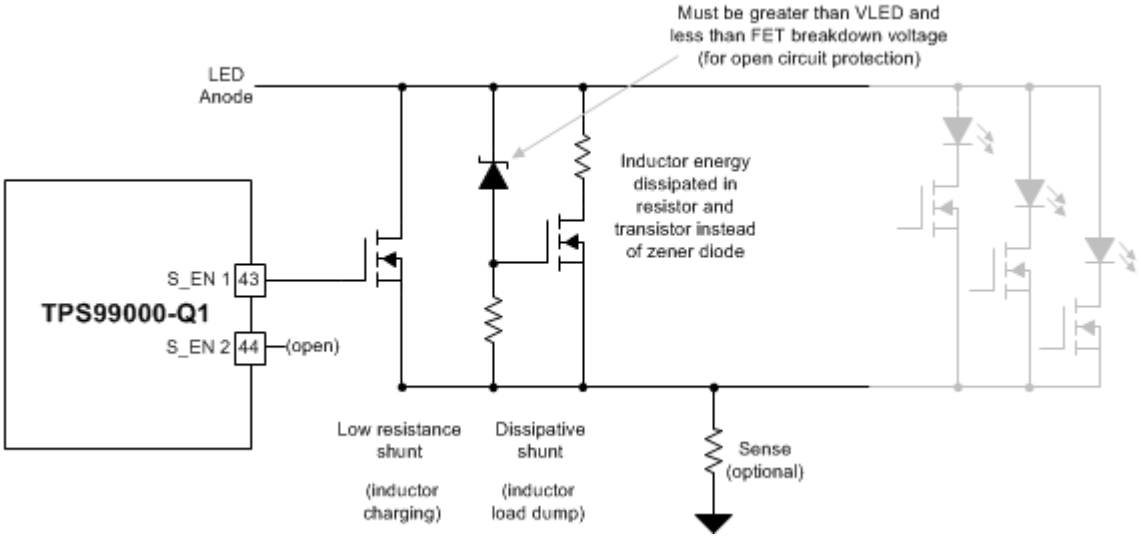

Figure 15. Dissipative Shunt / LED Open Circuit Protection Combination 1

In this case, a low power Zener diode is used to turn on a FET when the LED anode voltage exceeds the Zener voltage. The S_EN2 enable is not used in this configuration. Rather, the circuit intentionally is placed in an open circuit condition during the S_EN2 blanking time period. Then the protection circuit turns on and drains energy from the inductor (until the S_EN1 shunt is enabled and the LED anode voltage is reduced). The energy in this case is dissipated in a combination of the load resistor and FET. Care must be taken in selection of the Zener diode and resistor divider to ensure the LED anode voltage does not exceed the RGB select FET breakdown voltage. (An option is to delete the load resistor entirely. Then the dissipation will occur only in the FET, and the LED anode voltage will stay closer to the Zener voltage under all conditions). The Zener voltage must be higher than the worst case voltage of input VLED power rail to avoid unintentional triggering of circuit. And Zener voltage must be below the Vds breakdown voltage of the LED selection FETs.

Alternative circuits with the same functionality can be seen below.

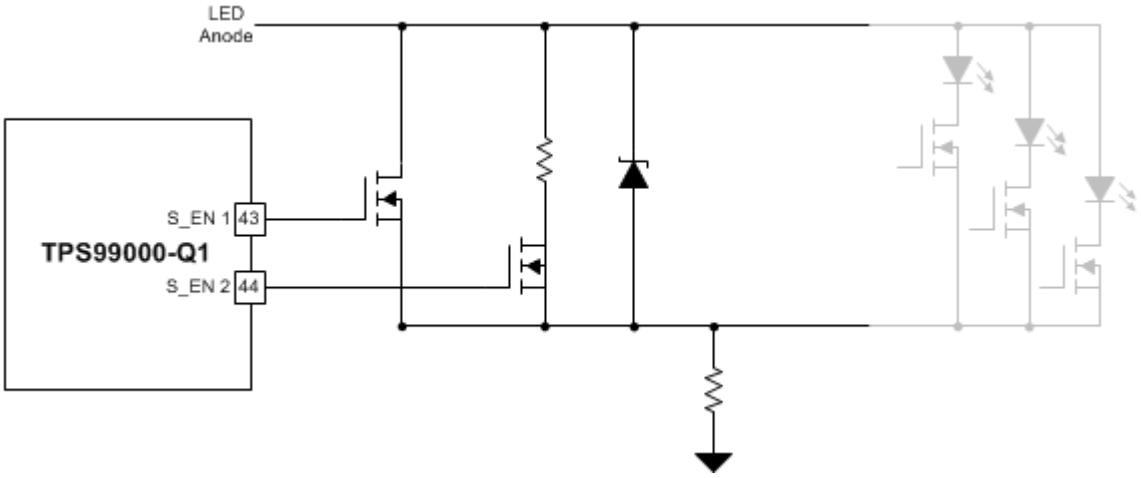

Figure 16. Dissipative Shunt / LED Open Circuit Protection Combination 2

In this circuit, the inductor current is discharged through the resistive path controlled by S_EN2.

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Feature Description (continued)

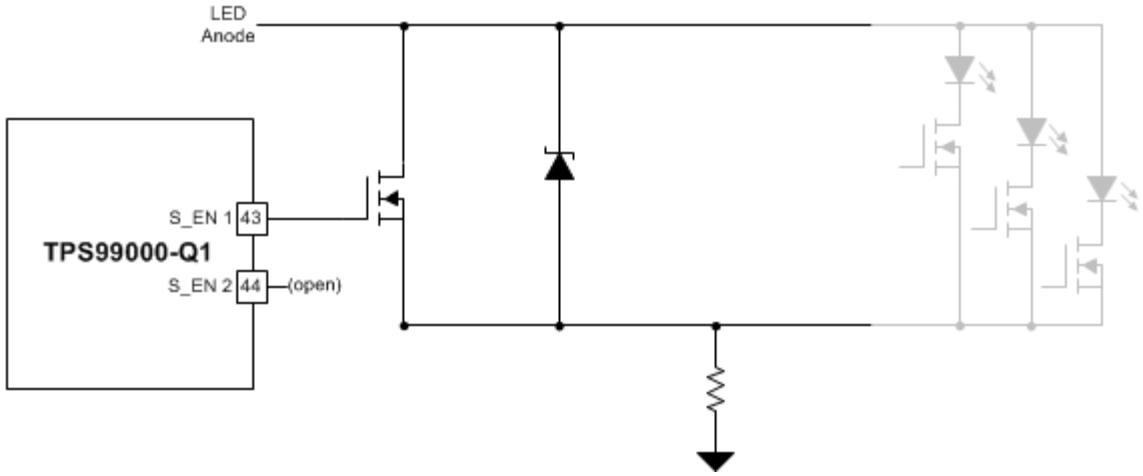

Figure 17. Dissipative Shunt / LED Open Circuit Protection Combination 3

In this circuit, the inductor current is discharged through the power Zener diode.

7.3.1.3.4 Continuous Mode Constant OFF Time

A constant off time feature (see COMPOUT_LOW signal in Figure 18) is included in continuous mode operation. During continuous mode operation, when the desired light level is achieved, the PFET gate drive is turned off by control of the DRV_EN signal and the light level begins to decrease as the inductor current begins to decrease. In a typical hysteretic controller, when a turn on threshold is reached, the PFET is turned on and the light/inductor current increases again. The frequency of switching is dependent on the difference between the turn on and turn off thresholds, loop delay and discrete component values (with the inductor inductance and voltage being most dominant factors).

In the TPS99000-Q1, the control is modified to regulate the operating frequency. A *constant off* timer is included in the TPS99000-Q1 control loop. When the photo feedback comparator threshold is achieved, a counter is started. The length of the counter is adjustable. While this counter is active, the output of the photo feedback comparator is ignored and the PFET drive (via DRV_EN output from TPS99000-Q1) is disabled. Once the constant off time period counter has expired, the output of the photo feedback comparator is once again used to control the LED current drive. The minimum off-time establishes an upper limit on the hysteretic control loop switching frequency, separate from the natural frequency of the circuit. This feature is useful for guaranteeing the circuit will not operate in the AM radio frequency band, and can also enable the usage of lower inductance value inductors (which can result in system cost savings and power efficiency improvements).

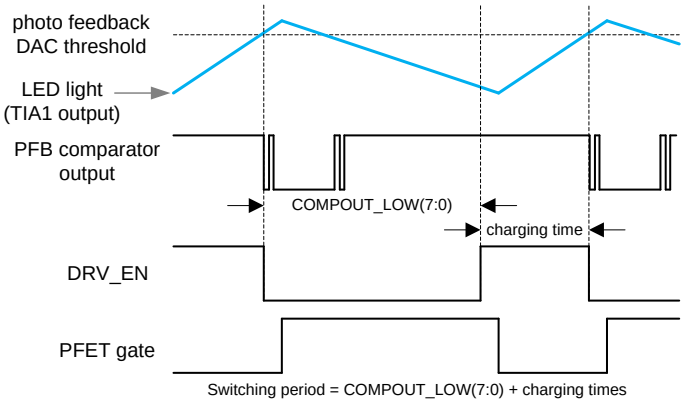

Figure 18. COMPOUT_LOW Constant Off Time

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Feature Description (continued)

7.3.1.3.5 Continuous Mode Current Limit

In continuous mode, a current limit feature prevents damage to LEDs if the requested light output cannot be achieved within LED current specifications. This could happen due to high temperature, or when an LED ages and requires more current to achieve the same brightness. Systems should be designed with sufficient thermal and LED life time margin that this would not happen in practice.

The control scheme utilizes the built in current limit feature of the LM3409 device plus a 10-bit DAC based adjustment feature included in the TPS99000-Q1. This serves as an alternate limit for the current for the LEDs – inductor drive will be disabled if either the current limit is met or if the photo feedback limit is met, whichever is lower. This peak current limit is configurable on a per LED basis, and is in use during the light-on active periods only. (During blanking periods, this same structure is used to control the blanking current, but different values are loaded onto the ILIM DAC).

The schematic for the current adjustment mechanism is shown in Figure 19.

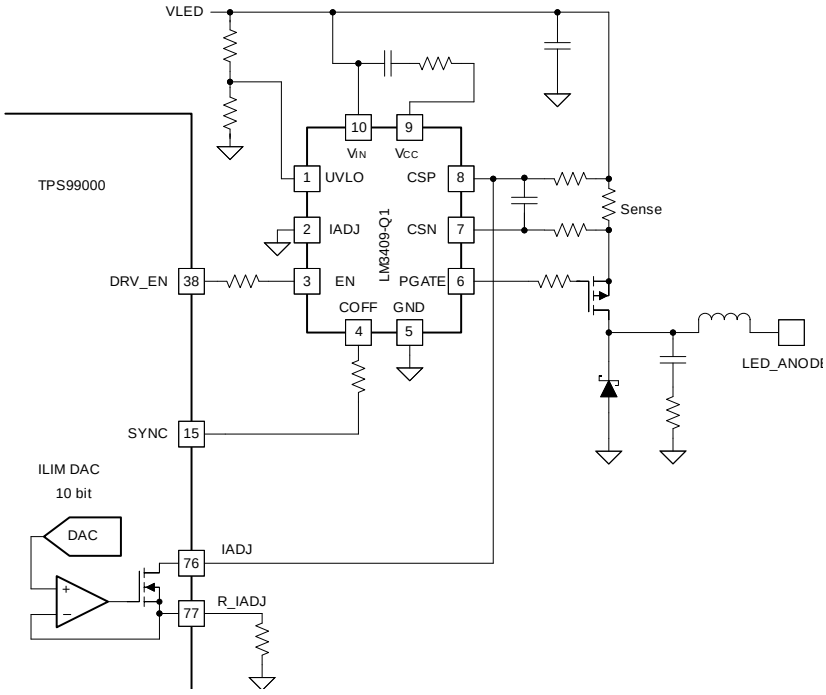

Figure 19. IADJ Peak Current Limit Schematic

By design, the LM3409 seeks to create a zero voltage difference between the CSP and CSN pins when IADJ pin is held low and system is operating in peak current limit mode. If the CSP pin voltage is higher than the CSN pin voltage, the PGATE driver is held high (PFET off).

When the ILIM DAC is set to a non-zero voltage, a current is established on the IADJ line of the TPS99000-Q1 device, which pulls the voltage of the CSP pin downward. If the LM3409 device is enabled and PFET drive not held off by state of the COFF pin, then the current will go up until the voltage across the sense resistor is such that the CSN pin is equal to or greater than the voltage on the CSP pin, at which point the PFET is turned off.

Care must be taken with the routing of the IADJ pin of the TPS99000-Q1 to insure that it is well isolated from noisy switching nodes, such as the PFET drain node.

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Feature Description (continued)

7.3.1.4 Discontinuous Mode Operation

Discontinuous mode is used to achieve lower dimming levels. It replaces the constant block of light during a bit slice with a series of light pulses of controlled amplitude, as illustrated in Figure 20. The number of pulses is controlled by the DLPC230-Q1 software.

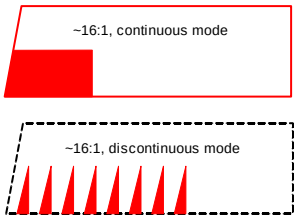

Figure 20. Comparison of Continuous and Discontinuous Operation at Equivalent Brightness

Figure 20 is an example diagram showing the Discontinuous Mode signals generating 8 pulses which are equivalent in brightness.

In discontinuous mode, the controller produces discrete pulses of light with fixed *off times* between pulses. The amount of light that these pulses produce can be precisely controlled to reach low dimming levels. Two control loops are used to create uniform light pulses:

- Peak current limit loop to create a desired current level in the inductor before it flows through the LED.
- Photo feedback loop to terminate each pulse when the desired light pulse level is achieved.

The initial inductor current and peak light threshold are independently adjustable for each color. See Figure 21 and Figure 22.

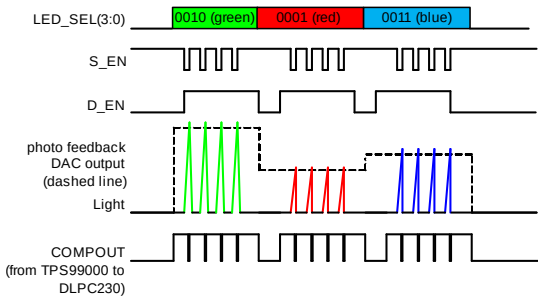

Figure 21. Discontinuous Operation DLPC230-Q1 to TPS99000-Q1 Signals

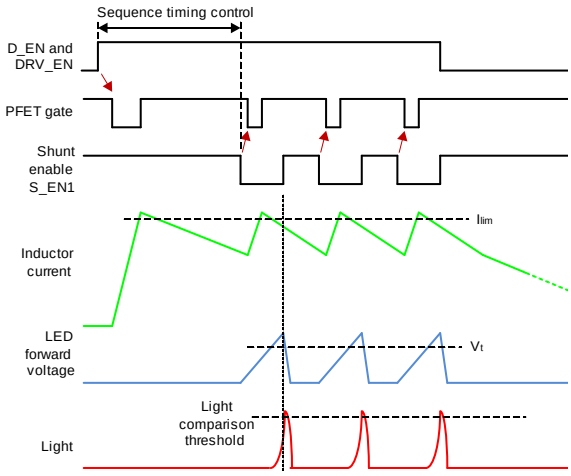

Figure 22. Discontinuous Mode Operation Inductor Current/LED Voltage

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Feature Description (continued)

Discontinuous mode consists of a series of triangular pulses of light. The DLPC230-Q1 is in charge of requesting and counting the total number of pulses. A bit slice begins with the low resistance shunt enable (S_EN1) on, and with an RGB color selected. Then DLPC230-Q1 asserts D_EN. This causes the TPS99000-Q1 to turn on the LED current drive (DRV_EN) and the system charges the inductor into the low resistance shunt until the peak current limit (as programmed with ILIM DAC) is reached. Then after a programmable amount of time the DLPC230-Q1 drives S_EN low, forcing inductor current to flow through the selected LED.

The TPS99000-Q1 detects the falling edge of S_EN from the DLPC230-Q1 and issues an on/off/on toggle of the DRV_EN signal. This allows current to flow through the inductor and increases the voltage at the LED anode. When the LED forward voltage is achieved, it begins to emit light. Once the photo feedback loop (TIA, photo feedback comparator, photo feedback DAC) senses the desired light threshold has been crossed, the S_EN1 signal is re-asserted high, and the light pulse is terminated.

The COMPOUT signal going low indicates to the DLPC230-Q1 that the pulse has been completed. The DLPC230-Q1 immediately sets S_EN output high (which sets TPS99000-Q1 output S_EN1 high), then waits for a programmable length of time. After that period of time, the DLPC230-Q1 will decide either to drive D_EN low and wait for the next bit slice or issue a request for a new pulse by placing the S_EN output low. When S_EN output is placed low, the TPS99000-Q1 places S_EN1 low (forcing current through LED) and toggles DRV_EN to request a new peak limit current pulse cycle. This process repeats until the correct number of pulses for the given bit slice have been completed.

In very low brightness operation, the TPS99000-Q1 SYNC (LM3409 COFF) timer is disabled. As a result, DRV_EN is only toggled at the beginning of each light pulse. This synchronizes the inductor and LED current. This synchronization keeps LED pulse heights very consistent from one video frame to the next, preventing flicker.

7.3.1.4.1 Discontinuous Mode Pulse Width Limit

The TPS99000-Q1 has a feature which limits the time duration of each discontinuous mode pulse. A count monitors the length of time current is applied to the LED during a pulse event and compares time to a programmable time limit. If the time limit expires before the light output threshold is reached, the discontinuous pulse is terminated. The pulses in both cases (photo level or time limit expiration) are terminated by enabling the S_EN1 low resistance shunt. This limits maximum brightness in the event photo feedback threshold is not reached. Independent RGB values for the discontinuous pulse width limit are supported. This process is illustrated in Figure 23.

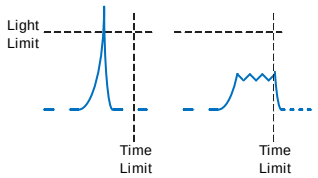

Figure 23. Discontinuous Mode Pulse Width Time Limit

7.3.1.4.2 COMPOUT_LOW Timer in Discontinuous Operation

In discontinuous operation, the same COMPOUT_LOW parameter that sets the switching frequency for the continuous mode case serves as a noise filter for discontinuous operation. The circuit triggers on the first falling edge of the photo threshold comparator, which equates to the end of a pulse. Then all subsequent rising and falling edges of the comparator output are ignored for a pre-defined amount of time, providing a glitch suppression filter function for discontinuous operation, and controlling the timing between pulses.

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Feature Description (continued)

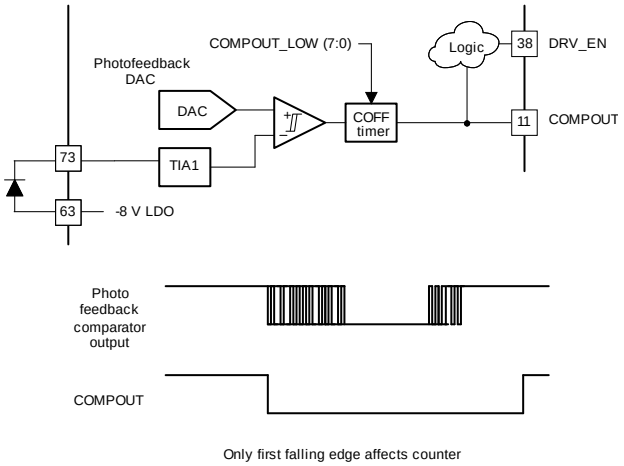

Figure 24. COMPOUT_LOW Timer as Glitch Filter in Discontinuous Operation

7.3.1.4.3 Dimming Within Discontinuous Operation Range

When operating in discontinuous mode, two methods of dimming are used concurrently to reduce brightness of the display:

1. Amplitude dimming using the photo feedback DAC settings.
2. Controlling the number of pulses per bit slice (via commands to DLPC230-Q1, selecting specific lookup table data).

Figure 25 is an example of the brightest LUT data table having 8 pulses per LSB (smallest bit slice). The LED pulse height is modulated to achieve a 2:1 dimming ratio while still maintaining 8 pulses per LSB. To allow for a seamless transition to lower dimming levels, a change to 4 pulses per LSB plus higher LED amplitude is made as illustrated in Figure 26. The total light generated in both cases in Figure 26 is approximately equal. A system calibration is used to determine this ½ LED amplitude photo feedback DAC setting.

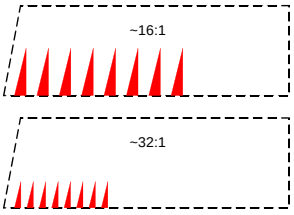

Figure 25. 2:1 Dimming Within a Sequence

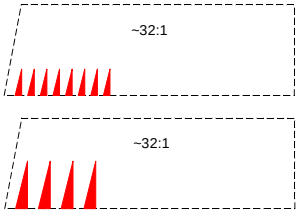

Figure 26. Discontinuous Operation Pulse Count Change

As a smooth dimming (brightness going down) sequence continues, the process above eventually results in using a 1 pulse per LSB. Amplitude dimming is used to dim to the absolute minimum display brightness level as illustrated in Figure 27.

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Feature Description (continued)

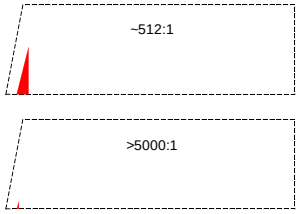

Figure 27. Discontinuous Dimming with One Pulse Per LSB Sequence

As shown in Figure 27, once a single pulse-per-LSB is selected, all remaining dimming must occur using only pulse height threshold reduction.

7.3.1.4.4 Multiple Pulse Heights to Increase Bit Depth

With the TPS99000-Q1, up to four sets of photo feedback threshold settings are supported within a given sequence. This is useful in discontinuous operation to create smaller sub-LSB bits (bits that are smaller than the normal LSB).

The LED_SEL(3:0) lines are encoded to include *group* information as well as color selection (and blanking current selection).

Each group can be defined to determine different behavior for specific color bits. For example, Group 0 can be used for LSB, and Group 1 can be used to create LSB-1.

Table 1. LED Selection Table

LED_SEL(3:0)	NAME	ACTION
"0000"	OFF	Driver Disabled Mode S_EN1 forced high RGB selects low
"0100"	R BLANKING	LED_SEL(1:0) - "00"=blanking LED_SEL(3:2): "01"=red "10"=green "11"=blue
"1000"	G BLANKING	
"1100"	B BLANKING	
"0001"	GRP0 RED	Driver Enabled Mode: LED_SEL(3:2) - Define Group: '00' - Group 0 '01' - Group 1 '10' - Group 2 '11' - Group 3 LED_SEL(1:0): "01" - red "10" - green "11" - blue
"0010"	GRP0 GREEN	
"0011"	GRP0 BLUE	
"0101"	GRP1 RED	
"0110"	GRP1 GREEN	
"0111"	GRP1 BLUE	
"1001"	GRP2 RED	
"1010"	GRP2 GREEN	
"1011"	GRP2 BLUE	
"1101"	GRP3 RED	
"1110"	GRP3 GREEN	
"1111"	GRP3 BLUE	

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The group1-3 RGB selections may be used to create fractional LSBs in the sequence, as illustrated in Figure 28.

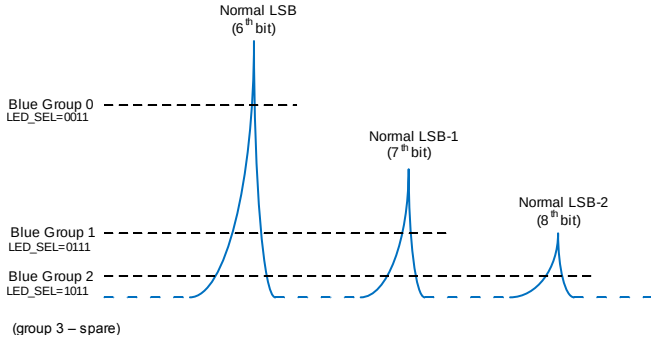

Figure 28. Extended LSB Bit Depth in Discontinuous Operation

This feature, combined with ability to make smaller absolute size light pulses, provides a method to extend the practical bit depth limit from the typical 6 bits per color, as is the case in legacy systems, to 7 or 8 bits with TPS99000-Q1/DLPC230-Q1 second generation systems.

7.3.1.4.5 TIA Gain Adjustment

The gain of TIA1 can be adjusted to achieve a larger dimming range. Increasing the TIA gain reduces the light output for a given photo feedback DAC level. A higher gain reduces the brightness range achievable but increases the resolution within the desired range.

7.3.1.4.6 Current Limit in Discontinuous Mode

The current limit determines the maximum current allowed through the inductor. A higher current limit enables higher pulse heights to be achieved. A lower current limit creates a slower rising edge on each pulse and reduces the overshoot of the pulse. Therefore, at lower dimming levels the current limit is reduced.

7.3.1.4.7 CMODE *Big Cap* Mode in Discontinuous Operation

The TPS99000-Q1 provides an output signal, CMODE, that can be used to drive the gate of a FET that switches in a larger capacitor for discontinuous operation. High capacitance mode is only used during discontinuous operation. (High capacitance causes issues in continuous operation, minimizing capacitance is preferred for that mode). The higher capacitance slows the rate at which the forward voltage of the LED increases during the pulse creation process. The slower charge rate causes the transition from no light emission to full light emission to extend in time. In selecting the proper capacitance, a balance between good edge rate control and total time for pulse to reach threshold must be made. Attention should be paid to the temperature characteristics of this capacitor. Less variation of capacitance over temperature will result in more accurate, repeatable results in cold/hot conditions.

Benefits:

- Pulse stability
- Support for lower light output thresholds, due to slower pulse edge rates

The charge and discharge loops using the CMODE *big cap* are as follows:

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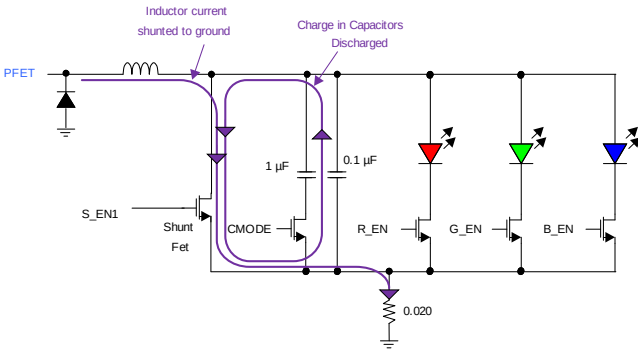

Figure 29. Discontinuous Mode Current Paths with Shunt Enabled

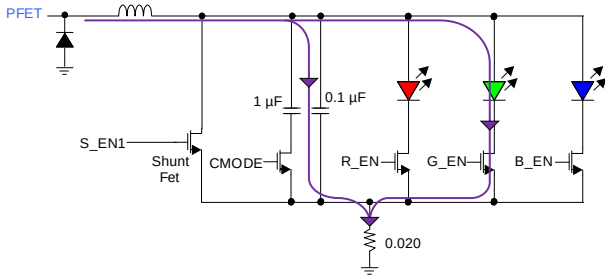

Figure 30. Discontinuous Mode Current Paths with Shunt Disabled

7.3.2 Over-Brightness Detection

The TPS99000-Q1 has two methods for detecting over-brightness conditions. The first method uses a combination of ADC measurements and photo feedback comparator output to detect breaks in the photo feedback loop. Another method uses a secondary photodiode to detect over-brightness in the HUD image.

7.3.2.1 Photo Feedback Monitor BIST

A disconnection of the primary photodiode breaks the feedback loop used to regulate LED output. Any disconnection of this photodiode should be detected so that the LEDs can be disabled.

The DLPC230-Q1 software and the TPS99000-Q1 implement a photo feedback monitor Built-In Self-Test (BIST) to detect a disconnected photodiode. Every video frame, the DLPC230-Q1 software uses ADC measurements of the LED current and TIA output, and COMPOUT falling edges to detect a disconnected photodiode.

In continuous mode, the DLPC230-Q1 software determines that the photodiode is disconnected if all the LED currents are at maximum, but the TIA measurements are at a minimum. This indicates that the LEDs are conducting current, but the photodiode is not responding to light output from the LEDs.

In discontinuous mode, COMPOUT edges are used to detect a photodiode disconnect. A falling edge on COMPOUT indicates that an LED pulse has reached the desired threshold. This is only possible if the photodiode is connected. Therefore, the COMPOUT edges are detected by the DLPC230-Q1 software to determine if the photodiode is connected.

7.3.2.2 Excessive Brightness BIST

The excessive brightness BIST uses a secondary photodiode connected to TIA2 to detect over-brightness conditions in the output image of the HUD.

The output of TIA2 is compared to a programmable threshold. If the output exceeds the threshold, the DLPC230-Q1 software will log an error. TIA2 can be used in a high bandwidth or low bandwidth configuration for this BIST.

The low bandwidth mode provides an RC filter low-passed value of the TIA2 output. The resistor element of the filter is embedded in the TPS99000-Q1, while the capacitor is an external component. If the low bandwidth input is used, the value of the capacitor should be expected such that the time constant is longer than the frame time.

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The hardware controls for the threshold are not synchronized to the dimming functionality of the TPS99000-Q1. Therefore, this feature may need to be enabled or disabled, or the thresholds may need to be adjusted based on the dimming level of the HUD.

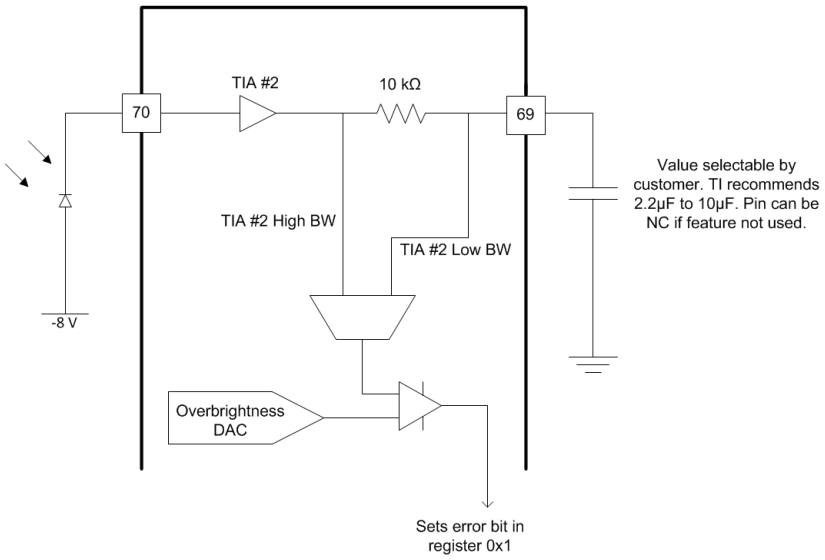

Figure 31. Excessive Brightness Detection Circuit

7.3.3 Analog to Digital Converter

The TPS99000-Q1 includes a 12-bit analog to digital converter block with a 32:1 input mux and dual sample-and-hold circuits. It also includes a custom high speed serial control interface which when used in tandem with the DLPC230-Q1 provides up to 63 DMD sequence-aligned samples per frame, with hardware-based sample timing and shadow-latched results. The hardware sample timing and shadow latch relieves the DLPC230-Q1 processor from ADC timing tasks, freeing up processor resources for other uses.

Figure 32 illustrates the structure of the ADC controller blocks in the two ASICs.

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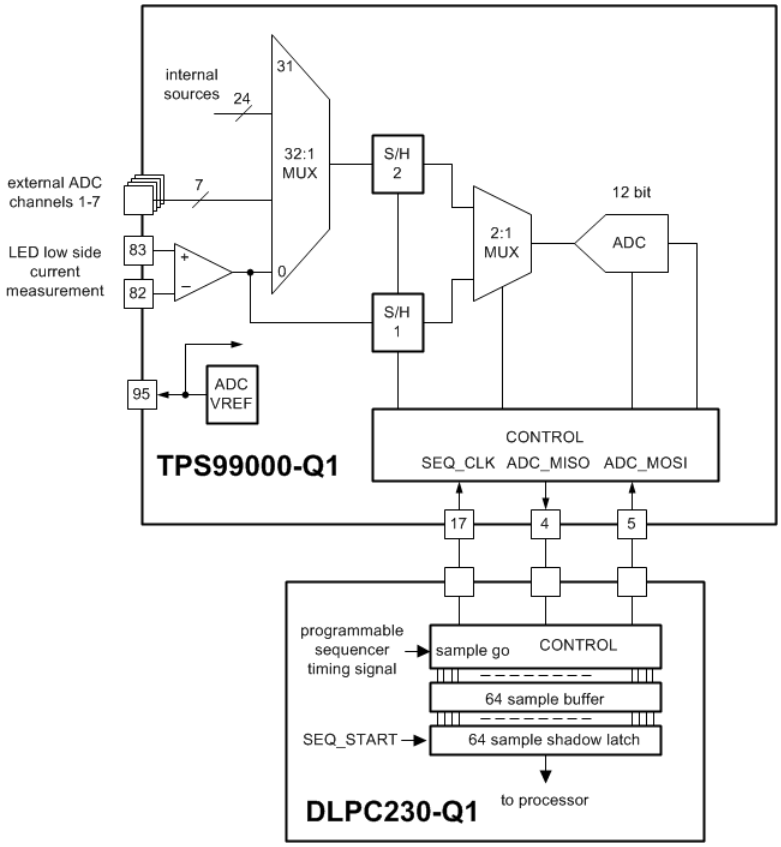

Figure 32. ADC Subsystem Block Diagram

The ADC block contains a dedicated channel reserved for differential low side LED current measurements. Two sample-and-hold circuits are included to support paired LED current/voltage measurements. (Note: when performing paired samples, they are sampled simultaneously, but converted sequentially, so the conversion time doubles). An additional seven external ADC channels are supported. The remaining 24 multiplexer inputs enable measurement of internal TPS99000-Q1 operating parameters.

The DLPC230-Q1 contains a custom ADC control block that supports up to 63 ADC samples per frame. The samples are aligned with DMD sequencer activity, configurable through system configuration tools. This alignment makes measurement of specific light pulses (LED current, voltage, and TIA output) within a sequence possible, with precise repeatability from frame to frame. Up to 63 samples per frame are supported. The 63 sample buffer includes a shadow latch that updates each frame. This latched output is held constant for a complete frame time, allowing time for the DLPC230-Q1 to collect and process the information.

A reference voltage output is also included in the ADC block. This provides a low current voltage reference which matches the reference used by the ADC for conversion. This external reference can be used to bias thermistor voltage dividers, providing greater accuracy than would be possible using a mix of external and internal references. (**Note**: Current supply is limited. Loads which exceed the specified current maximum rating on ADC_VREF output may result in unpredictable ADC behavior). Regardless of whether the reference voltage is used, a 0.1uF capacitor should be connected from this pin to ground.

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7.3.3.1 Analog to Digital Converter Input Table

Table 2. Analog to Digital Converter Input Table

PARAMETER		INTERNAL OR EXTERNAL	TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
Channel 0, Gain	Low side sense amp	External	Gain set to 24x	22.56	24	25.44	V/V
Channel 0, Gain	Low side sense amp	External	Gain set to 12x	11.28	12	12.72	V/V
Channel 0, Gain	Low side sense amp	External	Gain set to 9x	8.46	9	9.54	V/V
Channel 1, Gain	ADC_IN1_PAD (LED_ANODE)	External		0.980	1.000	1.020	V/V
Channel 2, Gain	ADC_IN2_PAD (VLED)	External		0.980	1.000	1.020	V/V
Channel 3, Gain	ADC_IN3_PAD	External		0.980	1.000	1.020	V/V
Channel 4, Gain	ADC_IN4_PAD	External		0.980	1.000	1.020	V/V
Channel 5, Gain	ADC_IN5_PAD (R_LED_THERM)	External		0.980	1.000	1.020	V/V
Channel 6, Gain	ADC_IN6_PAD (G_LED_THERM)	External		0.980	1.000	1.020	V/V
Channel 7, Gain	ADC_IN7_PAD (B_LED_THERM)	External		0.980	1.000	1.020	V/V
Channel 8, Gain	VBIAS	Internal		0.0596	0.0621	0.0646	V/V
Channel 9, Gain	VOFFSET	Internal		0.1112	0.117	0.1218	V/V
Channel 10, Gain	VRESET	Internal		–0.1978	–0.190	–0.1822	V/V
Channel 10, Offset	VRESET	Internal		–1.217	–1.1935	–1.169	V
Channel 11, Gain	VMAIN	Internal		0.52546	0.559	0.59254	V/V
Channel 12, Gain	DVDD	Internal		0.31302	0.333	0.35298	V/V
Channel 13, Gain	V1.1	Internal		0.65706	0.699	0.74094	V/V
Channel 14, Gain	V1.8	Internal		0.40326	0.429	0.45474	V/V
Channel 15, Gain	V3.3	Internal		0.2209	0.235	0.2491	V/V
Channel 16, Offset	M8 LDO offset	Internal		8.15	8.400	8.65	V
Channel 16, Gain	M8 LDO	Internal		0.980	1.000	1.020	V/V
Channel 17, Gain	ext ADC VREF	Internal		0.49	0.5	0.51	V/V
Channel 18, Gain	Driver Power	Internal		0.20398	0.217	0.23002	V/V
Channel 19, Gain	Die Temp1	Internal		0.490	0.500	0.510	V/V
Channel 20, Gain	Die Temp2	Internal		0.490	0.500	0.510	V/V
Channel 21, Gain	ILED Control DAC	Internal		0.490	0.500	0.510	V/V
Channel 22, Gain	Photo Feedback Control DAC	Internal		0.490	0.500	0.510	V/V
Channel 23, Gain	Over-Brightness Control DAC	Internal		0.490	0.500	0.510	V/V
Channel 24, Gain	TIA1 Real Time	Internal		0.490	0.500	0.510	V/V
Channel 25, Gain	TIA1 Low Bandwidth	Internal		0.490	0.500	0.510	V/V
Channel 26, Gain	TIA2 Real Time	Internal		0.490	0.500	0.510	V/V
Channel 27, Gain	TIA2 Low Bandwidth	Internal		0.490	0.500	0.510	V/V
Channel 28, Gain	Channel not used	Internal					
Channel 29, Gain	Main Bandgap, 0.5 V	Internal		0.980	1.000	1.020	V/V
Channel 30, Gain	TIA1 Monitor	Internal		0.980	1.000	1.020	V/V
Channel 31, Gain	TIA2 Monitor	Internal		0.980	1.000	1.020	V/V

(1) Conversion formula is (X + Offset) * Gain. X is the input voltage. Offset is 0 V unless specified above.

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7.3.4 Power Sequencing and Monitoring

The TPS99000-Q1 is specifically designed to perform correct power-up and power-down sequencing to ensure long term reliable operation of the DMD. The high voltage DMD mirror supplies require special power sequencing order, and restrictions on voltage differences between the power rails (VRESET, VBIAS, and VOFFSET) throughout power up, power down, and normal operation. The TPS99000-Q1 handles these requirements for the system designer.

7.3.4.1 Power Monitoring

Main asynchronous digital logic reset (DVDD_RSTZ) – Monitor of the main power of the 3.3 V power supply input to the TPS99000-Q1. This monitor output is used as an asynchronous reset for all of the digital logic inside TPS99000-Q1.

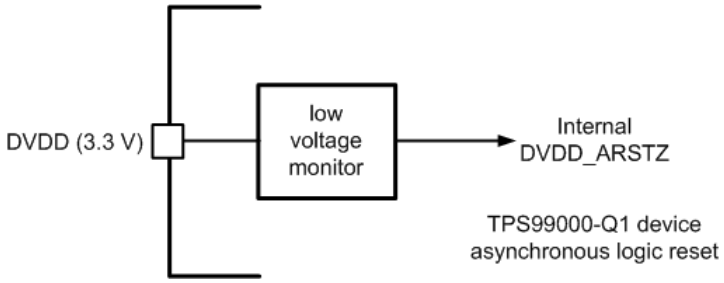

Figure 33. Internal DVDD Monitor

The PROJ_ON pin is the main on/off switch for DLP subsystem. *1* is ON, *0* is OFF. Once DVDD_ARSTZ is released, TPS99000-Q1 will begin sampling the PROJ_ON pin. If it is low, system stays in the OFF state. If it goes high, TPS99000-Q1 begins to progress through the power-on process.

The TPS99000-Q1 includes a VMAIN *brown out* monitor function. A voltage monitor observes the voltage on the VMAIN input pin, as shown in Figure 34. The Zener may be necessary for over voltage protection of the pin, in case the voltage being monitored has the potential to go high, such as a battery input.

Either PROJ_ON or VMAIN may be used to turn the system on and off, and doing so will remove power to the DLPC230-Q1. For fast control of turning the display on and off without removing power to the DLPC230-Q1, change the operating mode of the DLPC230-Q1 embedded software between 'Standby' and 'Display'.

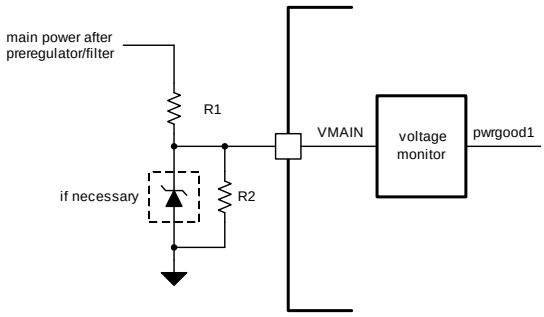

Figure 34. VMAIN *Brown Out* Monitor

This monitor is used to provide the DLP subsystem with an early warning that power to the unit is going away. The system will park the DMD mirrors and proceed to a ready for power-off state if the VMAIN input voltage falls below a fixed threshold. External resistors should be used to divide the input power rail. Once a VMAIN brown out occurs, the main power rails to the TPS99000-Q1 must remain within their operating ranges until the TPS99000-Q1 power-down is complete.

The main power rails to the chipset (6 V, 3.3 V, 1.8 V and 1.1 V) are monitored with real time power monitors as well. Each of these monitors is logically 'OR'ed together to produce the *pwrgood2* signal in Figure 35.

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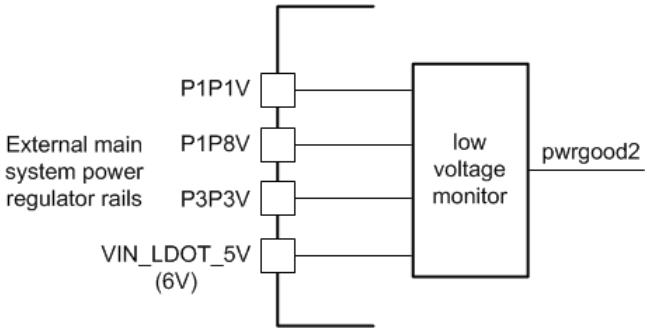

Figure 35. Real-Time Power Rail Monitors

Additionally, all power within the TPS99000-Q1 can be monitored by the ADC function. DLPC230-Q1 software configures the ADC block to collect all voltage information in the system each frame. Any gross out of specification issues are captured and reported as system errors in the DLPC230-Q1 system status.

7.3.5 DMD Mirror Voltage Regulator

The DMD mirror voltage regulator generates three high voltage supply rails: DMD_VRESET, DMD_VBIAS and DMD_VOFFSET. The DMD regulator uses a switching regulator where the inductor is time shared between all three supplies. The inductor is charged up to a certain current level and then discharged into one of the three supplies. In cases where a supply does not need additional charge, the time slot normally allocated to that supply is skipped and the supplies requiring more charge receive all of the charging time.

For proper operation, specific bulk capacitance values are required for each supply rail. Refer to *Electrical Characteristics - Temperature and Voltage Monitors* for recommended values for the capacitors. The regulator contains active power down/discharge circuits. To meet timing requirements, total capacitance (actual capacitance, not the nominal) must not exceed these levels by substantial amounts, as defined in *Electrical Characteristics - Temperature and Voltage Monitors*. Power down timing should be verified in each specific system design. Too low of a total capacitance will result in excessive ripple on the supply rails which may impact DMD mirror dynamic behavior. Care should be taken to use capacitors which maintain the recommended minimum capacitance over the expected operating device temperature range. Large size packages are required here that do not lose so much capacitance at high voltages.

Although the average current drawn by the DMD on these supplies is small (10’s of mA worst case), the peak currents can be several amps over 10’s of nano-seconds. To supply this peak current, use of small value, high frequency decoupling capacitors should be included as close as practical to the DMD power input pins.

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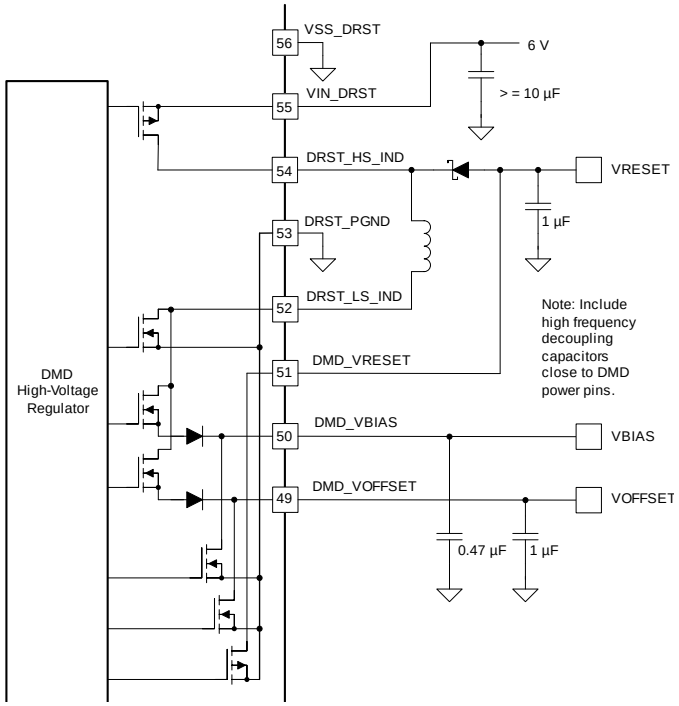

Figure 36. DMD Voltage Regulator Circuit

7.3.6 Low Dropout Regulators

The TPS99000-Q1 includes four low drop out regulators, dedicated to specific internal functions:

- A fixed –8 V negative regulator for photodiode reverse biasing (VIN_LDOT_M8 input, VLDOT_M8 output)
- A 5 V output regulator for internal analog circuits (VIN_LDOT_5V input, VLDOT_5V output)
- A 3.3 V output regulator for internal analog (VIN_LDOT_3P3V input, VLDOT_3P3V output)
- A 3.3 V output regulator dedicated to the ADC block (VIN_LDOA_3P3 input, VLDOA_3P3 output)

The positive output LDO regulators are all designed to operate from the same nominal 6 V input as is needed by the LED selection FET gate driver supply input, DRVR_PWR and the DMD mirror voltage regulator, VIN_DRST. However, care must be taken to isolate the sensitive analog circuit power supply inputs from switching noise, through dedicated sub-planes and supply filtering techniques. Noise on the analog supply rails will directly impact system dimming range performance, limiting stable operation at low brightness levels.

The negative 8 V LDO is designed to use the DMD_VRESET power rail as its power source. (Note that this usage implies that the TIA/photodiode path will not be available for use until the DMD is in a powered up state.)

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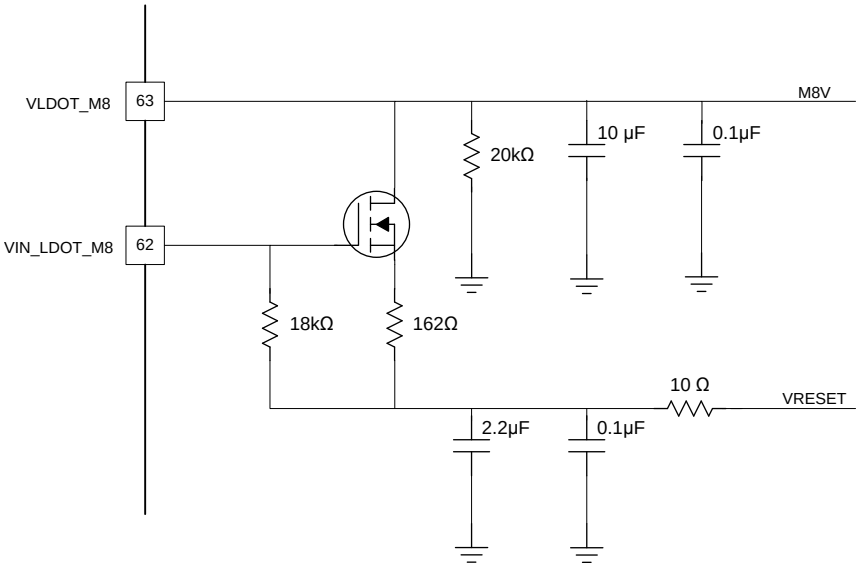

Figure 37. Negative 8 V LDO Circuit

CAUTION

Applications that do not use a photodiode do not require the -8 V regulator. VLDOT_M8 and VIN_LDOT_M8 may be left disconnected if the option in the DLPC230 SW to prevent enabling of the –8 V LDO is selected. If these pins are not connected, care must be taken to confirm that the -8 V LDO is not enabled. If this regulator is enabled while the pins are disconnected, permanent damage may be caused to the device.

7.3.7 System Monitoring Features

7.3.7.1 Windowed Watchdog Circuits

The TPS99000-Q1 contains two windowed watchdog circuits that can be used to detect malfunctions within the DLPC230-Q1.

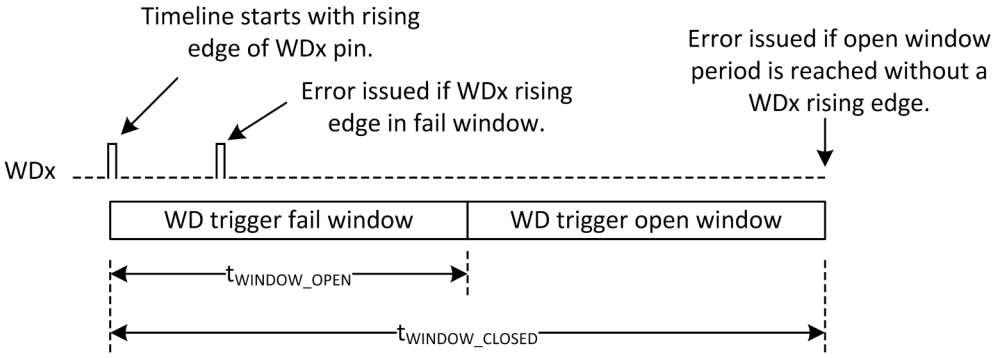

Figure 38. Windowed Watchdog Function

The DLPC230-Q1 software uses both watchdog circuits. Watchdog #1 (WD1) monitors the internal microprocessor of the DLPC230-Q1 through a wire connection to a dedicated GPIO line from DLPC230-Q1. Watchdog #2 (WD2) is used to monitor the DLPC230-Q1 sequencer operation (through monitoring of the SEQ_STRT pin, wired to WD2 input).

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When this function is enabled, two registers control the timing of the opening and closing of a watchdog trigger window. Process is initiated by a rising edge on the respective WDx pin. If another rising edge occurs before the WD trigger window opens, a watchdog error is issued. If the end of the open window period is reached without receiving a rising edge on WDx, an error is issued. The process restarts any time a WDx rising edge is received. The two watchdogs are independent.

7.3.7.2 Die Temperature Monitors

The TPS99000-Q1 contains two on-chip die temperature monitors, for reduncy purposes, to monitor the internal temperature of the TPS99000-Q1. Each monitor has an output that indicates whether the die temperature has exceeded one of two thresholds. One monitors a warning threshold, and the other monitors an over-tempreature error threshold. If the warning threshold is exceeded, a processor interrupt may be generated. If the over-temperature error threshold is exceeded during operation, the TPS99000-Q1 will initiate an emergency shutdown procedure and then wait for a toggle of the PROJ_ON pin to initiate a system restart while operating in a low power state. The system will not proceed through the power on initialization steps unless the on die temperature is below the warning threshold. The status of these temperature monitor output bits is available over the SPI buses as long as DVDD and VDD_IO power supplies are up and stable.

7.3.7.3 External Clock Ratio Monitor

The TPS99000-Q1 operates from two primary clock sources: an internal low frequency oscillator (2 MHz, used for system initialization and other maintenance purposes), and an external high speed (30 MHz) clock, SEQ_CLK, used for most timing critical applications, such as the logic inside the illumination control block and ADC. The TPS99000-Q1 includes a function that reports the ratio of this internal vs. external clock. This ratio is available over the SPI bus. The DLPC230-Q1 can check this ratio and compare to expected value. If the ratio is incorrect, there is a possibility the DLPC230-Q1 oscillator may have locked to an incorrect harmonic, or some other fault condition has occurred.

7.3.8 Communication Ports

7.3.8.1 Serial Peripheral Interface (SPI)

The TPS99000-Q1 provides two four-wire SPI ports that support transfers up to 30 MHz clock rates. The primary port (SPI1) supports register reads and writes, and serves as the primary set up and control interface for the device. The DLPC230-Q1 is the master of SPI1 to control the TPS99000-Q1 during system operation. A secondary read-only four wire SPI port (SPI2) is available to provide status information to an optional second microcontroller in the system.

For both ports, the SPIx_SS_Z serves as the active low chip select for the SPI port. A SPI frame is initiated by SPIx_SS_Z pin going low, and is completed when SPIx_SS_Z pin is driven high.

The secondary SPI port serves as a read-only system monitor port. All registers in the address space are read accessible over this port. The protocol is effectively the same as the main port except for being read-only. Note that data is clocked in on the rising edge of the SPI2_CLK.

When using this port, one must always transmit the full transaction packet. Failure to do so may result in corruption of data.

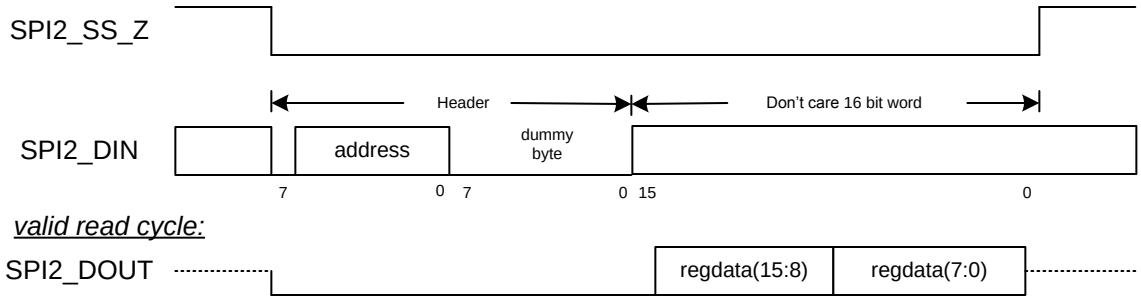
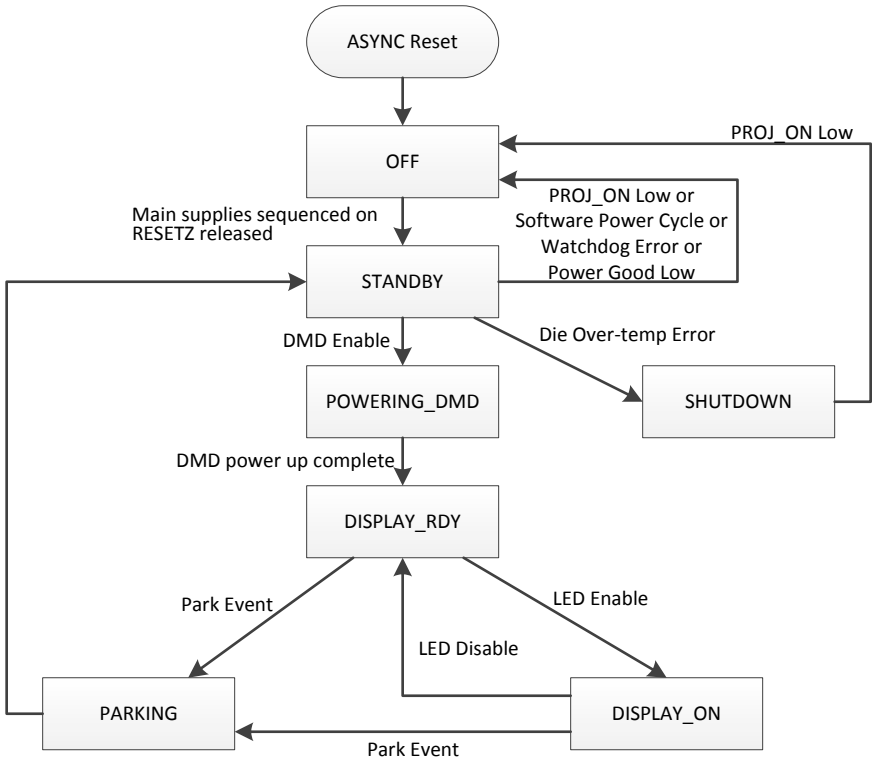


Figure 39. SPI Port 2 Protocol (Read Only)

7.4 Device Functional Modes

The following diagram in Figure 40 illustrates the functional operating modes of the TPS99000-Q1.



Park Events include:
Power good low
PROJ_ON Low
Die Over-Temp
Software Park
Watchdog Error

Figure 40. Top Level System States

7.4.1 OFF

The asynchronous internal reset of the device places system in this state. All supplies (DMD supplies, 1.1 V, 1.8 V, 3.3 V) are asynchronously disabled and RESETZ output to DLPC230-Q1 is held low. Once the internal reset is released, communication over SPI2 is supported.

Exit from OFF state progresses to the STANDBY state. To exit OFF state, the following must all be true:

- VMAIN input monitor must show good status.
- PROJ_ON (projector on) input pin must be high.
- The die temperature warning must indicate the die temperature is below the warning threshold. Upon exit of OFF state and before entry to STANDBY, the external 1.1 V, 1.8 V, and 3.3 V supplies are powered on in sequence – first 1.1 V, then 1.8 V, then 3.3 V.

Internal monitors of 1.1 V, 1.8 V, and 3.3 V (and 6 V input on VIN_LDOT_5V) will hold off progression to STANDBY until all 4 rails are in operational range. After power is good, RESETZ output signal is held low for a specific period to ensure a proper reset cycle for the DLPC230-Q1, and then it is released to transition to STANDBY.

7.4.2 STANDBY

Upon entry to STANDBY state, RESETZ is set high and DLPC230-Q1 begins its boot process.

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Device Functional Modes (continued)

Exit options from STANDBY state include:

- A die over temp error sends system to SHUTDOWN state. An over temperature error in the STANDBY state means something is wrong with the system.
- PROJ_ON low sends to OFF state.
- Software commanded power cycle. System proceeds to OFF state.
- If either of the watchdog timers have been enabled by software and an error occurs, system proceeds to OFF state.
- If power unexpectedly goes bad, system proceeds to OFF state.
- DLPC230-Q1 software begins to enable DMD voltages. Sends to POWERING_DMD state. This is the first step in DMD voltage enabling process.

During the STANDBY phase, the DLPC230-Q1 software performs DMD and DLPC230-Q1 sequencer configuration steps. The software is in charge of DMD voltage enable timing, interleaving necessary DMD configuration register writes, and DLPC230-Q1 ASIC block configuration steps. After the DLPC230-Q1 software begins enabling DMD voltages, the TPS99000-Q1 proceeds to POWERING_DMD state.

7.4.3 POWERING_DMD

Once the DLPC230-Q1 software begins enabling DMD voltages when in STANDBY, the system enters POWERING_DMD state. In this state, the DLPC230-Q1 software performs all steps needed to properly configure and power up the DMD safely.

Exiting from POWERING_DMD state, the DLPC230-Q1 software confirms that DMD is powered up. This sends the TPS99000-Q1 to DISPLAY_RDY state. This is the last step in DMD voltage enabling process.

If a PROJ_ON low is received during power on, the TPS99000-Q1 will still complete the power on sequence.

7.4.4 DISPLAY_RDY

In the display ready state, the DLPC230-Q1 may enable illumination at any time.

Once the DLPC230-Q1 software enables illumination, the TPS99000-Q1 enters the DISPLAY state.

Exit conditions:

- Illumination enabled: go to DISPLAY_ON state. (HUD only)
- A *DMD park* event has occurred including power not good, PROJ_ON low, die over temp error, software park initiated, or software power cycle initiated. These events send the TPS99000-Q1 to PARKING state.

Note: for headlight only applications the TPS99000-Q1 does not enter the DISPLAY_ON state. Illumination turns on and off while remaining in DISPLAY_RDY.

7.4.5 DISPLAY_ON

System operational, image being displayed. Exit conditions:

- Illumination disabled: go to DISPLAY_RDY state.
- An internal *DMD park* event has occurred (including power not good or PROJ_ON low or die over temp error, or software park initiated, or software power cycle initiated - sends TPS99000-Q1 to PARKING state.

7.4.6 PARKING

DMD parking is taking place. PARKZ output signal (to DLPC230-Q1) is asserted low in this state. Timers count down time then the control for the DMD voltage regulators is disabled. Once the final hardware delay elapses, the next state is STANDBY.

7.4.7 SHUTDOWN

The shutdown state is entered only when a die over temperature condition is experienced. All switchable on chip activity is halted. The only exit conditions from this state are PROJ_ON low (*0*) or true power off. This state is readable via the 2nd diagnostic SPI port. All power supplies are disabled.

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7.5 Register Maps

7.5.1 System Status Registers

ADDRESS	NAME	BITS	DESCRIPTION
Chip Revision ID, R-only, Reset Value 0000			
0x00	Unused	[15:8]	Unused
	Major	[7:4]	Major revision
	Minor	[3:0]	Minor revision
Status Set, R/W, Reset Value 0000 (Writing a *1* to any bit field sets flag)			
0x01	PG Fault Status	[15]	Asserted when any bin in user register 38h is set
	DM Max width limit	[14]	Maximum DM pulse width achieved. This may or may not be an error, depending on system operational mode
	VXPG Init	[13]	Power good timer for VOFS, VRST, or VBIAS expired
	Main SPI parity error	[12]	Parity error on a SPI1 port transaction occurred (command or write data) on previous command
	ADC block error	[11]	"OR" of all errors in ADC block. Refer to x0D to determine specific error.
	Checksum error 3	[10]	Checksum error in LED / dimming controller section
	Checksum error 2	[9]	Checksum error in light sensor conditioning section
	Checksum error 1	[8]	Checksum error in ADC sub-system section
	WD2	[7]	Watchdog #2 error
	WD1	[6]	Watchdog #1 error
	Top level state change	[5]	Indicates top level state machine has changed state. Can be used to indicate that the TPS99000-Q1 has exited DISPLAY state unexpectedly due to a random fault
	Excessive brightness	[4]	Excessive brightness detector indicates an over bright fault condition
	VXPG Fault	[3]	Set 1 by hardware if power good fault occurs for VOFS, VRST, or VBIAS
	DIE Over temp warning	[2]	Thermal conditions on chip have reached the warning level. If temperature continues to rise, system will reach die over temp error temperature and emergency actions will be taken by TPS99000-Q1
	DIE Over temp error	[1]	Thermal conditions on chip have reached the emergency/error. Emergency actions will be taken by TPS99000-Q1 to protect the system. This error bit is non-maskable for PARKZ output
	PROJ_ON_LOW	[0]	Projector ON input pin is low (produces a *1* on this status bit).

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Register Maps (continued)

ADDRESS	NAME	BITS	DESCRIPTION
General Status 1, R-only, Reset Value 0000			
0x05	Clock ratio monitor	[15:12]	Mid-scale reading (1000 ± 1) indicate approximately 30-MHz external signal has been applied
	Open	[11:8]	Reserved
	Last Reset (2:0)	[7:5]	Root cause of last reset cycle, last pass through the *OFF* state. “000” – true power on cycle, internal reset set/release “001” – PROJ_ON went low “010” – watchdog timer 1 error “011” – watchdog timer 2 error “100” – die over temperature error “101” – SW power cycle command all others unused
	Top State (4:0)	[4:0]	Top level state machine current state 0x00 = SHUTDOWN 0x01 = Internal initialization 0x02 = OFF 0x03 = Internal initialization 0x04 = Initializing 1P1V 0x05 = Initializing 1P8V 0x06 = Initializing 3P3V 0x07 = De-assert RESETZ 0x08 = STANDBY 0x09 = VOFFSET enabled 0x0A = VBIAS enabled 0x0B = VRESET enabled 0x0C = DISPLAY READY 0x0D = DISPLAY ON 0x0E = Parking initialized 0x0F = VBIAS and VRESET disabled 0x10 = VOFFSET disabled 0x11 = DMD voltage discharge

7.5.2 ADC Control

ADDRESS	NAME	BITS	DESCRIPTION
ADC Block Status SET, Read/Write, Reset Value 0000 (Writing *1* to any bit field sets flag. OR of all ADC error bits feed into single ADC error bit in main status.)			
0x0D	Unused	[15:8]	Reserved
	AD3 Command Stop-bit Error	[7]	Indicates that a stop bit was missing
	ADC Timeline Error	[6]	Indicates that a new command was received while previous command was still in progress
	Command error	[5]	An error was detected on a serial bus command
	Parity error detected	[4]	A parity error in bit stream was detected
	Ch2 underflow	[3]	ADC conversion results presented in channel two register experienced an underflow
	Ch2 saturated	[2]	ADC conversion results presented in channel two register are saturated
	Ch1 underflow	[1]	ADC conversion results presented in channel one register experienced an underflow
	Ch1 saturated	[0]	ADC conversion results presented in channel one register are saturated

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7.5.3 General Fault Status

ADDRESS	NAME	BITS	DESCRIPTION
General Fault Status, R-only, Reset Value 0000, Value of 1 indicates a Fault			
0x38	VBIAS Powergood Fault	[15]	VBIAS is below the minimum specified voltage
	VRST Powergood Fault	[14]	VRESET is below the minimum specified voltage
	VOFS Powergood Fault	[13]	VOFFSET is below the minimum specified voltage
	Powergood 1 Fault	[12]	VMAIN or AVDD rail is below the minimum specified voltage (Logical OR).
	Powergood 2 Fault	[10]	At least one of 1.1 V, 1.8 V, 3.3 V, and 6 V supplies is below the minimum specified voltage (Logical OR).
	ADC 3V LDO Powergood Fault	[9]	ADC 3V LDO is below the minimum specified voltage
	ADC 3V LDO Over Voltage Fault	[8]	ADC 3V LDO is above the maximum specified voltage
	TIA 3V LDO Powergood Fault	[7]	TIA 3V LDO is below the minimum specified voltage
	TIA 3V LDO Over Voltage Fault	[6]	TIA 3V LDO is above the maximum specified voltage
	TIA5 LDO Over Voltage Fault	[5]	TIA 5V LDO is above the maximum specified voltage
	TIAM8 LDO Powergood Fault	[4]	Negative 8 V Photo Diode Bias LDO is below the minimum specified voltage
	TIAM8 LDO Over Voltage Fault	[3]	Negative 8 V Photo Diode Bias LDO is above the maximum specified voltage
	V3P3 Powergood Fault	[2]	3.3 V is below the minimum specified voltage
	V1P8 Powergood Fault	[1]	1.8 V is below the minimum specified voltage
	V1P1 Powergood Fault	[0]	1.1 V is below the minimum specified voltage

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLP553x-Q1 chipset is designed to support projection-based automotive applications such as head-up displays (HUD) and high resolution headlights.

The DLP553x-Q1 chipset consists of three components—the DLP553x-Q1 (DMD), the DLPC230-Q1, and the TPS99000-Q1. The DMD is a light modulator consisting of tiny mirrors that are used to form and project images. The DLPC230-Q1 is a controller for the DMD; it formats incoming video and controls the timing of the DMD illumination sources and the DMD in order to display the incoming video. The TPS99000-Q1 is a controller for the illumination sources (LEDs or lasers) and a management IC for the entire chipset. In conjunction, the DLPC230-Q1 and the TPS99000-Q1 can also be used for system-level monitoring, diagnostics, and failure detection features.

8.2 Typical Applications

There are two configurations for this chip, HUD and headlight. Table 3 shows the differences for the pin connections between the two configurations.

Table 3. Pin Configuration Differences for HUD and Headlight

PIN	NAME	DESCRIPTION	HUD	HEADLIGHT
12	COMPOUT	Photodiode (PD) Interface High-speed comparator output	Connect to DLPC230-Q1 GPIO_02	No connect
15	SYNC	External LED buck driver sync strobe output	See *Setting the Current Limit*	No connect
18	D_EN	LED Interface; Buck High-Side FET Drive Enable	Connect to DLPC230-Q1 D_EN (GPIO_04)	Connect to DLPC230-Q1 D_EN (GPIO_04) or ground
19	S_EN	LED Bypass Shunt Strobe Input	Connect to DLPC230-Q1 S_EN (GPIO_03)	Connect to DLPC230-Q1 S_EN (GPIO_03) or ground
20	LED_SEL_0	LED Enable Strobe 0 Input	Connect to DLPC230-Q1 PMIC_LEDSEL_0	Connect to DLPC230-Q1 PMIC_LEDSEL_0 or ground
21	LED_SEL_1	LED Enable Strobe 1 Input	Connect to DLPC230-Q1 PMIC_LEDSEL_1	Connect to DLPC230-Q1 PMIC_LEDSEL_1 or ground
22	LED_SEL_2	LED Enable Strobe 2 Input	Connect to DLPC230-Q1 PMIC_LEDSEL_2	Ground
23	LED_SEL_3	LED Enable Strobe 3 Input	Connect to DLPC230-Q1 PMIC_LEDSEL_3	Ground
38	DRV_EN	Drive enable for LM3409	Driver select enable	Resistor to ground
39	CMODE	Capacitor selection output (allows for a smaller capacitance to be used in CM mode for less over/under shoot). Open drain	See *CMODE Big Cap Mode in Discontinuous Operation*	No connect
40	DMUX0	Digital test point output	Either connect to test point or leave unconnected. Do not ground.	Either connect to test point or leave unconnected. Do not ground.
41	DMUX1	Digital test point output	Either connect to test point or leave unconnected. Do not ground.	Either connect to test point or leave unconnected. Do not ground.
43	S_EN1	Low resistance shunt NFET drive enable [High means shunt active]	See *Continuous Mode S_EN2 Dissipative Load Shunt Options*	Shunt enable / No connect
44	S_EN2	High resistance shunt NFET drive enable [High means shunt active]	See *Continuous Mode S_EN2 Dissipative Load Shunt Options*	No connect
45	R_EN	Red channel select. Drive for low side NFET	FET enable	FET enable / No connect

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Typical Applications (continued)

Table 3. Pin Configuration Differences for HUD and Headlight (continued)

PIN	NAME	DESCRIPTION	HUD	HEADLIGHT
46	G_EN	Green channel select. Drive for low side NFET	FET enable	FET enable / No connect
47	B_EN	Blue channel select. Drive for low side NFET	FET enable	FET enable / No connect
57	AMUX1	Analog Test Mux Output 1	Either connect to test point or leave unconnected. Do not ground.	Either connect to test point or leave unconnected. Do not ground.
61	AMUX0	Analog Test Mux Output 0	Either connect to test point or leave unconnected. Do not ground.	Either connect to test point or leave unconnected. Do not ground.
62	VIN_LDOT_M8	Dedicated TIA Interface –8 V(nom) LDO external regulation FET drive signal for -8 V regulator	Refer to *Low Dropout Regulators*	Connect as described in*Low Dropout Regulators* or do not connect (select NC option in SW).
63	VLDOT_M8	Dedicated TIA Interface –8 V(nom) LDO filtered supply (regulated voltage feedback)	Refer to *Low Dropout Regulators*	Connect as described in*Low Dropout Regulators* or do not connect (select NC option in SW).
76	R_IADJ	External resistance for IADJ voltage to current transformation	See *Setting the Current Limit*	Ground
77	IADJ	Current output used to adjust external LED controller drive current set point	See *Setting the Current Limit*	Ground
85	ADC_IN1	External ADC Channel 1, see Table 2	Connect to LED anode with voltage divider	No connect / Optional (customer use)
86	ADC_IN2	External ADC Channel 2, see Table 2	Optional (LED input voltage)	No connect / Optional (customer use)
88	ADC_IN3	External ADC Channel 3, see Table 2	No connect / Optional (customer use)	No connect / Optional (customer use)
90	ADC_IN4	External ADC Channel 4, see Table 2	No connect / Optional (customer use)	No connect / Optional (customer use)
92	ADC_IN5	External ADC Channel 5, see Table 2	No Connect / Optional (Thermistor)	No connect / Optional (customer use)
93	ADC_IN6	External ADC Channel 6, see Table 2	No Connect / Optional (Thermistor)	No connect / Optional (customer use)
94	ADC_IN7	External ADC Channel 7, see Table 2	No Connect / Optional (Thermistor)	No connect / Optional (customer use)

Pulldown resistors are required on the pins in the below table to avoid a floating input during the power-up and power-down conditions.

Table 4. Pulldown Resistor Requirements

PIN	NAME	TYP
5	ADC_MOSI	10 kΩ
6	WD1	10 kΩ
16	SEQ_START	10 kΩ
17	SEQ_CLK	10 kΩ
18	D_EN(1)	10 kΩ
19	S_EN(1)	10 kΩ
20	LED_SEL_0(1)	10 kΩ
21	LED_SEL_1(1)	10 kΩ
22	LED_SEL_2(1)	10 kΩ
23	LED_SEL_3(1)	10 kΩ
27	SPI1_CLK	10 kΩ
30	SPI1_DIN	10 kΩ

(1) If these pins are not connected to the DLPC230-Q1 (as in a Headlight configuration) then they may be tied directly to ground without a pulldown resistor.

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Table 4. Pulldown Resistor Requirements (continued)

PIN	NAME	TYP
31	SPI2_DIN	10 kΩ
34	SPI2_CLK	10 kΩ
49	DMD_VOFFSET(2)	56 kΩ
50	DMD_VBIAS(2)	110 kΩ
51	DMD_VRESET(2)	68 kΩ

(2) Resistor pull downs are required to create a minimum load for DMD_VOFFSET, DMD_VBIAS, and DMD_VRESET. Each of these pulldowns should provide a load from 0.1mA to 1mA. If the -8 V LDO is used, then the pull down for DMD_VRESET may be eliminated. If only one or zero TIAs are used, then these pull downs may draw up to 1mA of current.

8.2.1 HUD

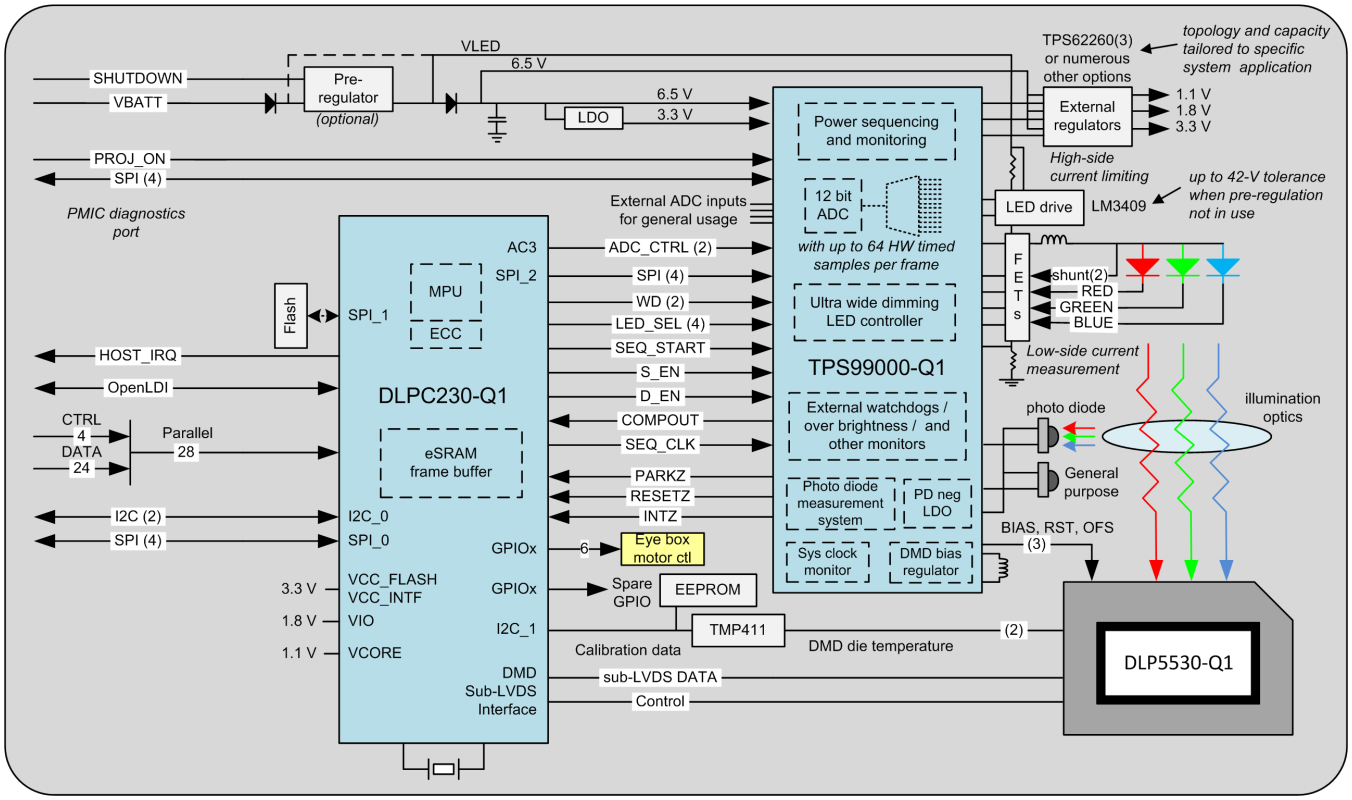

Figure 41. HUD System Block Diagram

8.2.1.1 Design Requirements

The DLPC230-Q1 is a controller for the DMD and the timing of the RGB LEDs in the HUD. It requests the proper timing and amplitude from the LEDs to achieve the requested color and brightness from the HUD across the entire operating range. It synchronizes the DMD with these LEDs in order to generate full-color video requested from the host.

The DLPC230-Q1 receives inputs from a host processor in the vehicle. The host provides commands and input video data. Read and write (R/W) commands can be sent using either the I^2C bus or SPI bus. The bus that is not being used for R/W commands can be used as a read-only bus for diagnostic purposes. Input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The SPI flash memory provides the embedded software for the DLPC230-Q1's ARM core, color calibration data, and default settings. The TPS99000-Q1 provides diagnostic and monitoring information to the DLPC230-Q1 using an SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The DLPC230-Q1 interfaces to a TPM411 via I^2C for temperature information.

The outputs of the DLPC230-Q1 are LED drive information to the TPS99000-Q1, control signals to the DMD, and monitoring and diagnostics information to the host processor. Based on a host requested brightness and the operating temperature, the DLPC230-Q1 determines the proper timing and amplitudes for the LEDs. It passes this information to the TPS99000-Q1 using an SPI bus and several additional control signals such as D_EN, S_EN, and SEQ_START. It controls the DMD mirrors by sending data over a sub-LVDS bus. It can alert the host about any critical errors using a HOST_IRQ signal.

The TPS99000-Q1 is a highly-integrated mixed-signal IC that controls DMD power, the analog response of the LEDs, and provides monitoring and diagnostics information for the HUD system. The power sequencing and monitoring blocks of the TPS99000-Q1 properly power up the DMD and provide accurate DMD voltage rails, and then monitor the system's power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The highly accurate photodiode (PD) measurement system and the dimming controller block precisely control the LED response. This enables a DLP technology HUD to achieve a very high dimming range (> 5000:1) with accurate brightness and color across the temperature range of the system. Finally, the TPS99000-Q1 has several general-purpose ADCs that designers can use for system-level monitoring, such as over-brightness detection.

The TPS99000-Q1 receives inputs from the DLPC230-Q1, power rail voltages for monitoring, a photodiode that is used to measure LED response, the host processor, and potentially several other ADC ports. The DLPC230-Q1 sends commands to the TPS99000-Q1 over a SPI port and several other control signals. The TPS99000-Q1 includes watchdogs to monitor the DLPC230-Q1 and ensure that it is operating as expected. The power rails are monitored by the TPS99000-Q1 to detect power failures or glitches and request a proper power down of the DMD in case of an error. The photodiode's current is measured and amplified using a transimpedance amplifier (TIA) within the TPS99000-Q1. The host processor can read diagnostics information from the TPS99000-Q1 using a dedicated SPI bus. Additionally the host can request the system to be turned on or off using a PROJ_ON signal. The TPS99000-Q1 has several general-purpose ADCs that can be used to implement other system features such as over-brightness and over-temperature detection.

The outputs of the TPS99000-Q1 are LED drive signals, diagnostic information, and error alerts to the DLPC230-Q1. The TPS99000-Q1 has signals connected to the LM3409 buck controller for high power LEDs and to discrete hardware that control the LEDs. The TPS99000-Q1 can output diagnostic information to the host and the DLPC230-Q1 over two SPI busses. It also has signals such as RESETZ, PARKZ, and INTZ that can be used to trigger power down or reset sequences.

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as an input (video data) and produces a mechanical output (mirror position). The electrical interface to the DMD is a sub-LVDS interface driven with the DLPC230-Q1. The mechanical output is the state of more than 1.3 million mirrors in the DMD array that can be tilted ±12°. In a projection system, the mirrors are used as pixels in order to display an image.

8.2.1.2 Application Design Considerations

8.2.1.2.1 Photodiode Considerations

Placement of the photodiode within the optical path is critical to system performance. Carefully optimizing the placement and electrical response of the photodiode will yield the widest dynamic range for dimming. Treatment of photodiode considerations are addressed in the *Photodiode Selection and Placement Guide* (DLPA082).

Several factors for the photodiode should be considered:

- **Position:**
  - Ideally, a position in the illumination path (Figure 42) should be located that produces strong, but also balanced amplitude signal responses from each of the three LEDs at the system's target white point. Imbalance between the three channels due to non-ideal placement of the detector will limit dynamic range of the dimming system. The TIA supports an RGB trim function to help re-balance an imbalanced system. This feature is useful for completing the process of optimizing the balance of the amplitude signal responses from each LED. But it is still advisable to take care in the design of the illumination path such that the natural balance of the colors is as ideal as practical.
  - An additional consideration when determining position of photodiode is back scattered light from the projection path. Some amount of *on state* light will reflect backwards from the surfaces of the projection lens and other objects in the light path after the DMD. If the photodiode is placed in a position that is illuminated by this back scattered light, the photodiode will see a mixture of true illumination light plus this back scattered output light. If the back scattered light is significant, the illumination control loop will be

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impacted. Also, the back scatter is dependent on the video content (i.e. a solid white pattern may cause more back scatter than a solid black pattern), which impacts the full-on full-off contrast.

- **Irradiance on the Photodiode:**
  - It is also important that the irradiance on the photodiode is not too high or too low. A high magnitude of irradiance can cause saturation and slower response from the photodiode. This varies depending on the specific photodiode selected for use. The TPS99000-Q1 provides a negative LDO and negative voltage source to provide a low noise –8 V reference for reverse biasing the photodiode. Reverse biasing the photodiode (photo conductive mode) increases the amount of irradiance the photodiode can accept without saturating as compared to a zero bias case (photovoltaic mode). On the other hand, a low magnitude of irradiance can make the system more susceptible to noise, including photodiode dark current. It is best to operate at photodiode current levels high enough so that dark current is negligible to avoid potential issues due to other noise sources (noise on cabling, grounding, etc).
- **Cable to remote PD placement:**
  - If the photodiode is located remotely it is recommended to use a low capacitance cable and minimize the cable length. At a minimum: for noise rejection, use a one conductor shielded cable with the photodiode bias (cathode) connected to the cable shield and the photodiode output (anode) connected to the inner conductor. Better noise rejection is possible using shielded two conductor cables with the shield tied to a low noise ground. Experiments may be necessary to determine an optimal photodiode position to achieve adequate response balance between the colors and an acceptable irradiance level. Care must be taken to not exceed the maximum total photodiode capacitance (diode plus cable and connectors) as specified in *Electrical Characteristics - Transimpedance Amplifier Parameters*. TIA design includes adjustable feedback capacitance to optimize response for specific solutions. DLPC230-Q1 flash configuration options allow tuning of this feedback capacitance for optimal slew rate and stability performance.

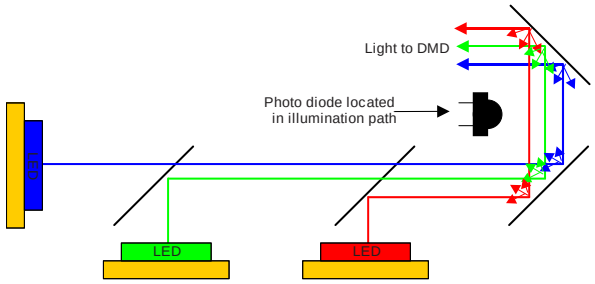

Figure 42. Photodiode Placement

The photodiode conditioning circuits include several features to improve performance and integration:

- Independent red, green and blue parameters for gain and offset
- Selectable feedback capacitance
- Integrated negative LDO, to provide photodiode reverse bias

8.2.1.2.2 LED Current Measurement

The TPS99000-Q1 includes a dedicated ADC channel for LED current measurement. The *blanking current* management process in system software, described in the *Continuous Mode Operation* section, relies on this measurement to coordinate the blanking current to the photo feedback current. The software measures the actual LED current in photo feedback (per color) and also measures the blanking current. The blanking current setting is fine trimmed during system operation to a level ideal for optimizing the initial current of each light pulse. As such, it is critical to system performance that this LED current measurement is as noise free as practical. Using a *Kelvin* connection to the low side sense resistor, and an RC filter is recommended to filter switching ripple, as illustrated in Figure 43. The Kelvin resistors should be < 100 Ω each and should have a tolerance of less than 0.5% matched resistors.

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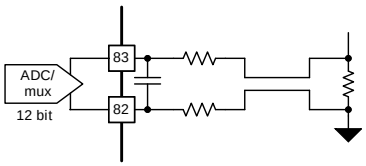

Figure 43. LED Current Measurement Wiring

8.2.1.2.3 Setting the Current Limit

The current limit of the LM3409 is determined by the current draw of the IADJ pin of the TPS99000-Q1, which is controlled by an internal DAC and an external resistor connected to the R_IADJ pin of the TPS99000-Q1. The approximate peak current limit can be calculated by the following equation:

$$I_{LIM} = \frac{V_{DAC}}{R_{ADJ}} * \frac{R_{CSP}}{R_{HSS}}$$

Where:

- V_{DAC} is the voltage of the current control DAC.
- R_{ADJ} is the resistor attached to the R_IADJ pin of the LM3409. Do to the max current this circuit can output, it is recommended that this value be 1 kΩ or higher
- R_{SCP} is the resistor attached to the CSP pin of the LM3409. Use the same value for R_{CSN}.
- R_{HSS} is the high side sense resistor of the LM3409 control circuit.

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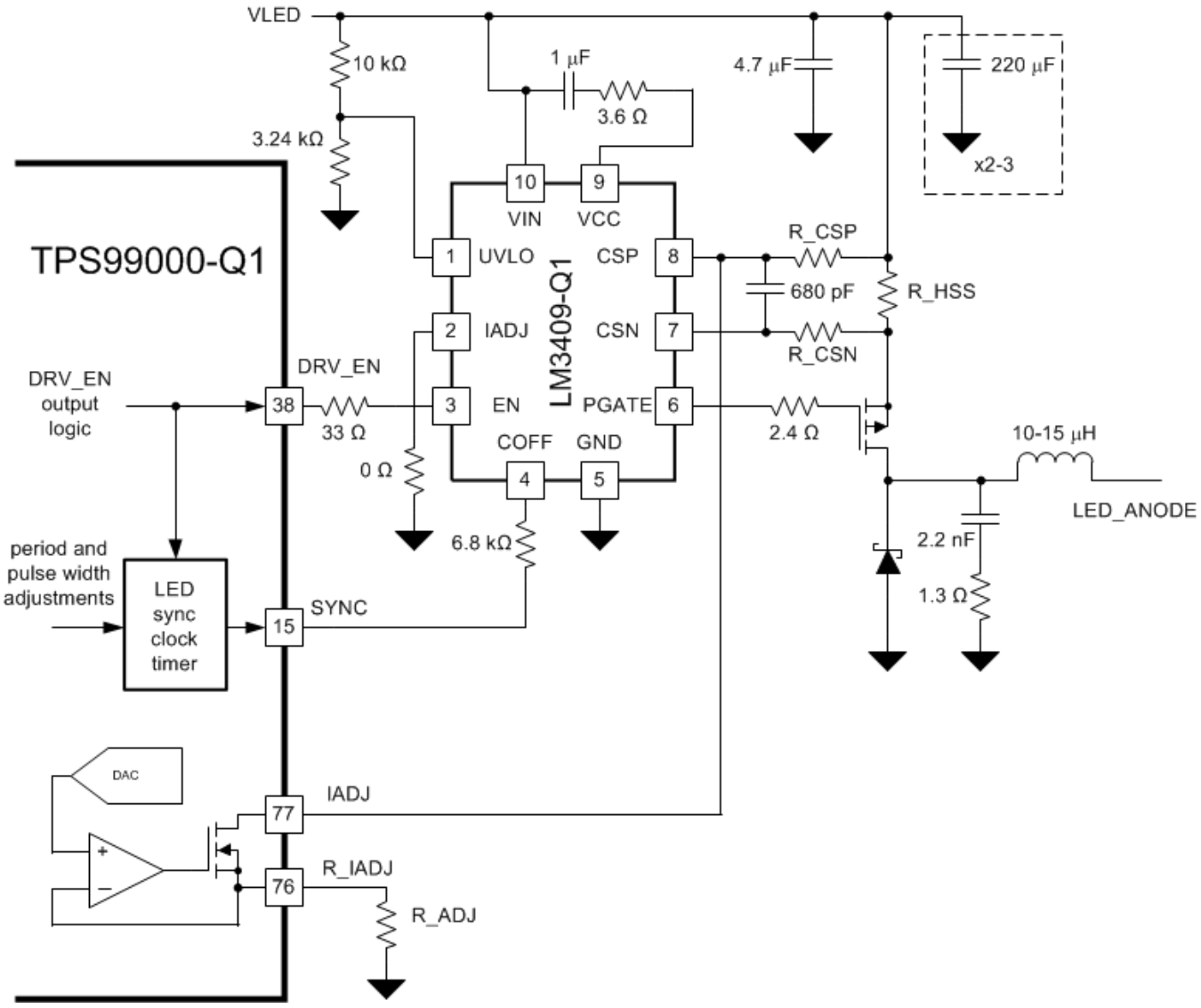

Figure 44. Current Limit Configuration Circuit

8.2.1.2.4 Input Voltage Variation Impact

Although the blanking current control makes the TPS99000-Q1-based systems less susceptible to ill effects from input voltage variations, it is still recommended that a stable, pre-regulation voltage source be used to supply the VLED power rail (as shown in the functional block diagram). Changes in input voltage to the driver will have impact on slew rates or rising edges of ripple waveforms in continuous operation mode. These variations will slightly alter the total integrated light output per pulse, which can cause noticeable variations in color balance and brightness as input voltage changes.

8.2.1.2.5 Discontinuous Mode Photo Feedback Considerations

System designs should consider the amount of additional capacitance placed in parallel with the photodiode, and the capacitance of the photodiode itself. While the TPS99000-Q1 is designed to function with a very wide range of total capacitance, the lowest light level brightness performance is directly impacted by this capacitance. Higher TIA1 input capacitance will result in a brighter minimum brightness achievable by the system due to this light pulse overrun phenomenon. This results in a reduction of dimming range. (For highest performance, system designer should minimize total capacitance of the photodiode, photodiode cable and connector system).

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The leading edge of the light pulse in discontinuous mode is controlled by the charging rate of the capacitance in parallel with the LED. The photo feedback DAC sets the threshold to turn on the shunt FET which shunts the current away from the LED. Latency in the photo feedback loop will result in the light climbing higher than the threshold as shown in Figure 45. The amount of light that occurs after the threshold is reached (shown as hashed green area) is the majority of the light at the lowest discontinuous mode brightness levels. Figure 45 also shows that a reduction in photo feedback DAC level by a factor of two does not reduce the total light pulse power by a factor of two because of the light that occurs after the threshold. The amount of light overrun after the threshold is a function of the photo feedback latency, inductor initial current, capacitance in parallel with the LED, LED voltage to current characteristics and shunt FET timing.

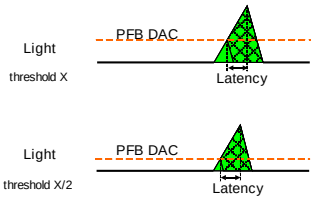

Figure 45. Discontinuous Pulse Overrun

8.2.1.2.6 Transimpedance Amplifiers (TIAs, Usage, Offset, Dark Current, Ranges, RGB Trim)

The TPS99000-Q1 includes support for up to 2 system photodiode inputs.

TIA1 is used as the primary photo feedback channel. It supports 14 unique gain settings, spanning 0.75 kV/A to 288 kV/A. In addition, these gain settings can be adjusted downward by a high resolution trim function, in a range of 1.0x to 0.2x. This trim function has independent RGB settings, supporting color rebalancing (such as trimming RGB feedback signals so that white light produces roughly equal voltages at TIA output for each color). Color rebalancing helps keep all three color channels in the working voltage range to maximize dynamic range. Figure 46 shows the TIA1 model.

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TIA_GAIN(3:0)	GAIN#1	GAIN#2	GAIN#3	GAIN2*3	V/A
“0000”	375	2	1	2	750
“0001”	750	2	1	2	1.5k
“0010”	750	4	1	4	3k
“0011”	750	8	1	8	6k
“0100”	750	4	3	12	9k
“0101”	750	4	4	16	12k
“0110”	750	8	3	24	18k
“0111”	750	8	4	32	24k
“1000”	750	4	12	48	36k
“1001”	3k	4	4	16	48k
“1010”	3k	8	3	24	72k
“1011”	3k	8	4	32	96k
“1100”	3k	4	12	48	144k
“1101”	3k	8	12	96	288k

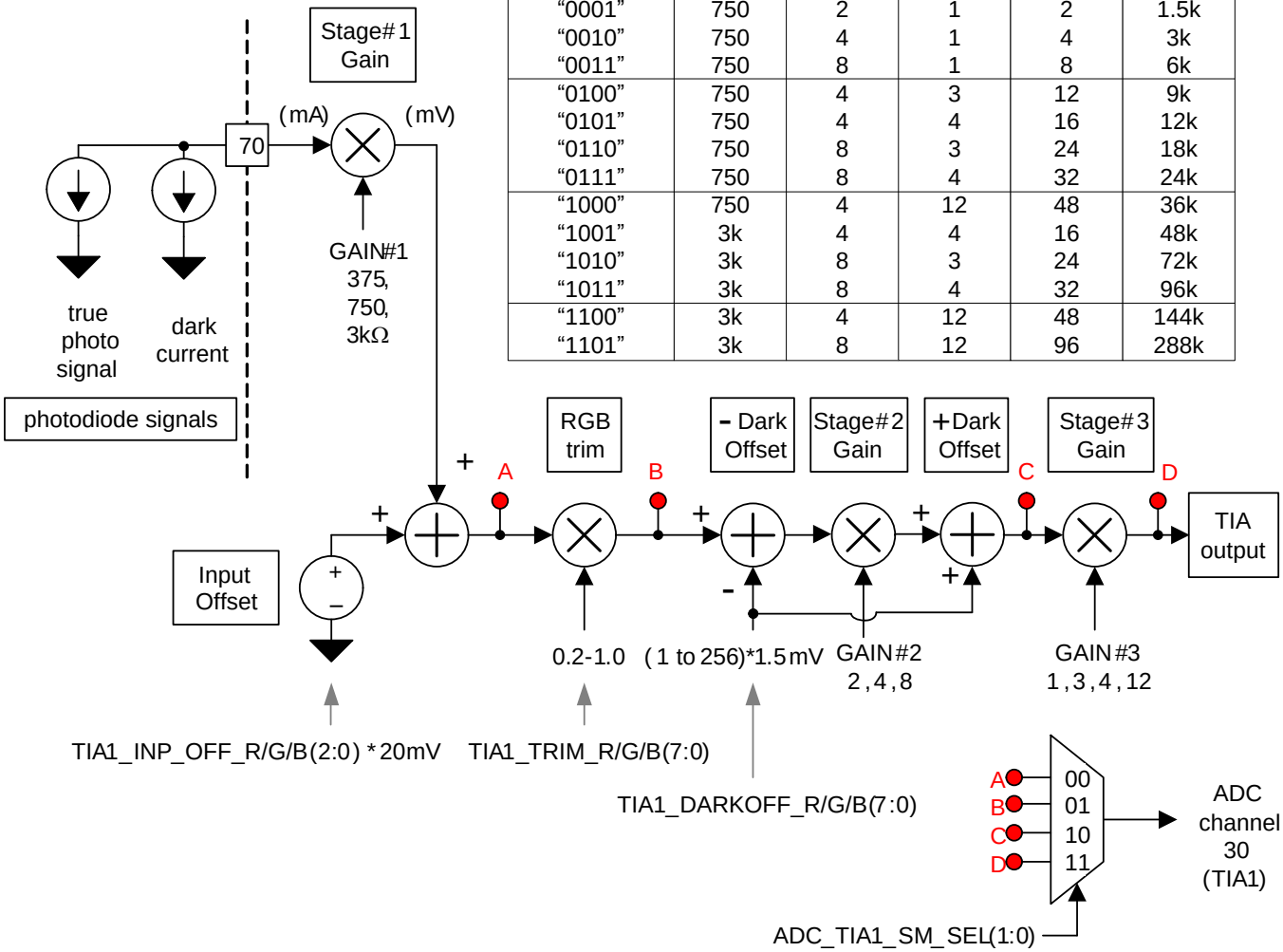

Figure 46. TIA1 Trim, Offset, and Gain Stages

TIA2 supports a single trim value and single *darkoffset* value, but is otherwise identical to TIA1.

NOTE

TIA2 shall only be used for diagnostic purposes, and it is not recommended to use for primary photo feedback amplification. If TIA2 is used to measure projector output or illumination light, this lack of multiplexed RGB parameters for trim and dark offset will limit its usage to looking only at one color at a time for situations where highest gain settings are used in combination with high color to color electrical response imbalance. For lower gain settings or situations where the photodiode responses are naturally balanced, all 3 colors likely can be monitored with TIA2.

The trim settings may be used to lower the total gain of the TIA amplifiers. This provides flexibility to allow higher photo diode currents to be used without saturating the TIA. For example, with the trim setting limited to 0.5×, a 0.75 kV/A gain selection can be considered a 0.375 kV/A effective gain setting. The supported maximum photo diode current doubles in this case.

Both TIAs are designed to support a wide range of photo diode capacitances. A variable, internal compensation capacitor network is available to tune the circuit for maximum performance for a given photo diode and cable combination.

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Both TIAs can be independently enabled or disabled. When a TIA is disabled, it is placed in a low power mode to optimize power consumption.

TIA2 can be used for an over-brightness detection input or ADC measurements. It supports two outputs: 1) a higher bandwidth output, optimized for measuring photo diode response of CM bit slice light pulses, and 2) a much lower bandwidth output, optimized for measuring light flux filter over periods spanning at least one video frame. TIA1 supports these same two outputs, plus one more: a very high bandwidth output used for the real-time color control loop photo feedback. See *Electrical Characteristics - Transimpedance Amplifier Parameters* for BW and slew rate specifications for this use case.

One potential use for TIA2 is for system level brightness detection.

8.2.2 Headlight

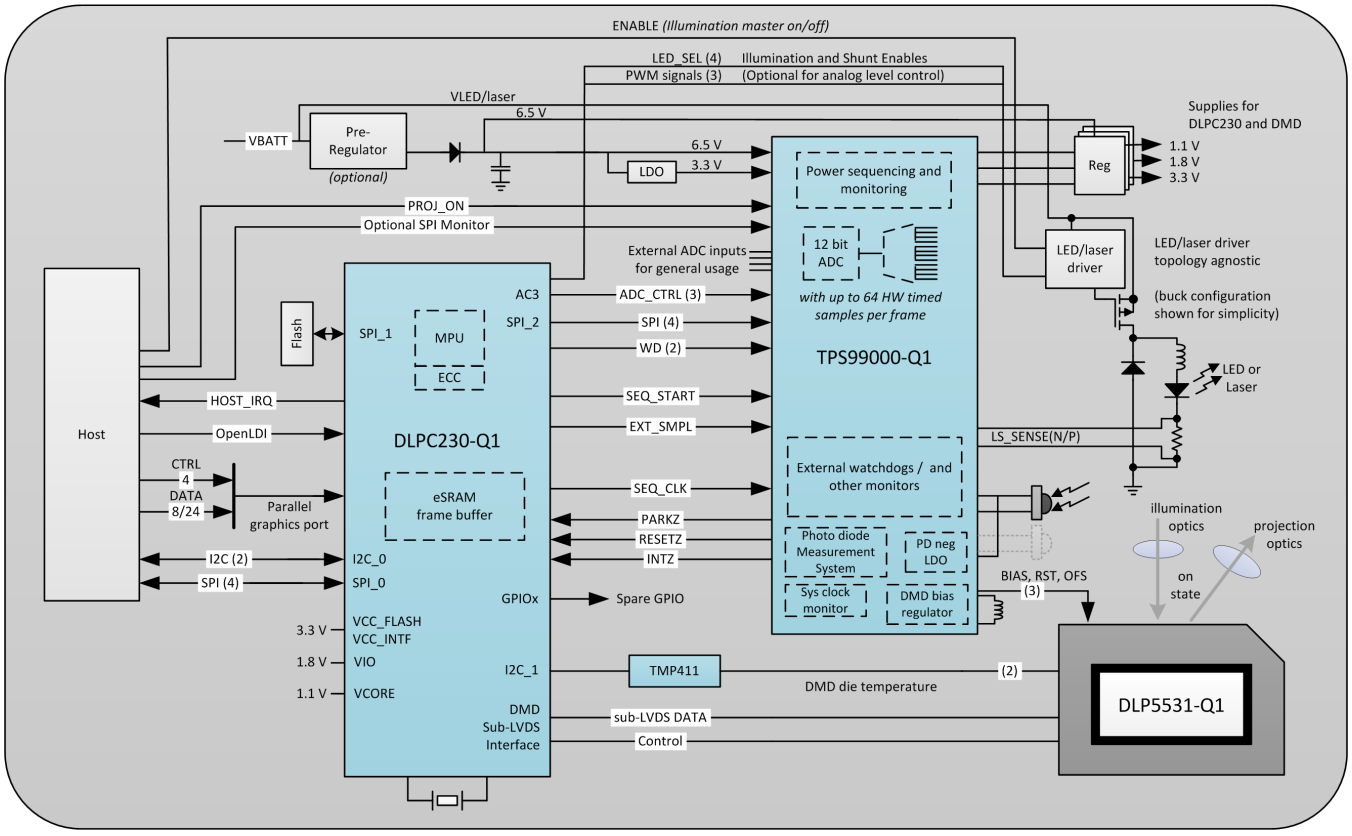

Figure 47. Headlight System Block Diagram

8.2.2.1 Design Requirements

The DLPC230-Q1 is a controller for the DMD and the light sources in headlight applications. It receives input video from the host and synchronizes DMD and light source timing in order to achieve the desired video. The DLPC230-Q1 formats input video data that is displayed on the DMD. It synchronizes these video segments with light source timing in order to create video with grayscale shading.

The DLPC230-Q1 receives inputs from a host processor in the vehicle. The host provides commands and input video data. R/W commands can be sent using either the I^2C bus or SPI bus. The bus that is not being used for R/W commands can be used as a read-only bus for diagnostic purposes. Input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The 24-bit bus can be limited to only 8-bits of data for single light source systems such as headlights. The SPI flash memory provides the embedded software for the DLPC230-Q1's ARM core, any calibration data, and default settings. The TPS99000-Q1 provides diagnostic and monitoring information to the DLPC230-Q1 using an SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The TMP411 uses an I^2C interface to provide the DMD array temperature to the DLPC230-Q1.

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The outputs of the DLPC230-Q1 are configuration and monitoring commands to the TPS99000-Q1, timing controls to the LED or laser driver, control signals to the DMD, and monitoring and diagnostics information to the host processor. The DLPC230-Q1 communicates with the TPS99000-Q1 over an SPI bus. It uses this to configure the TPS99000-Q1 and to read monitoring and diagnostics information from the TPS99000-Q1. The DLPC230-Q1 sends drive enable signals to the LED or laser driver, and synchronizes this with the DMD mirror timing. The control signals to the DMD are sent using a sub-LVDS interface.

The TPS99000-Q1 is a highly integrated mixed-signal IC that controls DMD power, the timing and amplitude of the LEDs or lasers, and provides monitoring and diagnostics information for the headlight system. The power sequencing and monitoring blocks of the TPS99000-Q1 properly power up the DMD and provide accurate DMD voltage rails, and then monitor the system's power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The TPS99000-Q1 also has several output signals that can be used to control a variety of LED or laser driver topologies. The TPS99000-Q1 also has several general-purpose ADCs that designers can use for system level monitoring, such as over-brightness detection.

The TPS99000-Q1 receives inputs from the DLPC230-Q1, the power rails it monitors, the host processor, and potentially several other ADC ports. The DLPC230-Q1 sends configuration and control commands to the TPS99000-Q1 over an SPI bus and several other control signals. The TPS99000-Q1 includes watchdogs to monitor the DLPC230-Q1 and ensure that it is operating as expected. The power rails are monitored by the TPS99000-Q1 in order to detect power failures or glitches and request a proper power down of the DMD in case of an error. The host processor can read diagnostics information from the TPS99000-Q1 using a dedicated SPI bus. Additionally the host can request the image to be turned on or off using a PROJ_ON signal. Lastly, the TPS99000-Q1 has several general-purpose ADCs that can be used to implement system level monitoring functions.

The outputs of the TPS99000-Q1 are diagnostic information and error alerts to the DLPC230-Q1, and control signals to the LED or laser driver. The TPS99000-Q1 can output diagnostic information to the host and the DLPC230-Q1 over two SPI busses. In case of critical system errors, such as power loss, it outputs signals to the DLPC230-Q1 that trigger power down or reset sequences. It also has output signals that can be used to implement various LED or laser driver topologies.

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as an input (video data), and produces a mechanical output (mirror position). The electrical interface to the DMD is a sub-LVDS interface with the DLPC230-Q1. The mechanical output is the state of more than 1.3 million mirrors in the DMD array that can be tilted ±12°. In a projection system the mirrors are used as pixels in order to display an image.

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9 Power Supply Recommendations

The TPS99000-Q1 requires two power inputs and also provides several power outputs, as well as controlling additional external power supplies. The power supply architecture is explained in *Power Supply Architecture*.

9.1 TPS99000-Q1 Power Supply Architecture

- 6.5 V is the recommended operating voltage for HUD designs because the LM3409 locks out at voltages below 6 V; therefore, the system designer may choose 6.5 V to power both devices. If the LM3409 is not used with the TPS99000 (as in most headlight designs), then any voltage may be used that meets the Recommended Operating Conditions of the device.
- 3.3 V (LDO recommended)

9.2 TPS99000-Q1 Power Outputs

- DMD Required Voltages:
  - DMD_VOFFSET
  - DMD_VBIAS
  - DMD_VRESET
- –8 V Photodiode Bias
- Internally used LDOs. These are not designed to be used externally, but are listed here as they require external bypass capacitors:
  - 5 V
  - 3.3 V TIA
  - 3.3 V ADC

9.3 Power Supply Architecture

The power supply architecture depends on the amount of power required for the illumination source. For HUD applications which require precise color and white point control, it is highly recommended to pre-regulate the illumination power supply, as voltage variations can cause variations in the LED output. For non-color critical applications, the designer may choose to completely isolate the illumination driver. In addition, if 2 or more LEDs are driven in series, then the pre-regulated voltage must be higher than the voltage of the LEDs. The different architectures are shown below.

Note that the architectures make use of the LM25118 as a pre-regulator. This part uses a buck-boost architecture which allows it to supply the required 6.5 V with a battery voltage input of 6 V to 18 V. If the battery input can be guaranteed to be above the 6.5 V output voltage, then a buck architecture can be used instead, resulting in BOM savings.

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Power Supply Architecture (continued)

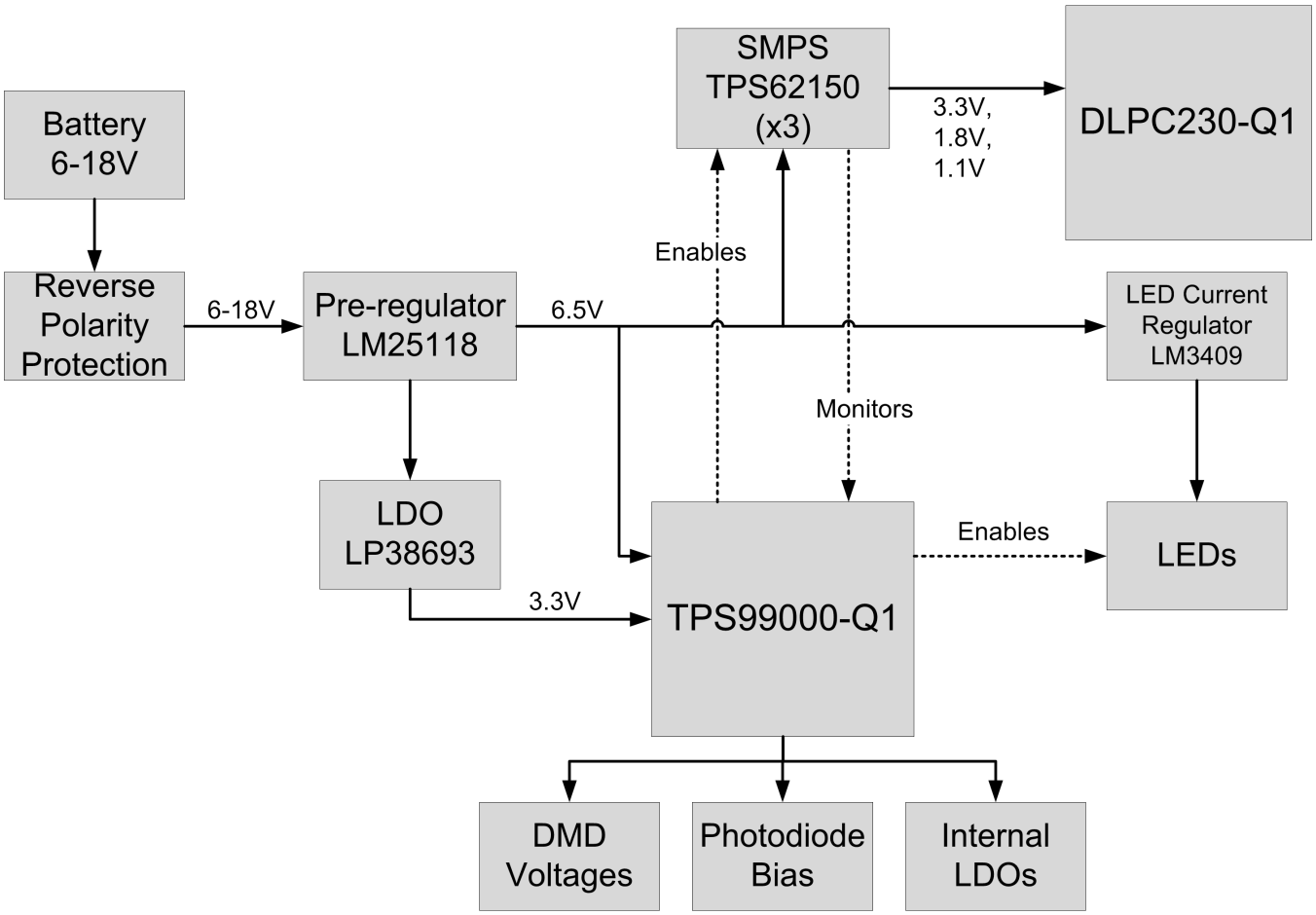

Figure 48. Architecture Number 1: HUD Application with LED Forward Voltage Less Than 5 V

In this application, the same pre-regulator is used to power the 6.5 V rail as well as the LM3409. Since the LM3409 input voltage must be kept above 6 V, the pre-regulator is set to 6.5 V.

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Power Supply Architecture (continued)

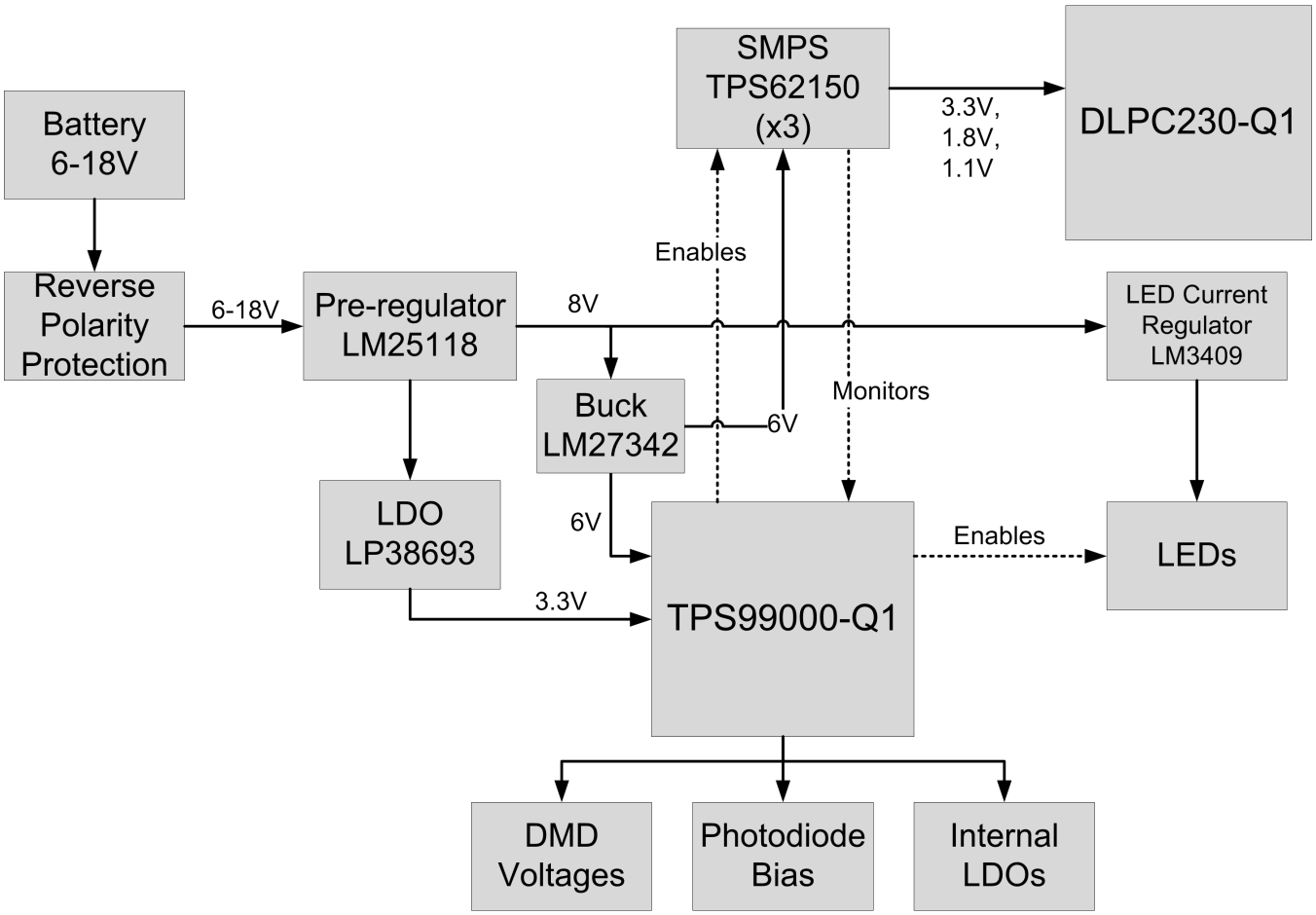

Figure 49. Architecture Number 2: HUD Application with Two LEDs in Series Configuration

In this application, the pre-regulator must be designed to operate at a higher output voltage in order to drive 2 LEDs in series. Because the TPS99000-Q1 requires a VIN from 5.5 V to 7 V, a small buck regulator is used to generate a 6 V power rail.

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Power Supply Architecture (continued)

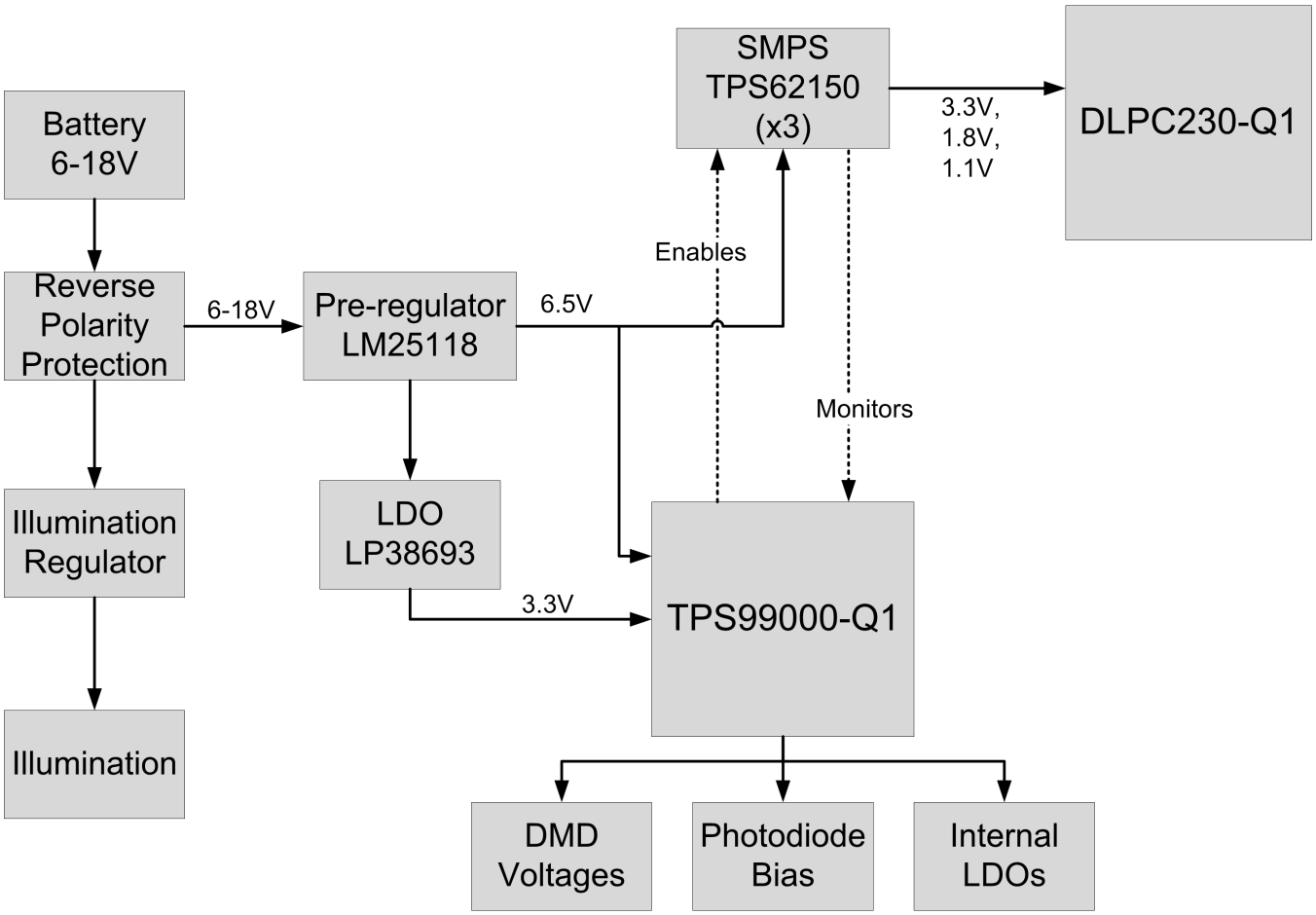

Figure 50. Architecture Number 3: Headlight Application with Independent Illumination

In this application, the power used to drive the illumination is separate from the TPS99000-Q1. This is possible in applications where the illumination driver can be very simple. Although the LM25118 is shown here, a different regulator would likely be selected in this application because the maximum current requirements are much less with the illumination power path removed.

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10 Layout

10.1 Layout Guidelines

The TPS99000-Q1 is both a power and precision analog IC. As such, care must be taken to the layout of certain signals and circuits within the system. Along with general layout best practices, pay attention to the following areas of detail, which are discussed in this document.

- Power/high current signals
- Sensitive analog signals
- High speed digital signals
- High power current loops
- Kelvin sensing connections
- Ground separation

10.1.1 Power/High Current Signals

The TPS99000-Q1 contains two blocks that switch a relatively high amount of current. The first of these is the switching regulator which generates the voltages used by the DMD. The second is the integrated LED FET gate drivers.

The DMD regulator consists of the following pins of the TPS99000-Q1:

Table 5. TPS99000-Q1 DMD Regulator Pins

PIN	NAME	PEAK BOARD CURRENT
49	DMD_VOFFSET	800 mA
50	DMD_VBIAS	800 mA
51	DMD_VRESET	800 mA
52	DRST_LS_IND	800 mA
53	DRST_PGND	800 mA
54	DRST_HS_IND	800 mA
55	VIN_DRST	800 mA
56	VSS_DRST	800 mA

The value of 800 mA for these pins relates to the peak current through the inductor due to the nature of the switching regulator architecture. The DC current for these paths will be closer to the load current drawn by the DMD.

The high current LED gate drive pins consist of the following pins of the TPS99000-Q1:

Table 6. TPS99000-Q1 High Current LED Gate Driver Pins

PIN	NAME	PEAK BOARD CURRENT
42	DRVR_PWR	1 A
43	S_EN1	1 A
44	S_EN2	1 A
45	R_EN	100 mA
46	G_EN	100 mA
47	B_EN	100 mA
48	VSS_DRVR	1 A

Again, these values are for peak currents. In a typical application, these signals will be driven at a relatively low average frequency, about 10 kHz. Assuming a FET gate capacitance of 2 nF and that the FETS are driven at 6 V, the magnitude of the DC current draw of these signals is approximately:

$$I = 2 \times C \times deltaV \times f = 2(2\ nF)(6\ V)(10\ kHz) = 240\ \mu A \quad (1)$$

For the power and ground signals, this number should be multiplied by the number of active FETs, giving a value around 1.25 mA.

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In addition to these high current signals that are driven by the TPS99000-Q1, the LED driver electronics will likely have other circuits which handle the high currents required by the LEDs. These currents may be as high as 6 A and therefore will also require special consideration by the layout engineer. As a guide for the PCB trace width requirements, the reader is referred to TI's Application Note (SLUA366). The PCB trace widths used in TI's design were:

Table 7. PCB Trace Widths

SIGNAL GROUP	PCB TRACE WIDTH
DMD Regulator	10 mils
Gate Drivers	5 mils
LED Driver	200 mils minimum, but maximize where possible to decrease power loses

10.1.2 Sensitive Analog Signals

The following signals are analog inputs to TPS99000-Q1. Most of these analog inputs are DC levels and are somewhat insensitive to noise, but others are part of the real-time color control algorithm of the TPS99000-Q1 and therefore must be kept immune from noise injection from other signals. The list of analog input pins is as follows:

Table 8. TPS99000-Q1 Analog Input Pins

PIN	NAME	SIGNAL TYPE
70	TIA_PD2	Real-time
73	TIA_PD1	Real-time
82	LS_SENSE_N	Real-time
83	LS_SENSE_P	Real-time
85	ADC_IN1	Real-time
86	ADC_IN2	DC
88	ADC_IN3	DC
90	ADC_IN4	DC
92	ADC_IN5	DC
93	ADC_IN6	DC
94	ADC_IN7	DC
96	V3P3V	DC
97	V1P8V	DC
98	V1P1V	DC

In particular, the photodiode inputs TIA_PD1 and TIA_PD2 are especially sensitive to noise as they are inputs to very high gain amplifiers. It is recommended to shield these signals from noise with a ground trace next to the signal.

10.1.3 High Speed Digital Signals

The TPS99000-Q1 has three serial interfaces that are used to transmit data into and out of the device. All these of these interfaces have a maximum clock speed of 30 MHz. In order to help prevent against high levels of EMI emissions, these signals should be laid out with impedance matched, low inductance traces. In particular, the three clocks for these interfaces should be low inductance, and if a cable or a connector is used, the clock signal should be adjacent to the ground signal return.

Table 9. SPI1 Interface from DLPC230-Q1 to TPS99000-Q1

PIN	NAME	FUNCTION
27	SPI1_CLK	Clock (30 MHz)
28	SPI1_SS_Z	Slave Select
29	SPI1_DOUT	Data
30	SPI1_DIN	Data

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Table 10. SPI2 Interface from Customer MCU to TPS99000-Q1

PIN	NAME	FUNCTION
31	SPI2_DIN	Data
32	SPI2_DOUT	Data
33	SPI2_SS_Z	Slave Select
34	SPI2_CLK	Clock (Up to 30 MHz)

Table 11. ADC3 Interface from DLPC230-Q1 to TPS99000-Q1

PIN	NAME	FUNCTION
4	ADC_MISO	Data
5	ADC_MOSI	Data
17	SEQ_CLK	Clock (30 MHz)

To avoid crosstalk, a PCB trace spacing requirement is suggested, such as the “3 W rule” which specifies that if the trace width is 5 mils, then traces should be spaced out at least 15 mils from center to center. On TI’s PCB design, the typical trace spacing was 20 mils.

As explained in the *Discontinuous Mode Operation* section, the COMPOUT signal indicates to the DLPC230-Q1 that the discontinuous mode light pulses have been completed. It is critical that this signal has a fast response time in order to create small light pulses. For this reason, it is recommended that this signal has a limited trace capacitance, as mentioned in Table 12.

Table 12. Trace Capacitance

PIN	NAME	PARAMETER	TYP	MAX	UNIT
12	COMPOUT	Trace capacitance	20	50	pF

10.1.4 High Power Current Loops

Due to the architecture of switched mode power supplies used to power the LED driver, there exist several current loops which can create interference. The best way to mitigate the effects of these loops is to minimize the area. Since the location of these loops is dependent on the LED drive architecture, the reader is referred to the data sheets of those parts for specific layout recommendation guidelines.

However, the TPS99000-Q1 does add an additional current loop which is specific to how it enables the LEDs in low brightness conditions. When operating the TPS99000-Q1 in discrete pulsed mode to achieve low light levels of LEDs, current flows through a shunt FET in the LED driver, creating a current loop which can inject noise into other circuits. The current loop is shown in Figure 51.

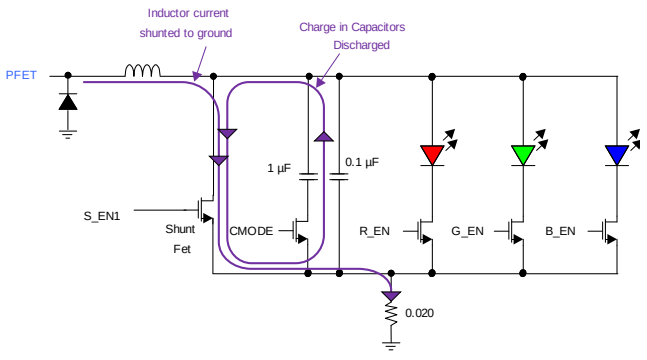

Figure 51. Discontinuous Mode Current Loop

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Here, the net LED_COMMON_ANODE is at the forward voltage of the LED when it is conducting current, and LOW_SIDE_SENSE is at near ground potential. When forming pulses in discrete pulsed mode, the S_EN1 FET redirects the current from the LED, causing it to turn off quickly. This has the added effect of discharging the 1 µF capacitor, creating a brief, high current loop consisting of the S_EN1 FET, the CMODE FET, and the 1 µF capacitor. There is also a secondary loop created by the S_EN1 FET and the 0.1 µF capacitor. This set of components should be placed in a way to keep these loops small. One such possible placement is shown in Figure 52.

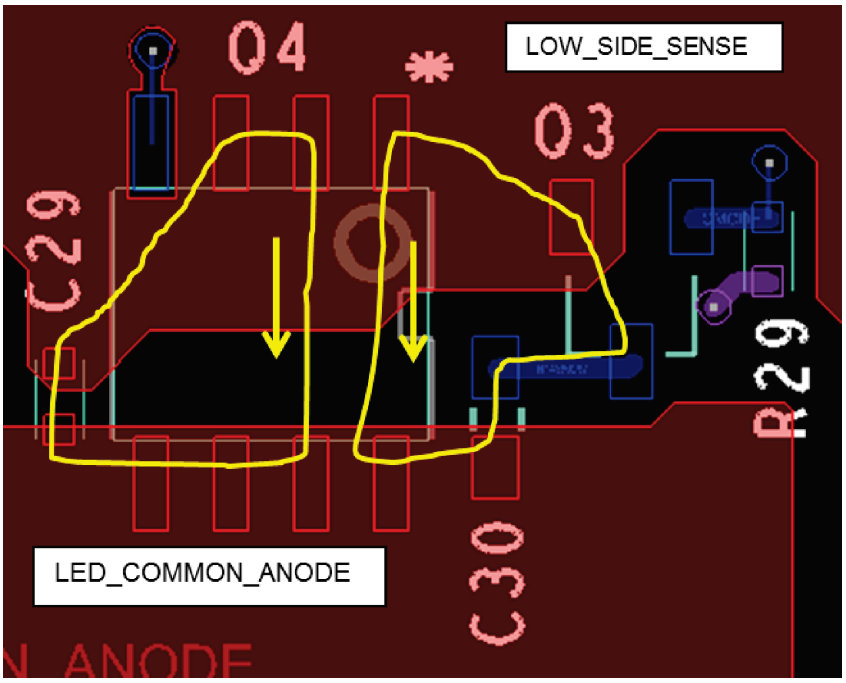

Figure 52. High Power Layout

10.1.5 Kelvin Sensing Connections

There are many places in the system design where the current through a signal path is measured by use of a sense resistor in series with the signal path. In these cases, the resistor should be connected by use of a “Kelvin” connection, or a “Force-Sense” connection. This means that two connections are made to the resistor that carry the high level of current, and two connections are made separately to measure the voltage across the resistor. This prevents the sense lines from being affected by the extra resistance of the copper traces, and makes the measurement more accurate. An example of the “Force-Sense” connection is shown in Figure 53.

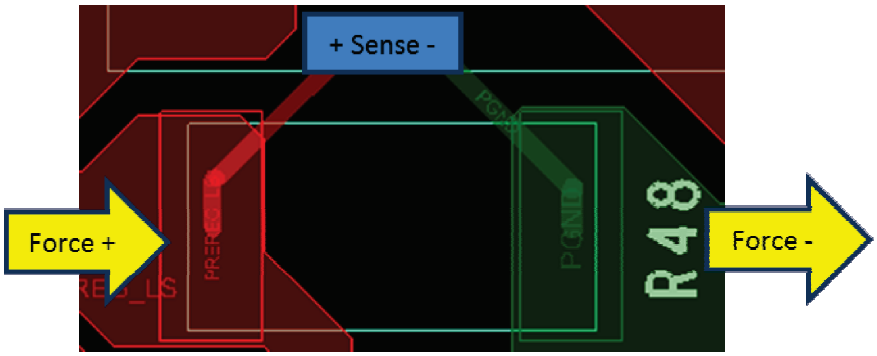

Figure 53. Kelvin Sensing Layout

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The TPS99000-Q1 uses a sense resistor to measure the current delivered to the LEDs. These differential sense lines are the inputs to the part LS_SENSE_P and LS_SENSE_N. It is important to notice that although LS_SENSE_N may be electrically connected to ground by the netlist, this signal must be routed as a separate trace to prevent it from being affected by changes in the ground plane.

10.1.6 Ground Separation

Separated ground planes are good for isolating noise from different parts of the circuit to other. However, when designing with separate ground planes, one must be careful of how the signals are routed to avoid large inductive loops. If separate ground planes are used, TI recommends the following ground connections to the TPS99000-Q1. In addition, the grounds should be connected electrically by a via or 0 Ω resistor. If a unified ground plane is used, the following can be used as a guideline for which groups of signals should be routed apart from other signals.

Table 13. TPS99000-Q1 Ground Separation

PIN	NAME	GROUND
13, 35	VSS_IO	Digital
24	DVSS	Digital
25, 60, 75, 99	PBKG	Analog
48	VSS_DRVR	Power
53	DRST_PGND	Power
56	VSS_DRST	Power
66	GND_LDO	Analog
71, 72	VSS_TIA	Analog
78, 100	AVSS	Analog
81, 84, 87, 89, 91	VSSL_ADC	Analog
Thermal Pad	DAP	Analog

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Trademarks

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11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTP99000ACPZPR	ACTIVE	HTQFP	PZP	100		TBD	Call TI	Call TI	-40 to 105		Samples
TPS9900TPZPQ1	ACTIVE	HTQFP	PZP	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS9900TPZP	Samples
TPS9900TPZPRQ1	ACTIVE	HTQFP	PZP	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS9900TPZP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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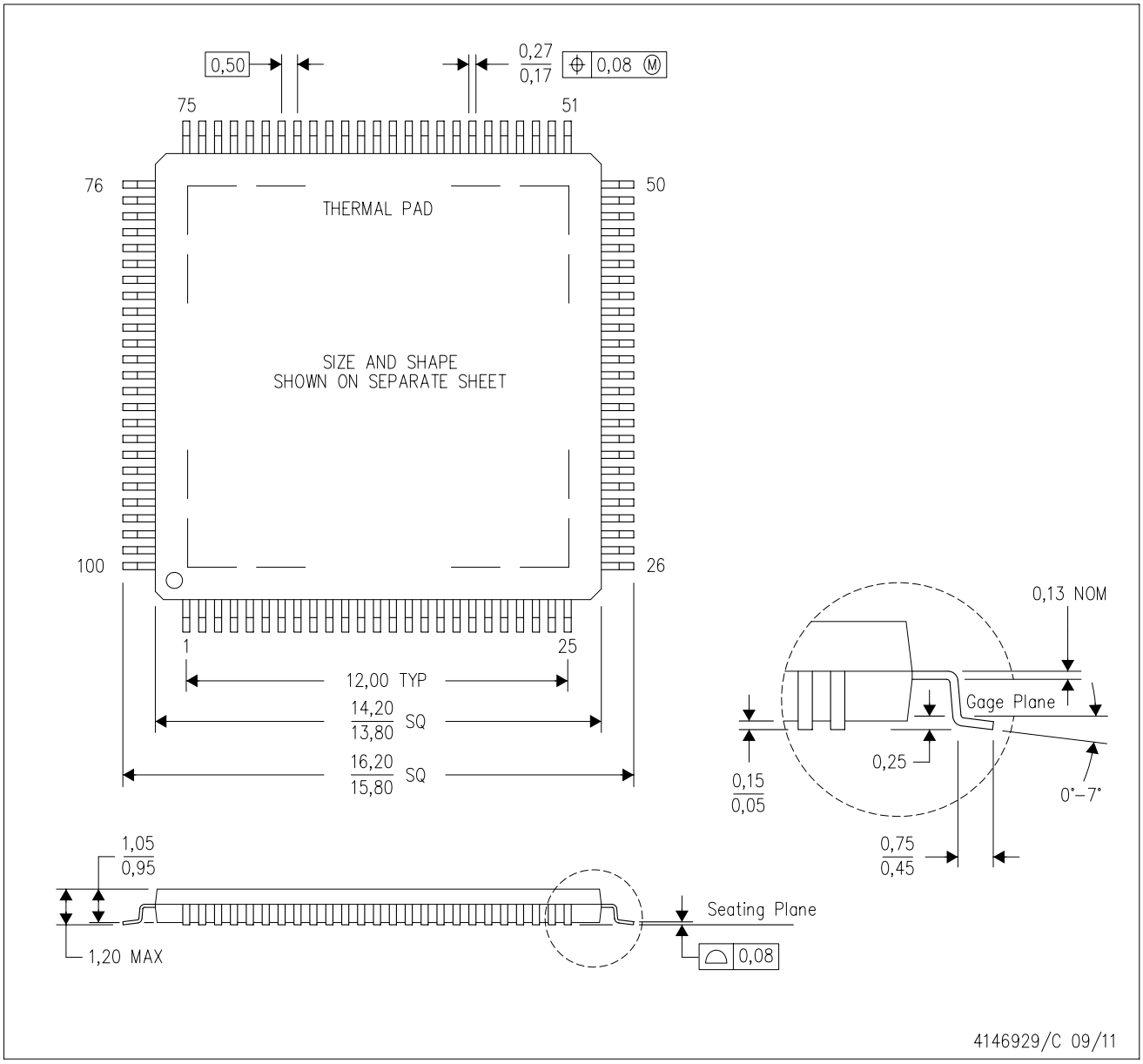
PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

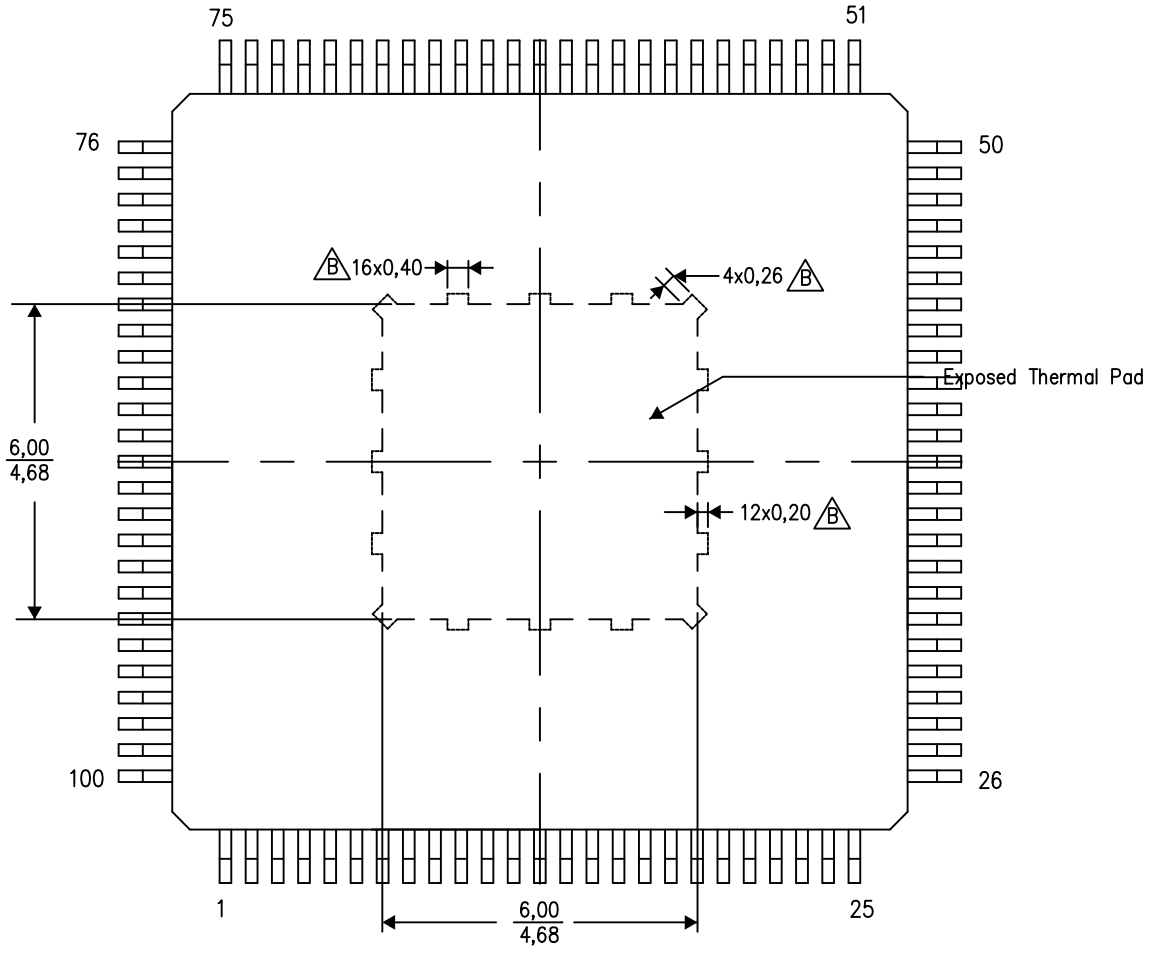
PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206333–6/L 05/14

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

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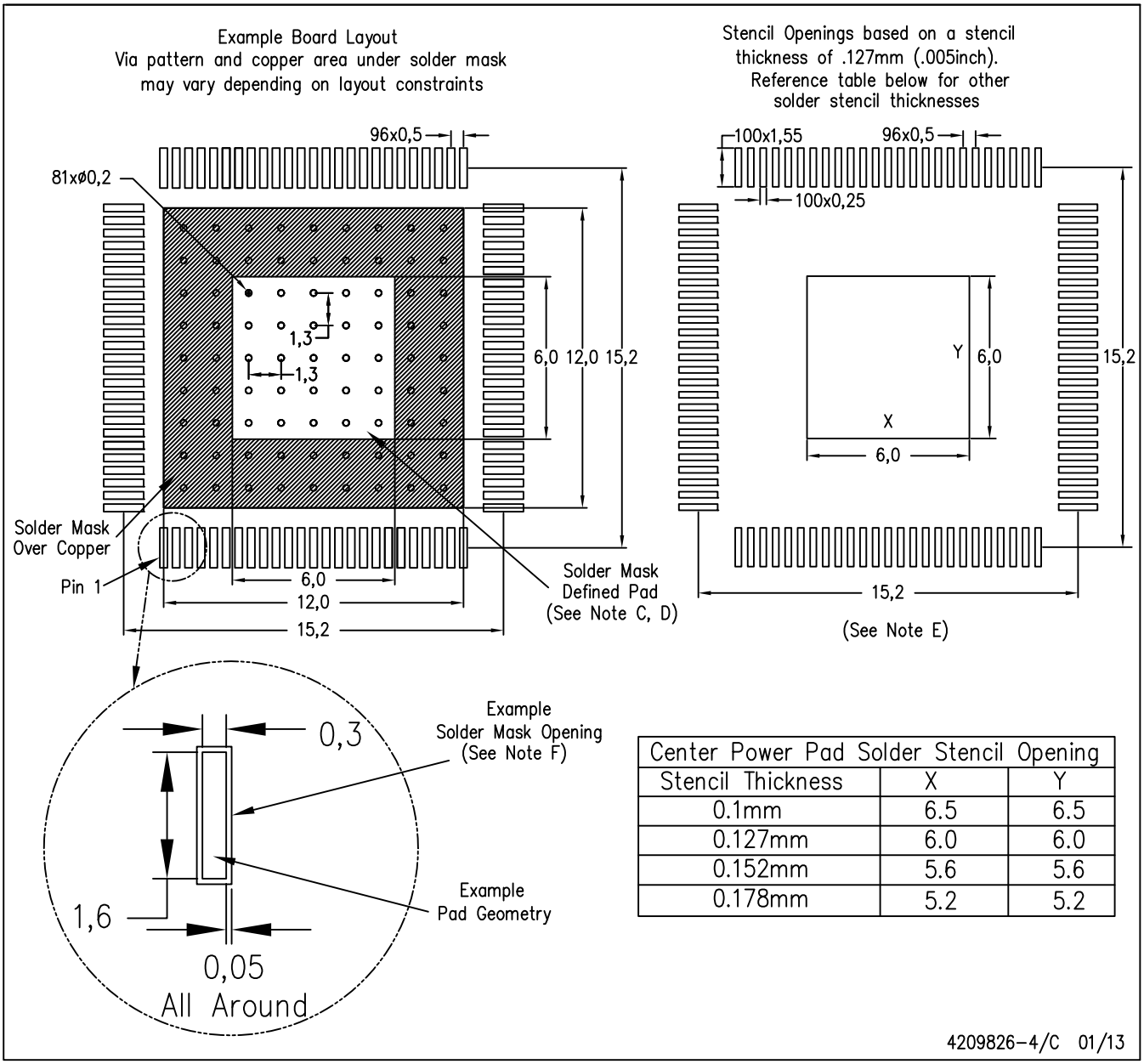
PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.5	6.5
0.127mm	6.0	6.0
0.152mm	5.6	5.6
0.178mm	5.2	5.2

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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