GENERAL PURPOSE LED LIGHTING PWM CONTROLLER

Check for Samples: TPS92001, TPS92002

FEATURES

- **Ideal for Single Stage Designs**
- **Supports Isolated and Non-Isolated Topologies**
- **Phase-Cut TRIAC Dimmable**
- **Few External Components Mode Operation**
- **Wide Duty Cycle Range for Wide-Input Voltage or Dimming Range**
- **Convenient 5-V Reference Output**
- **Undervoltage Lockout for Safe Operation**
- **Operation to 1-MHz**
- **0.4-A Source/0.8-A Sink FET Driver**
- **Low 100-µA Startup Current**

APPLICATIONS

- **Residential LED Lighting Drivers for A19 E12/E26/27, GU10, MR16, PAR30/38 Integral Lamps**
- **Drivers for Wall Sconces, Pathway Lighting and Overhead Lighting**
- **Drivers for Wall Washing, Architectural and Display Lighting**

DEVICE NUMBER	TURN-ON THRESHOLD (V)	TURN-OFF THRESHOLD (V)
TPS92001	10	8
TPS92002	15	

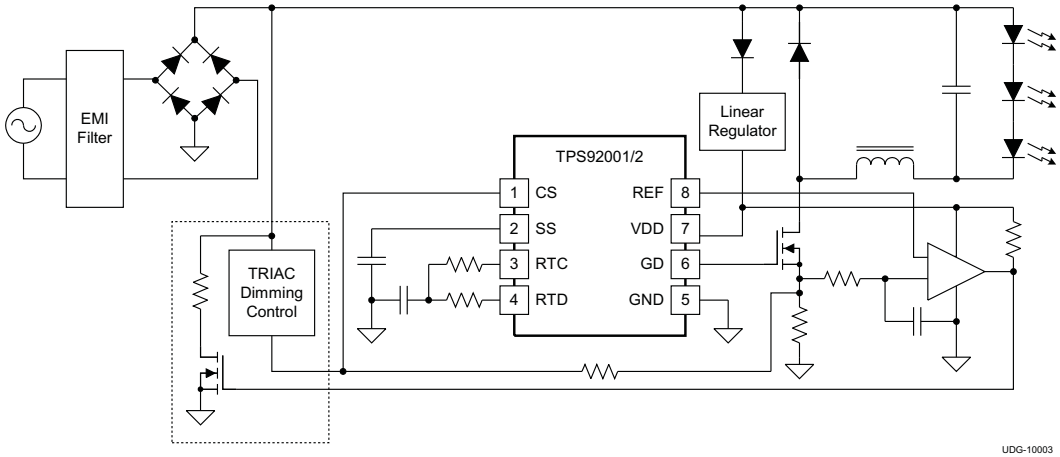
DESCRIPTION

The TPS92001/2 family of general LED lighting PWM controllers contains control and drive circuitry required for off-line isolated or non-isolated LED lighting applications.

The controllers can support Phase Cut TRIAC dimming with minimal external components. The controllers can also be implemented for stage conversion where the power factor (PF) exceeds regulatory requirements for lighting. These controllers also have an accessible 5-V reference that could be used to power a microcontroller or other low power peripheral components. The controllers operate in fixed frequency current mode switching with minimal external parts count. Internally implemented circuits include undervoltage lockout featuring startup current less than 100 µA, logic to ensure latched operation, a PWM comparator, and a totem pole output stage to sink or source peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state. Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor.

The TPS92001/2 family also features full cycle soft start. The family offers UVLO thresholds and hysteresis levels for off-line and DC-to-DC systems. The TPS92001/2 is offered in the 8-pin MSOP (DGK) and 8-pin SOIC (D) packages. The small MSOP package makes the device ideally suited for applications where board space and height are at a premium.

SIMPLIFIED APPLICATION



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		RANGE	UNIT
Input voltage range	VDD	19	V
	SS	-0.3 to REF + 0.3	
	RTC, RTD	-0.3 to REF + 0.3	
Continuous input current	I_{REF}	-15	mA
	I_{VDD}	25	
Output current	I_{GD} (tpw < 1 µs and Duty Cycle < 10%)	-0.4 to 0.8	A
Operating junction temperature	T_J	−55 to +150	°C
Storage temperature	T_{stg}	−65 to +150	
Lead temperature	Soldering, 10 s	+300	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
VDD	Input voltage		21	V
I_{GD}	Output sink current	0		A
T_J	Operating junction temperature	–40	105	°C

DISSIPATION RATINGS

PACKAGE	θ_{JA}, THERMAL IMPEDANCE JUNCTION-TO-AMBIENT, NO AIRFLOW (°C/W)	θ_{JB}, THERMAL IMPEDANCE JUNCTION-TO-BOARD, NO AIRFLOW (°C/W)	T_A = 25°C POWER RATING (mW)	T_A = 85°C POWER RATING (mW)	T_B = 85°C POWER RATING (mW)
SOIC-8 (D)	165(1)	55	606(2)	242(2)	730(2)(3)
MSOP-8 (DGK)	181(1)	62	552(2)	221(2)	664(3)(2)

(1) Tested per JEDEC EIA/JESD51-1. Thermal resistance is a function of board construction and layout. Air flow will reduce thermal resistance. This number is included only as a general guideline; see TI document SPRA953 *IC Package Thermal Metrics*.
(2) Maximum junction temperature T_J, equal to 125°C.
(3) Thermal resistance to the circuit board is lower. Measured with standard single-sided PCB construction. Board temperature, T_B, measured approximately 1 cm from the lead to board interface. This number is provided only as a general guideline.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model		2000	V
CDM		1500	

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ELECTRICAL CHARACTERISTICS

V_{VDD} = 12 V, C_{REF} = 0.47-µF, $T_A = T_J$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION							
VDD	Supply clamp		I_{VDD} = 10 mA	16	17.5	19	V
I_{VDD}	Supply current		No Load		600	900	µA
I_{VDD}	Supply current startup(1)				110		µA
	Supply current standby	TPS92001	V_{VDD} = Start threshold – 300 mv		110	125	µA
		TPS92002			130	170	
UNDERVOLTAGE LOCKOUT SECTION							
	Start threshold	TPS92001		9.4		10.4	V
		TPS92002		14.0		15.6	
	UVLO hysteresis	TPS92001		1.65			
		TPS92002		6.2			
VOLTAGE REFERENCE SECTION							
	Output voltage		I_{REF} = 0 mA	4.75	5	5.25	V
	Line regulation		10 V ≤ V_{VDD} ≤ 15 V		2		mV
	Load regulation		0 mA ≤ I_{REF} ≤ 5 mA		2		mV
COMPARATOR SECTION							
I_{CS}	Current sense		Output OFF		-100		nA
	Comparator threshold			0.9	0.95	1	V
GD_{DLY}	GD propagation delay (No Load)		0.8 V ≤ V_{CS} ≤ 1.2 V at T_R = 10 ns		50	100	ns
SOFT START SECTION							
I_{SS}	Soft-start current		V_{VDD} = 16 V, V_{SS} = 0 V, -40°C ≤ T_A ≤ 85°C	-4.9	-7.0	-9.1	µA
			V_{VDD} = 16 V, V_{SS} = 0 V, -40°C ≤ T_A ≤ 85°	-4.9	-7.0	-10.0	µA
V_{SS}	Low-level output voltage		V_{VDD} = 7.5 V, I_{SS} = 200 µA			0.2	V
	Shutdown threshold			0.44	0.48	0.52	V
OSCILLATOR SECTION							
	Switching frequency		R_{RTC} = 10 kΩ, R_{RTD} = 4.32 kΩ, C_{CT} = 820pF	90	100	110	kHz
	Frequency change with voltage		10 V ≤ V_{VDD} ≤ 15 V		0.1		%/V
$V_{CT(peak)}$	Timing capacitor peak voltage				3.33		V
$V_{CT(valley)}$	Timing capacitor valley voltage				1.67		V
$V_{CT(p-p)}$	Timing capacitor peak-to-peak voltage			1.54	1.67	1.80	V
GATE DRIVE SECTION							
	Power driver V_{SAT} low		I_{GD} = 80 mA (dc)		0.8	1.5	V
	Power driver V_{SAT} high		I_{GD} = -40 mA (dc), (V_{VDD} – V_{GD})		0.8	1.5	V
	Power driver low-voltage during UVLO		I_{GD} = 20 mA (dc)			1.5	V
D_{MIN}	Minimum duty cycle		V_{CS} = 2 V		0%		
D_{MAX}	Maximum duty cycle				70%		
t_{RISE}	Rise Time		C_{GD} = 1nF		35		ns
t_{FALL}	Fall Time		C_{GD} = 1nF		18		ns

(1) Specified by design. Not production tested.

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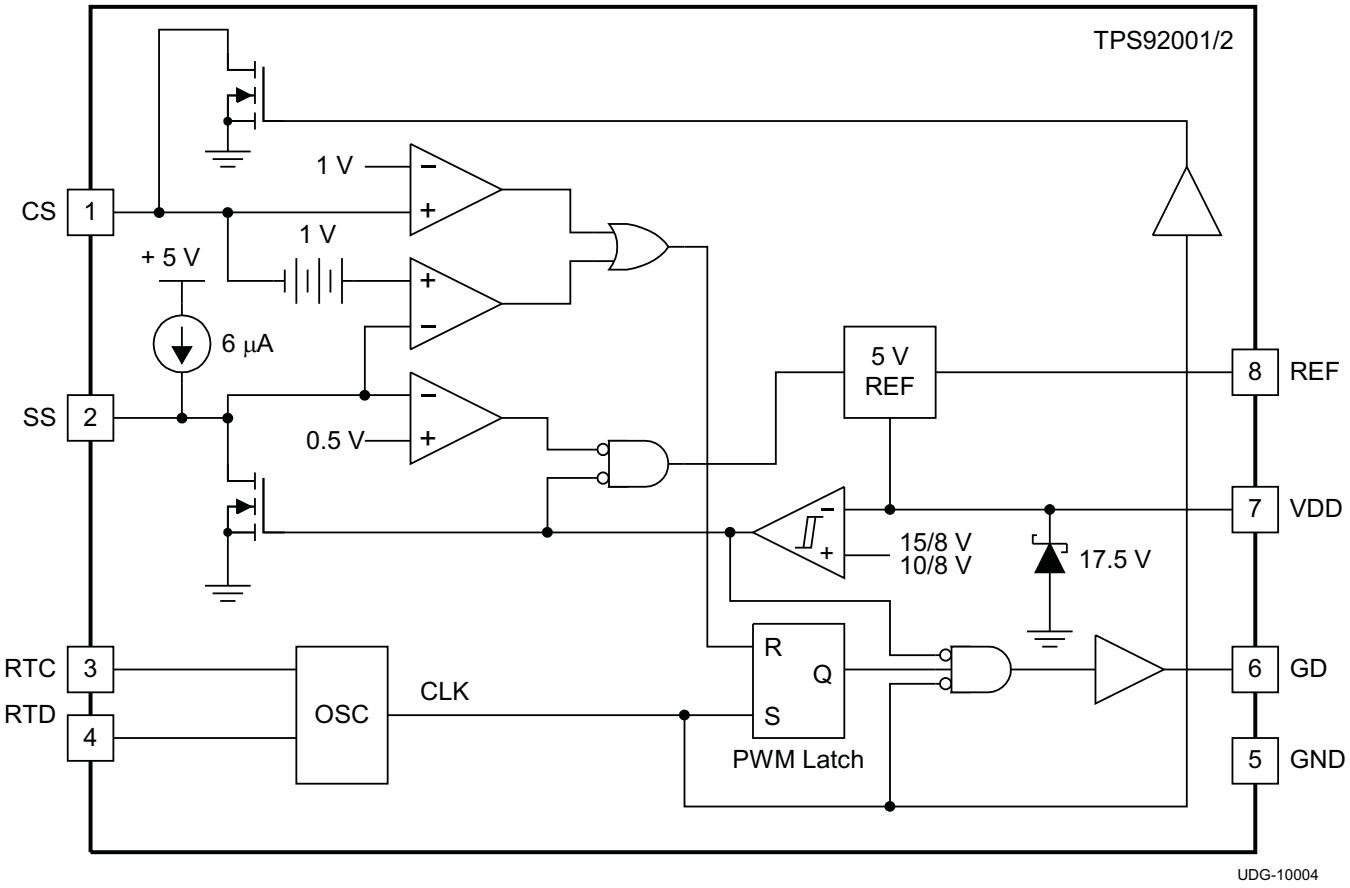
FUNCTIONAL BLOCK DIAGRAM



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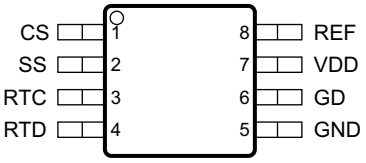
ORDERING INFORMATION

OPERATING TEMPERATURE RANGE T_A	PACKAGE	THRESHOLD		ORDERABLE DEVICE NUMBER	PINS	TRANSPORT MEDIA	QUANTITY
		TURN-ON	TURN-OFF				
–40°C to 85°C	Plastic Small Outline (MSOP)	10	8	TPS92001DGK	8	Tube	80
				TPS92001DGKR		Tape and Reel	2500
	Plastic Small Outline (SOIC)			TPS92001D		Tube	75
				TPS92001DR		Tape and Reel	2500
	Plastic Small Outline (MSOP)	15		TPS92002DGK		Tube	80
				TPS92002DGKR		Tape and Reel	2500
	Plastic Small Outline (SOIC)			TPS92002D		Tube	75
				TPS92002DR		Tape and Reel	2500

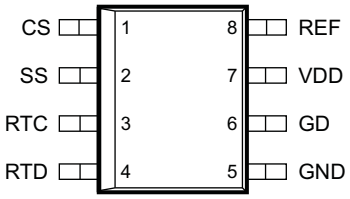
DEVICE INFORMATION

TPS92001/2

DGK Package
(Top View)



D Package
(Top View)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
CS	1	I	This pin is the summing node for current sense feedback, voltage sense feedback (by optocoupler) and slope compensation. Slope compensation is derived from the rising voltage at the timing capacitor and can be buffered with an external small signal NPN transistor. External high frequency filter capacitance applied from this node to GND is discharged by an internal 250ohm on resistance NMOS FET during PWM off time. It offers effective leading edge blanking, with the delay set by the RC time constant of the feedback resistance from current sense resistor to CS input and the high frequency filter capacitor at this node to GND.
GND	5	–	Reference ground and power ground for all functions.
GD	6	O	This pin is the high current power driver output. A minimum series gate resistor of 3.9 Ω is recommended to limit the gate drive current when operating with high-bias voltages.
REF	8	O	The internal 5-V reference output. This reference is buffered and is available on the REF pin. The REF pin should be bypassed with a 0.47-µF ceramic capacitor to GND.
RTC	3	I	This pin connects to timing resistor R_{RTC} , and controls the positive ramp (rise) time of the internal oscillator (see Equation 1). The positive threshold of the internal oscillator is sensed through inactive timing resistor R_{RTD} which connects to pin RTD and timing capacitor, C_{CT}. $t_{RISE} = 0.74 \times (C_{CT} + 27\,pF) \times R_{RTC}$ (1)
RTD	4	I	This pin connects to timing resistor RTD and controls the negative ramp (fall) time of the internal oscillator (see Equation 2). The negative threshold of the internal oscillator is sensed through inactive timing resistor R_{RTC} which connects to pin RTC and timing capacitor, C_{CT}. $t_{FALL} = 0.74 \times (C_{CT} + 27\,pF) \times R_{RTD}$ (2)
SS	2	I	This pin serves two functions. The soft start timing capacitor connects to SS and is charged by an internal 6-µA current source. Under normal soft-start, the SS pin is discharged to at least 0.4 V and then ramps positive to 1 V during which time the output driver is held low. As the SS pin charges from 1 V to 2 V, the soft-start is implemented by an increasing output duty cycle. If the SS pin is taken below 0.5 V, the output driver is inhibited and held low. The user accessible 5-V voltage reference also goes low and I_{VDD} = 100 µA
VDD	7	I	The power input connection for this device. This pin is shunt regulated at 17.5 V which is sufficiently below the voltage rating of the DMOS output driver stage. VDD should be bypassed with a 1-µF ceramic capacitor.

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APPLICATION INFORMATION

Introduction

The typical application diagrams in Figure 3 and Figure 4 show isolated and non-isolated flyback converters utilizing the TPS92001. Note that the capacitors C_{REF} and C_{VDD} are local decoupling capacitors for the reference and device input voltage, respectively. Both capacitors should be low ESR and ESL ceramic, placed as close as possible to the device pins, and returned directly to the ground pin of the device for best stability. The REF pin provides the internal bias to many of the device functions and C_{REF} should be at least 0.47-µF to prevent the REF voltage from drooping.

Current Sense (CS) Pin

In the TPS92001/2, the current regulation is obtained through the summation of the primary current sense and any slope compensation at the CS pin compared to a 1-V threshold, as shown in the FUNCTIONAL BLOCK DIAGRAM. Crossing this 1-V threshold resets the PWM latch and modulates the output driver on-time. In the absence of a CS signal, the output obeys the programmed maximum on-time of the oscillator. When adding slope compensation, it is important to use a small capacitor to AC couple the oscillator waveform before summing this signal into the CS pin. By forcing the CS node to exceed the 1-V threshold the TPS92001/2 is forced to zero percent duty cycle.

Oscillator

Equation 3 calculates the oscillator frequency setting.

$$f_{OSC} = \left(0.74 \times \left(C_{CT} + 27\,pF\right) \times \left(R_{RTC} + R_{RTD}\right)\right)^{-1} \quad (3)$$

$$D_{MAX} = 0.74 \times R_{TC} \times \left(C_T + 27\,pF\right) \times f_{OSC} \quad (4)$$

Referring to Figure 1 and the waveforms in Figure 2, when Q1 is on, C_{CT} charges via the on-resistance of the Q1 MOSFET and the RTC pin. During this charging process, the voltage of C_{CT} is sensed through the RTD pin. The S input of the oscillator latch, S_{OSC}, is level sensitive, so crossing the upper threshold (set at 2/3 VREF or 3.33 V for a typical 5.0 V reference) sets the Q output (CLK signal) of the oscillator latch high. A high CLK signal results in turning off Q1 and turning on Q2. The timing capacitor then discharges through RTD and the $R_{DS(on)}$ of Q2. C_{CT} discharges from 3.33 V to the lower threshold (set at 1/3 REF or 1.67 V for a typical 5.0-V reference) sensed through RTC. The R input to the oscillator latch, R_{OSC}, is also level sensitive and resets the CLK signal low when C_{CT} crosses the 1.67-V threshold, turning off Q2 and turning on Q1, initiating another charging cycle.

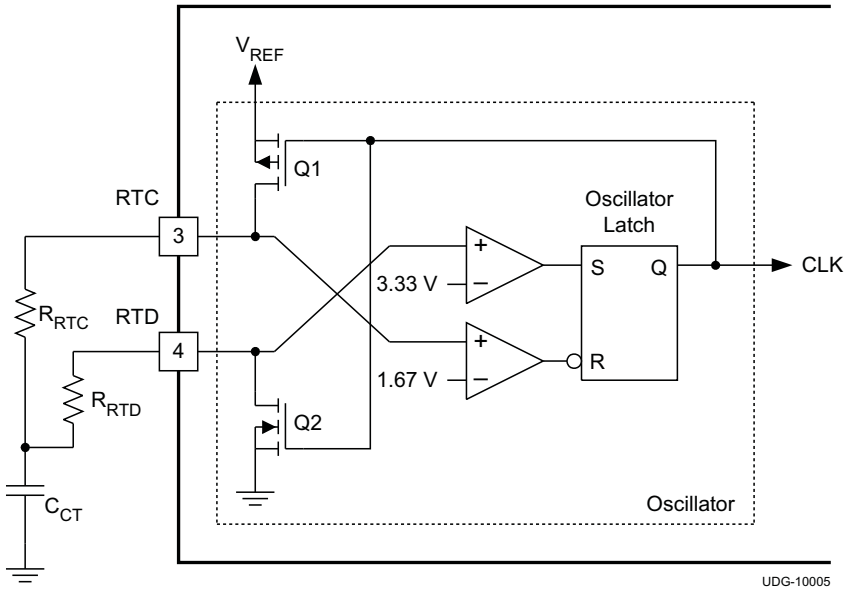

Figure 1. Oscillator Function

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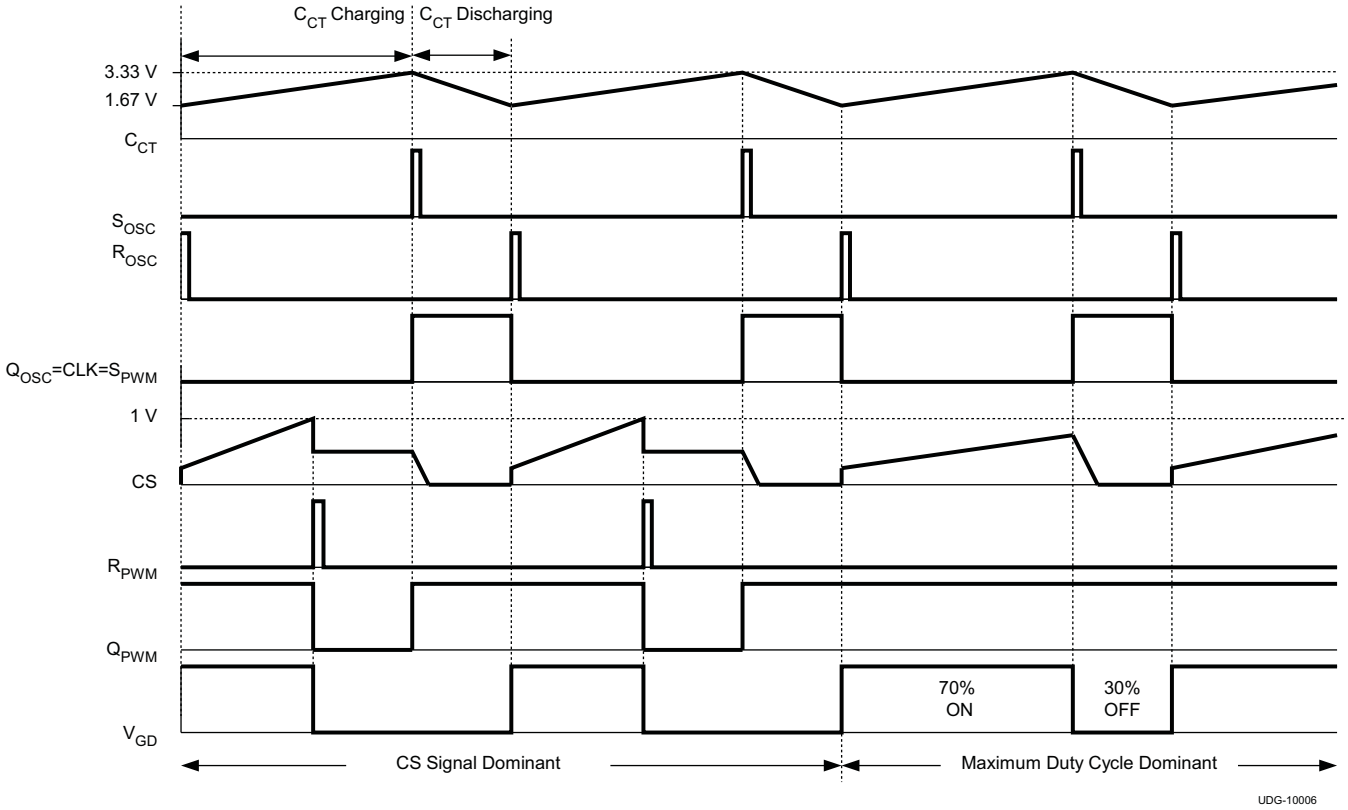

Figure 2. Oscillator Latch and PWM Latch Waveforms

Figure 2 shows the waveforms associated with the oscillator latch and the PWM latch (shown in the Typical Application Diagram). A high CLK signal not only initiates a discharge cycle for C_{CT}, it also turns on the internal N-channel MOSFET on the CS pin causing any external capacitance used for leading edge blanking connected to this pin to be discharged to ground. By discharging any external capacitor completely to ground during the external switch off-time, the noise immunity of the converter is enhanced allowing the user to design in smaller R-C components for leading edge blanking. A high CLK signal also sets the level sensitive S input of the PWM latch, S_{PWM}, high, resulting in a high output, Q_{PWM}, as shown in Figure 2. This Q_{PWM} signal remains high until a reset signal, R_{PWM} is received. A high R_{PWM} signal results from the CS signal crossing the 1-V threshold, or during soft-start or if the SS pin is disabled.

Assuming the UVLO threshold is satisfied, the GD signal of the device remains high as long as Q_{PWM} is high and S_{PWM}, also referred to as CLK, is low. The GD signal is dominated by the CS signal as long as the CS signal trips the 1-V threshold while CLK is low. If the CS signal does not cross the 1-V threshold while CLK is low, the GD signal will be dominated by the maximum duty cycle programmed by the user. Figure 2 illustrates the various waveforms for a design set up for a maximum duty cycle of 70%.

The recommended value for C_{CT} is 1 nF for frequencies in the 100 kHz or less range and smaller C_{CT} for higher frequencies. The minimum recommended values of R_{RTC} is 10 kΩ. The minimum recommended value of R_{RTD} is 4.32 kΩ. Using these values maintains a ratio of at least 20:1 between the $R_{DS(on)}$ of the internal FETs and the external timing resistors, resulting in minimal change in frequency over temperature. Because of the oscillator susceptibility to capacitive coupling, examine the oscillator frequency by looking at the common RTC-RTD-CT node on the circuit board as opposed to looking at pins 3 and 4 directly. For good noise immunity, the RTC and RTD resistors should be placed as close to pins 3 and 4 of the device as possible. The timing capacitor should be returned directly to the ground pin of the device with minimal stray inductance and capacitance.

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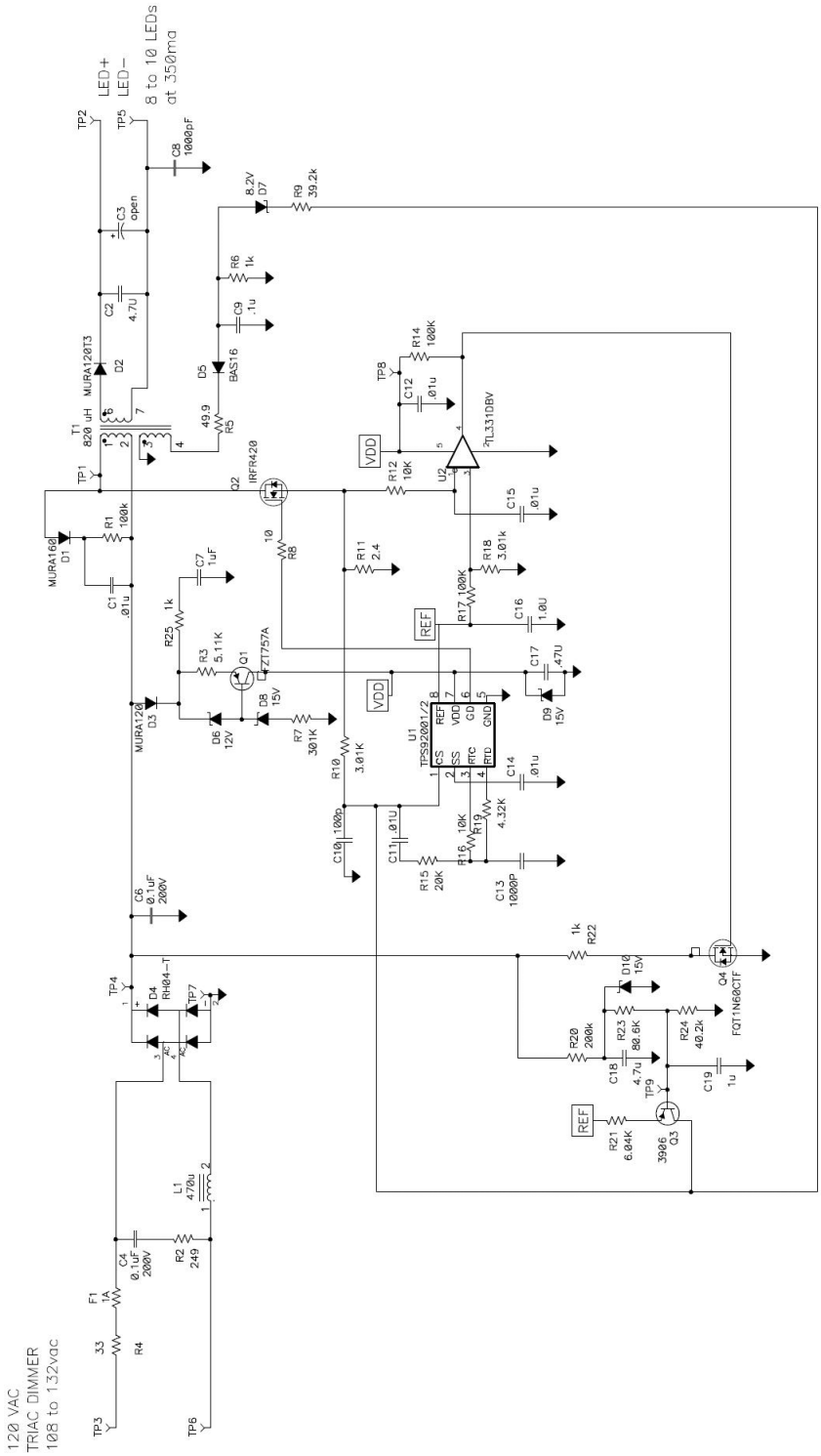

Figure 3. Isolated Flyback with TRIAC Dimming Interface

CAUTION

Do not operate the Isolated Flyback described in Figure 3 without load.

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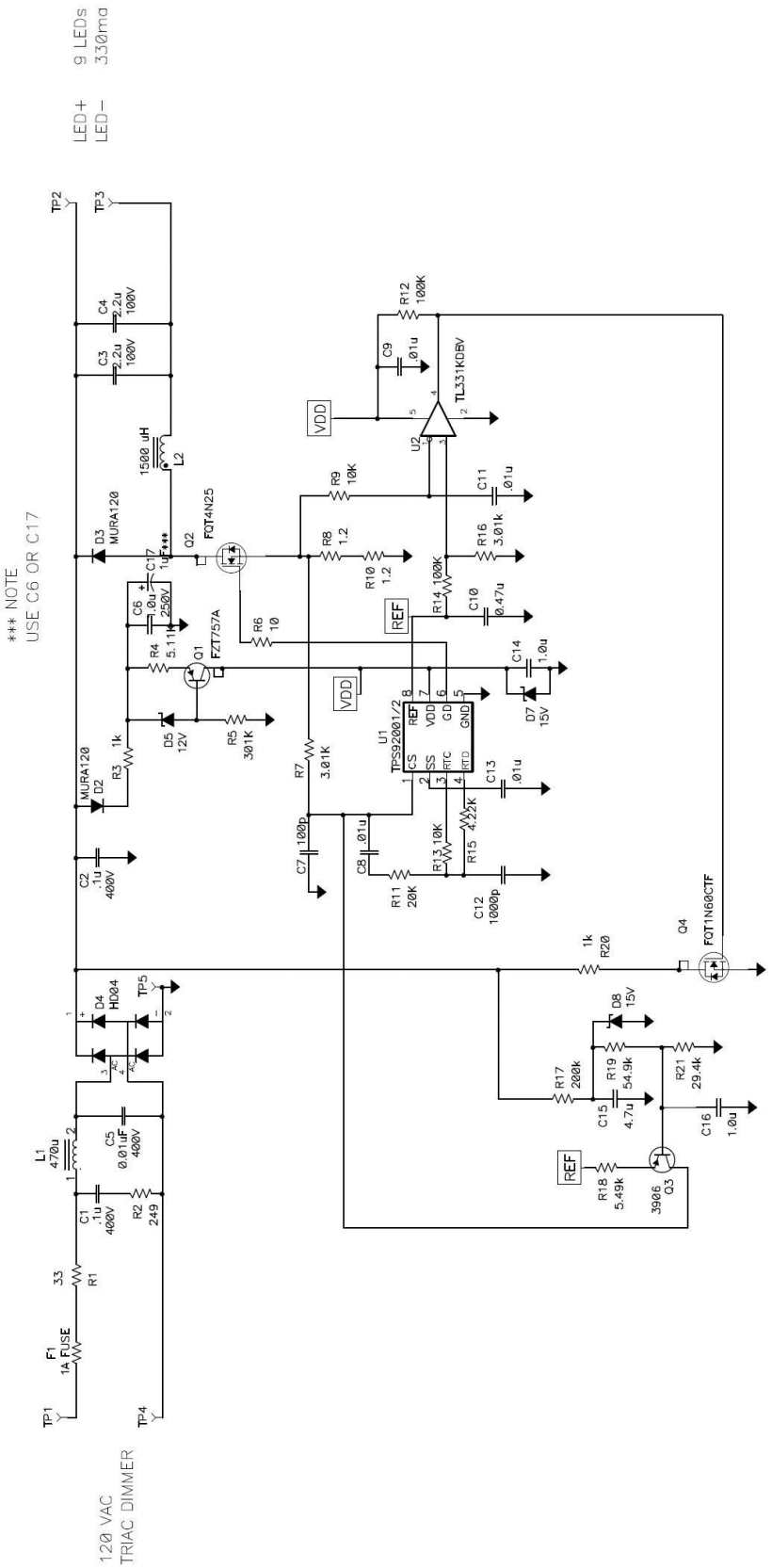

Figure 4. Low-Side (Inverted) Buck with TRIAC Dimming Interface

TYPICAL CHARACTERISTICS

VDD STANDBY CURRENT vs JUNCTION TEMPERATURE

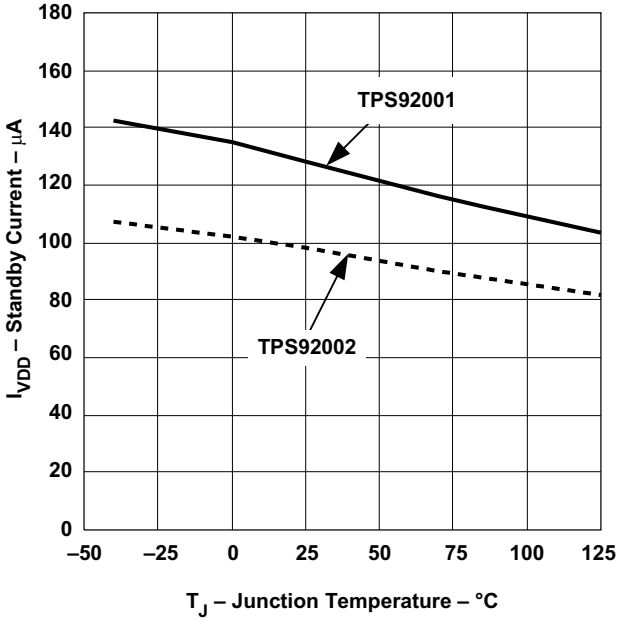

Figure 5.

UNDERVOLTAGE LOCKOUT THRESHOLD vs JUNCTION TEMPERATURE

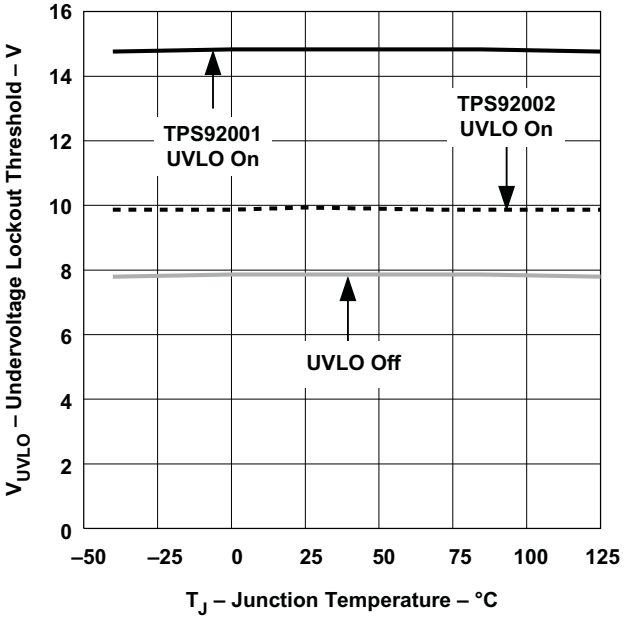

Figure 6.

OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

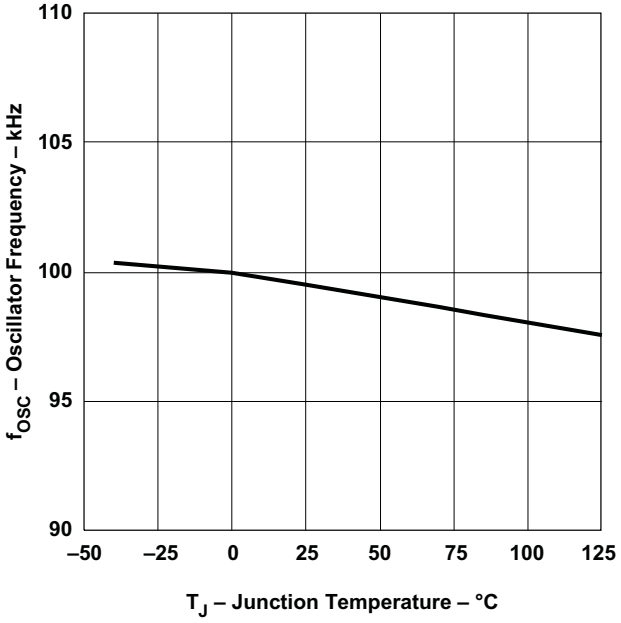

Figure 7.

OVERVOLTAGE PROTECTION THRESHOLD vs TEMPERATURE

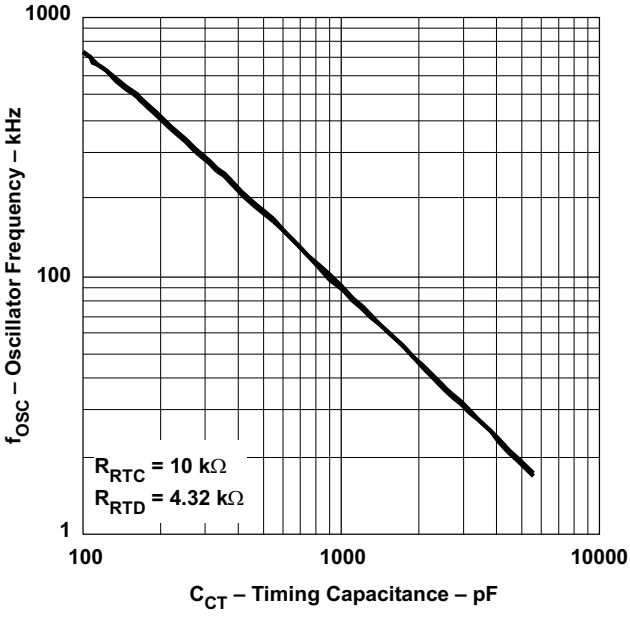

Figure 8.

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REVISION HISTORY

Changes from Original (FEBRUARY 2010) to Revision A	Page
• Changed diode direction	1
• Changed Figure 4 title	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92001D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 105	92001D	Samples
TPS92001DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	92001	Samples
TPS92001DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	92001	Samples
TPS92001DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 105	92001D	Samples
TPS92002D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 105	92002D	Samples
TPS92002DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	92002	Samples
TPS92002DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	92002	Samples
TPS92002DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 105	92002D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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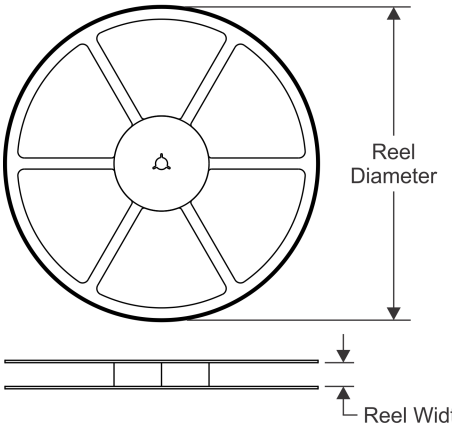
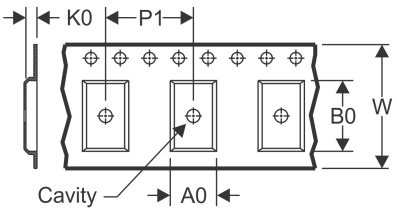
TAPE AND REEL INFORMATION

REEL DIMENSIONS

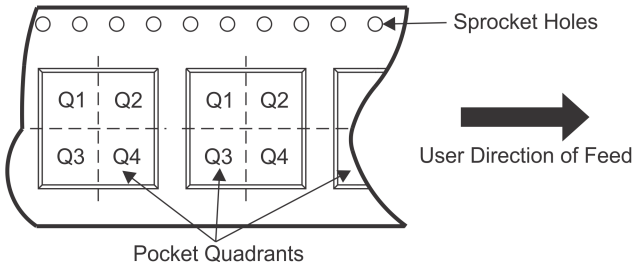


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

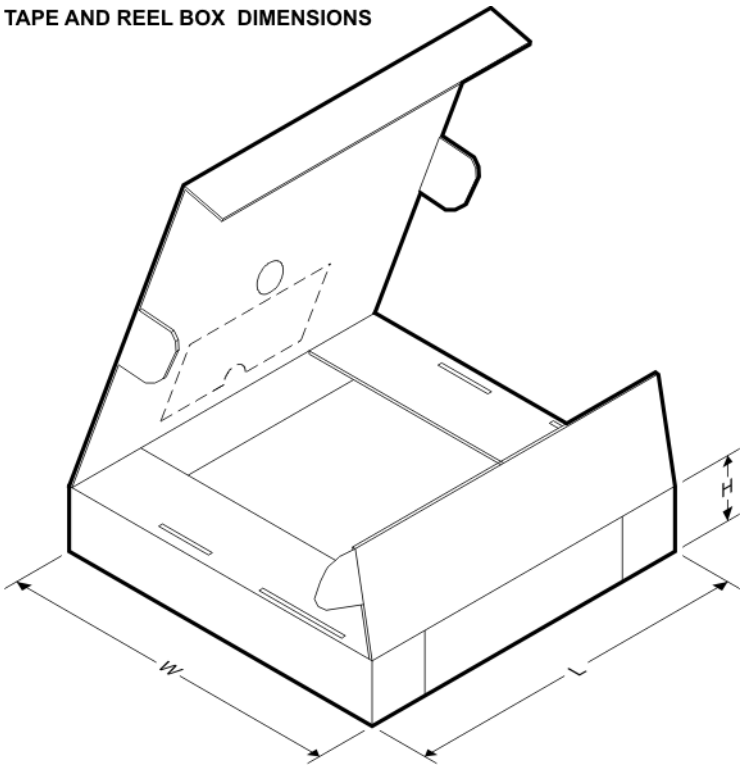
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

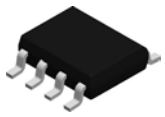
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92001DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS92001DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS92002DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS92002DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92001DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TPS92001DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS92002DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TPS92002DR	SOIC	D	8	2500	340.5	338.1	20.6

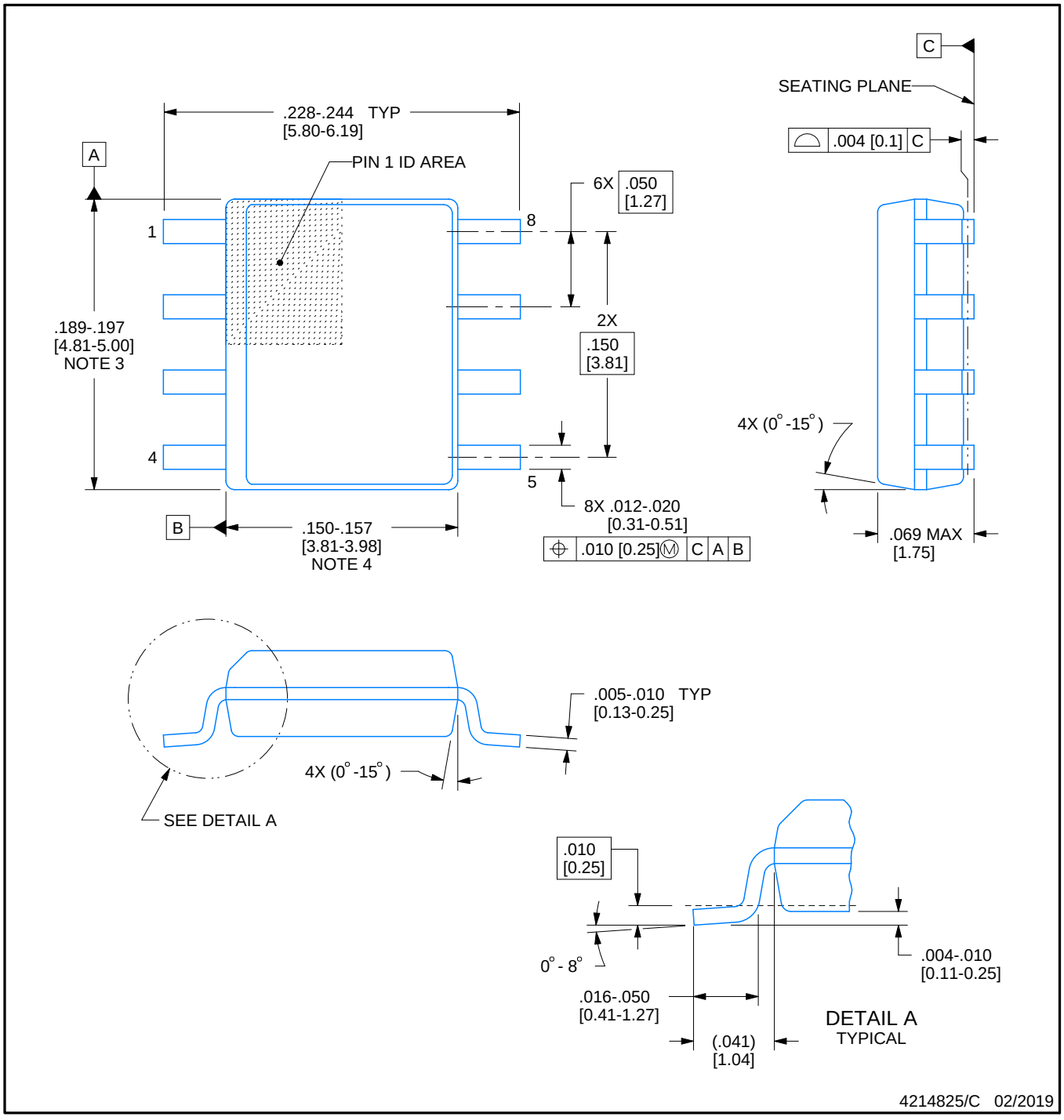


PACKAGE OUTLINE

D0008A

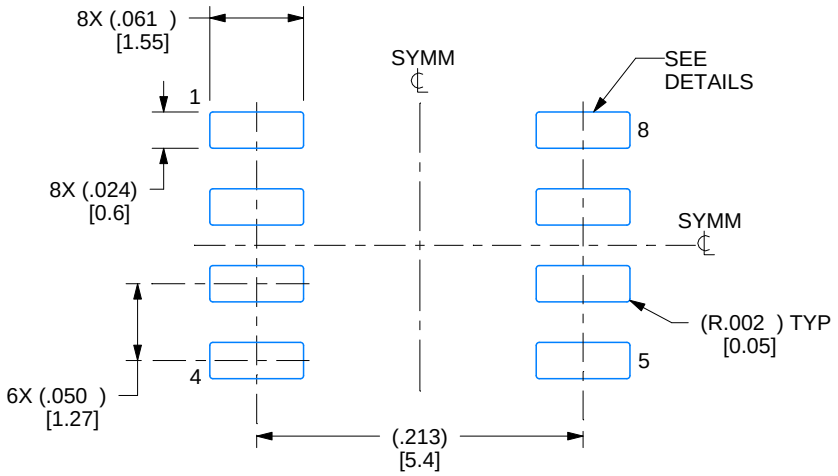
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

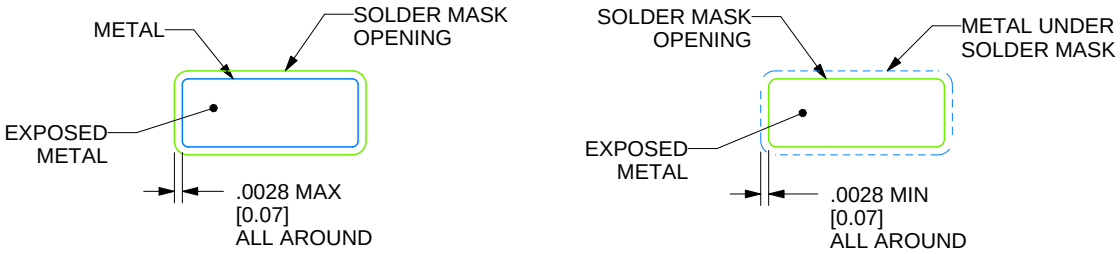


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

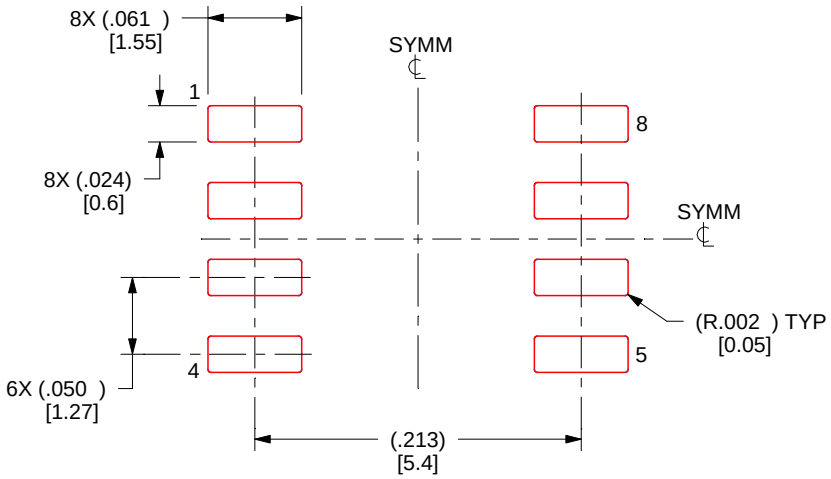
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



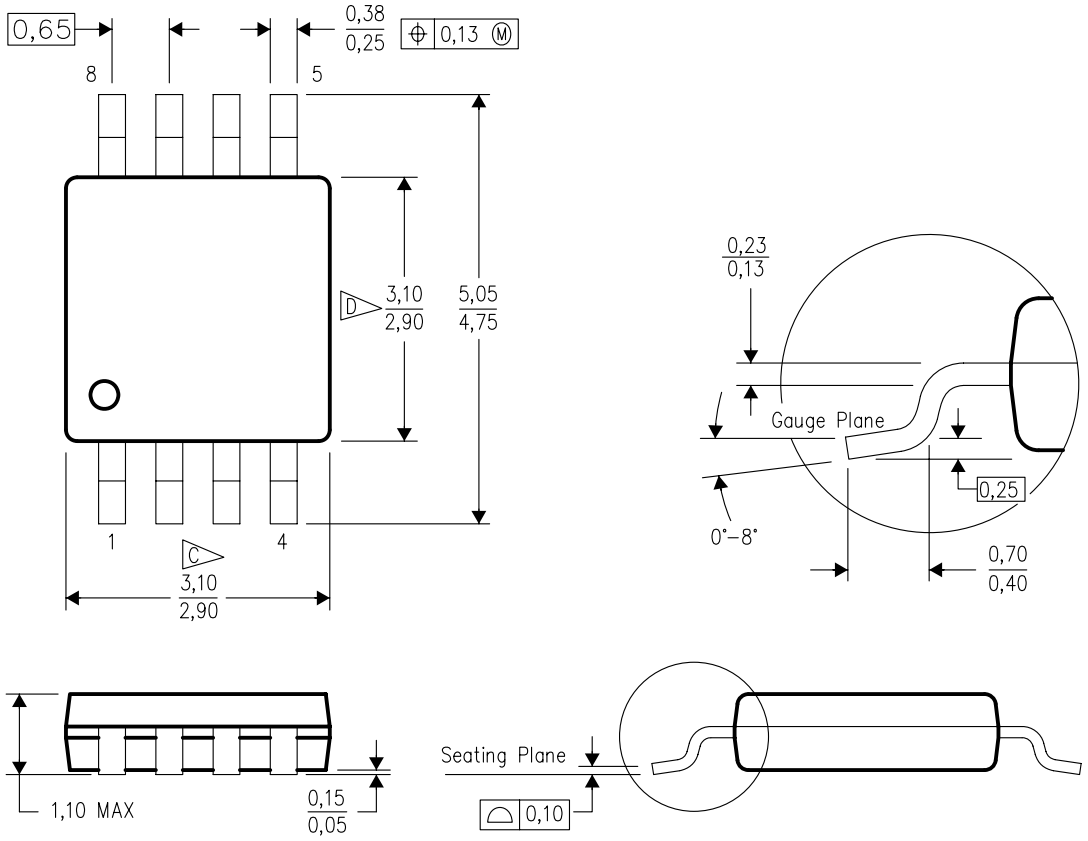
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

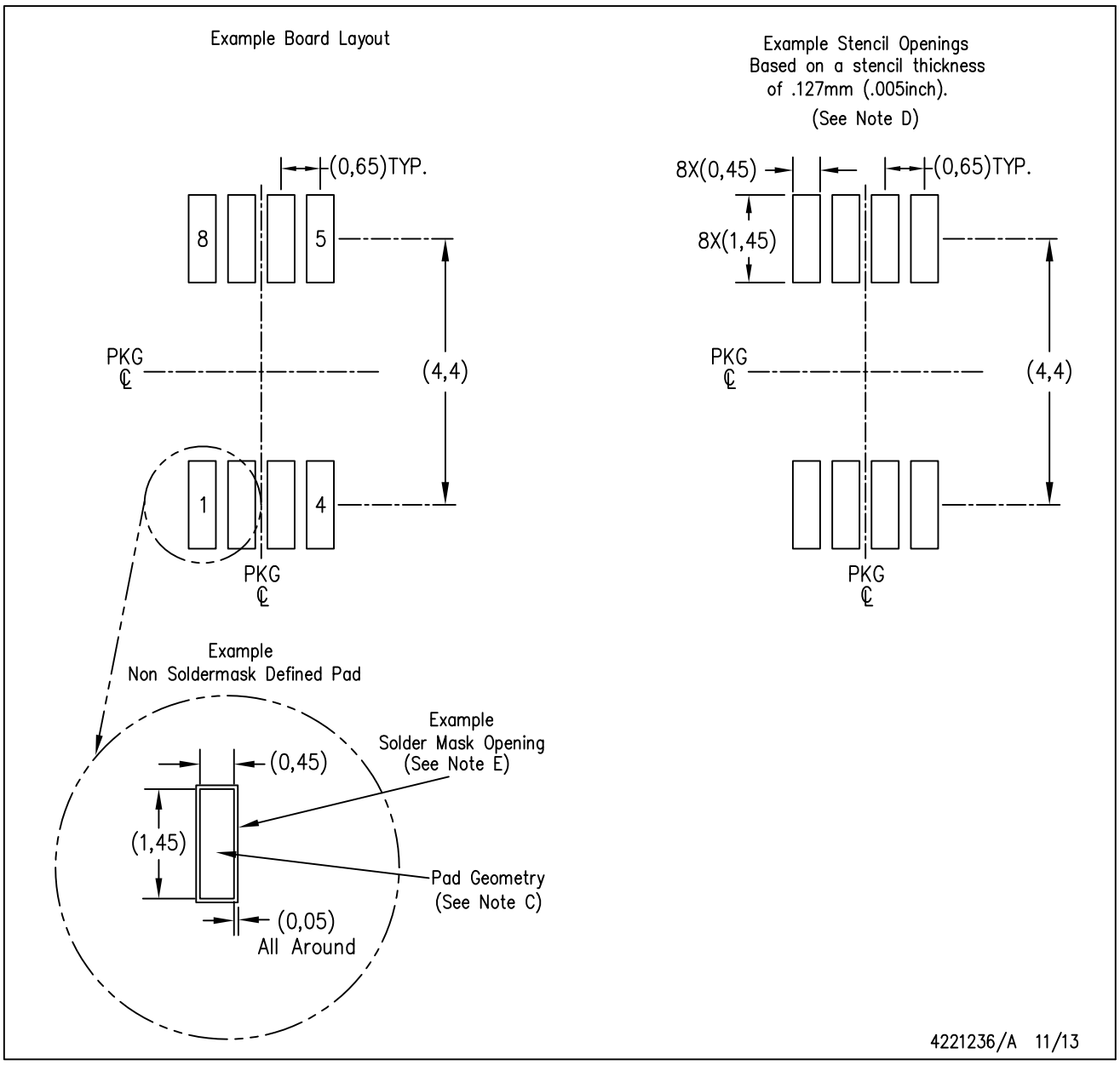
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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