

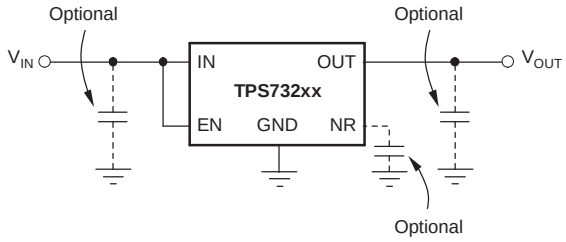
CAP-FREE NMOS 250-mA LOW DROPOUT REGULATOR WITH REVERSE CURRENT PROTECTION

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Stable with No Output Capacitor or Any Value or Type of Capacitor**
- **Input Voltage Range: 1.7 V to 5.5 V**
- **Ultralow Dropout Voltage: 40 mV Typ at 250 mA**
- **Excellent Load Transient Response—with or without Optional Output Capacitor**
- **New NMOS Topology Provides Low Reverse Leakage Current**
- **Low Noise: 30 μV_{RMS} Typ (10 kHz to 100 kHz)**
- **0.5% Initial Accuracy**
- **1% Overall Accuracy (Line, Load, and Temperature)**
- **Less Than 1 µA Max I_Q in Shutdown Mode**
- **Thermal Shutdown and Specified Min/Max Current Limit Protection**
- **Available in Multiple Output Voltage Versions**
  - **Fixed Outputs of 1.2 V to 5 V**
  - **Adjustable Outputs from 1.2 V to 5.5 V**
  - **Custom Outputs Available**

APPLICATIONS

- **Portable/Battery-Powered Equipment**
- **Post-Regulation for Switching Supplies**
- **Noise-Sensitive Circuitry such as VCOs**
- **Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors**

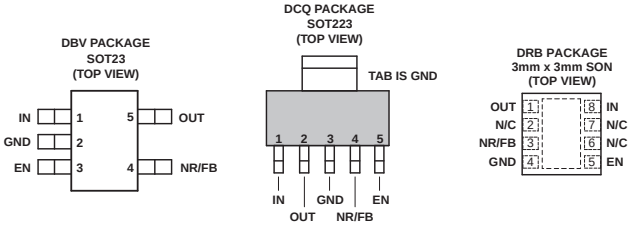


Typical Application Circuit for Fixed-Voltage Versions

DESCRIPTION

The TPS732xx family of low-dropout (LDO) voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR and even allows operation without a capacitor. It also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS732xx uses an advanced BiCMOS process to yield high precision while delivering low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1 µA and ideal for portable applications. The low output noise (30 μV_{RMS} with 0.1 µF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.



(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS732**xxyyyz**	**XX** is the nominal output voltage (for example, 25 = 2.5 V, 01 = Adjustable(3)). **YYY** is the package designator. **Z** is the package quantity.

(1) For the most current specification and package information, see the Package Option Addendum located at the end of this data sheet or see the TI website at www.ti.com.
(2) Output voltages from 1.2 V to 4.5 V in 50-mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.
(3) For fixed 1.2 V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range unless otherwise noted(1)

V_{IN} range	–0.3 V to 6 V
V_{EN} range	–0.3 V to 6 V
V_{OUT} range	–0.3 V to 5.5 V
Peak output current	Internally limited
Output short-circuit duration	Indefinite
Continuous total power dissipation	See Dissipation Ratings Table
Ambient temperature range, T_A	–55°C to 150°C
Storage temperature range	–65°C to 150°C
ESD rating, HBM	2 kV
ESD rating, CDM	500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS(1)

BOARD	PACKAGE	$R_{\Theta JC}$	$R_{\Theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
Low-K(2)	DBV	64°C/W	255°C/W	3.9 mW/°C	450 mW	275 mW	215 mW	58 mW
High-K(3)	DBV	64°/W	180°C/W	5.6 mW/°C	638 mW	388 mW	305 mW	83 mW

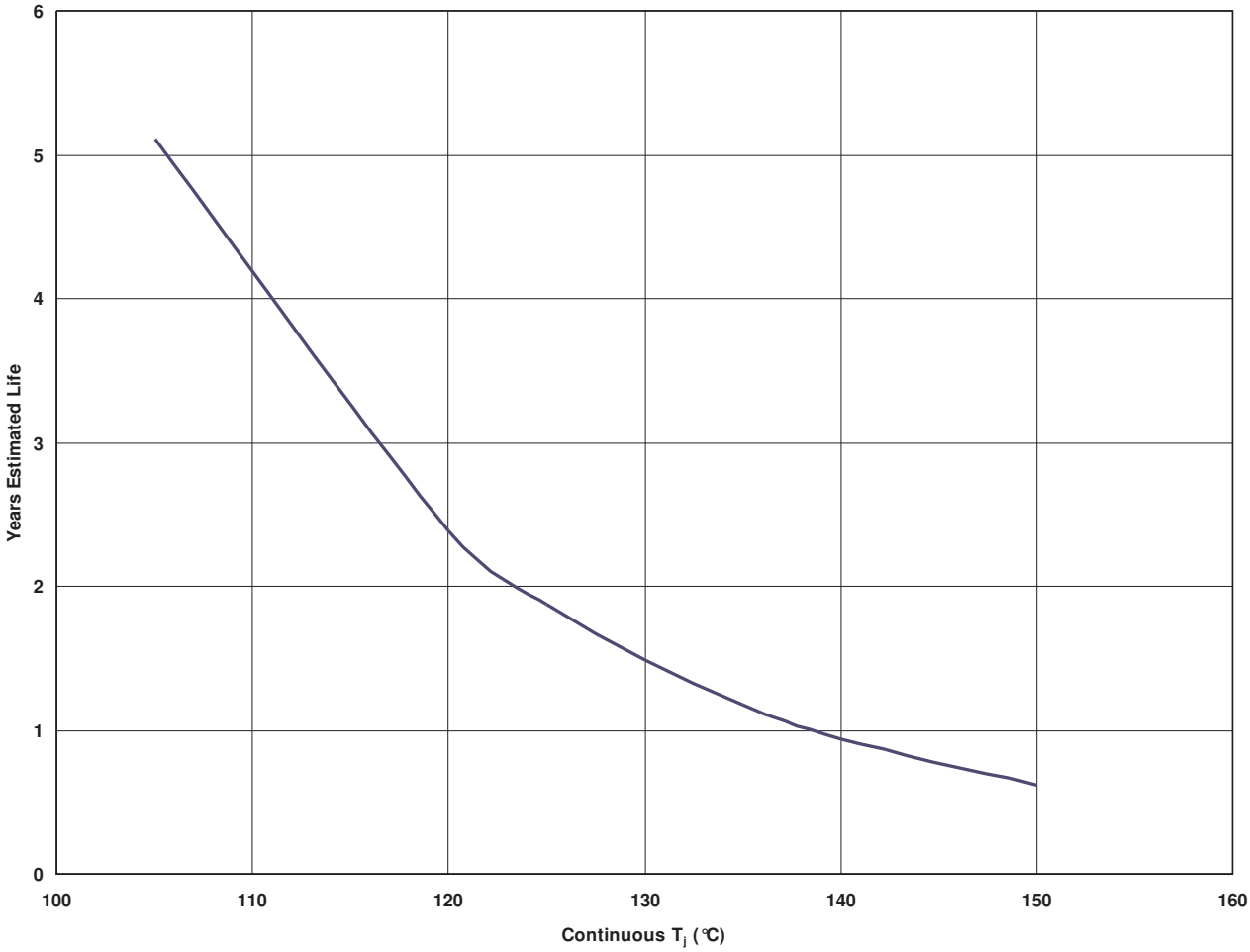
(1) See *Power Dissipation* in the ***Applications*** section for more information related to thermal design.
(2) The JEDEC Low-K (1s) board design used to derive this data was a 3 inch × 3 inch, two-layer board with 2-ounce copper traces on top of the board.
(3) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch × 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_A = –55°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V(1), I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			1.7		5.5	V
V_{FB}	Internal reference (TPS73201)		T_A = 25°C	1.198	1.2	1.21	V
V_{OUT}	Output voltage range (TPS73201)(2)			V_{FB}		5.5 – V_{DO}	V
	Accuracy(1)	Nominal	T_A = 25°C		±0.5%		
		V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V; 10 mA ≤ I_{OUT} ≤ 250 mA	–1%	±0.5%	+1%	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation(1)		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		1 mA ≤ I_{OUT} ≤ 250 mA		0.002		%/mA
			10 mA ≤ I_{OUT} ≤ 250 mA		0.0005		
V_{DO}	Dropout voltage(3) (V_{IN} = V_{OUT} (nom) – 0.1V)		I_{OUT} = 250 mA		40	150	mV
Z_O(DO)	Output impedance in dropout		1.7 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	250	425	600	mA
I_{SC}	Short-circuit current		V_{OUT} = 0 V		300		mA
I_{REV}	Reverse leakage current(4) (–I_{IN})		V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1	15	µA
I_{GND}	Ground pin current		I_{OUT} = 10 mA (I_Q)		400	550	µA
			I_{OUT} = 250 mA		650	950	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5		0.02	1	µA
I_{FB}	FB pin current (TPS73201)				.1	.45	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 250 mA		58		dB
			f = 10 kHz, I_{OUT} = 250 mA		37		
V_N	Output noise voltage BW = 10 Hz to 100 kHz		C_{OUT} = 10 µF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
			C_{OUT} = 10 µF, C_{NR} = 0.01 µF		8.5 × V_{OUT}		
t_{STR}	Startup time		V_{OUT} = 3 V, R_L = 30 Ω, C_{OUT} = 1 µF, C_{NR}= 0.01 µF		600		µs
V_{EN}(HI)	Enable high (enabled)			1.7		V_{IN}	V
V_{EN}(LO)	Enable low (shutdown)			0		0.5	V
I_{EN}(HI)	Enable pin current (enabled)		V_{EN} = 5.5 V		0.02	0.1	µA
T_{SD}	Thermal shutdown temperature		Shutdown, Temperature increasing		160		°C
			Reset, Temperature decreasing		140		
T_A	Operating ambient temperature			–55		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7 V, whichever is greater.
(2) TPS73201 is tested at V_{OUT} = 2.5 V.
(3) V_{DO} is not measured for the TPS73214, TPS73215, or TPS73216, since minimum V_{IN} = 1.7 V.
(4) Fixed-voltage versions only; see the ***Applications*** section for more information.



A. $T_j = \theta_{JA} \times W + T_A$ (at standard JESD 51 conditions)

Figure 1. Estimated Device Life at Elevated Temperatures Electromigration Fail Mode

FUNCTIONAL BLOCK DIAGRAMS

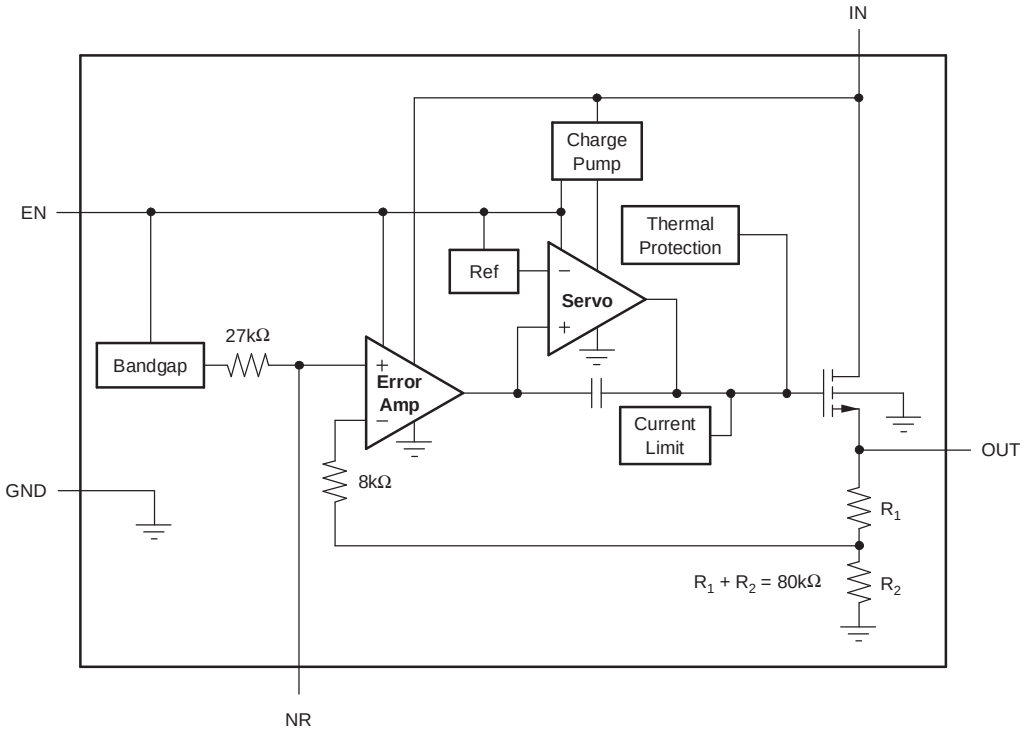


Figure 2. Fixed Voltage Version

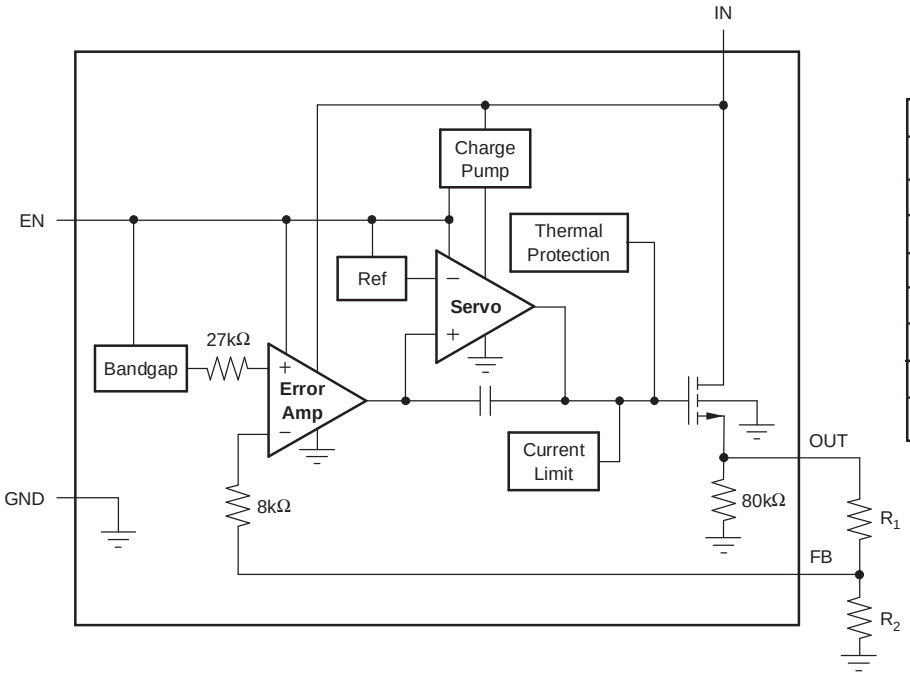


Figure 3. Adjustable Voltage Version

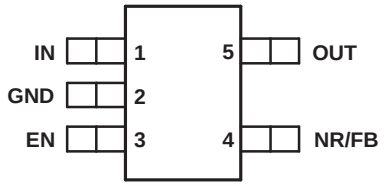
Table 1. Standard 1% Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28.0kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3.0V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ
5.0V	78.7kΩ	24.9kΩ

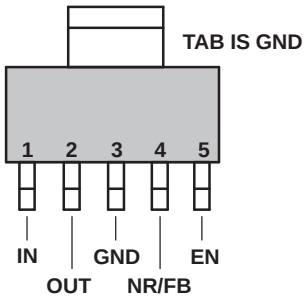
NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 || R_2 \cong 19k\Omega$ for best accuracy.

PIN ASSIGNMENTS

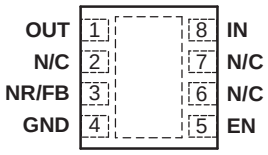
DBV PACKAGE
SOT23
(TOP VIEW)



DCQ PACKAGE
SOT223
(TOP VIEW)



DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL				DESCRIPTION
NAME	SOT23 (DBV) PIN NO.	SOT223 (DCQ) PIN NO.	3×3 SON (DRB) PIN NO.	
IN	1	1	8	Unregulated input supply
GND	2	3	4, Pad	Ground
EN	3	5	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the *Shutdown* section under *Applications Information* for more details. EN can be connected to IN if not used.
NR	4	4	3	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
FB	4	4	3	Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	2	1	Output of the Regulator. There are no output capacitor requirements for stability.

TYPICAL CHARACTERISTICS

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

LOAD REGULATION

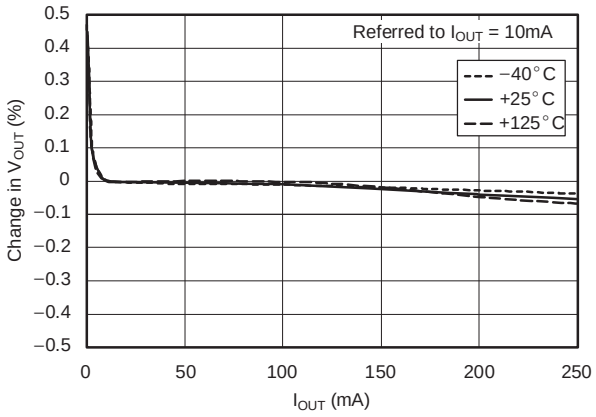


Figure 4.

LINE REGULATION

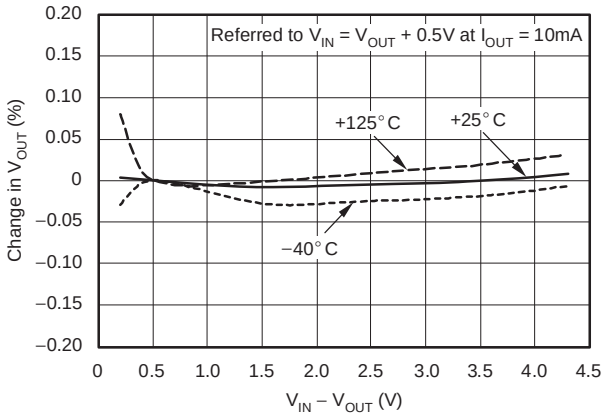


Figure 5.

DROPOUT VOLTAGE vsOUTPUT CURRENT

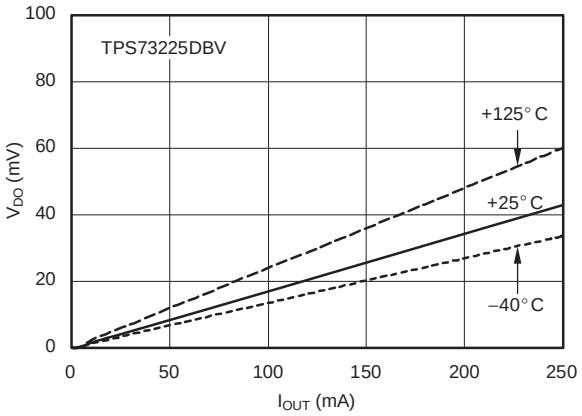


Figure 6.

DROPOUT VOLTAGE vs TEMPERATURE

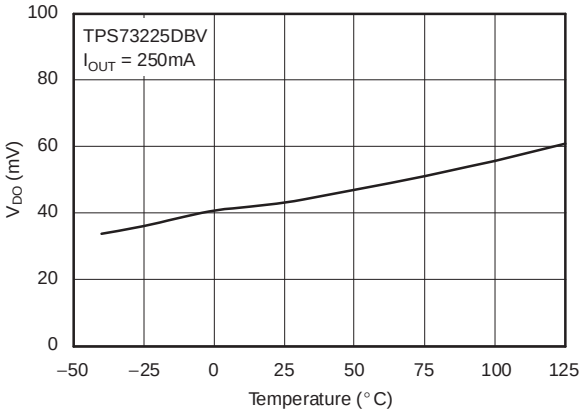


Figure 7.

OUTPUT VOLTAGE ACCURACY HISTOGRAM

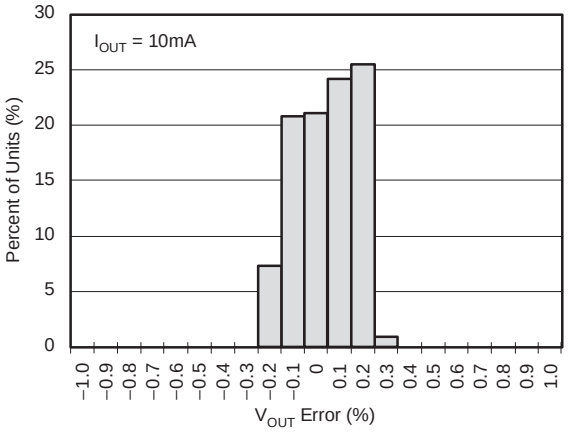


Figure 8.

OUTPUT VOLTAGE DRIFT HISTOGRAM

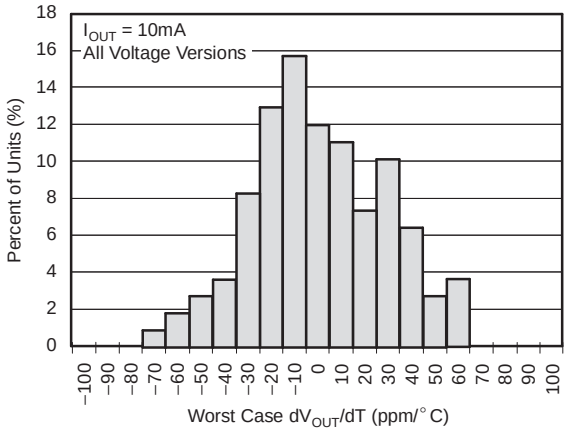


Figure 9.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

GROUND PIN CURRENT vs OUTPUT CURRENT

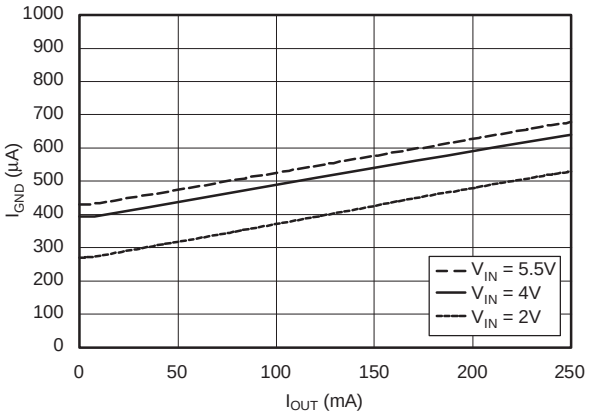


Figure 10.

GROUND PIN CURRENT vs TEMPERATURE

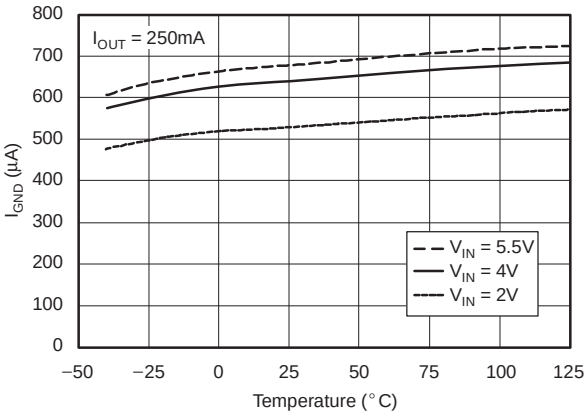


Figure 11.

CURRENT LIMIT vs V_{OUT} (FOLDBACK)

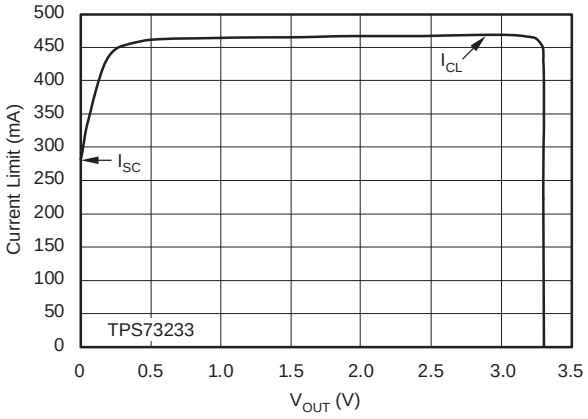


Figure 12.

GROUND PIN CURRENT in SHUTDOWN vs TEMPERATURE

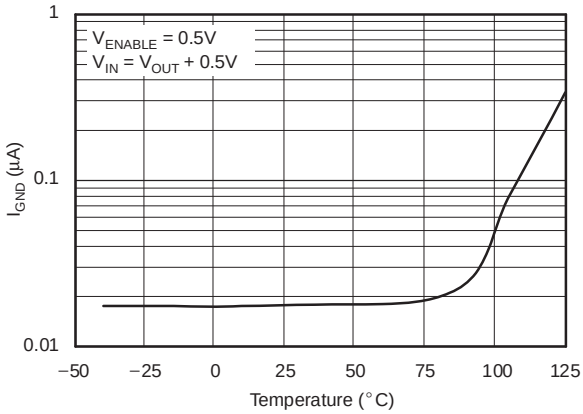


Figure 13.

CURRENT LIMIT vs V_{IN}

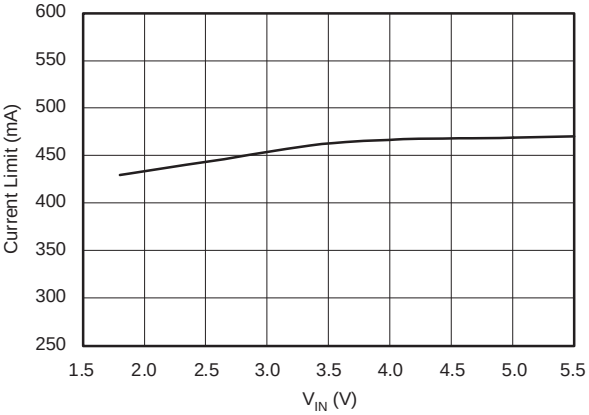


Figure 14.

CURRENT LIMIT vs TEMPERATURE

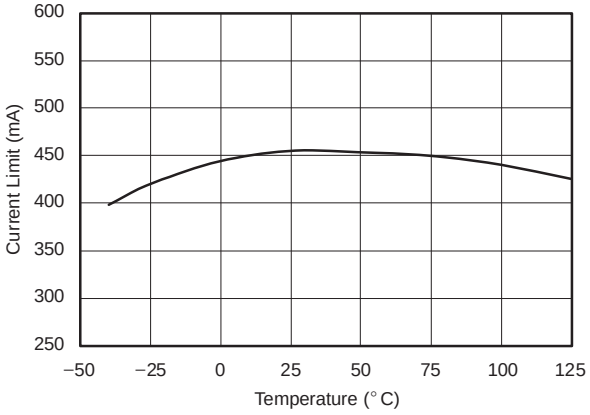


Figure 15.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

PSRR (RIPPLE REJECTION) vs FREQUENCY

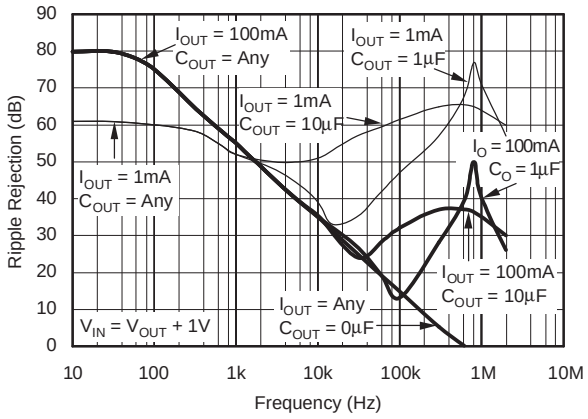


Figure 16.

PSRR (RIPPLE REJECTION) vs V_{IN} – V_{OUT}

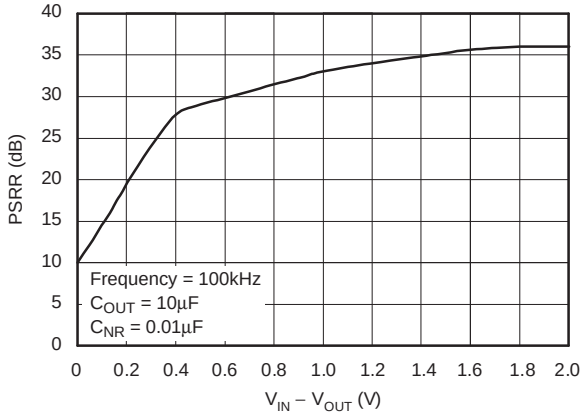


Figure 17.

NOISE SPECTRAL DENSITY
C_{NR} = 0 µF

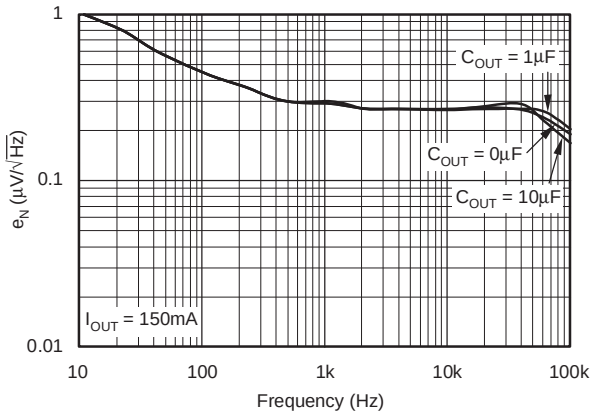


Figure 18.

NOISE SPECTRAL DENSITY
C_{NR} = 0.01 µF

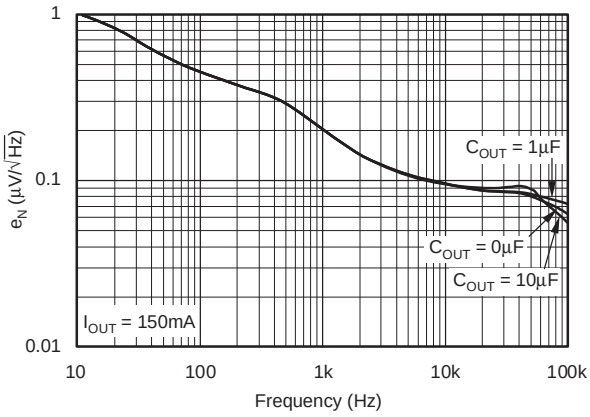


Figure 19.

RMS NOISE VOLTAGE vs C_{OUT}

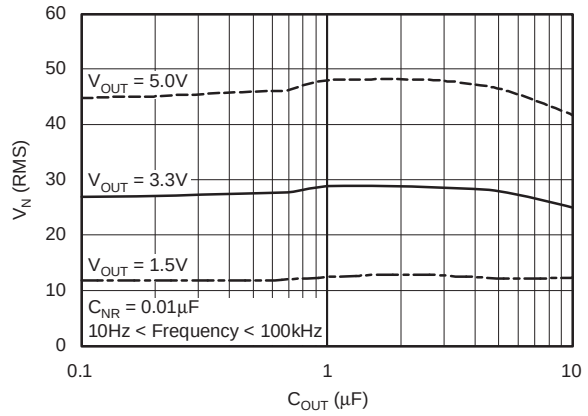


Figure 20.

RMS NOISE VOLTAGE vs C_{NR}

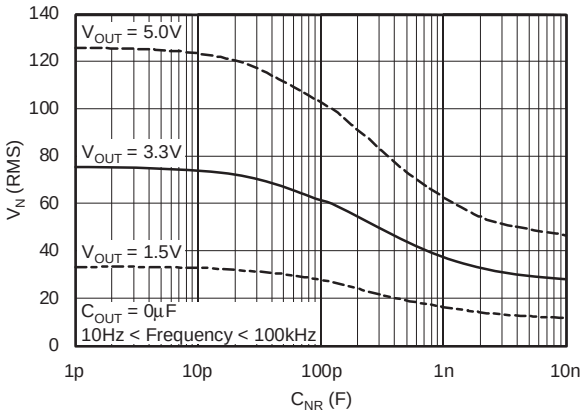


Figure 21.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

TPS73233
LOAD TRANSIENT RESPONSE

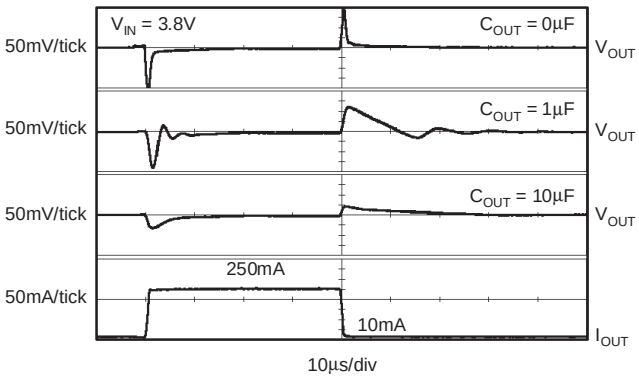


Figure 22.

TPS73233
LINE TRANSIENT RESPONSE

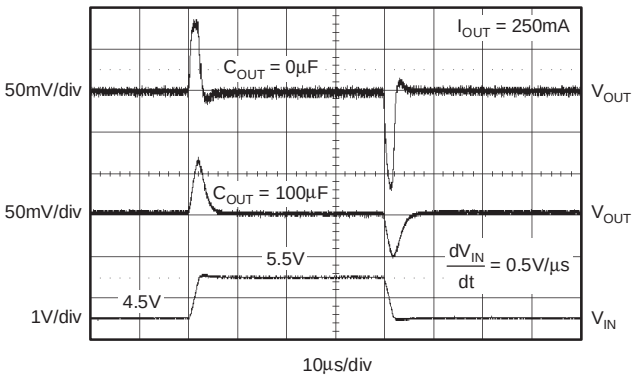


Figure 23.

TPS73233
TURN-ON RESPONSE

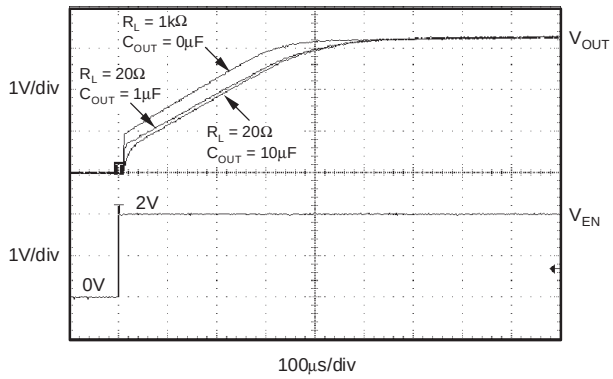


Figure 24.

TPS73233
TURN-OFF RESPONSE

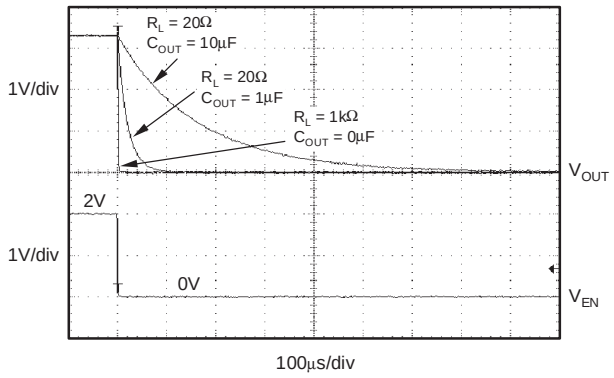


Figure 25.

TPS73233
POWER UP / POWER DOWN

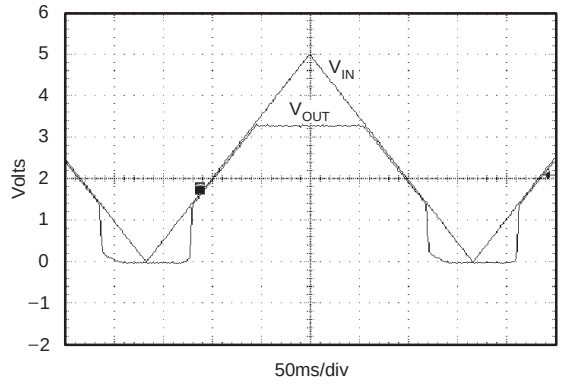


Figure 26.

I_{ENABLE} vs TEMPERATURE

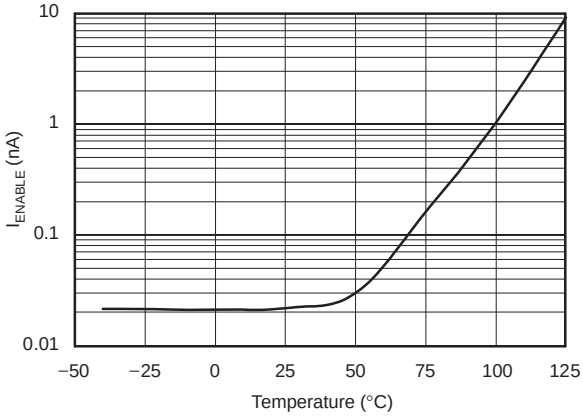


Figure 27.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

TPS73201
RMS NOISE VOLTAGE vs C_{ADJ}

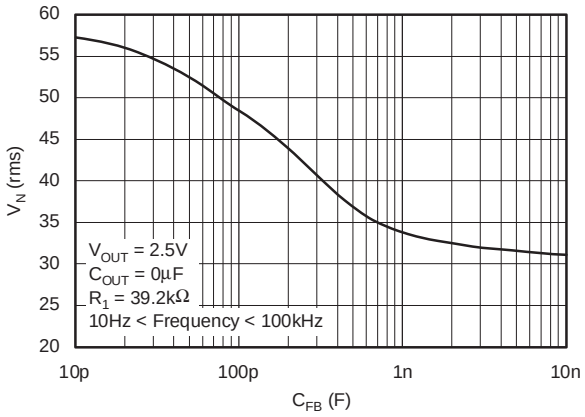


Figure 28.

TPS73201
I_{FB} vs TEMPERATURE

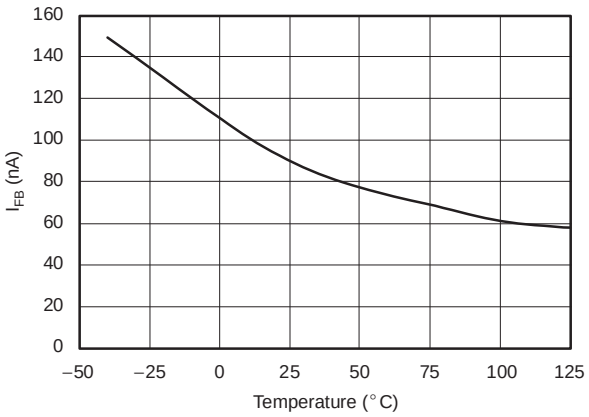


Figure 29.

TPS73201
LOAD TRANSIENT, ADJUSTABLE VERSION

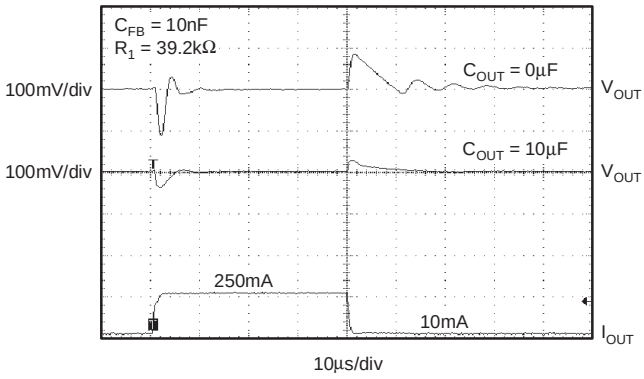


Figure 30.

TPS73201
LINE TRANSIENT, ADJUSTABLE VERSION

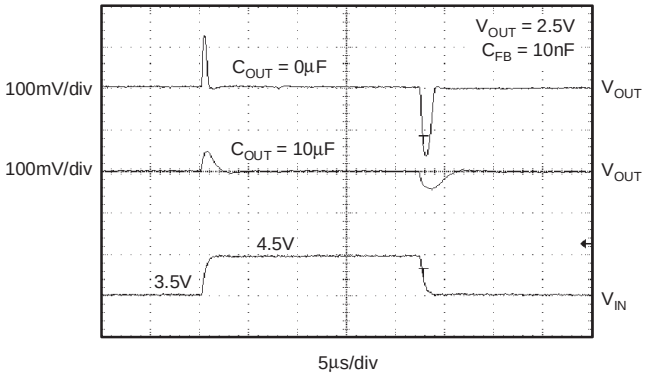


Figure 31.

APPLICATION INFORMATION

The TPS732xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS732xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Figure 32 shows the basic circuit connections for the fixed voltage models. Figure 33 gives the connections for the adjustable output version (TPS73201).

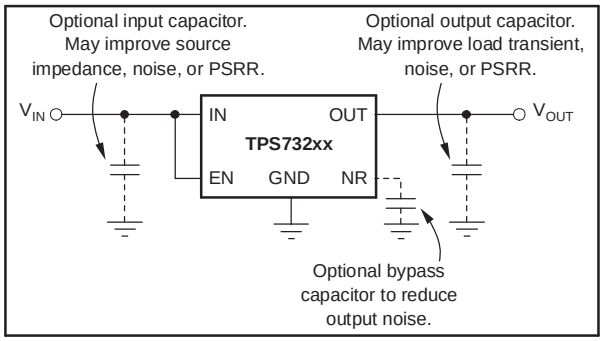


Figure 32. Typical Application Circuit for Fixed-Voltage Versions

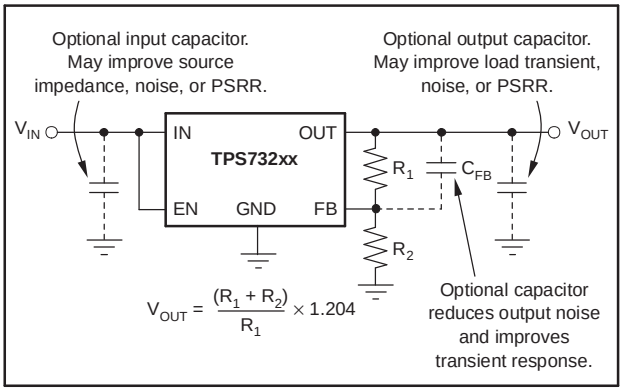


Figure 33. Typical Application Circuit for Adjustable-Voltage Versions

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 33. Sample resistor values for common output voltages are shown in Figure 3. For the best accuracy, make the parallel combination of R_1 and R_2 approximately 19 kΩ.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1 µF to 1 µF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS732xx does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where $V_{IN} - V_{OUT} < 0.5$ V and multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 nΩF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

OUTPUT NOISE

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS732xx and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

for the case of no C_{NR}.

An internal 27 kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10 Hz to 100 kHz bandwidth is reduced by a factor of ~3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

for C_{NR} = 10nF.

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in the Typical Characteristics section.

The TPS73201 adjustable version does not have the noise-reduction pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the FB pin reduces output noise and improve load transient performance.

The TPS732xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates ~250 μV of switching noise at ~2 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TPS732xx internal current limit helps protect the regulator during fault conditions. Foldback helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See Figure 12 in the Typical Characteristics section for a graph of I_{OUT} vs V_{OUT}.

SHUTDOWN

The Enable pin is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5 V (max) turns the regulator off and drops the ground pin current to approximately 10 nA. When shutdown capability is not required, the Enable pin can be connected to V_{IN}. When a pullup resistor is used, and operation down to 1.8 V is required, use pullup resistor values below 50 kΩ.

DROPOUT VOLTAGE

The TPS732xx uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the R_{DS-ON} of the NMOS pass element.

For large step changes in load current, the TPS732xx requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} – V_{OUT} above this line insure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to dc dropout levels], the TPS732xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

TRANSIENT RESPONSE

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1 μF) from the output pin to ground reduces undershoot magnitude but increase duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the output to the adjust pin also improves the transient response.

The TPS732xx does not have active pulldown when the output is overvoltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

REVERSE CURRENT

The NMOS pass element of the TPS732xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the enable pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the enable pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There will be additional current flowing into the OUT pin due to the 80-kΩ internal resistor divider to ground (see Figure 2 and Figure 3).

For the TPS73201, reverse current may flow when V_{FB} is more than 1 V above V_{IN}.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS732xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS732xx into thermal shutdown will degrade device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low-K and high-K boards are shown in the Power Dissipation Ratings table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

Package Mounting

Solder pad footprint recommendations for the TPS732xx are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (AB-132), available from the Texas Instruments web site at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS73201MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73215MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73216MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73218MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73225MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73230MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73233MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73250MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06644-01XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06644-02XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06644-03XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06644-04XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06644-05XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06644-06XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06644-07XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06644-08XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TPS73201-EP, TPS73215-EP, TPS73216-EP, TPS73218-EP, TPS73225-EP, TPS73230-EP, TPS73233-EP, TPS73250-EP :

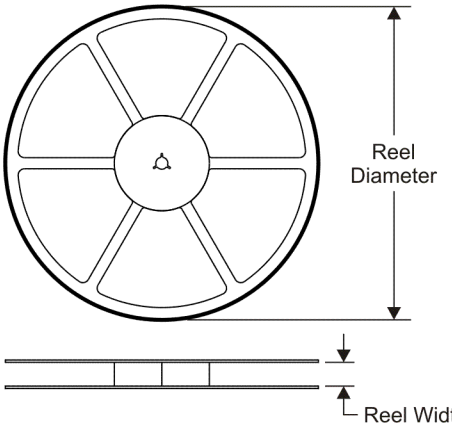
- Catalog: TPS73201, TPS73215, TPS73216, TPS73218, TPS73225, TPS73230, TPS73233, TPS73250
- Automotive: TPS73201-Q1, TPS73225-Q1

NOTE: Qualified Version Definitions:

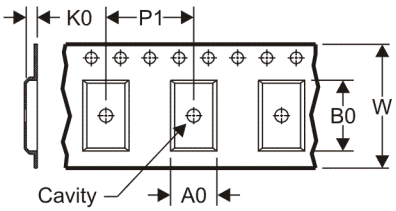
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

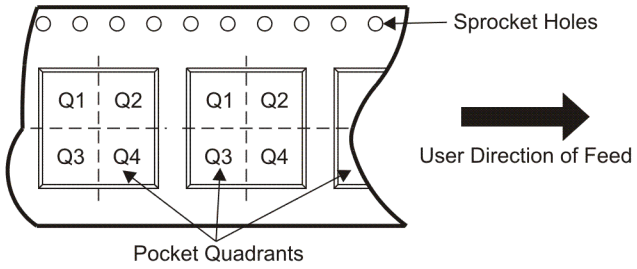


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

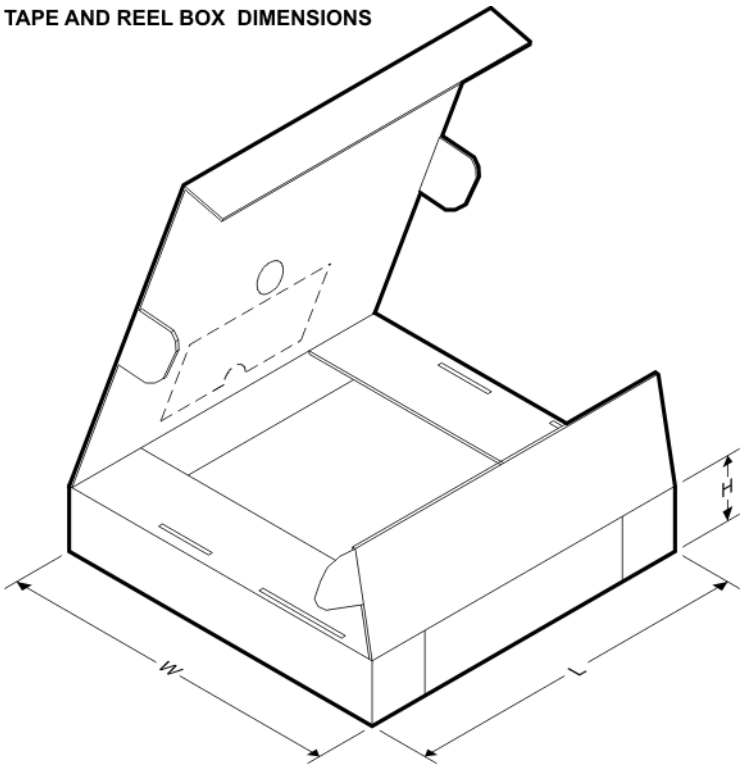
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73201MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73215MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73216MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73218MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73225MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73230MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73233MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73250MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

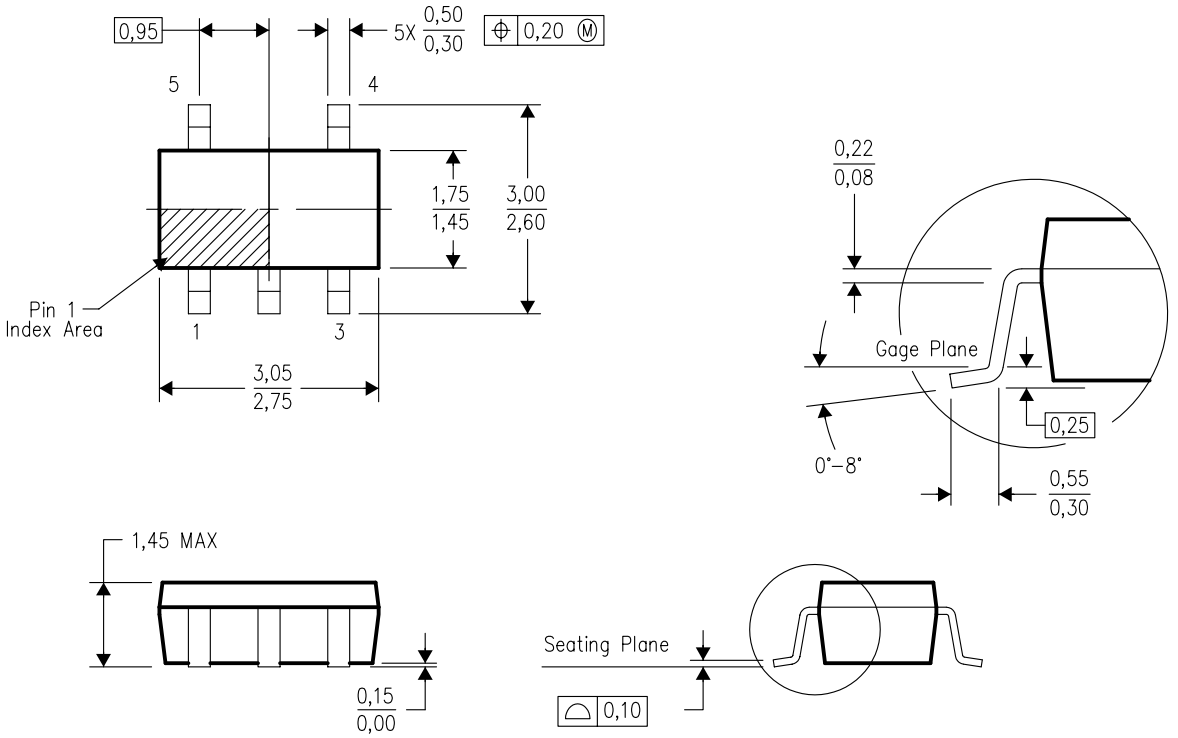
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73201MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73215MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73216MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73218MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73225MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73230MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73233MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73250MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0

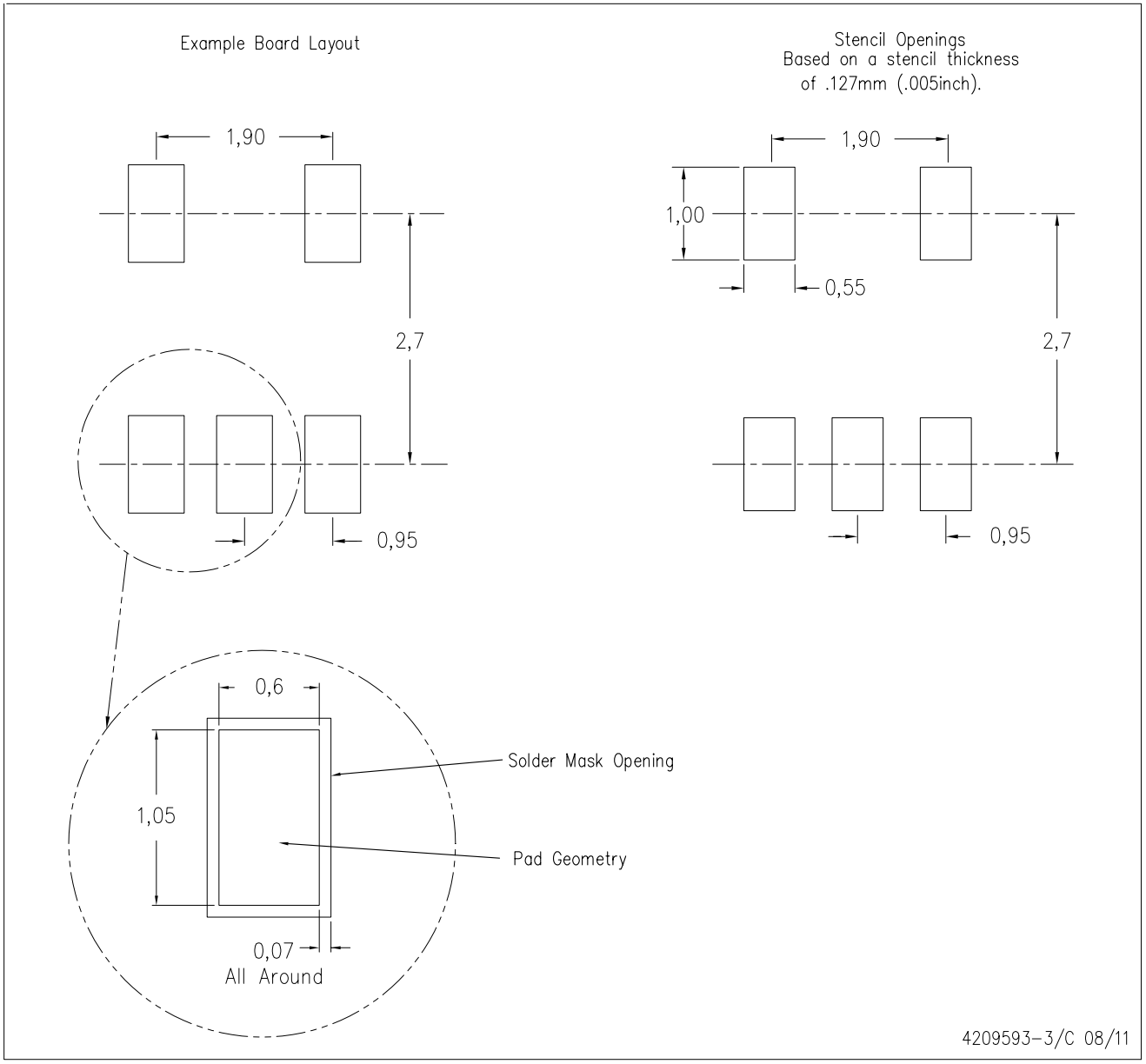
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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