# TPS6602x Integrated Source and Sink Power Multiplexer with VBUS LDO Regulator

## 1 Features

- Integrated 30 mΩ (typical), 32-V tolerant NFET 5-V source path, up to 3 A
- Integrated 22 mΩ (typical), 32-V tolerant NFET 4-V to 22-V sink path, up to 5 A
- Selectable current limit for 5-V source path
- Built-in soft-start to limit in-rush currents
- Integrated high voltage VBUS LDO regulator (3.3-V or 5.0-V per device type)
- Optional VBUS overvoltage protection via pin configuration.
- System supply and VBUS undervoltage protection
- 5-V System supply overvoltage protection
- Overtemperature protection
- Reverse-current protection
- Fault pin with de-glitched fault reporting
- Support for fast role swap
- IEC/UL Certificate No. US-34369-UL
  - Standards: IEC 62368-1 Ed. 2, UL 2367 Ed. 1
- Small footprint WCSP packaging, no HDI required.

## 2 Applications

- Desktop PC/motherboard
- Standard notebook PC
- Chromebook and WOA
- Docking station
- Port/cable adapters and dongles

## 3 Description

The TPS6602x is a full-featured power switch multiplexer that contains an integrated 5-V Source power path and a 4-V to 22-V Sink power path. The 5-V Source path limits the output current to a safe level by operating in a constant-current mode when the output load exceeds the selected current-limit threshold. Each power path supports overtemperature and reverse current protection. VBUS has overvoltage protection with its level being set by an optional external resistor divider. If no overvoltage protection is desired, it may be disabled by grounding the OVP terminal. The TPS6602x series supports a fault pin that indicates overcurrent and overtemperature events.

TPS6602x series also supports a high voltage VBUS LDO regulator (3.3-V or 5-V per device type) useful for supplying power to the device and other system components when operating in dead battery conditions. The TPS66020 regulates to 3.3-V and the TPS66021 regulates to 5-V.

**Device Information**[1]

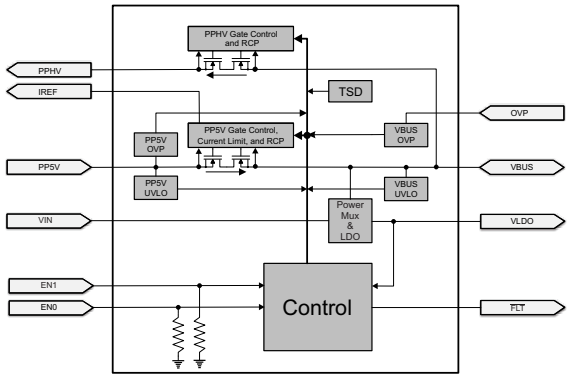
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS66020 | WCSP (28) | 1.606 mm x 2.806 mm |
| TPS66021 | | |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Function Table**

| EN1 | EN0 | Device State |
|---|---|---|
| 0 | 0 | Source and Sink paths disabled |
| 0 | 1 | Sink path enabled |
| 1 | 0 | Source path enabled, 1.5 A |
| 1 | 1 | Source path enabled, 3.0 A |

**TPS6602x Block Diagram**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

**Changes from Revision A (September 2019) to Revision B** — **Page**

- Changed from Advance Information to Production Data ... 1

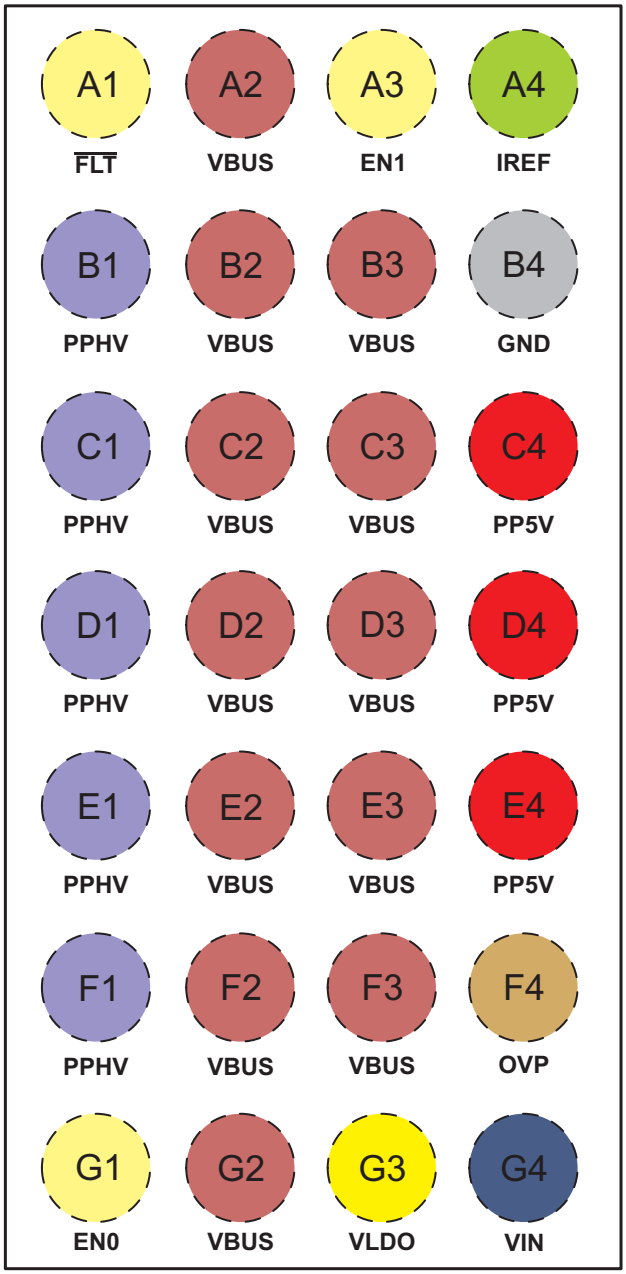
**Changes from Original (August 2019) to Revision A** — **Page**

- Updated Applications section with links ... 1
- Added Typical Characteristics section ... 11
- Added Application Curves section ... 35


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# 5 Pin Configuration and Functions

**TPS6602x YBG Package**
**28-Pin WCSP**
**Top View**




**Pin Functions**

| Pin | | I/O | Reset State | Description |
|---|---|---|---|---|
| Name | No. | | | |
| PP5V | C4, D4, E4 | Power | Off | 5-V System Supply to VBUS. Bypass with capacitance CPP5V to GND. |
| PPHV | B1, C1, D1, E1, F1 | Power | Off | HV System Supply from VBUS. Bypass with capacitance CPPHV to GND. |

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**Pin Functions (continued)**

| Pin | | I/O | Reset State | Description |
|---|---|---|---|---|
| Name | No. | | | |
| VBUS | A2, B2, B3, C2, C3, D2, D3, E2, E3, F2, F3, G2 | Power | - | 5-V to 20-V nominal input supply to PPHV or 5-V output supply from PP5V. Bypass with capacitance CVBUS to GND. |
| VIN | G4 | Power | - | Device input supply. Bypass with capacitance CVIN to GND. |
| VLDO | G3 | Power | - | VIN supply or VBUS LDO regulated supply output from power multipexer. Bypass with capacitance CVLDO to GND. |
| GND | B4 | Ground | - | Ground. Connect all pins to ground plane. |
| OVP | F4 | Analog | - | Selects VBUS OVP. Tie pin to VBUS resistor divider output to set desired VBUS OVP level. Tie pin to GND to remove VBUS OVP function. |
| EN1 | A3 | Digital Input | Pull-down | Enable control signal for PPHV Sink and PP5V Source paths. Internal pull-down. |
| EN0 | G1 | Digital Input | Pull-down | Enable control signal for PPHV Sink and PP5V Source paths. Internal pull-down. |
| IREF | A4 | Analog | | Used to set the PP5V source path current limit bias using an external resistor tied to GND. |
| $\overline{\text{FLT}}$ | A1 | Digital Output | Hi-Z | Fault Output Indicator. Active low. This pin is a true open-drain (no PMOS). Float pin when unused. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Terminal voltage range (2) | PP5V, EN0(3), EN1(3), $\overline{\text{FLT}}$, VIN, VLDO | –0.3 | 6.2 | V |
| Terminal voltage range (2) | OVP | –0.3 | VBUS | V |
| Terminal voltage range (2) | VBUS, power path disabled (stand off voltage) | –0.5 | 32 | V |
| Terminal voltage range (2) | VBUS, power path enabled(4) | –0.5 | 26 | V |
| Terminal voltage range (2) | PPHV | –0.3 | 26 | V |
| Terminal voltage range (2) | IREF | –0.3 | 4.5 | V |
| Terminal positive source current | IREF | | Internally limited | mA |
| Terminal positive source current | VLDO sourced from VBUS VLDO | | Internally limited | mA |
| | VLDO sourced from VIN | | 50 | mA |
| Storage temperature | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
(3) EN0 and EN1 each have an internal voltage clamp and may be driven above the absolute maximium voltage rating up to EN_CLAMP maximum specification if current is limited to less than 100µA.
(4) For VBUS, a TVS protection with a break down voltage falling between the Recommended and Absolute maximum ratings is recommended, such as the TVS2200.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{VIN}$ | Input voltage range (1) | VIN, TPS66020 only. | 2.85 | 3.6 | V |
| | | VIN, TPS66021 only. | 4.5 | 5.5 | V |
| $V_{PP5V}$ | Input voltage range (1) | PP5V | 4.9 | 5.5 | V |
| $V_{PPHV}$ | Output voltage range (1) | PPHV | 0 | 22 | V |
| $V_{VBUS}$ | Output voltage range (1) | VBUS when sourcing | 0 | 5.5 | V |
| $V_{VBUS}$ | Input voltage range (1) | VBUS when sinking | 4 | 22 | V |
| $V_{EN}$ | Input voltage range (1) | EN0, EN1 | 0 | 5.5 | V |
| $V_{\overline{FLT}}$ | Output voltage range (1) | $\overline{FLT}$ | 0 | 5.5 | V |
| $I_{O_PP5V}$ | Continuous current from PP5V to VBUS | $T_J$ = 105℃ | | 3 | A |
| $I_{O_PPHV}$ | Continuous current from VBUS to PPHV | $T_J$ = 105℃ | | 4 | A |
| | | $T_J$ = 100℃ | | 5 | A |
| $I_{O_VLDO}$ | Output current from VBUS LDO | | | 30 | mA |
| $R_{IREF}$ | External resistor current limit reference | 75kΩ ±1% overall tolerance | 74.25 | 75.75 | kΩ |
| $T_J$ | Operating junction temperature | | –10 | 125 | °C |
| RR_PP5V | Maximum ramp rate on PP5V input supply | | –2 | 2 | V/µs |
| RR_PPHV | Maximum ramp rate on PPHV input supply | | –2 | 2 | V/µs |
| RR_VBUS | Maximum ramp rate on VBUS input supply | | –2 | 2 | V/µs |
| RR_VIN | Maximum ramp rate on VIN input supply | | | 30 | mV/µs |

(1) All voltage values are with respect to network GND. GND pin must be connected directly to the ground plane of the board.

## 6.4 Recommended Supply Load Capacitance

over operating free-air temperature range (unless otherwise noted)

| PARAMETER(1) | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| CVIN | Capacitance on VIN | 1 | | | µF |
| CVLDO | Capacitance on VLDO | 2.5 | 4.7 | 10 | µF |
| CVBUS | Capacitance on VBUS | 1 | | 10 | µF |
| CPP5V | Capacitance on PP5V | 2.5 | 4.7 | | µF |
| CPPHV | Capacitance present on PPHV(2) | 1 | 47 | 100 | µF |

(1) Capacitance values do not include any derating factors. For example, if 5.0 µF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value would be 10 µF.
(2) This capacitance represents the system side load capacitance that may be seen by the device e.g. from a typical battery charging system. Discrete capacitance is not required for proper operation.

## 6.5 Thermal Information

| THERMAL METRIC(1) | | TPS6602x YBG (WCSP) 28 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA,EFF}$ | Effective Junction-to-ambient thermal resistance(2) | 44.3 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 62.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 0.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 13.7 | °C/W |
| $\psi_{JB,EFF}$ | Effective Junction-to-board characterization parameter(2) | 14.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Models based on typical application layout.

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## 6.6 PP5V Power Switch Characteristics

Operating under these conditions unless otherwise noted: -10 ℃ ≤ $T_J$ ≤ 125 ℃, 2.85V ≤ $V_{VIN}$ ≤ 5.5V, $R_{IREF}$ = 75 kΩ ±1% overall tolerance, 4.9V ≤ $V_{PP5V}$ ≤ 5.5V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{PP5V}$ | Resistance from PP5V to VBUS | $I_{LOAD}$ = 1 A, PP5V = 5.0V, $T_J$ = 25℃, SRC 1P5A or SRC 3P0A state. | | 30 | 35 | mΩ |
| | | $I_{LOAD}$ = 1 A, PP5V = 5.0V, -10 ℃ ≤ $T_J$ ≤ 125 ℃, SRC 1P5A or SRC 3P0A state. | | 30 | 50 | mΩ |
| $I_{SC_IREF}$ | Short circuit current from VBUS with IREF terminal shorted. | $V_{IREF}$ = 0V, SRC 1P5A or SRC 3P0A state. | | | 8 | A |
| $V_{IREF}$ | Output voltage | SRC 1.5A state | | 0.56 | | V |
| | | SRC 3.0A state | | 1.13 | | V |
| $I_{LIM_PP5V_1P5}$ | Current limit for 1.5A setting | SRC 1.5A state | 1.60 | 1.74 | 1.87 | A |
| $I_{LIM_PP5V_3P0}$ | Current limit for 3.0A setting | SRC 3.0A state | 3.2 | 3.45 | 3.7 | A |
| $I_{LIMPP5VF}$ | Difference between current limit and current limit fault flag assertion, $I_{LIM5VF}$ ≤ $I_{LIM5V}$. | SRC 1P5A or SRC 3P0A state. PP5V = 5V. Sweep load current and monitor $\overline{FLT}$ transition from 1 to 0 (50% point). $C_{\overline{FLT}}$ = 20pF, $R_{PU}$ = 10 kΩ to VLDO. | | 12 | | mA |
| $t_{ILIMIT_FLT}$ | Time from PP5V current limit detected until $\overline{FLT}$ asserted low. | SRC 1P5A or SRC 3P0A state. PP5V = 5V. Sweep load current and monitor $\overline{FLT}$ transition from 1 to 0 (50% point). $C_{\overline{FLT}}$ = 20pF, $R_{PU}$ = 10 kΩ to VLDO. | 4 | 10 | 16 | ms |
| $V_{PP5V_RCP}$ | Maximum voltage due to reverse current. Source path disables due to RCP comparator. | SRC 1P5A or SRC 3P0A state. $V_{PP5V}$ = 5.5V, ramp $V_{VBUS}$ from 5.5V to 21V at 75 V/ms, $C_{PP5V}$ = 47µF, measure $V_{PP5V}$ | | | 5.8 | V |
| $V_{PP5V_RCP_OVP}$ | Maximum voltage due to reverse current. Source path disables due to OVP protection on PP5V. | SRC 1P5A or SRC 3P0A state. $V_{PP5V}$ = 5.5V, ramp $V_{VBUS}$ from 5.5V to 21V at 5 V/ms, $C_{PP5V}$ = 4.7µF, measure $V_{PP5V}$ | | | 6.25 | V |
| $V_{RCP_THRES_PP5V}$ | Reverse current blocking voltage threshold for PP5V switch | | 25 | 35 | 45 | mV |
| $t_{OS_PP5V}$ | Response time to VBUS short circuit | VBUS to GND through 10mΩ | | 2.0 | | µs |
| $t_{ON_PP5V}$ | PP5V enable time. | $R_L$ = 100Ω, $V_{PP5V}$ = 5V, $C_L$=0, Transition from DISABLED state to SRC 1.5A state, $V_{VBUS}$ reaches 90% of final value. | 2.6 | 4.5 | 5.3 | ms |
| $t_{OFF_PP5V}$ | PP5V disable time. | $R_L$ = 100Ω, $V_{PP5V}$ = 5V, $C_L$=0, Transition from SRC 1.5A or SRC 3.0A state to DISABLED state, $V_{VBUS}$ at 10% of final value. | 0.5 | 0.7 | 1.2 | ms |
| $t_{RISE_PP5V}$ | VBUS from 10% to 90% of final value | $R_L$ = 100Ω, $V_{PP5V}$ = 5V, $C_L$=0, Transition from DISABLED state to SRC 1.5A state | 0.5 | 0.9 | 1.5 | ms |
| $t_{FALL_PP5V}$ | VBUS from 90% to 10% of initial value | $R_L$ = 100Ω, $V_{PP5V}$ = 5V, $C_L$=0, Transition from SRC 1.5A or SRC 3.0A state to DISABLED state | 0.1 | 0.16 | 0.25 | ms |


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## 6.7 PPHV Power Switch Characteristics

Operating under these conditions unless otherwise noted: -10 ℃ ≤ $T_J$ ≤ 125 ℃, 2.85V ≤ $V_{VIN}$ ≤ 5.5V, $R_{IREF}$ = 75 kΩ ±1% overall tolerance

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{PPHV}$ | Resistance from PPHV to VBUS | $I_{LOAD}$ = 1 A, $T_J$ = 25 ℃, SNK state. | | 22 | 26 | mΩ |
| | | $I_{LOAD}$ = 1 A, -10 ℃ ≤ $T_J$ ≤ 125 ℃, SNK state. | | 22 | 45 | mΩ |
| $V_{PPHV_RCP}$ | Maximum voltage due to reverse current during RCP response. | SNK state, $V_{VBUS}$ = 5.5V, ramp $V_{PPHV}$ from 5.5V to 21V at 100 V/ms, $C_{VBUS}$ = 10µF, measure $V_{VBUS}$ | | | 5.8 | V |
| $V_{PPHV_OVP}$ | Maximum voltage rise due to reverse current during VBUS OVP response. | SNK state, $V_{VBUS}$ = 5.5V, set $V_{OVP}$ = 6V, ramp $V_{VBUS}$ from 5.5V to 21V at 100 V/ms, $C_{PPHV}$ = 4.7µF, measure $V_{PPHV}$ | | | 6.2 | V |
| $V_{RCP_THRES_PPHV}$ | Reverse current blocking voltage threshold for PPHV switch | | 2 | 6 | 10 | mV |
| SS | Soft-start slew rate | Transition from DISABLED state to SNK state, $V_{VBUS}$ = 5V, $C_{PPHV}$ = 100µF. Measure slew rate on PPHV. | 0.2 | | 0.6 | V/ms |
| $t_{ON_PPHV}$ | PPHV enable time including Soft-start. | $R_{PPHV}$ = 100Ω, $V_{VBUS}$ = 5V, $C_{PPHV}$ = 100 µF. Transition from DISABLED state to SNK state, $V_{PPHV}$ at 90% of final value. | 9 | 15 | 29 | ms |
| $t_{OFF_PPHV}$ | PPHV disable time. | $R_{PPHV}$ = 100Ω, $V_{VBUS}$ = 5V, $C_{PPHV}$ = 4.7 µF. Transition from SNK state to DISABLED state, $V_{PPHV}$ falls to 4.5V. | 0.9 | 2.2 | 4.3 | ms |

## 6.8 Power Path Supervisory

Operating under these conditions unless otherwise noted: -10 ℃ ≤ $T_J$ ≤ 125 ℃, 2.85V ≤ $V_{VIN}$ ≤ 5.5V, $R_{IREF}$ = 75 kΩ ±1% overall tolerance

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| UV_VIN_R | Undervoltage threshold for VIN. VBUS LDO disables when threshold reached. | VIN rising, TPS66020 only. | 2.45 | | 2.75 | V |
| | | VIN rising, TPS66021 only. | 3.89 | | 4.40 | V |
| UV_VIN_F | Undervoltage threshold for VIN. Device resets. | VIN falling, TPS66020 only. | 2.35 | | 2.65 | V |
| | | VIN falling, TPS66021 only. | 3.79 | | 4.30 | V |
| UVH_VIN | Undervoltage hysteresis for VIN. | | | 100 | | mV |
| UV_VBUS_R | Undervoltage threshold for VBUS. PPHV switch disabled unitl threshold reached. | VBUS rising | 3.35 | | 3.75 | V |
| UV_VBUS_F | Undervoltage threshold for VBUS. PPHV switch disables when threshold reached. | VBUS falling | 3.15 | | 3.55 | V |
| UVH_VBUS | Undervoltage hysteresis for VBUS | | | 200 | | mV |
| OVP_REF | OVP reference voltage. | | 0.93 | 1 | 1.07 | V |
| UV_PP5V_R | Undervoltage threshold for PP5V. PP5V switch disabled unitl threshold reached. | PP5V rising | 3.9 | | 4.5 | V |
| UVH_PP5V | Undervoltage hysteresis for PP5V | | | 100 | | mV |
| UV_PP5V_F | Undervoltage threshold for PP5V. PP5V swtch disables when threshold reached. | PP5V falling | 3.8 | | 4.4 | V |
| OV_PP5V_R | Overvoltage threshold for PP5V. PP5V switch disabled if threshold reached. | PP5V rising | 5.60 | 5.9 | 6.2 | V |
| OV_PP5V_F | Overvoltage threshold for PP5V. PP5V switch enabled if threshold reached. | PP5V falling | 5.50 | 5.8 | 6.1 | V |
| OVH_PP5V | Overvoltage hysteresis for PP5V | | | 100 | | mV |
| VFWD_DROP_VIN | Forward voltage drop across VIN to VLDO switch | $I_{VLDO}$ = 35 mA | | | 90 | mV |

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## Power Path Supervisory (continued)

Operating under these conditions unless otherwise noted: -10 ℃ ≤ $T_J$ ≤ 125 ℃, 2.85V ≤ $V_{VIN}$ ≤ 5.5V, $R_{IREF}$ = 75 kΩ ±1% overall tolerance

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{VIN_STABLE}$ | When VIN is above UV_VIN_R for this duration, VIN is considered valid. If device is being powered by VBUS LDO, it will then switch to VIN supply and VBUS LDO will be disabled. | | 5 | | 15 | ms |

## 6.9 VBUS LDO Characteristics

Operating under these conditions unless otherwise noted: -10 ℃ ≤ $T_J$ ≤ 125 ℃, 2.85V ≤ $V_{VIN}$ ≤ 5.5V, $R_{IREF}$ = 75 kΩ ±1% overall tolerance

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| V_VBUS_LDO_3V | Output voltage of VBUS LDO | For TPS66020: VIN = 0V, VBUS ≥ 3.8V, 0 ≤ I_VBUS_LDO ≤ 30mA | 3.07 | 3.3 | 3.53 | V |
| V_VBUS_LDO_5V | Output voltage of VBUS LDO | For TPS66021: VIN = 0V, VBUS ≥ 5.5V, 0 ≤ I_VBUS_LDO ≤ 30mA | 4.65 | 5.0 | 5.35 | V |
| VDO_VBUS_LDO_3V | Drop out voltage of VDD LDO | For TPS66020: VIN = 0V, VBUS = 3.135 V, I_VBUS_LDO = 30 mA | | | 0.5 | V |
| VDO_VBUS_LDO_5V | Drop out voltage of VDD LDO | For TPS66021: VIN= 0V, VBUS = 4.75V, I_VBUS_LDO = 30 mA | | | 0.5 | V |
| ILIMIT_VBUS_LDO | Current limit VBUS LDO. | VBUS = 5.5V, VIN= 0V, VLDO = 0V | 50 | | 100 | mA |
| $t_{EN_VBUS_LDO}$ | Turn-on time of VBUS LDO. | For TPS66020: I_VBUS_LDO = 30mA, CVLDO = 4.7 µF, VIN = 0V. Ramp $V_{VBUS}$ from 0 to 5V at ≥50V/ms. Measure from VBUS = 4.5V to VLDO = 3V. | | | 1.2 | ms |
| | | For TPS66021: I_VBUS_LDO = 30mA, CVLDO = 4.7 µF, VIN = 0V. Ramp $V_{VBUS}$ from 0 to 7.5V at ≥50V/ms. Measure from VBUS = 7V to VLDO = 4.5V. | | | 1.2 | ms |

## 6.10 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| TSD_PP5V_R | Thermal Shutdown Temperature of the PP5V power path. | Temperature rising | 128 | 150 | 172 | °C |
| TSD_PP5V_F | Thermal Shutdown Temperature of the PP5V power path. | Temperature falling | 115 | 140 | 165 | °C |
| TSDH_PP5V | Thermal Shutdown hysteresis of the PP5V power path. | | | 10 | | °C |
| TSD_PPHV_R | Thermal Shutdown Temperature of the PPHV power path. | Temperature rising | 128 | 150 | 172 | °C |
| TSD_PPHV_F | Thermal Shutdown Temperature of the PPHV power path. | Temperature falling | 115 | 140 | 165 | °C |
| TSDH_PPHV | Thermal Shutdown hysteresis of the PPHV power path. | | | 10 | | °C |
| TSD_MAIN_R | Thermal Shutdown Temperature of the entire device. | Temperature rising | 140 | 160 | 178 | °C |
| TSD_MAIN_F | Thermal Shutdown Temperature of the entire device. | Temperature falling | 120 | 140 | 160 | °C |
| TSDH_MAIN | Thermal Shutdown hysteresis of the entire device. | | | 20 | | °C |


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## 6.11 Input-output (I/O) Characteristics

Operating under these conditions unless otherwise noted: -10 ℃ ≤ $T_J$ ≤ 125 ℃, 2.85 V ≤ $V_{VIN}$ ≤ 5.5V, $R_{IREF}$ = 75 kΩ ±1% overall tolerance

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| EN_Vt+ | Positive going input-threshold voltage, % of VLDO | VLDO = 2.85 - 5.5V | 40 | | 70 | % |
| EN_Vt- | Negative going input-threshold voltage, % of VLDO | VLDO = 2.85 - 5.5V | 30 | | 60 | % |
| EN_HYS | Input hysteresis voltage, % of VLDO | VLDO = 2.85 - 5.5V | | 10 | | % |
| EN_RPD | Pull-down resistance EN pin. | Measured with pin voltage $V_{EN}$ = 3.3V | 500 | 650 | 800 | kΩ |
| EN_CLAMP | Voltage clamp on EN pin. | $I_{EN}$ = 100 µA | | 6 | 7.1 | V |
| FLT_VOL | Output Low Voltage, $\overline{FLT}$ pin | $I_{OL}$ = 2mA, $\overline{FLT}$ driven low. | | | 0.4 | V |
| FLT_ILKG | Leakage Current, $\overline{FLT}$ pin | $\overline{FLT}$ not driven low. | –1 | | 1 | µA |
| $t_{H_FLT}$ | Time $\overline{FLT}$ pin remains asserted low. | | 4 | 10 | 16 | ms |
| $t_{DG_EN}$ | Enable deglitch filter. Pulses on EN0 or EN1 < $t_{DG_EN(MIN)}$ are not propagated to the control logic. Pulses on EN0 or EN1 > $t_{DG_EN(MAX)}$ are propagated to the control logic. Pulses on EN0 or EN1 ≥ $t_{DG_EN(MIN)}$ and ≤ $t_{DG_EN(MAX)}$ may or may not propagate to the control logic. The filter is not applied to EN1 transition to the FRS state. | | 78 | | 242 | µs |

## 6.12 Power Consumption Characteristics

Operating under these conditions unless otherwise noted: -10 ℃ ≤ $T_J$ ≤ 85 ℃, 2.85V ≤ $V_{VIN}$ ≤ 5.5V, $R_{IREF}$ = 75 kΩ ±1% overall tolerance

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{VIN_DISABLE}$ | Current consumed by VIN(1) | VIN = 3.3V, VBUS = 0V, PP5V = 0V, PPHV = 0V, DISABLED state. Measure $I_{VIN}$. TPS66020 only. | | | 19 | 27 | µA |
| | | VIN = 5V, VBUS = 0V, PP5V = 0V, PPHV = 0V, DISABLED state. Measure $I_{VIN}$. TPS66021 only. | | | 25 | 36 | µA |
| $I_{VIN_SRC}$ | Current consumed by VIN(1) | VIN = 3.3V, PP5V = 5.5V, PPHV = 0V, SRC 1.5A or SRC 3.0A state. Measure $I_{VIN}$. TPS66020 only. | | | 136 | | µA |
| | | VIN = 5V, PP5V = 5.5V, PPHV = 0V, SRC 1.5A or SRC 3.0A state. Measure $I_{VIN}$. TPS66021 only. | | | 214 | | µA |
| $I_{VIN_SNK}$ | Current consumed by VIN(1) | VIN = 3.3V, PP5V = 0V, SNK state. Measure $I_{VIN}$. TPS66020 only. | VBUS = 5.5V/22V | | 130 | | µA |
| | | VIN = 5V, PP5V = 0V, SNK state. Measure $I_{VIN}$. TPS66021 only. | VBUS = 5.5V/22V | | 215 | | µA |

(1) Measured with EN0 and/or EN1 set to GND or VLDO levels as required for the respective state.

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## Power Consumption Characteristics (continued)

Operating under these conditions unless otherwise noted: -10 ℃ ≤ $T_J$ ≤ 85 ℃, 2.85V ≤ $V_{VIN}$ ≤ 5.5V, $R_{IREF}$ = 75 kΩ ±1% overall tolerance

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{SD_PP5V}$ | Current consumed by PP5V(1) | VIN = 3.3V, PP5V = 5.5V, PPHV = 0V, VBUS = 0V, DISABLED state. Measure $I_{PP5V}$. TPS66020 only. | | | 2 | | µA |
| | | VIN = 5V, PP5V = 5.5V, PPHV = 0V, VBUS = 0V, DISABLED state. Measure $I_{PP5V}$. TPS66021 only. | | | 2 | | µA |
| $I_{ACT_PP5V}$ | Current consumed by PP5V(1) | VIN = 3.3V, PP5V = 5.5V, PPHV= 0V, SRC 1.5A or SRC 3.0A state. Measure $I_{PP5V}$. TPS66020 only. | | | 109 | | µA |
| | | VIN = 5V, PP5V = 5.5V, PPHV= 0V, SRC 1.5A or SRC 3.0A state. Measure $I_{PP5V}$. TPS66021 only. | | | 109 | | µA |
| $I_{SD_VBUS}$ | Current consumed by VBUS(1) | VIN = 3.3V, PP5V = 0V, PPHV= 0V, DISABLED state. Measure $I_{VBUS}$. TPS66020 only. | VBUS = 5.5V | | 12 | 26 | µA |
| | | | VBUS = 22V | | 34 | | µA |
| | | VIN = 5V, PP5V = 0V, PPHV= 0V, DISABLED state. Measure $I_{VBUS}$. TPS66021 only. | VBUS = 5.5V | | 8 | | µA |
| | | | VBUS = 22V | | 30 | | µA |
| $I_{SD_VBUS_LDO}$ | Current consumed by VBUS(1) | VIN = 0V, PP5V = 0V, PPHV= 0V, DISABLED state. Measure $I_{VBUS}$. | VBUS = 5.5V | | 45 | | µA |
| | | | VBUS = 22V | | 69 | | µA |
| $I_{ACT_VBUS}$ | Current consumed by VBUS(1) | VIN = 3.3V, PP5V = 0V, SNK state. Measure $I_{VBUS}$. TPS66020 only. | VBUS = 5.5V | | 325 | | µA |
| | | | VBUS = 22V | | 360 | | µA |
| | | VIN = 5V, PP5V = 0V, SNK state. Measure $I_{VBUS}$. TPS66021 only. | VBUS = 5.5V | | 342 | | µA |
| | | | VBUS = 22V | | 377 | | µA |
| $V_{OC_VBUS}$ | Open circuit voltage, VBUS | PP5V = 5.5V, PPHV = 22V, DISABLED state, no DC loading on VBUS. Measure $V_{VBUS}$ under steady state conditions. | | | | 0.8 | V |
| $V_{OC_PP5V}$ | Open circuit voltage, PP5V | VBUS = 22V, PPHV = 0V, DISABLED state, no DC loading on PP5V. Measure $V_{PP5V}$ under steady state conditions. | | | | 0.8 | V |
| $V_{OC_PPHV}$ | Open circuit voltage, PPHV | VBUS = 22V, PP5V = 0V, DISABLED state, no DC loading on PPHV. Measure $V_{PPHV}$ under steady state conditions. | | | | 0.8 | V |


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## 6.13 Typical Characteristics

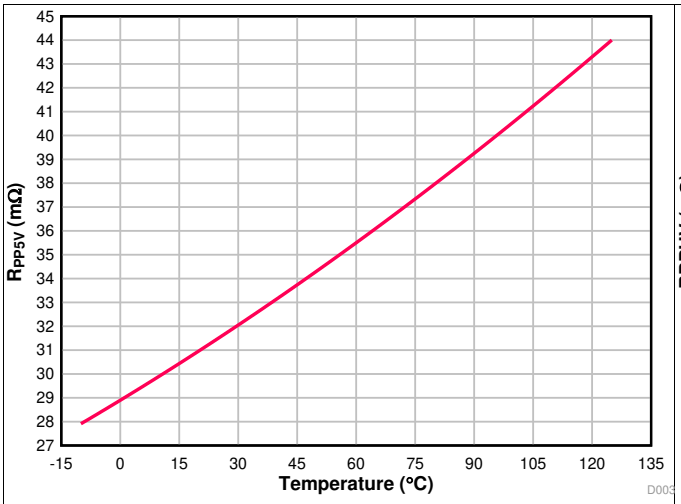



Figure 1. $R_{PP5V}$ versus Temperature

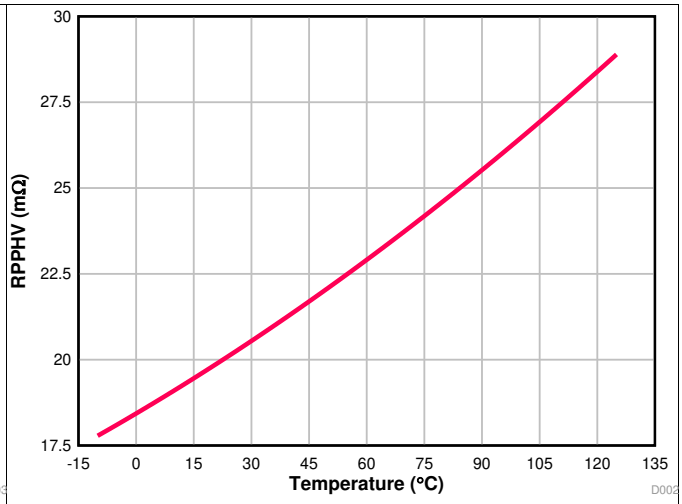



Figure 2. $R_{PPHV}$ versus Temperature

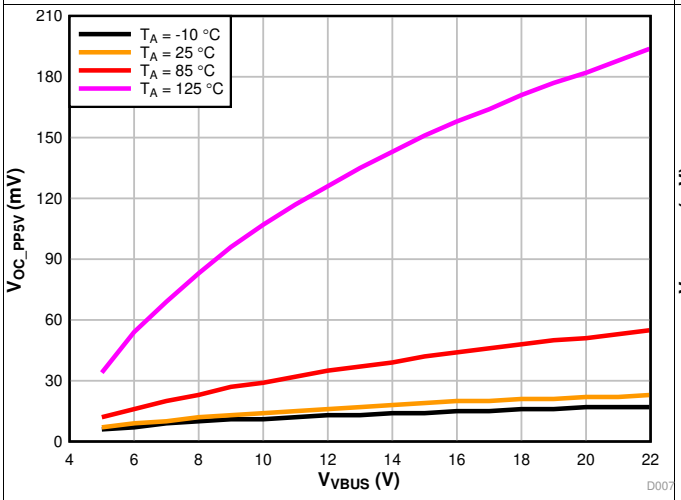



Figure 3. $V_{OC_PP5V}$, PP5V Open Circuit Voltage versus VBUS

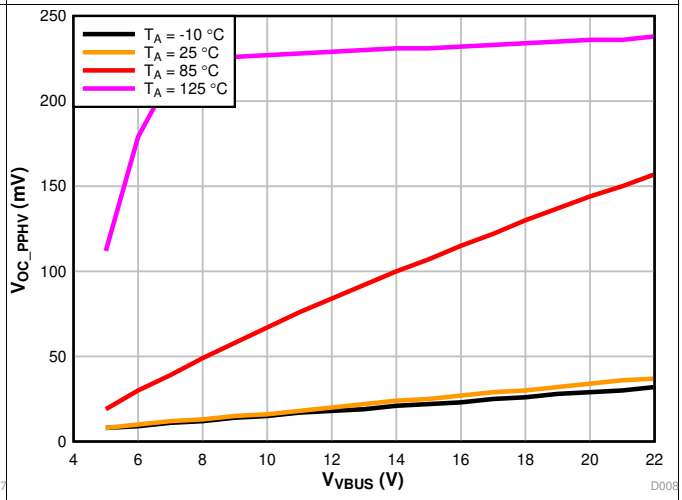



Figure 4. $V_{OC_PPHV}$, PPHV Open Circuit Voltage versus VBUS

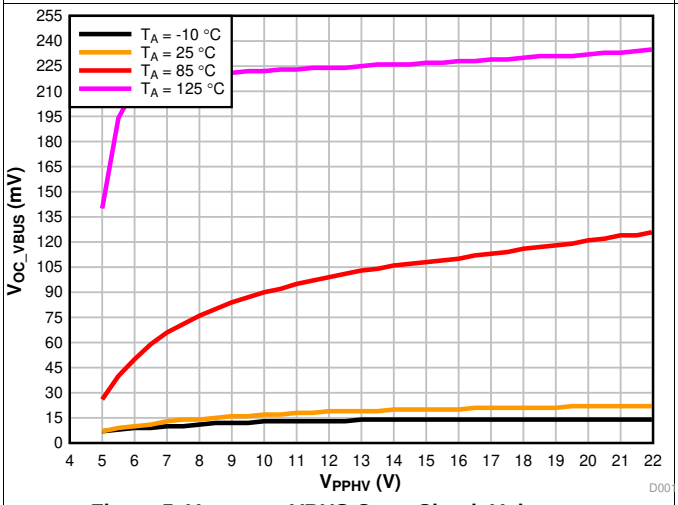



Figure 5. $V_{OC_VBUS}$, VBUS Open Circuit Voltage versus PPHV

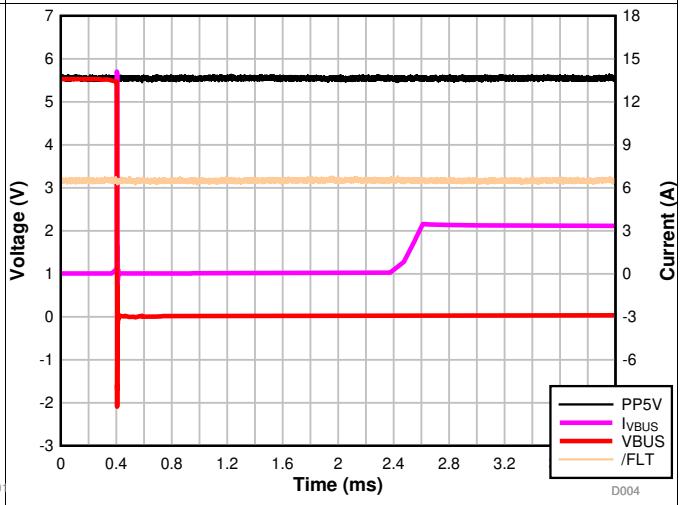



Figure 6. PP5V Current Limit (3 A) Response with Short (Zoomed Out)

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## Typical Characteristics (continued)

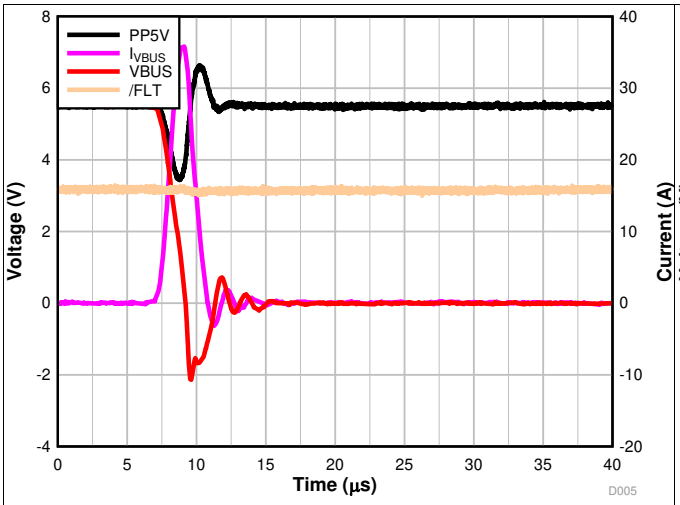



**Figure 7. PP5V Current Limit (3 A) Response with Short (Zoomed In At Time of Short)**

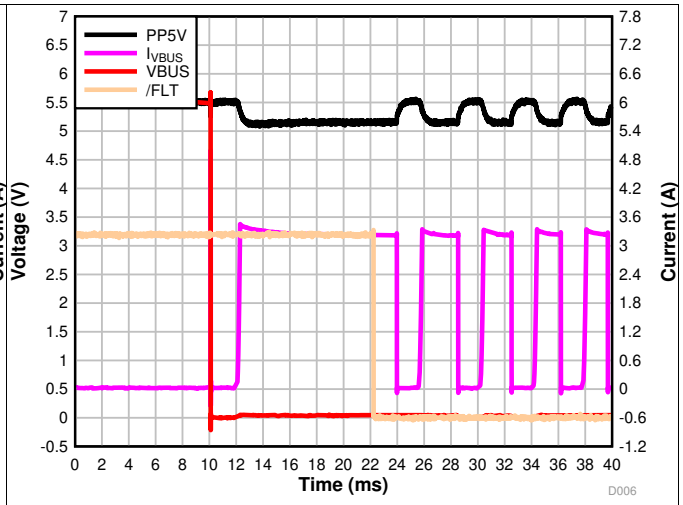



**Figure 8. PP5V Current Limit (3 A) Response with Persistent Short Showing TSD Protection and Recovery**

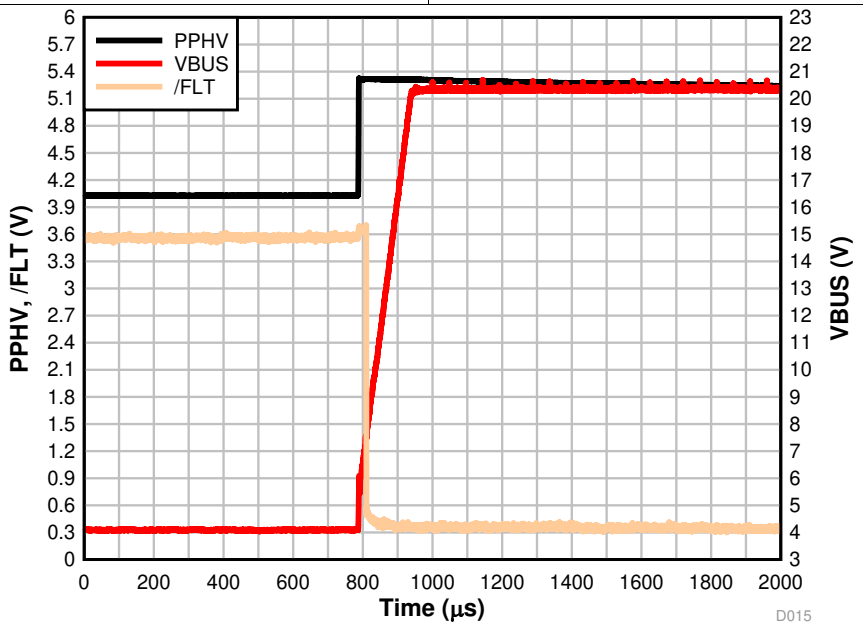



**Figure 9. VBUS OVP Response with 6-V Threshold**


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# 7 Parameter Measurement Information

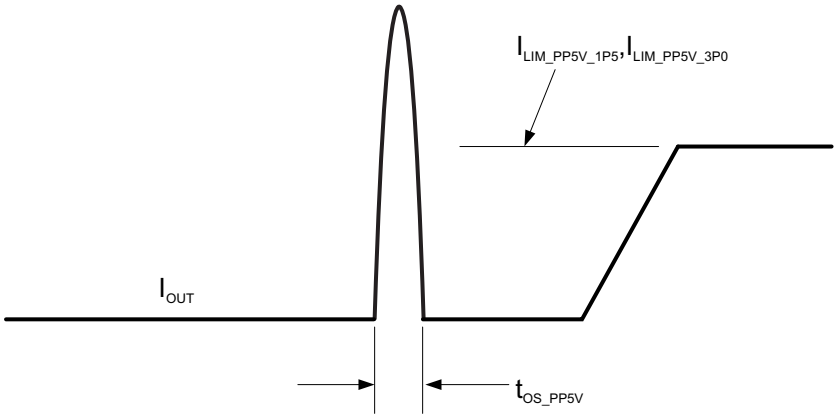



**Figure 10. PP5V to VBUS Short Circuit Parameter Diagram**

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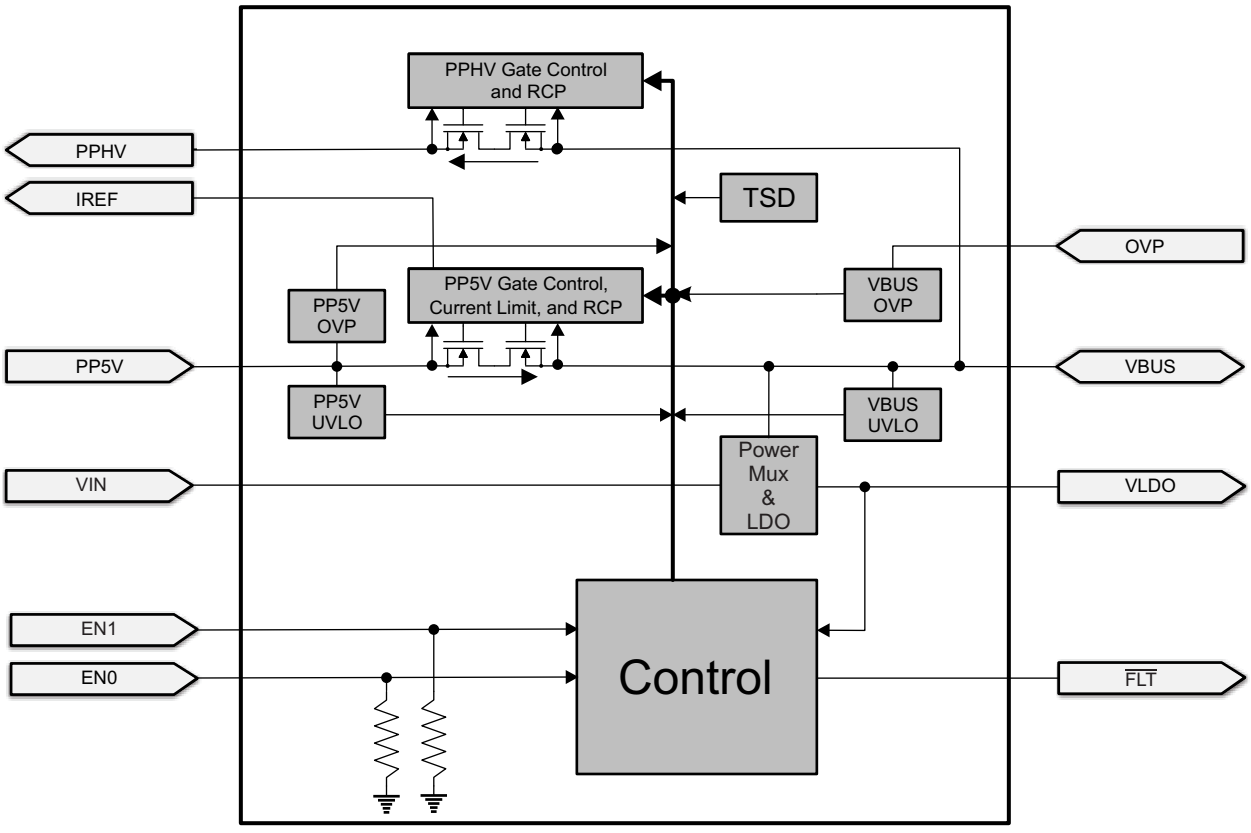
# 8 Detailed Description

## 8.1 Overview

The TPS6602x is a fully featured power multiplexer with an integrated Source power path, a Sink power path, and a high voltage VBUS LDO voltage regulator. The Source power path can supply 5-V nominal power and supports two current limit settings (1.5 A or 3 A) controlled by general-purpose I/O. The Source power path includes current limit protection, overtemperature protection, reverse-current protection, undervoltage protection, and overvoltage protection. See the *5-V Source (PP5V Power Path)* section. The Sink power path can support up to 5 A at 20 V controlled by general-purpose I/O. The Sink power path includes soft-start to minimize in-rush currents, overtemperature protection, reverse-current protection, undervoltage protection, and an optional overvoltage protection configured in the application. See the *20-V Sink (PPHV Power Path)* section. The TPS6602x fully supports Fast Role Swap operation as specified in the Power Delivery specification. See the *Fast Role Swap (FRS)* section.

The VBUS low dropout voltage regulator may be used in systems that require power during dead battery conditions and can provide up to 30 mA to the system via the VLDO pin. Once VIN power is available, VLDO pin power is switched from the VBUS LDO regulator to the VIN pin. The TPS66020 devices VBUS LDO regulator nominally supplies 3.3 V where the TPS66021 device VBUS LDO nominally supplies 5 V. See the *Power Management and Supervisory* section.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 5-V Source (PP5V Power Path)

The PP5V power path uses two back-to-back N-channel MOSFETs, and blocks current in both directions when the power path is disabled. The PP5V power path is a Source only path and when enabled provides power from the PP5V terminal to the VBUS terminal. The PP5V path provides up to 3-A current delivery to VBUS.


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## Feature Description (continued)

#### 8.3.1.1 PP5V Current Limit

The current through PP5V to VBUS current limit may be dynamically selected to support 1.5-A or 3-A operation via EN0 and EN1. An external resistance to GND on IREF terminal is required to set the bias current for accurate current limit operation.

Under overload conditions, the internal current-limit regulator limits the output current to the selected current limit setting, $I_{LIM_PP5V}$, where $I_{LIM_PP5V}$ is $I_{LIM_PP5V_1P5}$ or $I_{LIM_PP5V_3P0}$, as shown in the *PP5V Power Switch Characteristics* table. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by ($I_{LIM_PP5V}$ x $R_{LOAD}$ ). Two possible overload conditions can occur. The first overload condition occurs when either: 1) PP5V input voltage is first applied, PP5V source path is enabled (EN1_EN0 = 10b or EN1_EN0 = 11b), and a short circuit is presented (load which draws $I_{OUT} > I_{LIM_PP5V}$), or 2) PP5V input voltage is present and the PP5V source path is enabled into a short circuit. The output voltage is held near zero potential with respect to ground and the TPS6602x ramps the output current to $I_{LIM_PP5V}$. The TPS6602x limits the current to $I_{LIM_PP5V}$ until the overload condition is removed or the device begins to thermal cycle. This is demonstrated in Figure 31 where the device was enabled into a short, and subsequently cycles current off and on as the thermal protection engages.

The second condition is when an overload occurs while the PP5V source path is enabled and fully turned on. The device responds to the overload condition within time $t_{OS_PP5V}$ (see Figure 10) when the specified overload (per Electrical Characteristics) is applied. The response speed and shape vary with the overload level, input circuit and rate of application. The current-limit response varies between simply settling to $I_{LIM_PP5V}$ or turning off and a controlled return to $I_{LIM_PP5V}$. Similar to the previous case, the TPS6602x limits the current to $I_{LIM_PP5V}$ until the overload condition is removed or the device begins to thermal cycle. The TPS6602x thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation [($V_{PP5V}$ – $V_{VBUS}$) x $I_{LIM_PP5V}$] elevating the junction temperature. The PP5V source path turns off when its temperature reaches its thermal shutdown temperature of TSD_PP5V_R while in current limit. The PP5V source path remains off until its temperature cools to TSD_PP5V_F and then re-enables automatically.

#### 8.3.1.2 PP5V Reverse Current Protection (RCP)

When the PP5V power path is enabled, the RCP circuitry monitors the voltage across the path. If the RCP monitor detects $V_{VBUS}$ - $V_{PP5V}$ ≥ $V_{RCP_THRES_PP5V}$, the PP5V path will be disabled preventing additional current flow from VBUS to PP5V. The power path will be completely disabled and remain disabled as long as the RCP condition persists. After the RCP event, the PP5V path will automatically re-enable. $\overline{FLT}$ is asserted when a reverse current protection event occurs on the PP5V path.

### 8.3.2 20-V Sink (PPHV Power Path)

The PPHV path is a Sink only path, providing power from the VBUS terminal to the PPHV terminal when enabled. The PPHV power path uses two back-to-back N-channel MOSFETs, and blocks current in both directions when the power path is disabled.

#### 8.3.2.1 PPHV Soft Start

The TPS6602x PPHV power path has soft start circuitry to control in-rush current when the PPHV power path is enabled. DC loading should be minimized during soft start since the PPHV path may experience high power dissipation especially at higher VBUS voltages. This may lead to a PPHV overtemperature protection event.

#### 8.3.2.2 PPHV Reverse Current Protection (RCP)

When the PPHV power path is enabled, the RCP circuitry monitors the voltage across the path. If the RCP monitor detects $V_{PPHV}$ - $V_{VBUS}$ ≥ $V_{RCP_THRES_PPHV}$, the PPHV path will be disabled preventing additional current flow from PPHV to VBUS. The power path will be completely disabled and remain disabled as long as the RCP condition persists. After the RCP event, the PPHV path will automatically re-enable. $\overline{FLT}$ is not asserted when a reverse current protection event occurs on the PPHV path.

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## Feature Description (continued)

### 8.3.3 Overtemperature Protection

The PP5V and PPHV power paths each have an integrated temperature sensor to protect these paths from excessive heating. When the sensor in each respective path detects an overtemperature condition, the path will be automatically disabled (if enabled) and cannot be enabled until the overtemperature condition has been removed. $\overline{FLT}$ is asserted when an overtemperature event occurs.

In addition, the device has an integrated main temperature sensor. When the sensor detects an overtemperature condition, the PP5V and PPHV power paths and the VBUS LDO of the device are completely disabled until the overtemperature condition has been removed.

### 8.3.4 VBUS Overvoltage Protection (OVP)

TPS6602x supports overvoltage protection on the VBUS terminal. When the voltage detected on OVP exceeds a set level, the PPHV power path will automatically be disabled (if enabled), and will remain disabled until the OVP event is removed. $\overline{FLT}$ is asserted when an overvoltage event occurs. The VBUS OVP threshold may be set using a resistor divider from VBUS to GND, whose divider output is connected to the OVP terminal as shown in Figure 11. Table 1 shows resistor divider settings for common USB Power Delivery fixed voltage supply contracts along with the resulting nominal OVP thresholds. These thresholds may be adjusted based on desired margins for a given application. If VBUS OVP is not required or needs to be disabled, the OVP terminal may be tied or driven to GND as shown in Figure 12. Lastly, as one example implementation, the OVP threshold may be controlled dynamically using outputs from a PD controller or microcontroller as shown in Figure 13. By selecting each output, different VBUS OVP threshold settings are possible.

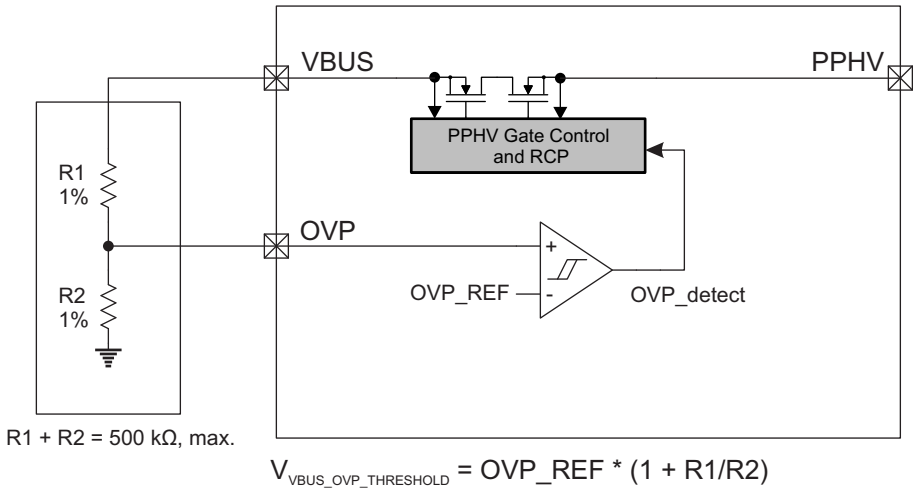



**Figure 11. VBUS OVP Threshold Set by External Resistor Divider**

**Table 1. Typical External Resistor Divider Settings**

| PD Fixed Contract | R1, kΩ | R2, kΩ | Nominal VBUS OVP Threshold, V |
|---|---|---|---|
| 5 V | 102 | 20 | 6.1 |
| 9 V | 182 | 20 | 10.1 |
| 15 V | 309 | 20 | 16.5 |
| 20 V | 432 | 20 | 22.6 |


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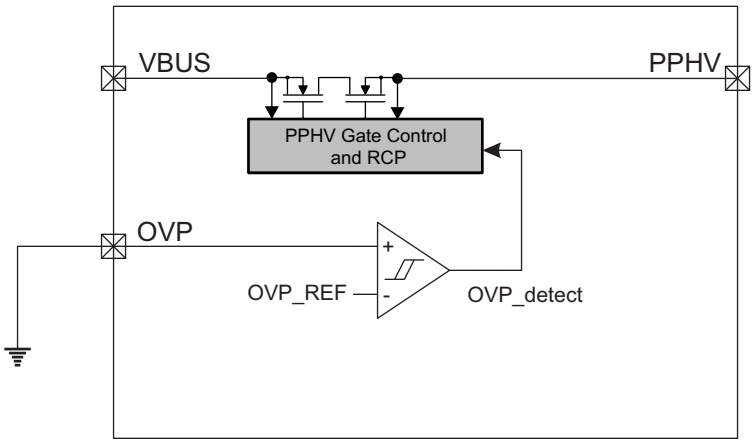



**Figure 12. VBUS OVP Disabled**

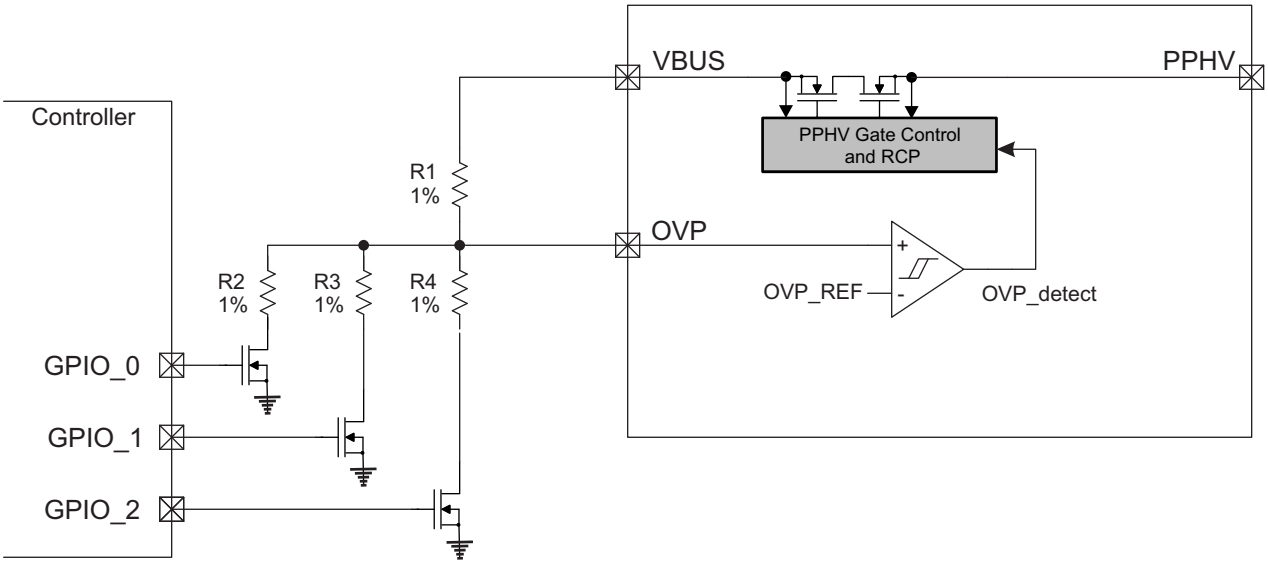



**Figure 13. Selectable VBUS OVP Thresholds**

### 8.3.5 Power Management and Supervisory

The TPS6602x Power Management block receives power from VIN or VBUS and generates voltages to provide power to the TPS6602x internal circuitry, as well as, provides power to VLDO. The power supply management and supervisory block is shown in Figure 14.

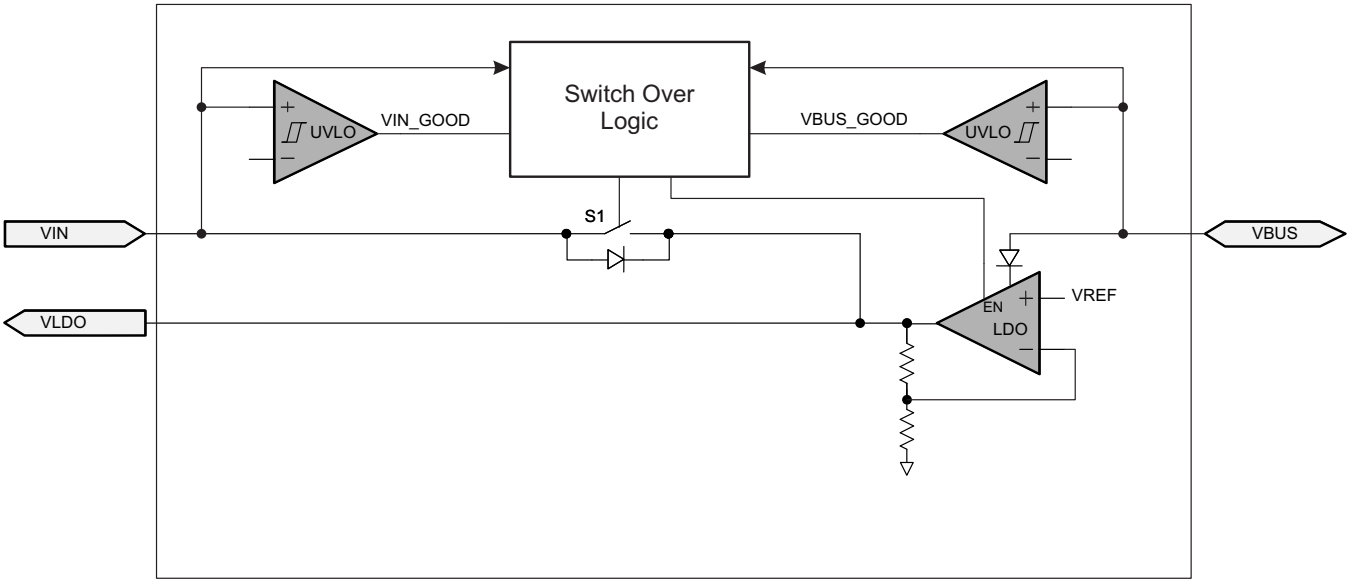



**Figure 14. Power Management and Supervisory**

The VLDO terminal may be powered from either VIN or VBUS. The normal power supply input is VIN. When VIN is present, S1 is closed and current flows from VIN to VLDO and the VBUS LDO is disabled. When VIN power is unavailable, as in a dead battery condition, the VBUS LDO will be automatically enabled when VBUS is present, and the VLDO terminal is powered by the VBUS LDO. The Switch Over Logic provides the decision making capability to choose VIN or VBUS power, depending on the state of these voltages (based on their respective UVLO comparators) and their relative levels to each other.

#### *8.3.5.1 Supply Connections*

Figure 15 shows the TPS66020 VIN being supplied from a 3.3-V supply. The VLDO output may or may not be used to supply other circuitry in the application, for example a PD Controller. During a dead battery condition, the internal 3.3-V VBUS LDO provides power to the TPS66020 and the VLDO output. Once VIN input supply becomes available, the VBUS LDO is disabled and VIN provides power to the VLDO output.

The TPS66021 is well suited for 5 V only systems. VIN of the TPS66021 may be powered from an independent supply, but in most applications it will be connected to the PP5V supply. Figure 16 shows where the VIN supply is shared with PP5V. The VLDO output may be used optionally to supply power to external circuitry. During a dead battery condition, the internal 5-V VBUS LDO provides power to the TPS66021 and the VLDO output. Once the VIN input supply, in this case PP5V, becomes available, the VBUS LDO is disabled and PP5V provides power to the VLDO output.


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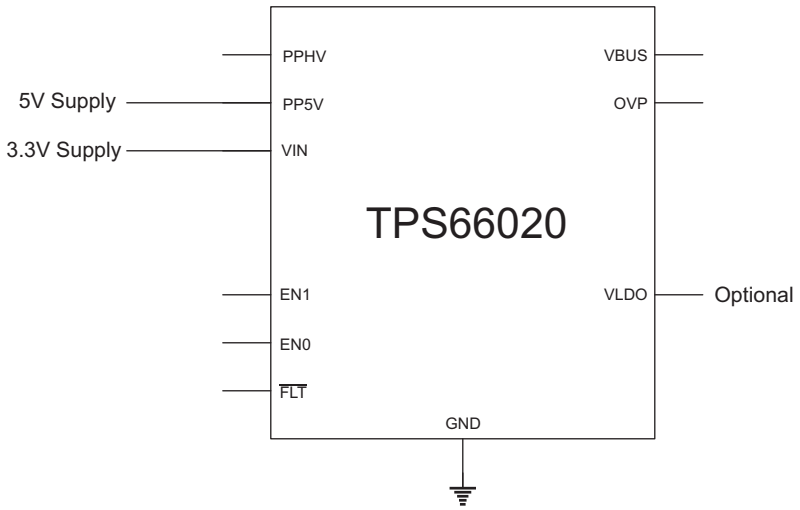



**Figure 15. TPS66020 VIN 3.3-V Supply**

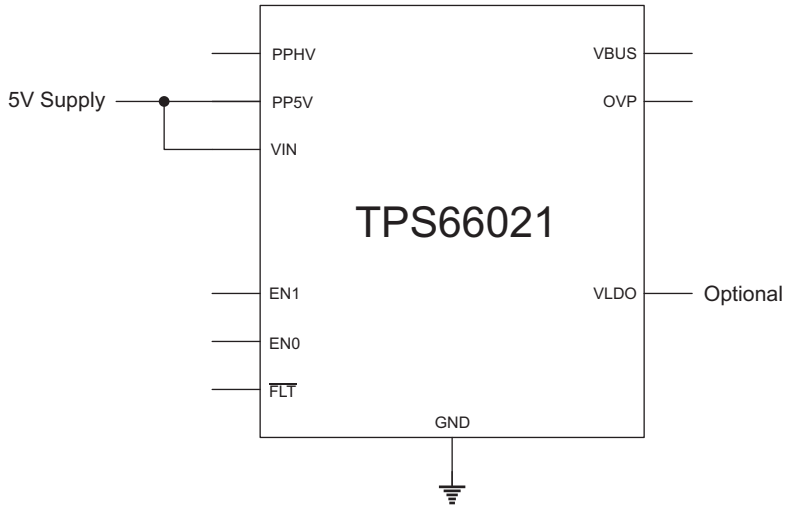
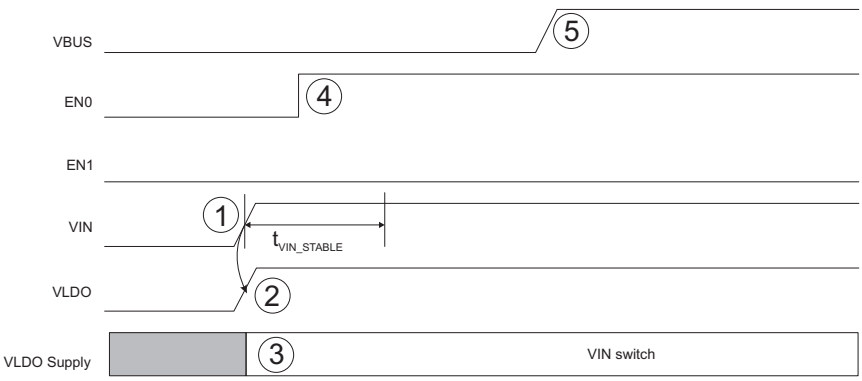



**Figure 16. TPS66021 VIN 5-V Shared Supply**

### *8.3.5.2 Power Up Sequences*

#### 8.3.5.2.1 Normal Power Up

Figure 17 shows a typical power up sequence. During normal power up, VIN supplies power to the TPS6602x. In this case, VBUS remains powered down. It is assumed a PD Controller is controlling the TPS6602x, and Sink operation is being requested.




1. Both the VBUS and VIN supplies are powered down. VIN supply begins to rise.

2. VLDO terminal begins to rise.

3. VLDO supplied by VIN via switch S1. VBUS LDO remains disabled.

4. PD Controller requests Sink path to be enabled. Since VIN supply has not been above its UVLO threshold for $t_{VIN_STABLE}$, Sink path remains disabled. In addtion, VBUS is not above its UVLO switch threshold, which also keeps the Sink path disabled.

5. VIN supply remained above its UVLO threshold for $t_{VIN_STABLE}$ and VBUS is above its UVLO threshold. The Sink path enables. VBUS LDO remains disabled since VIN supply is available.

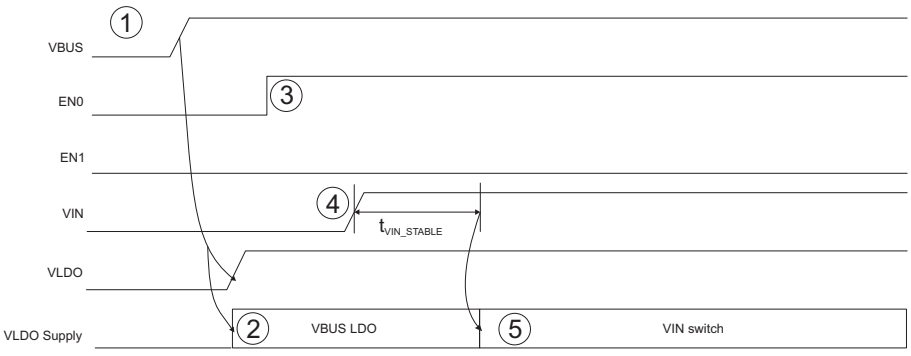
**Figure 17. Normal Power Up Sequence**

#### 8.3.5.2.2 Dead Battery Operation

Figure 18 shows the typical power up sequence during a dead battery condition. During a dead battery condition, the TPS6602x is internally powered by the VBUS LDO. The VBUS LDO may be used to supply a limited amount of current for use in the system during dead battery, such as supplying power to a PD controller. In this case, it is assumed the VLDO terminal is providing power to a PD controller that is controlling the TPS6602x. Once VIN is stable, the VLDO terminal switches from being supplied by the VBUS LDO to being supplied by the VIN terminal, and the VBUS LDO is automatically disabled. The switch over process is completely seamless.

**NOTE**

Switching from VBUS LDO operation to VIN operation is seamless and no device reset will occur. When switching from VIN power to VBUS LDO operation, the switch over circuitry will attempt to switch over to the VBUS LDO, however it is not assured that the VLDO level will be maintained above the VLDO UVLO threshold. In this case, a device reset may or may not occur.




1. Device is in dead battery condition. PD controller advertises as a Sink. Upon connection to a Source, VBUS begins to rise.

2. VBUS LDO is selected by the power management logic and VLDO begins to rise.

3. PD Controller negotiates a contract (may be 5V or higher) and asserts EN0 to turn on the PPHV Sink path in order to charge the system.

4. System begins to charge and VIN begins to rise. VIN passes its UVLO threshold.

5. If VIN supply remains above its UVLO threshold for $t_{VIN_STABLE}$, VBUS LDO is disabled and VLDO is switched over to be supplied by VIN via switch S1.

**Figure 18. Dead Battery Power Up Sequence**


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## 8.4 Device Functional Modes

### 8.4.1 State Transitions

EN0 and EN1 are used by the application to control the state of the device. Figure 19 shows the supported state transitions.

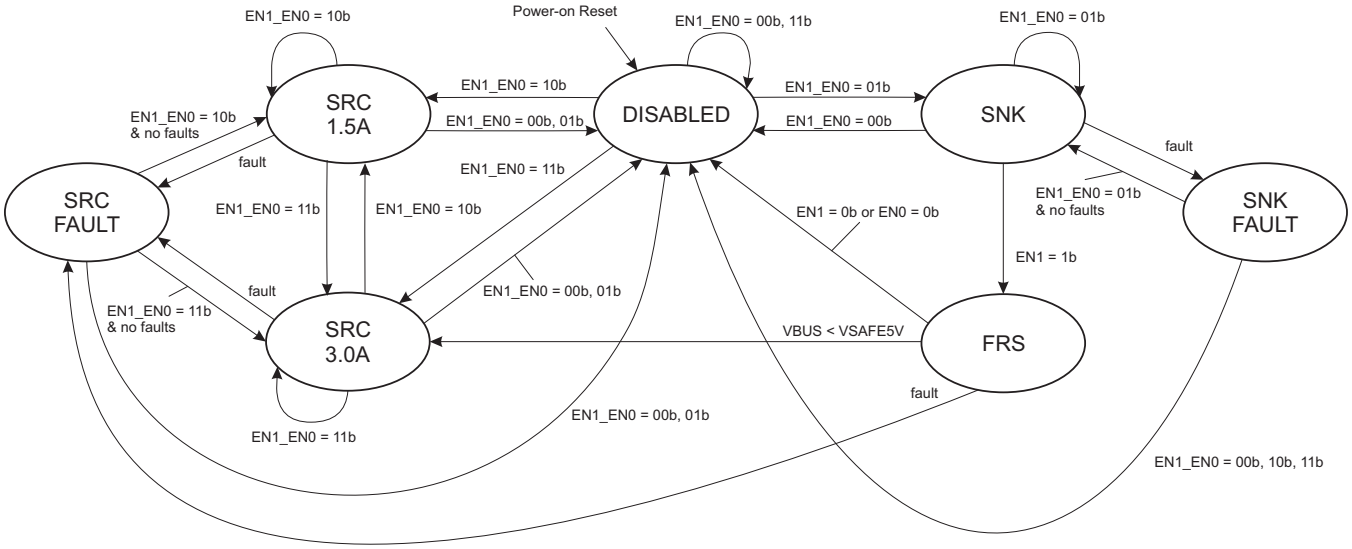



**Figure 19. TPS6602x Functional State Diagram**

#### *8.4.1.1 DISABLED State*

In the DISABLED state, EN1 = 0, EN0 = 0. While in the DISABLED state:

- PP5V power path is disabled
- PP5V current limit, overvoltage, overtemperature, and reverse current protections are disabled
- PPHV power path is disabled
- PPHV overtemperature, reverse-current, and VBUS overvoltage protections are disabled
- VIN and VBUS undervoltage lockout are enabled

The following transitions are possible from the DISABLED state:

- SRC 1.5-A state if (EN1 = 1) and (EN0 = 0) and (PP5V UVLO event not detected) and (PPHV path is completely off)
- SRC 3.0-A state if (EN1 = 1) and (EN0 = 1) and (PP5V UVLO event not detected) and (PPHV path is completely off)
- SNK state if (EN1 = 0) and (EN0 = 1) and (VBUS UVLO event not detected) and (PP5V is completely off)

#### *8.4.1.2 SRC 1.5-A State*

In the SRC 1.5-A state, EN1 = 1, EN0 = 0. While in the SRC 1.5-A state:

- PP5V power path is enabled with current limit set to $I_{LIM_PP5V_1P5}$
- PP5V overvoltage, overtemperature and reverse current protections are enabled
- PPHV power path is disabled
- PPHV overtemperature, reverse-current and VBUS overvoltage protections are disabled
- VIN and PP5V undervoltage lockout are enabled

The following transitions are possible from the SRC 1.5-A state:

- SRC 3-A state if (EN1 = 1) and (EN0 = 1)
- DISABLED state if:
  - (EN1 = 0) and (EN0 = 0) -or-
  - (EN1 = 0) and (EN0 = 1)

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## Device Functional Modes (continued)

- SRC FAULT state if:
  - PP5V UVLO, PP5V OVP, or PP5V RCP event detected -or-
  - PP5V current limit and PP5V TSD events detected

#### 8.4.1.3 SRC 3-A State

In the SRC 3-A state, EN1 = 1, EN0 = 1. While in the SRC 3-A state:

- PP5V power path is enabled with current limit set to $I_{LIM_PP5V_3P0}$
- PP5V overvoltage, overtemperature and reverse current protections are enabled
- PPHV power path is disabled
- PPHV overtemperature, reverse-current, and VBUS overvoltage protections are disabled
- VIN and PP5V undervoltage lockout are enabled

The following transitions are possible from the SRC 3-A state:

- SRC 1.5-A state if (EN1 = 1) and (EN0 = 0)
- DISABLED state if:
  - (EN1 = 0) and (EN0 = 0) -or-
  - (EN1 = 0) and (EN0 = 1)
- SRC FAULT state if:
  - PP5V UVLO, PP5V OVP, or PP5V RCP event detected -or-
  - PP5V current limit and PP5V TSD events detected

#### 8.4.1.4 SNK State

In the SNK state, EN1 = 0, EN0 = 1. While in the SNK state:

- PP5V power path is disabled
- PP5V overvoltage, overtemperature and reverse current protections are disabled
- PPHV power path is enabled
- PPHV overtemperature, VBUS overvoltage (if OVP terminal not grounded) and reverse-current protections are enabled
- VIN and VBUS undervoltage lockout are enabled

The following transitions are possible from the SNK state:

- FRS (Fast Role Swap) state
- DISABLED state if:
  - (EN1 = 0) and (EN0 = 0)
- SNK FAULT state if:
  - VBUS OVP (if OVP terminal not grounded) event detected -or-
  - PPHV TSD event detected

#### 8.4.1.5 FRS (Fast Role Swap) State

In the FRS state, EN1 = 1, EN0 = 1. The FRS state is a transitional state, that transitions automatically from the SNK state to the SRC 3-A state upon successful completion of the fast role swap sequence:

- PPHV power path is automatically disabled
- PPHV overtemperature, VBUS overvoltage (if OVP terminal not grounded) protections are disabled
- VIN and PP5V undervoltage lockout are enabled
- PP5V power path is automatically enabled along with its overvoltage, overtemperature and RCP protection circuits upon successfully completing the fast role swap sequence.

The following transitions are possible from the FRS state:

- SRC 3-A state. This transition is automatic upon successful completion of the fast role swap sequence.
- DISABLED state if:
  - (EN1 = 0) or (EN0 = 0). This may allow for exiting a FRS sequence depending on the current status of the


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## Device Functional Modes (continued)

FRS sequence.

- SRC FAULT state if:
  - PP5V UVLO, PP5V OVP event detected -or-
  - PP5V current limit and PP5V TSD events detected

### 8.4.2 SRC FAULT State

The SRC FAULT state is entered when any PP5V fault event is detected. Upon entering the SRC FAULT state, the PP5V power path is disabled. The following transitions are possible from the SRC FAULT state:

- DISABLED state if:
  - (EN1 = 0) and (EN0 = 0) -or-
  - (EN1 = 0) and (EN0 = 1)
- SRC 1.5-A state if:
  - (EN1 = 1) and (EN0 = 0) -and-
  - PP5V TSD, PP5V OVP, PP5V RCP, PP5V UVLO, and PP5V current limit events are not detected.
- SRC 3-A state if:
  - (EN1 = 1) and (EN0 = 1) -and-
  - PP5V TSD, PP5V OVP, PP5V RCP, PP5V UVLO, and PP5V current limit events are not detected.

### 8.4.3 SNK FAULT State

The SNK FAULT state is entered when any PPHV fault event is detected. Upon entering the SNK FAULT state, the PPHV power path is disabled. The following transitions are possible from the SNK FAULT state:

- DISABLED state if:
  - (EN1 = 1) or (EN0 = 0)
- SNK state if:
  - (EN1 = 0) and (EN0 = 1) -and-
  - PPHV TSD, VBUS OVP (if OVP terminal not grounded) events are not detected

### 8.4.4 Device Functional Mode Summary

Table 2 summarizes the functional modes for the TPS6602x. As shown, the enabling and disabling of the respective Source or Sink is dependent upon the voltages present on PP5V and VBUS, as well as, the EN0 and EN1 control signals.

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## Device Functional Modes (continued)

**Table 2. TPS6602x Device Functional Modes(1)**

| EN1 | EN0 | VIN | $V_{VBUS}$ | $V_{PP5V}$ | $\overline{FLT}$ | Device State | Source Path | Sink Path |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | ≥ UV_VIN | X | X | Hi-Z | DISABLED | Disabled<br>Safety engaged. | Disabled<br>Safety engaged. |
| 1 | 0 | ≥ UV_VIN | X | ≥ UV_PP5V | Hi-Z | SRC 1.5 A | Enabled<br>RCP, OVT, ILIM 1.5-A enabled. | Disabled<br>Safety engaged. |
| | | | | | L | SRC FAULT | Disabled<br>OVP, OVT, ILIMIT, or RCP event. | Disabled<br>Safety engaged. |
| | | | | < UV_PP5V | L | SRC FAULT | Disabled<br>PP5V UVLO event. | Disabled<br>Safety engaged. |
| 1 | 1 | ≥ UV_VIN | X | ≥ UV_PP5V | Hi-Z | SRC 3 A | Enabled<br>RCP, OVT, ILIM 3-A enabled. | Disabled<br>Safety engaged. |
| | | | | | L | SRC FAULT | Disabled<br>OVP, OVT, ILIMIT, or RCP event. | Disabled<br>Safety engaged. |
| | | | | < UV_PP5V | L | SRC FAULT | Disabled<br>PP5V UVLO event. | Disabled<br>Safety engaged. |
| 0 | 1 | ≥ UV_VIN | ≥ UV_VBUS | X | Hi-Z | SNK | Disabled<br>Safety engaged. | Enabled<br>RCP, OVT enabled |
| | | | | X | Hi-Z | SNK FAULT | Disabled<br>Safety engaged. | Enabled with Blocking RCP event. |
| | | | | X | L | SNK FAULT | Disabled<br>Safety engaged. | Disabled<br>OVP(2) or OVT event. |
| | | | < UV_VBUS | X | Hi-Z | SNK FAULT | Disabled<br>Safety engaged. | Disabled<br>VBUS UVLO event. |
| 1 | 1 | ≥ UV_VIN | ≥ vSafe5V | ≥ UV_PP5V | Hi-Z | FRS | Disabled<br>OVT, ILIM 3-A enabled | Disabled<br>Safety engaged. |
| | | | < vSafe5V | ≥ UV_PP5V | Hi-Z | SRC 3 A | Enabled<br>RCP, OVT, ILIM 3-A enabled | Disabled<br>Safety engaged. |
| | | | | ≥ UV_PP5V | L | SRC FAULT | Disabled<br>OVP, OVT, ILIMIT, or RCP event. | Disabled<br>Safety engaged. |
| | | | | < UV_PP5V | L | SRC FAULT | Disabled<br>PP5V UVLO event. | Disabled<br>Safety engaged. |
| X | X | < UV_VIN | < UV_VBUS | X | Hi-Z | DISABLED | Disabled<br>Safety engaged. | Disabled<br>Safety engaged. |
| 0 | 0 | < UV_VIN | ≥ UV_VBUS | X | Hi-Z | DISABLED | Disabled<br>Safety engaged. | Disabled<br>Safety engaged. |
| 1 | 0 | < UV_VIN | ≥ UV_VBUS | ≥ UV_PP5V | L | SRC FAULT | Disabled<br>RCP, OVT, ILIM 1.5A enabled | Disabled<br>Safety engaged. |
| 1 | 1 | < UV_VIN | ≥ UV_VBUS | ≥ UV_PP5V | L | SRC FAULT | Disabled<br>RCP, OVT, ILIM 3A enabled | Disabled<br>Safety engaged. |

(1) X: do-not-care.
(2) When OVP function used and VBUS exceeds OVP threshold, $V_{VBUS_OVP_THRESHOLD}$.


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## Device Functional Modes (continued)

**Table 2. TPS6602x Device Functional Modes[0] (continued)**

| EN1 | EN0 | VIN | $V_{VBUS}$ | $V_{PP5V}$ | $\overline{FLT}$ | Device State | Source Path | Sink Path |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | < UV_VIN | ≥ UV_VBUS(3) | X | Hi-Z | SNK | Disabled<br>Safety engaged. | Enabled<br>RCP, OVT enabled |
| | | | | X | Hi-Z | SNK FAULT | Disabled<br>Safety engaged. | Enabled with Blocking<br>RCP event. |
| | | | | X | L | SNK FAULT | Disabled<br>Safety engaged. | Disabled<br>OVP(2) or OVT event. |
| | | | < UV_VBUS(3) | X | Hi-Z | SNK FAULT | Disabled<br>Safety engaged. | Disabled<br>VBUS UVLO event. |

(3) In this case VLDO is supplying power to the device.

### 8.4.5 Enabling the PP5V Source Path

The timing diagram of enabling the PP5V Source path with a current limit set to 1.5 A is shown in Figure 20. As shown, transitions from either the Source path to the Sink path or vice-versa always requires a transition first to the DISABLED state, EN1_EN0 = 00b. Figure 21 shows the timing diagram going from a Sink to a 3-A Source. Figure 22 shows changing the current limit back to 1.5 A from its original 3-A setting.

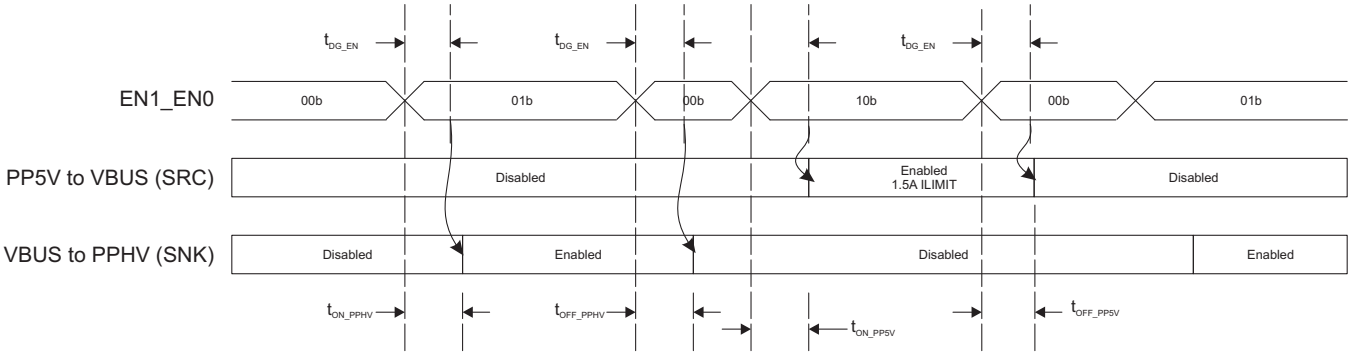



**Figure 20. Enabling the PP5V Source Path to 1.5-A Current Limit**

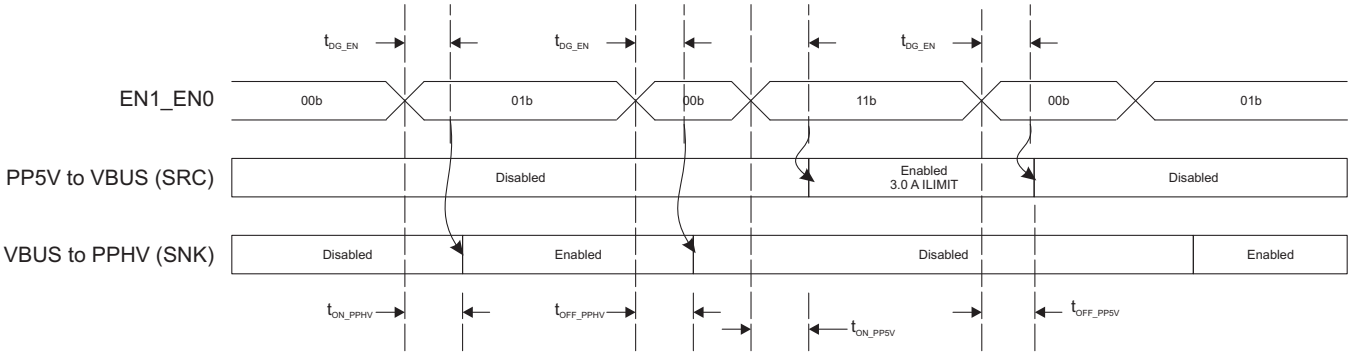



**Figure 21. Enabling the PP5V Source Path to 3-A Current Limit**

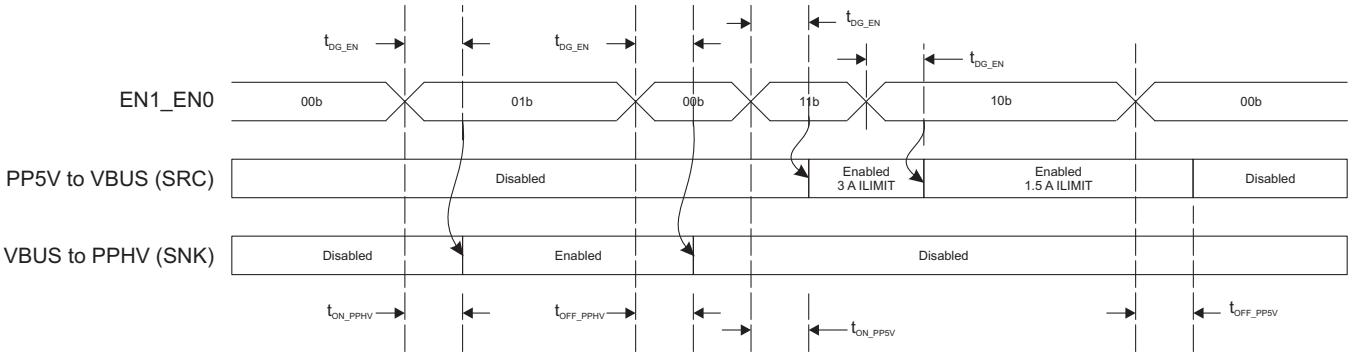



**Figure 22. Changing the PP5V Source Path from 3-A to 1.5-A Current Limit**

### 8.4.6 Enabling the PPHV Sink Path

The timing diagram of enabling the PPHV Sink path is shown in Figure 23. As stated earlier, transitions from either the Source path to the Sink path or vice-versa always requires a transition first to the DISABLED state, EN1_EN0 = 00b.

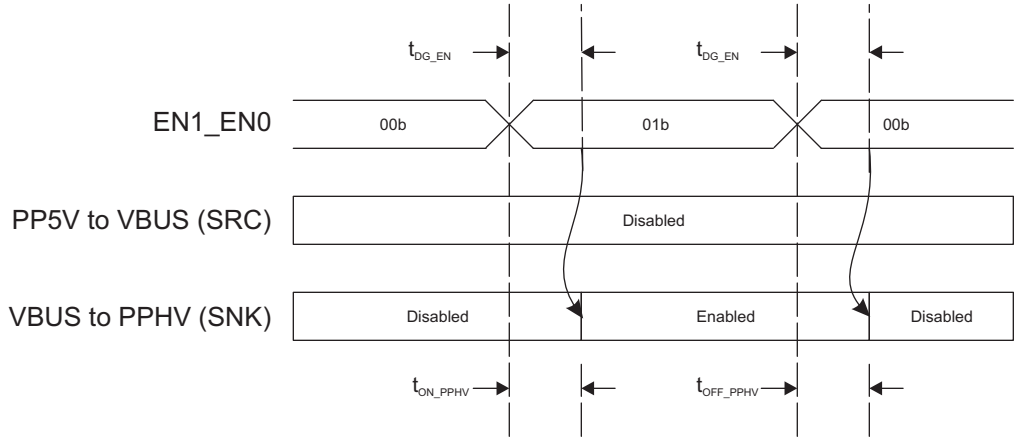



**Figure 23. Enabling the PPHV Sink Path**

### 8.4.7 Fast Role Swap (FRS)

#### *8.4.7.1 Overview*

For a hub application, the hub may be supplied by an external power source that is supplying power to a Host (via the Source path of the dual-role power (DRP) of the hub), as well as, a downstream Bus Powered Device (BPD) (DFP Source to the BPD). A communication path is formed from Host to the Bus Powered Device. Prior to FRS, power flows from the external power source to the Host and the Bus Powered Device. If the external power is removed, FRS operation will attempt to change the power role of the Host to a Source and the hub DRP port to a Sink allowing power to change direction from the Host to the BPD in an attempt to maintain the connection. It should be noted that after FRS, the contract is 5 V. Refer to the PD3.0 specification for further details on the Fast Role Swap function.

Two PD controllers are used in the FRS process. One PD controller resides on the Host side (USB PD Capable Host); the other resides on the hub side (USB PD Capable Hub). Both PD controllers are DRP since they must support power role swapping. Prior to FRS, the Hub DRP is a Source (known as the old Source) and may be supplying power to the DRP Host, which is acting as a Sink (known as the old Sink). After FRS, the Host DRP is a 5-V Source (known as the new Source, old Sink), and is supplying power to the Hub DRP configured as a Sink (known as the new Sink, old Source).


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### 8.4.7.2 Fast Role Swap Use Cases

When the TPS6602x is used on the Host side, prior to a FRS event, the PD Controller power role is the Sink (old Sink). Since the TPS6602x only supports Sink operation via PPHV, PPHV is configured as a Sink (old Sink) and is receiving power from VBUS. Upon fast role signaling from the Hub, the TPS6602x power role will change to a Source (new Source) via the PP5V path.

**NOTE**

The TPS6602x does not support a fast turn-on of the PPHV path, so it cannot be used effectively as a new Sink in a fast role condition. Fast turn-on is only possible with the PP5V (Source only path) for fast role swap scenarios.

Figure 24 shows the supported TPS6602x usage case before and after a fast role swap. The TPS6602x is used in the Host DRP. Prior to a fast role swap, PPHV is configured as a Sink (old Sink) and the PP5V path is disabled. Once a Fast Role Swap signal is requested by the PD Controller, by the transition of EN1_EN0 from 01b to 11b, the TPS6602x disables its PPHV path, waits until VBUS drops vSafe5V (maximum) and then quickly enables the PP5V path, which is now the new Source.

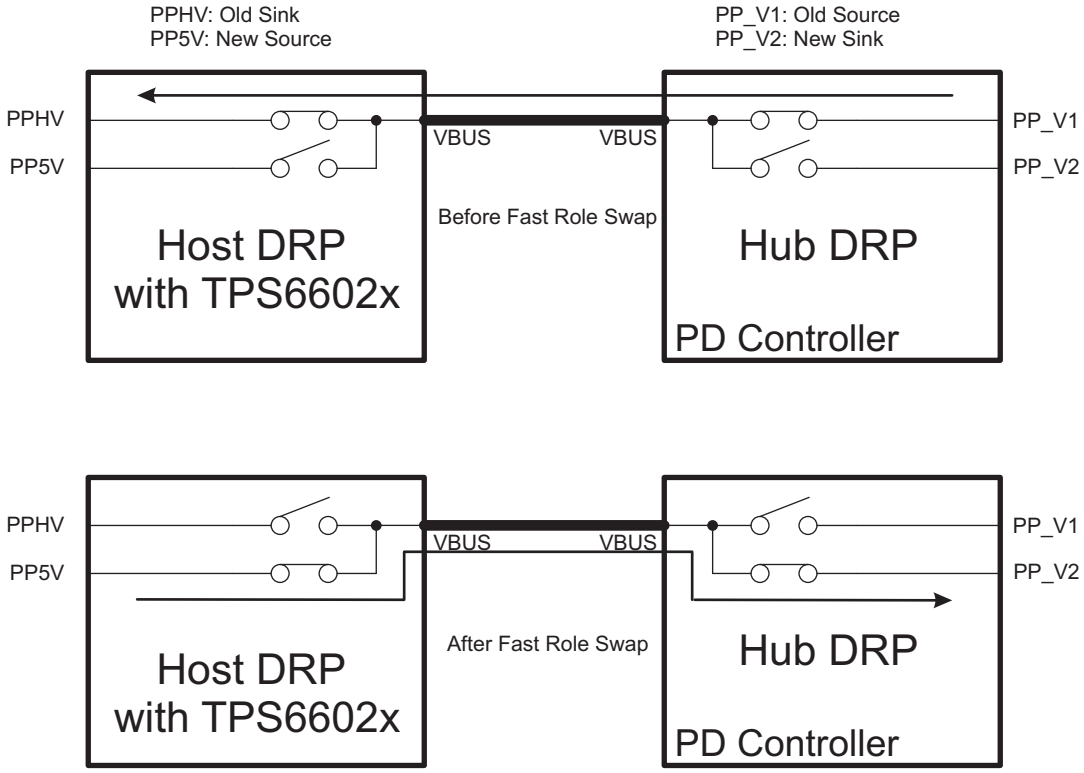



**Figure 24. TPS6602x Fast Role Swap Usage Case**

### 8.4.7.3 Fast Role Swap Sequence

The TPS6602x supports specialized hardware to minimize unnecessary delays upon a Fast Role Swap event. Figure 25 shows the fast role swap sequencing.

1. At some point, the Hub device connected to the Host detects a power loss condition and begins to transmit fast role swap signaling on its CC line to the Host PD Controller.
2. The Host PD Controller's CC detection circuitry detects fast role swap signaling applied by observing the CC line and is validated.
3. Upon validating the FRS signaling, the Host PD Controller shall assert EN1 = 1 of the TPS6602x as soon as possible to initiate the power role swap. It should be noted that since the transition of the FRS is initiated by the PD Controller, it is critical that the delay from detection of the FRS signaling to the assertion of EN1 be minimized.

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4. Upon EN1 = 1 assertion, the TPS6602x PPHV path is disabled automatically by the fast role swap hardware.
5. There are two cases to consider. In Case 1, as shown in Figure 26, VBUS begins to decay, while being continuously monitored by the vSafe5V comparator circuitry that indicates when VBUS has fallen below vSafe5V. Once this occurs, the comparator output is asserted indicating to the fast role swap hardware that it is safe to turn on the PP5V path, and the PP5V path is enabled automatically. In Case 2, as shown in Figure 27, VBUS may have fallen below vSafe5V, or even fully discharged to ground, so the comparator output may already be asserted low. If so, the PP5V path shall be immediately enabled. It should be noted in this scenario, since the VBUS capacitance has been fully discharged, a significant in-rush current will occur when the PP5V path is enabled. Application should ensure sufficient decoupling capacitance is applied on the PP5V supply or that the supply is designed to react to fast transient responses to avoid brown-out of the supply rail.
6. PP5V is initially enabled with a higher current limit to ensure fast turn-on. Once fast role swap is completed, it reverts back to the 3-A setting. The application may then choose to stay at the 3-A setting or switch to the 1.5-A setting.

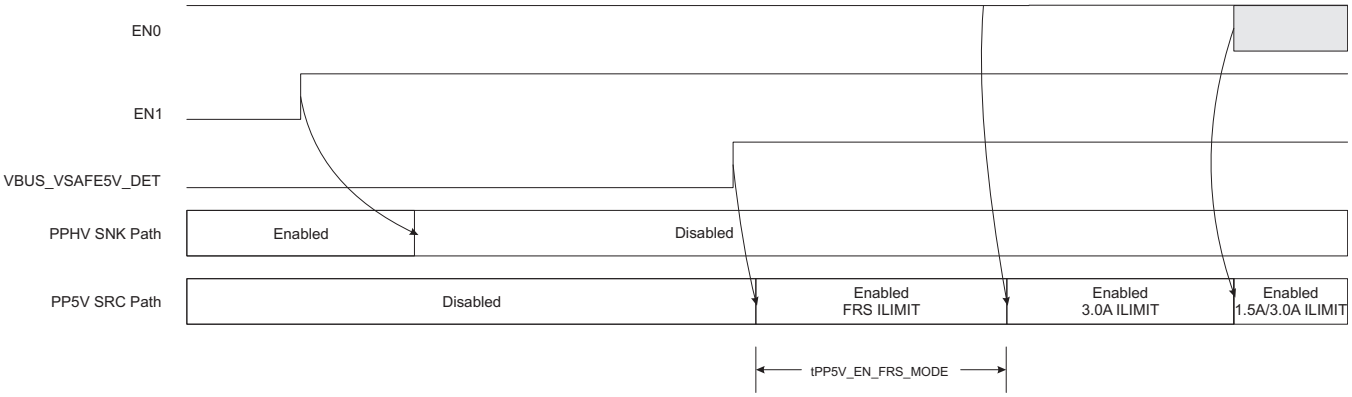



**Figure 25. Fast Role Swap Timing**

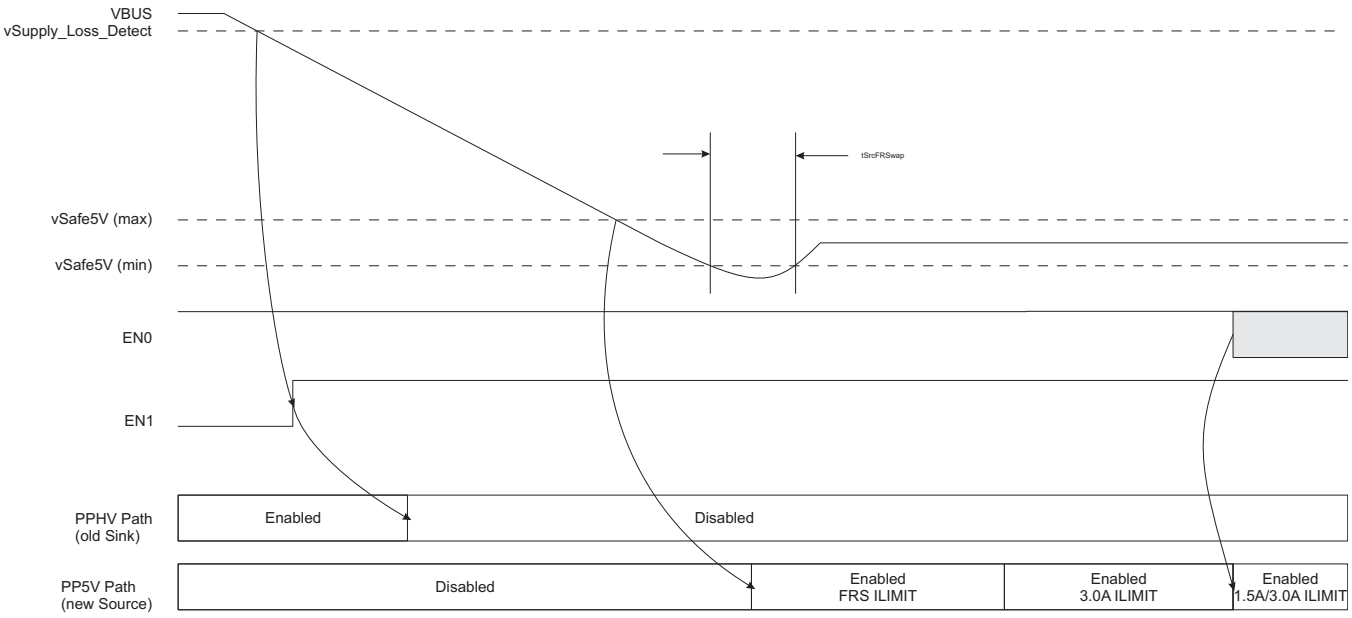



**Figure 26. Fast Role Swap Events - Case 1**


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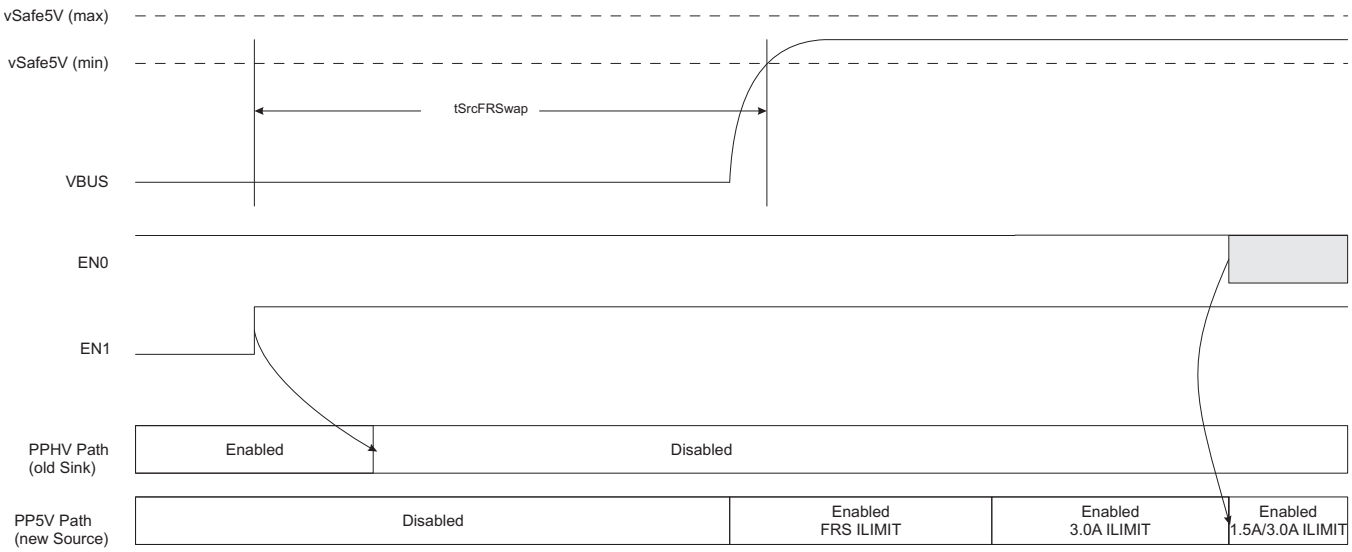



**Figure 27. Fast Role Swap Events - Case 2**

### 8.4.8 Faults

The TPS6602x includes a fault pin, $\overline{FLT}$. The $\overline{FLT}$ pin is an open-drain output and requires an external pull-up resistor. If the $\overline{FLT}$ pin is not required, it may be tied to GND or left floating. The $\overline{FLT}$ pin will be asserted low only under certain conditions and not all fault conditions will assert the $\overline{FLT}$ pin, see Table 3. If the $\overline{FLT}$ pin is asserted, it will remain asserted for a minimum of tHOLD_FLT regardless if the fault condition is removed. After $t_{HOLD_FLT}$, if all fault conditions have surpassed, the $\overline{FLT}$ pin is released.

#### *8.4.8.1 Fault Types*

Table 3 summarizes the various fault types available and when the $\overline{FLT}$ shall be asserted.

**Table 3. Fault Types**

| Fault Name | Fault | $\overline{FLT}$ | Description |
|---|---|---|---|
| PP5V_UVLO | PP5V undervoltage Lockout | Low | If PP5V input supply is below the PP5V UVLO threshold, the PP5V path is disabled automatically if enabled or remains disabled until the PP5V UVLO threshold is exceeded. If a SRC state is selected to be entered, the device will remain in the DISABLED state until the UVLO event is removed. The $\overline{FLT}$ pin will not be asserted. If a SRC state has been entered successfully and a UVLO event occurs, the device will enter the DISABLED state, and the $\overline{FLT}$ pin will be asserted. |
| PP5V_OVP | PP5V overvoltage Protection | Low | If a SRC state is selected to be entered or device currently is in a SRC state (SRC 1.5 A or SRC 3 A) and the PP5V input supply rises above the PP5V OVP threshold, the PP5V path is disabled automatically and the $\overline{FLT}$ pin will be asserted. |
| PP5V_ILIMIT | PP5V Current Limit Protection | Low | The PP5V power path has a closed-loop current limit protection. If the load current exceeds the selected current limit, the control loop will increase the voltage across the FET to compensate. Note: $\overline{FLT}$ will not be asserted unless the current limit event lasts longer than $t_{ILIMIT_FLT}$. |
| PP5V_OVT | PP5V overtemperature Protection | Low | If a SRC state is selected to be entered or device currently is in a SRC state (SRC 1.5 A or SRC 3 A) and the local temperature of PP5V power path exceeds TSD_PP5V_R while in current limit, the PP5V path is disabled automatically and the $\overline{FLT}$ pin will remain asserted. PP5V power path will remain disabled until temperature falls below TSD_PP5V_F. |

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**Table 3. Fault Types (continued)**

| Fault Name | Fault | $\overline{FLT}$ | Description |
|---|---|---|---|
| PP5V_RCP | PP5V Reverse-Current Protection | Low | If a SRC state is selected to be entered or device currently is in a SRC state (SRC 1.5 A or SRC 3 A) and a reverse-current condition is detected, the PP5V path is disabled automatically and the $\overline{FLT}$ pin will be asserted. If the reverse-current condition is removed, the PP5V path will automatically re-enable. |
| VBUS_UVLO | VBUS undervoltage Lockout | Hi-Z | If VBUS supply is below the VBUS UVLO threshold, the PPHV path is disabled automatically if enabled or remains disabled. If the SNK state is selected to be entered, the device will remain in the DISABLED state until the UVLO event is removed. If the SNK state has been entered successfully and a UVLO event occurs, the PPHV path is disabled automatically. |
| VBUS_OVP(1) | VBUS overvoltage Protection | Low | If the SNK state is selected to be entered or device currently is in the SNK state and the VBUS supply rises above the VBUS OVP threshold, the PPHV path is disabled automatically and the $\overline{FLT}$ pin will be asserted. |
| VBUS_RCP | VBUS Reverse-Current Protection | Hi-Z | If the SNK state is selected to be entered or device currently is in the SNK state and a reverse-current condition is detected, the PPHV path is disabled automatically, but the $\overline{FLT}$ is not asserted.. If the reverse-current condition is removed, the PPHV path will automatically re-enable. |
| PPHV_OVT | PPHV overtemperature Protection | Low | If the SNK state is selected to be entered or device currently is in the SNK state and the local temperature of PPHV power path exceeds TSD_PPHV_R, the PPHV path is disabled automatically and the $\overline{FLT}$ pin will be asserted. PPHV power path will remain disabled until temperature falls below TSD_PPHV_F. |

(1) OVP terminal is not connected to GND.


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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The typical applications of the TPS6602x include chargers, notebooks, tablets, ultra-books, dongles and any other product supporting USB Type-C and/or USB-PD as a power source or power sink. The typical applications outlined in the following sections detail a Fully-Featured USB Type-C using a single 5-V supply and another using a separate 3.3-V supply.

## 9.2 Typical Application

Figure 28 shows a USB Type-C single port design using a Power Delivery (PD) controller that supports 5-V operation. For this system, a single 5-V supply is used to supply power to the PP5V and VIN supplies of the TPS66021, as well as, the connector power, VCONN. The TPS66021 supplies power to the 5-V supply of the PD controller via its VLDO output which is sourced either from the integrated 5-V VBUS LDO for dead battery operation or from VIN once the dead battery condition ends.

Similarly, Figure 29 shows a USB Type-C single port design using a PD controller that only supports 3.3-V operation. In this case, a separate 3.3-V supply in the system is used to supply power to the TPS66020. The TPS66020 supplies power to the 3.3-V supply of the PD controller via its VLDO output which is sourced either from the integrated 3.3-V VBUS LDO for dead battery operation or from VIN once the dead battery condition ends.

The PP5V integrated power path is used to provide 5-V VBUS power when the device is enabled as Source. The PPHV integrated power path provides power to the system and battery charger from VBUS when the device is enabled as a Sink.

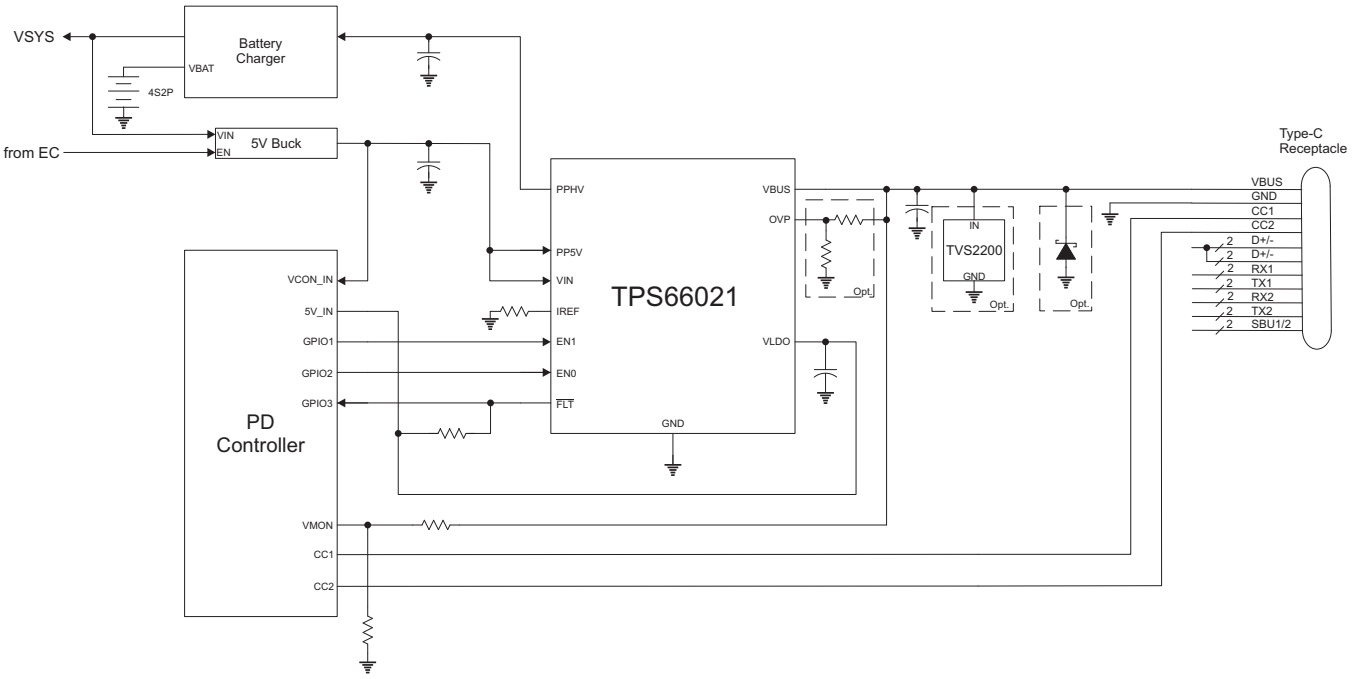



**Figure 28. Single Port Type-C PD Port Using a Single 5-V Supply**

## Typical Application (continued)

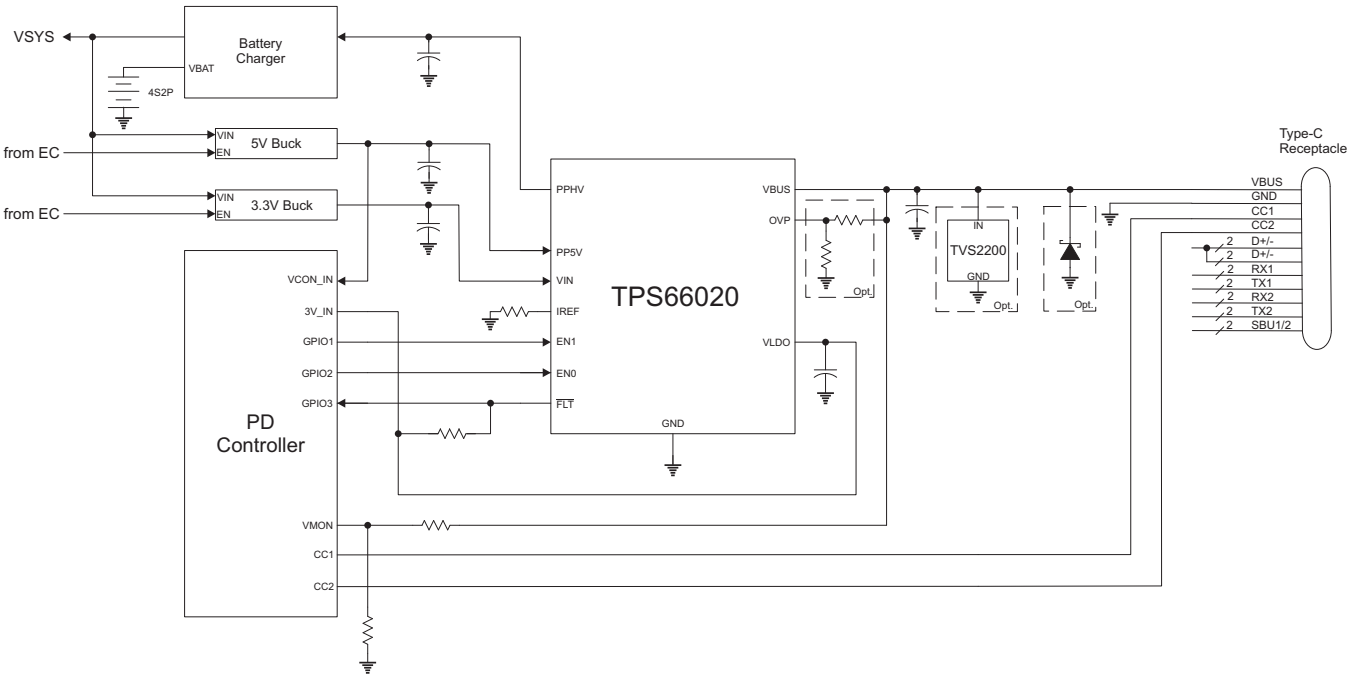



**Figure 29. Single Port Type-C PD Port Using a 3.3-V Supply**

### 9.2.1 Design Requirements

For a single port notebook application, Table 4 lists the input voltage requirements and expected current capabilities.

**Table 4. Single-Port Notebook Application Design Parameters**

| DESIGN PARAMETERS | EXAMPLE VALUE(S) | POWER PATH DIRECTION |
|---|---|---|
| PP5V Input Voltage and Current Capabilities | 5V/3A | Source from PP5V to VBUS |
| VCON_IN Input Voltage and Current Capabilities | 5V/300mA (1.5W) | Source to VCONN |
| VBUS Input Voltage and Current Capabilities | 5V/3A, 9V/3A, 15V/3A, 20V/3A | Sink from VBUS to PPHV |
| 5V_IN Input Voltage and Current Capabilities | 4.5-5.5V/30mA | 5-V PD Controller Supply |
| 3V_IN Input Voltage and Current Capabilities | 3.0-3.6V/30mA | 3.3-V PD Controller Supply |

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 External Current Reference Resistor ($R_{IREF}$)*

A 75-kΩ resistor is required from the TPS6602x IREF terminal to ground. $R_{IREF}$ is used to set the proper reference current required to meet the min/max current limit specifications in the datasheet of the PP5V power path. An overall resistance tolerance of +/- 1% is required to meet the datasheet specifications which includes aging, temperature, and resistance variation. A +/- 0.5% resistor is recommended. Care should be taken to ensure the ground return of $R_{IREF}$ is in close proximity to the GND terminal of the TPS6602x to minimize error in the current limit setting due to voltage drops that may occur across the ground supply.


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#### 9.2.2.2 External VLDO Capacitor (CVLDO)

For all capacitances, the DC operating voltage must be factored into the derating of ceramic capacitors. Generally, the effective capacitance is 35-50% of the nominal capacitance with voltage applied. Assuming VLDO = 5 V, and a minimum derated capacitance of 2.5 uF, a 10-V rated 4.7-uF capacitor is sufficient.

#### 9.2.2.3 PP5V Power Path Capacitance

For most systems, the PP5V terminal is supplied by a DC-DC converter. Typically, the capacitance placed on the output of the DC-DC converter is significant in order to handle current load steps. This capacitance value will be dependent on the DC-DC converter selected. A ceramic 10 uF (X7R/X5R) 10-V rated capacitor coupled with a 0.1-uF high frequency capacitor placed, is placed as close as possible to the PP5V terminal of the TPS6602x. This is in addition to the DC-DC converter required capacitance should be sufficient, but may need to be adjusted based on the specific application.

It should be noted that in many Type-C/PD systems, the VCONN supply is shared with the PP5V path. Therefore, in these systems, the application must budget the power requirements of the DC-DC converter for the VCONN and PP5V paths combined. For this example, a minimum of 5 V at 3.3 A is required to meet the defined system specifications.

#### 9.2.2.4 PPHV, VBUS Power Path Capacitance

The PPHV power path is a Sink. The capacitance on the PPHV shown in Figure 29 represents capacitance of the charger sub-system. In a typical application, this capacitance can be in the range of 47 uF up to 100 uF, far exceeding the 1-uF minimum specification for the TPS6602x, so no external capacitance is required to meet this requirement in most cases. As per the PD Specification, the total capacitance on VBUS should be maximum 10 uF at connection.

The TPS6602x PPHV power path has soft start circuitry to control in-rush current when the PPHV power path is enabled. DC loading should be minimized during soft start since the PPHV path may experience high power dissipation especially at higher VBUS voltages. This in turn may lead to a PPHV overtemperature protection event.

#### 9.2.2.5 VBUS TVS Protection (Optional)

It is recommended that each VBUS port in the system have TVS protection to protect the VBUS terminal. Inductive ringing during momentary disconnects and reconnects due to mechanical vibration or plug removal while sinking large current loads may cause large peak voltages to be present on the VBUS terminal that may exceed the absolute maximums of the TPS6602x. Under such events, the TVS2200 clamps the VBUS terminal and prevents VBUS from exceeding the maximum specification. The TVS trip point should be chosen to be safely above the normal operating ranges of the device. For this case, it is assumed VBUS voltage contracts are less than 22-V maximum which is below the minimum breakdown voltage of the TVS2200. The maximum clamping voltage of 28.3 V of the TVS2200 is sufficient to protect the VBUS terminal of the TPS6602x.

#### 9.2.2.6 VBUS Schottky Diode Protection (Optional)

To prevent the possibility of large ground currents into the TPS6602x during sudden disconnects because of inductive effects in a cable, it is recommended that a Schottky diode be placed from VBUS to GND. The NSR20F30NXT5G or comparable device is recommended.

#### 9.2.2.7 VBUS Overvoltage Protection (Optional)

VBUS Overvoltage Protection (OVP) is optional. If VBUS OVP is not required, then the OVP terminal should be tied to ground as shown in Figure 12. VBUS OVP is used to detect voltages on VBUS that exceed a set threshold. Upon detection, the PPHV power path is disabled quickly to help protect components connected downstream of the PPHV terminal. It should be noted that VBUS OVP is not a replacement for VBUS TVS protection which is protecting the VBUS terminal itself.

The VBUS OVP threshold is set by a resistor divider from the VBUS terminal to ground as shown in Figure 11. For this design, R1 and R2 are fixed values to provide VBUS OVP protection at the highest voltage contract level. Using R1 = 432-kΩ and R2 =20-kΩ sets a nominal VBUS OVP threshold of 22.6 V. For some applications, it may be desirable to dynamically change the VBUS OVP level based on the negotiated power contract. One possible way is shown in Figure 13. In this case, the PD controller via GPIO, selects the proper divider ratio to set the VBUS OVP threshold based on the negotiated voltage contract level.

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#### 9.2.2.8 Dead Battery Support

The TPS6602x integrates a high-voltage VBUS LDO that can be used to supply power to a PD Controller and other supporting circuitry when only VBUS power is available, such as in a dead battery condition. As shown in Figure 29, the TPS66020 VLDO output supplies power to the PD Controller's 3V_IN supply. Similarly, Figure 28 shows the TPS66021 VLDO output supplies power to the PD Controller's 5V_IN supply. During a dead battery condition, the PD Controller presents its Type-C RPD pull-downs on the CC1 and CC2 lines. Upon connection to a Type-C/PD Source, 5 V is provided to VBUS from the Source partner which powers the TPS6602x. The VBUS LDO is enabled and provides power to the PD Controller. Once powered, the PD Controller can decide to enable the TPS6602x PPHV Sink path by asserting EN0 high and use the 5-V VBUS to charge the battery or it may choose to negotiate a higher voltage contract first. Either way, once the contract is negotiated, the PD Controller will enable the PPHV Sink path and charge the system. Once the system is sufficiently charged, the VIN terminal will rise and will exceed the VIN UVLO threshold. If VIN remains above the UVLO threshold for $t_{VIN_STABLE}$, VLDO will be supplied from VIN and the VBUS LDO will be disabled.

#### 9.2.2.9 Fast Role Swap (FRS) (Optional)

The TPS6602x supports Fast Role Swap operation as in the new Source, old Sink scenario shown in Figure 24. The PPHV power path represents the old Sink and the PP5V power path represents the new Source. During FRS, the PP5V power path of the TPS6602x has a much faster turn-on compared to normal operation, for example entering SRC 1P5A or SRC 3P0A states from the DISABLED state. This faster turn-on is required in order to meet the USB PD fast role swap timing requirements (tSrcFRSwap) for the new Source.

To enable FRS, the TPS6602x must first be operating as a Sink (SNK state). The TPS6602x must then transition to the FRS state by asserting EN1 high. EN1 is asserted high by the PD Controller as soon as possible once it has properly detected FRS signaling from its port partner on its CC line. The FRS signaling from the port partner to the PD Controller indicates that the port partner has lost its power and requires a fast role swap sequence to be performed.

It should be noted that the timing of when EN1 is asserted high relative to the port partner losing power is highly application, and implementation dependent. Some of these dependencies include:

- Loss of power detection accuracy, margin and propagation delay of the port partner.
- Timing from loss of power detection to FRS signaling transmitted on the CC line.
- Detection by the PD Controller of the FRS signaling received on its CC line.
- Assertion of a GPIO from the PD Controller after detection of the FRS signaling.

In systems that require good FRS performance, these should be optimized to minimize unnecessary delays from significantly impacting the turn-on of the new Source. Once the FRS state is entered, the TPS6602x will automatically handle the power role swap from Sink to Source as shown in Figure 25. In most applications, there is significant charge being stored in reserve while power is being provided. Upon loss of power, this charge is then used to supply power to the application until the FRS completes. As this charge depletes, the voltage on VBUS will decay at some rate based on the current load and the amount of charge that has been stored. USB PD requires that the new Source only be enabled once VBUS is detected below vSafe5V (maximum). Therefore, the amount of voltage that VBUS drops below vSafe5V will depend heavily on the amount of remaining charge and what current load is on VBUS, along with how fast the PP5V power path can enable. It should be noted that the PD Specification allows VBUS to be discharged completely to ground and is shown in Figure 32 typical response curve.


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### 9.2.3 Application Curves

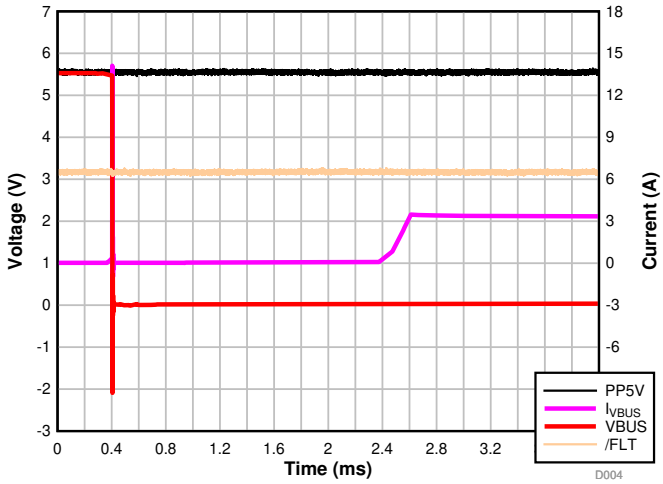



Figure 30. PP5V Current Limit Response

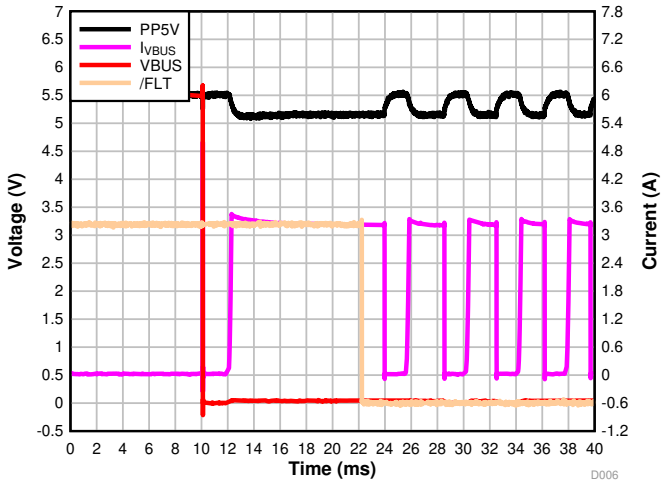



Figure 31. PP5V Enable into Short with Thermal Cycling

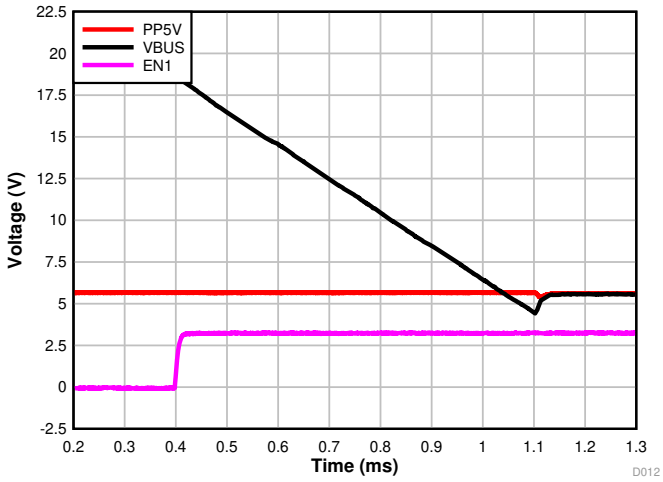



Figure 32. Fast Role Swap Response, 20-V Sink Contract, $C_{VBUS}$= 20 µF, $I_{VBUS}$ = 0.5 A

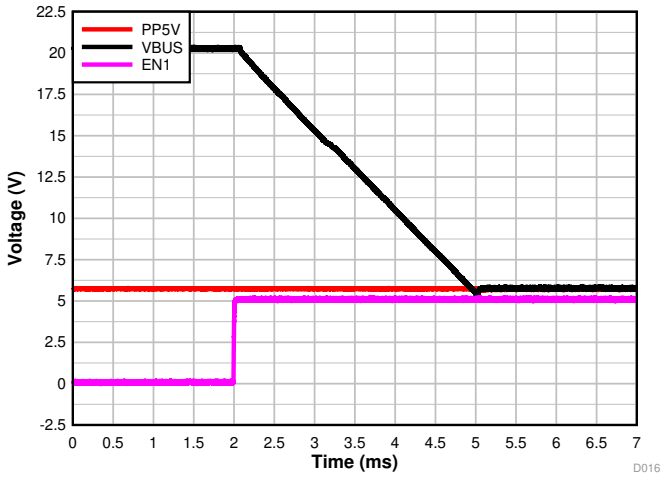



Figure 33. Fast Role Swap Response, 20-V Sink Contract, $C_{VBUS}$= 120 µF, $I_{VBUS}$ = 0.5 A

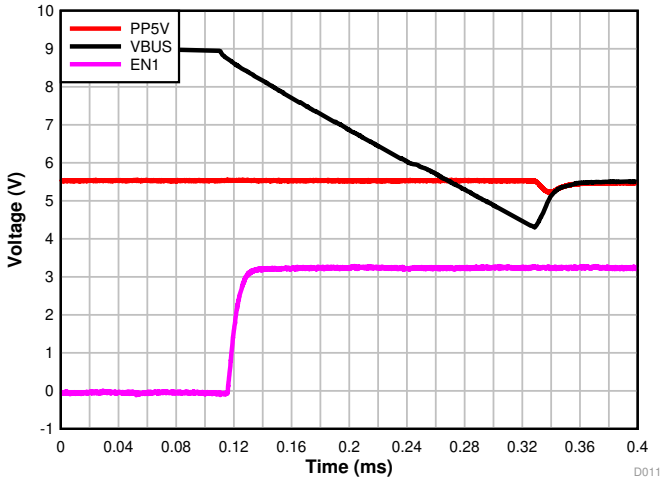



**Figure 34. Fast Role Swap Response, 9-V Sink Contract, $C_{VBUS}$= 20 µF, $I_{VBUS}$ = 0.5 A**

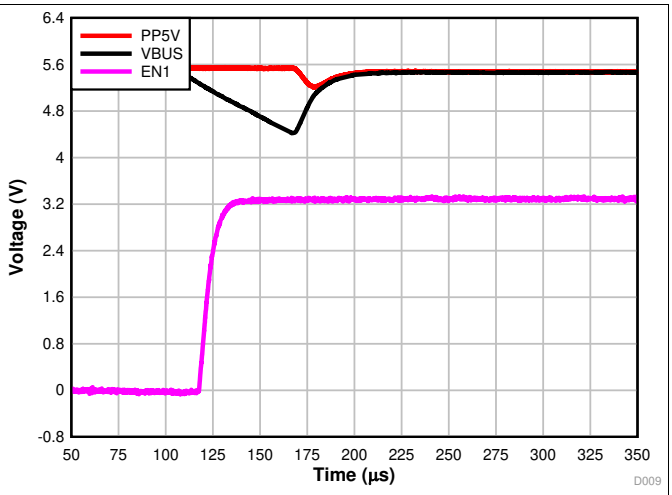



**Figure 35. Fast Role Swap Response, 5-V Sink Contract, $C_{VBUS}$= 20 µF, $I_{VBUS}$ = 0.5 A**

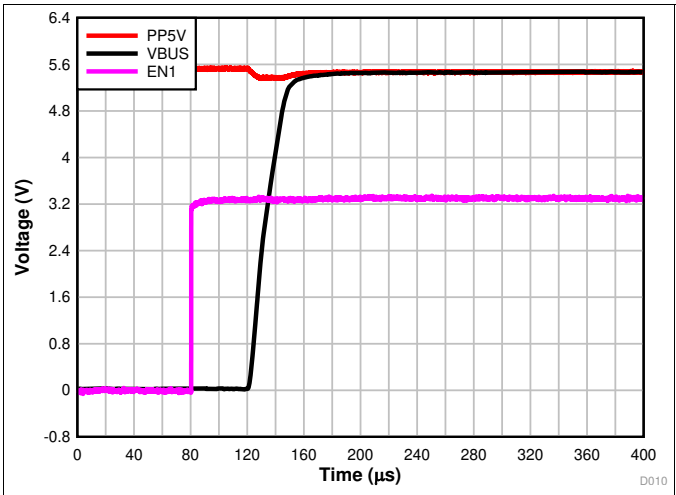



**Figure 36. Fast Role Swap Response, 5-V Sink Contract, VBUS Fully Discharged, $C_{VBUS}$= 20 µF, $I_{VBUS}$ = 0.5 A**

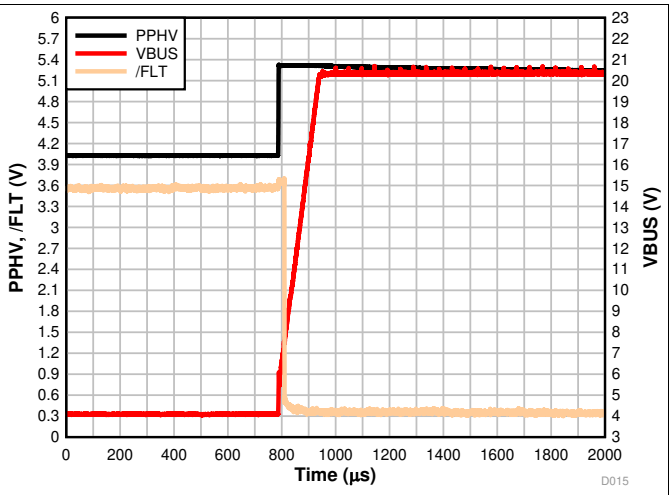



**Figure 37. VBUS OVP Response with 6-V Threshold**

## 10 Power Supply Recommendations

The device has a single input supply, VIN. VIN may be shared with PP5V when using the TPS66021 device. When shared with PP5V, the capacitance required on PP5V is sufficient for the VIN supply. When VIN is not shared, a 1-uF or higher ceramic bypass capacitor between VIN and GND is recommended as close to the VIN as possible for local noise decoupling.

USB Specification Revisions 2.0 and 3.1 require VBUS voltage at the connector to be between 4.75 V to 5.5 V. Depending on layout and routing from supply to the connector the voltage droop on VBUS has to be tightly controlled. Locate the input supply close to the device. For all applications, a maximum 10-µF ceramic bypass capacitor between VBUS and GND is recommended as close to the Type-C connector of the device as possible for local noise decoupling. The input power supply should be rated higher than the current limit set to avoid voltage droops during overcurrent and short-circuit conditions.


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# 11 Layout

## 11.1 Layout Guidelines

1. PP5V, PPHV, and VBUS traces must be as short and wide as possible to accommodate for high currents.
2. A ceramic 10 uF (X7R/X5R) 10-V rated capacitor coupled with a 0.1-uF high frequency capacitor placed, is placed as close as possible to the PP5V terminal of the TPS6602x.
3. Care should be taken to ensure the ground return of $R_{IREF}$ is in close proximity to the GND terminal of the TPS6602x to minimize error in the current limit setting due to voltage drops that may occur across the ground supply.
4. A ceramic 4.7 uF (X7R/X5R) 10-V rated capacitor is placed as close as possible to the VLDO terminal of the TPS6602x.

## 11.2 Layout Example

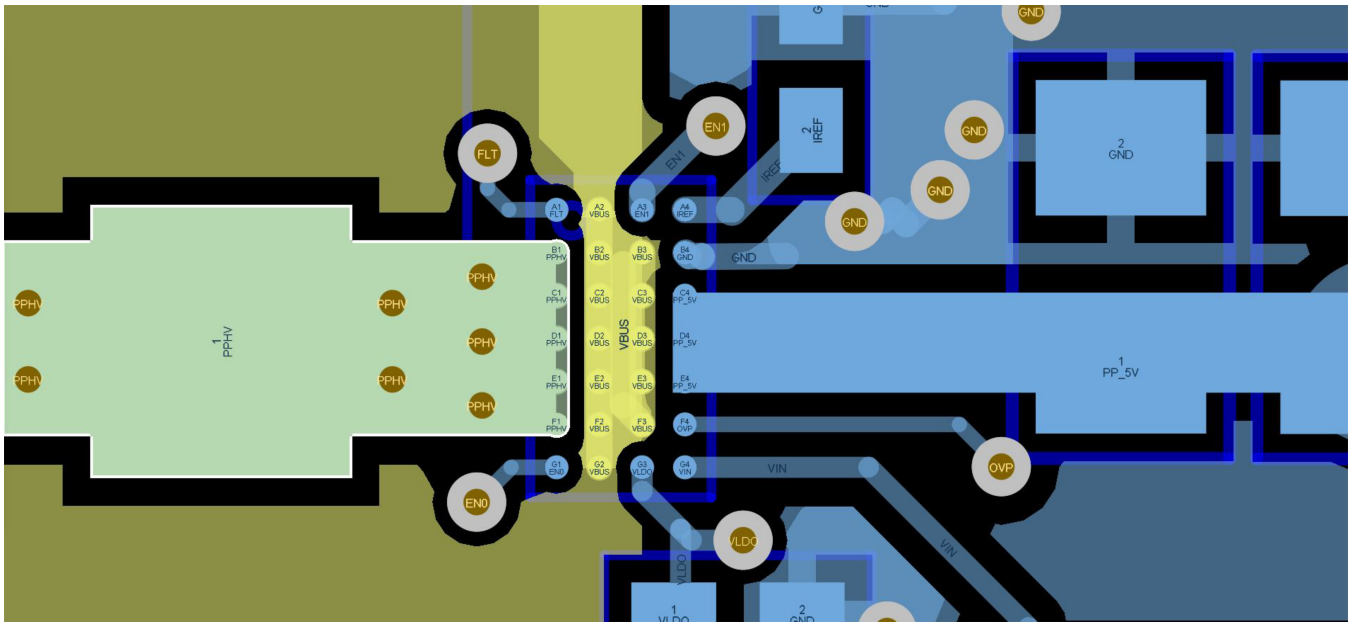



**Figure 38. Layout Example**

# 12 Device and Documentation Support

## 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 5. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS66020 | Click here | Click here | Click here | Click here | Click here |
| TPS66021 | Click here | Click here | Click here | Click here | Click here |

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

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All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS66020YBGR | ACTIVE | DSBGA | YBG | 28 | 3000 | Green (RoHS & no Sb/Br) | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -10 to 85 | TPS66020 | Samples |
| TPS66021YBGR | ACTIVE | DSBGA | YBG | 28 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -10 to 85 | TPS66021 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

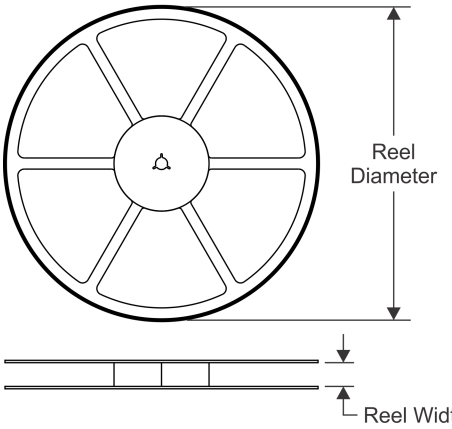
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

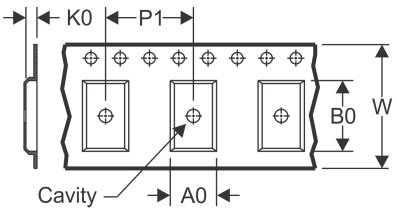
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

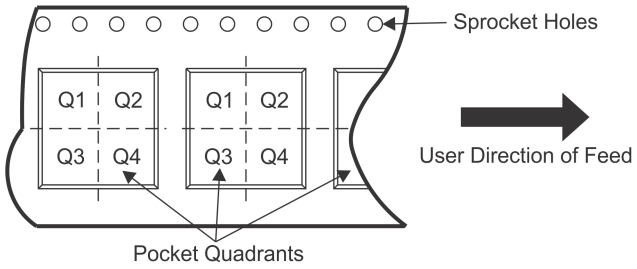



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

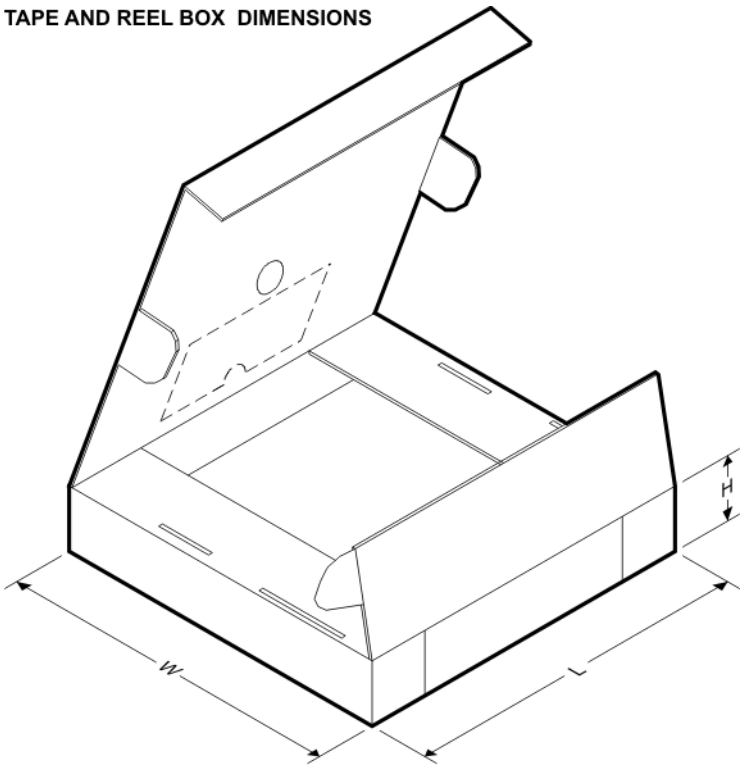
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS66020YBGR | DSBGA | YBG | 28 | 3000 | 330.0 | 12.4 | 1.78 | 2.98 | 0.6 | 4.0 | 12.0 | Q1 |
| TPS66020YBGR | DSBGA | YBG | 28 | 3000 | 330.0 | 12.4 | 1.78 | 2.98 | 0.7 | 4.0 | 12.0 | Q1 |
| TPS66021YBGR | DSBGA | YBG | 28 | 3000 | 330.0 | 12.4 | 1.78 | 2.98 | 0.7 | 4.0 | 12.0 | Q1 |
| TPS66021YBGR | DSBGA | YBG | 28 | 3000 | 330.0 | 12.4 | 1.78 | 2.98 | 0.6 | 4.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

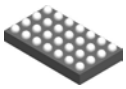



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS66020YBGR | DSBGA | YBG | 28 | 3000 | 335.0 | 335.0 | 25.0 |
| TPS66020YBGR | DSBGA | YBG | 28 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS66021YBGR | DSBGA | YBG | 28 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS66021YBGR | DSBGA | YBG | 28 | 3000 | 335.0 | 335.0 | 25.0 |

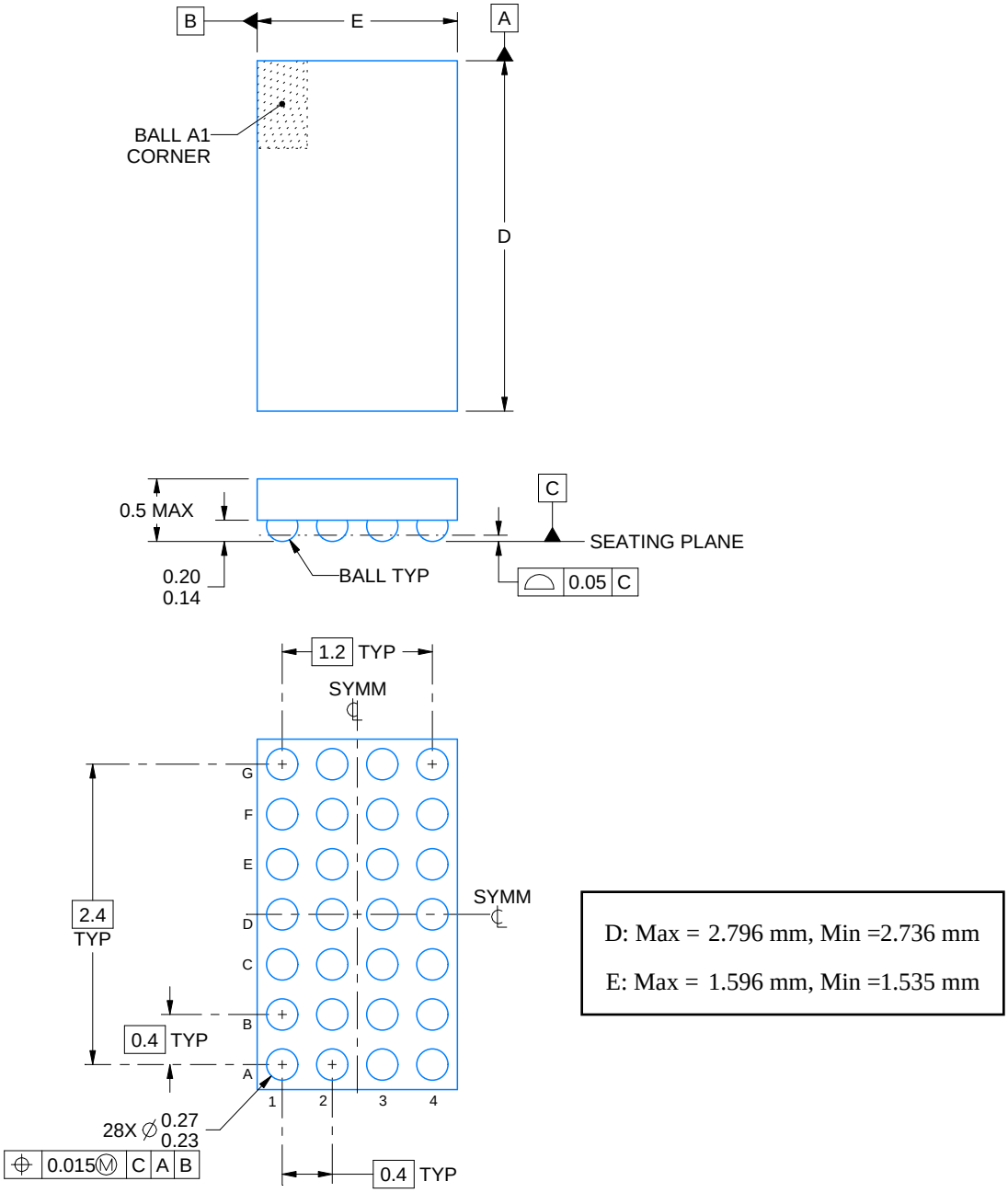
# PACKAGE OUTLINE

## YBG0028



## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




D: Max = 2.796 mm, Min =2.736 mm

E: Max = 1.596 mm, Min =1.535 mm

4224767/A 01/2019

NOTES:

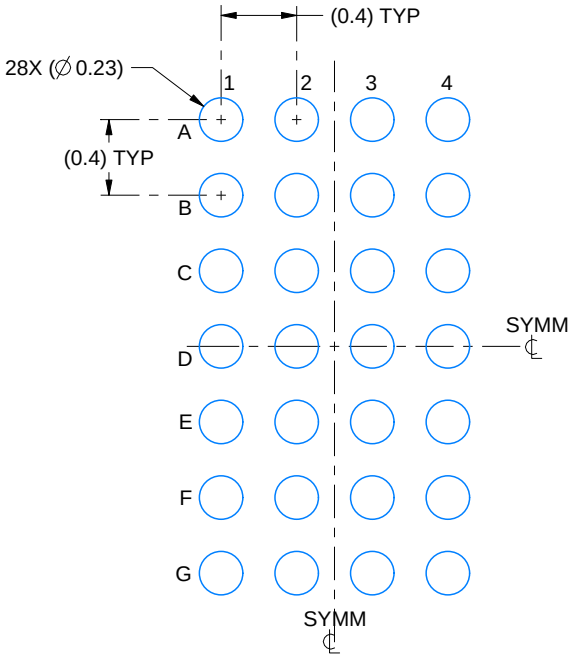
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

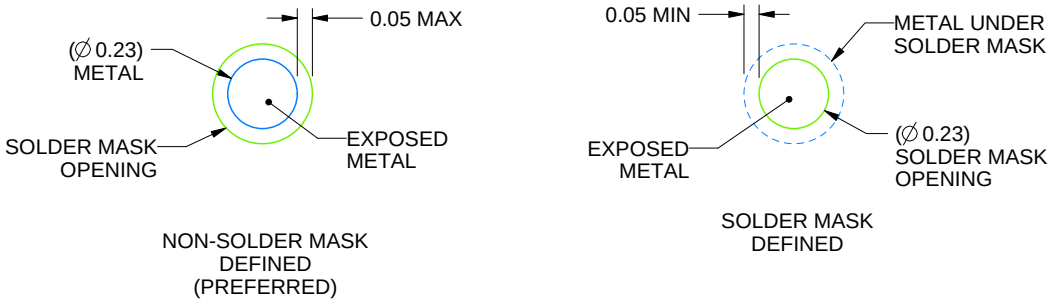
## YBG0028

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

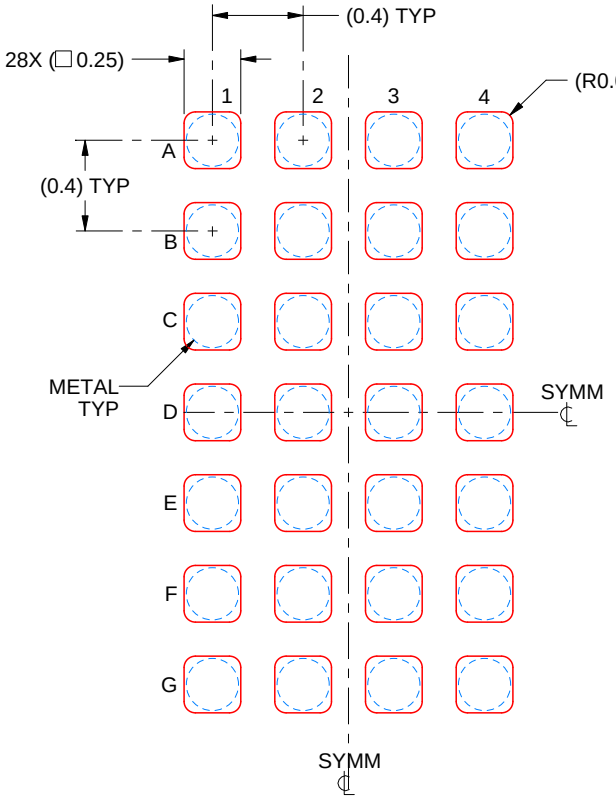



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224767/A 01/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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