TPS65735 System Evaluation Board

This user's guide describes the characteristics, operation, and use of the TPS65735EVM-703 evaluation module (EVM). The TPS65735EVM-703 is a fully assembled and tested platform for evaluating the performance of the TPS65735 single-chip power management device. This document includes schematic diagrams, a printed circuit board (PCB) layout, bill of materials, and test data. Throughout this document, the abbreviations EVM, TPS65735EVM, and the term evaluation module are synonymous with the TPS65735EVM-703 unless otherwise noted.

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1 Introduction

The TPS65735 is a single-chip power management IC for active lens 3D glasses consisting of a battery charger with Power Path management for a single lithium-ion (Li-Ion) or lithium-polymer (Li-Polymer) or standard coin cell, a low drop out linear regulator (LDO), a boost converter and two H-bridges.

1.1 Features

- Battery Charger
  - Power Path management
- Low Dropout Linear Regulator (LDO)
- Boost Converter
- Two H-Bridges

1.2 Applications

- Active 3D glasses
  - Television
  - Computer
  - Handheld
  - Theater
  - Gaming

1.3 Requirements

In order to operate this EVM properly, the hardware must be connected and properly configured. All components and connectors are installed on the EVM as shipped, except the dc power supply.

2 Electrical Performance Specifications

Input Voltage VIN 3.7 to 6.4 V

Input Voltage Vbat BAT 2.5 to 6.4 V

Output Voltage LDO VLDO 2.2 (default) or 3.0 V

Output Voltage Boost BST_OUT 8 to 16 V, 10 V default

Charge Current Ichg=Kiset/Riset 5 to 100 mA, 70 mA default

Input Voltage Low VIL (BST_EN, CHG_EN, SW_SEL, VLDO, HBRx, HBLx) 0.4 V

Input Voltage High VIH (BST_EN, CHG_EN, SW_SEL, VLDO, HBRx, HBLx) 1.2 V

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3 Schematic

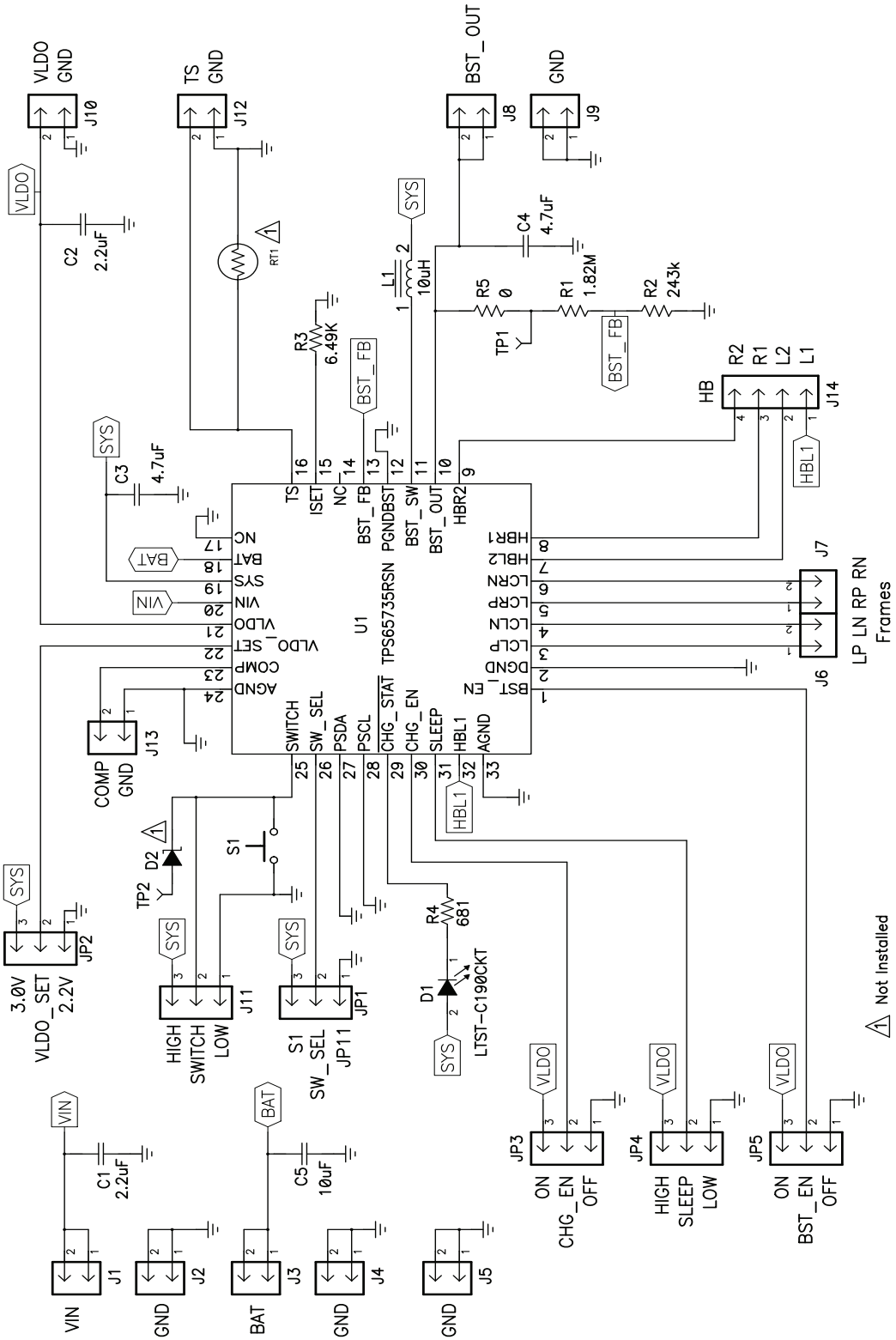

Figure 1. Schematic

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4 Connector and Test Point Descriptions

4.1 Headers and Switch

J1 : VIN
J1 pin 1 and pin 2 are VIN of the TPS65735. Connect the VIN (Charger) power supply positive terminal to J1.

J2 : GND
J2 pin 1 and pin 2 are GND of the TPS65735. Connect the VIN (Charger) power supply negative terminal to J2.

J3 : BAT
J3 pin 1 and pin 2 are BAT of the TPS65735. Connect the second power supply (Battery)(capable of sinking current) positive terminal to J3.

J4 : GND
J4 pin 1 and pin 2 are GND of the TPS65735. Connect the second power supply (Battery)(capable of sinking current) negative terminal to J4.

J5 : GND
J5 pin 1 and pin 2 are GND of the TPS65735. These are provided as an extra set of ground terminals.

J6 : LP, LN
J6 pin 1 is LCLP, liquid crystal left positive, of the TPS65735 and pin 2 is LCLN, liquid crystal left negative, of the TPS65735. Connect the left lens across pin 1 and 2 of header J6.

J7 : RP, RN
J7 pin 1 is LCRP, liquid crystal right positive, of the TPS65735 and pin 2 is LCRN, liquid crystal right negative, of the TPS65735. Connect the left lens across pin 1 and 2 of the J7.

J8 : BST_OUT
J8 pin 1 and pin 2 are BST_OUT of the TPS65735. In a typical application, the boost will be loaded only through the h-bridge on pins LCLP, LPLN, LCRP,LCRN (J6,J7) by the liquid crystal lenses.

J9 : GND
J9 pin 1 and pin 2 are GND.

J10 : VLDO, GND
J10 pin 1 is GND and pin 2 is VLDO, the output of the TPS65735 LDO.

J11 (3-pin header): SWITCH, HIGH, LOW
J11 pin 1 is GND, pin 2 is the SWITCH pin of the TPS65735 and pin 3 is the SYS voltage output of the TPS65735. This header, J11, is to simulate the use of a slide switch and should only be used when JP1 pins 1 and 2 are shorted. If instead, a push-button switch is used, J11 should be left open and the push-button will pull SWITCH to GND when pressed and release (float) it otherwise (SWITCH has an internal pull-up only when JP1 pins 2 and 3 are shorted). Note there is an alternate configucation for J11.

J11 (2-pin header): SWITCH (alternate configuration)
J11 pin 1 is GND, pin 2 is the SWITCH pin of the TPS65735. This header, J11, is to simulate the use of a slide switch and should only be used when JP1 pins 1 and 2 are shorted. To simluated the use of a slide switch the switch pin of the TPS65735 must be connected to SYS (HIGH) to keep the device on and connected to ground to turn the device off. If instead, a push-button switch is used, J11 should be left open and the push-button will pull SWITCH to GND when pressed and release (float) it otherwise (SWITCH has an internal pull-up only when JP1 pins 2 and 3 are shorted).

S1: Push-Button Switch
S1 is the push-button switch connected to the SWITCH pin of the TPS65735. When the button on S1 is pressed, the SWITCH pin is connected to ground for the duration that the button is held. When the button is released, the SWITCH pin goes back up to SYS. S1 should only be used if JP1 is in the S1 position (pin 2 and pin 3 shorted of JP1).

J12 : TS, GND
J12 pin 1 is GND, pin 2 is the TS pin of the TPS65735. This header, J12, is to connect an external thermistor to the TPS65735 and should be left floating if not used.

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J13 : COMP, GND
J13 pin 1 is GND, pin 2 is the COMP pin of the TPS65735. COMP is the BAT voltage divided down through an internal resistor divider where VCOMP = 0.5 × VLDO + 300 mV. This is intended to be an output to a low voltage microcontroller

J14 : HBL1, HBL2, HBR1, HBR2
J14 pin 1 is HBL1, pin 2 is HBL2, pin 3 is HBR1 and pin 4 is HBR2 of the TPS65735. These are the inputs to the H-Bridge logic as noted in the datasheet.

4.2 Jumpers

JP1 : SW_SEL, S1, JP11
JP1 pin 1 is GND, pin 2 is the SW_SEL pin of the TPS65735 and pin 3 is the SYS voltage output of the TPS65735. Short pins 1 and 2 to use a slide switch on SWICTH pin of TPS65735 or short pins 2 and 3 to use the installed push-button switch S1 on SWITCH pin of TPS65735.

JP2 : VLDO_SET, 2.2V, 3.0V
JP2 pin 1 is GND, pin 2 is the VLDO_SET pin of the TPS65735 and pin 3 is the SYS voltage output of the TPS65735. Short pins 1 and 2 to set the LDO output voltage to 2.2V or short pins 2 and 3 to set the LDO output voltage to 3.0V.

JP3 : CHG_EN, ON, OFF
JP3 pin 1 is GND, pin 2 is the CHG_EN pin of the TPS65735 and pin 3 is VLDO of the TPS65735. Short pins 1 and 2 to disable the charger or short pins 2 and 3 to enable the charger.

JP4 : SLEEP, HIGH, LOW
JP4 pin 1 is GND, pin 2 is the SLEEP pin of the TPS65735 and pin 3 is VLDO of the TPS65735. Short pins 1 and 2 to put the TPS65735 in sleep mode or short pins 2 and 3 to disable sleep mode of the TPS65735.

JP5 : BST_EN, ON, OFF
JP5 pin 1 is GND, pin 2 is the BST_EN pin of the TPS65735 and pin 3 is VLDO of the TPS65735. Short pins 1 and 2 to disable the boost converter or short pins 2 and 3 to enable the boost converter.

4.3 Test Points

TP1 : When R5 is replaced with a 50-Ω resistor, TP1 is used to inject an AC signal which may be measured at BST_OUT to verify frequency response and converter stability.

TP2 : When D2 is populated, TP2 can be used to connect a microcontroller GPIO to implement special push-button power/on power off timing.

5 Setup

Set the first input power supply voltage to 5 V before connecting the EVM then power it off. Connect the positive lead to J1, VIN. The power supply return lead is connected to J2 GND.

Set the second input power supply (capable of sinking capable of sinking at least 200 mA) to 3.6 V before connecting to the EVM then power it off. The positive lead is connected to J3, BAT. The power supply return lead is connected to J4, GND.

With JP3 shorting jumper connected between CHG_EN and OFF, JP4 shorting jumper connected between SLEEP and OFF and JP5 shorting jumper connected between BST_EN and OFF apply 5V to the VIN input.

With JP2-VLDO_SET set to 3.0V, verify with voltmeter that the VLDO output voltage is 3V ± 100 mV.

Position JP2 shorting jumper between VLDO_SET and 2.2V. Verify with voltmeter that the VLDO output voltage is 2.2V ± 100m V.

Position JP5 shorting jumper between BST_EN and ON. Verify that input current is less than 50mA with and input voltage of 5 V.

Verify JP1 is set with S1 and SWITCH shorted, press the push-button (S1) and verify with voltmeter that the output voltage is 10V ± 1 V.

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Connect HBL1 to VLDO and HBL2 to GND with wire jumpers. Verify LCLP is 10 V ± 1 V and verify LCRP is 0V ± 1 V.

Connect HBL1 to GND and HBL2 to VLDO with wire jumpers. Verify LCLN is 10 V ± 1 V and verify LCLP is 0V ± 1 V.

Connect HBR1 to VLDO and HBR2 to GND with wire jumpers. Verify LCRP is 10 V ± 1 V and verify LCRN is 0V ± 1 V.

Connect HBR1 to GND and HBR2 to LVDO with wire jumpers. Verify LCRN is 10 V ± 1 V and verify LCRP is 0V ± 1 V.

Set input voltage supply capable of sinking at least 500mA on BAT to 3.6 V and power on.

Verify that input current is less than 200mA with input voltage of 5 V VIN power supply. Verify D1 lights up to indicate charging.

6 TPS65735EVM Test Data

This section presents typical performance data for the TPS65735EVM. Actual performance data can be affected by measurement techniques and environmental variables; therefore, these results are presented for reference and may differ from actual results obtained by some users.

6.1 Operation Waveforms

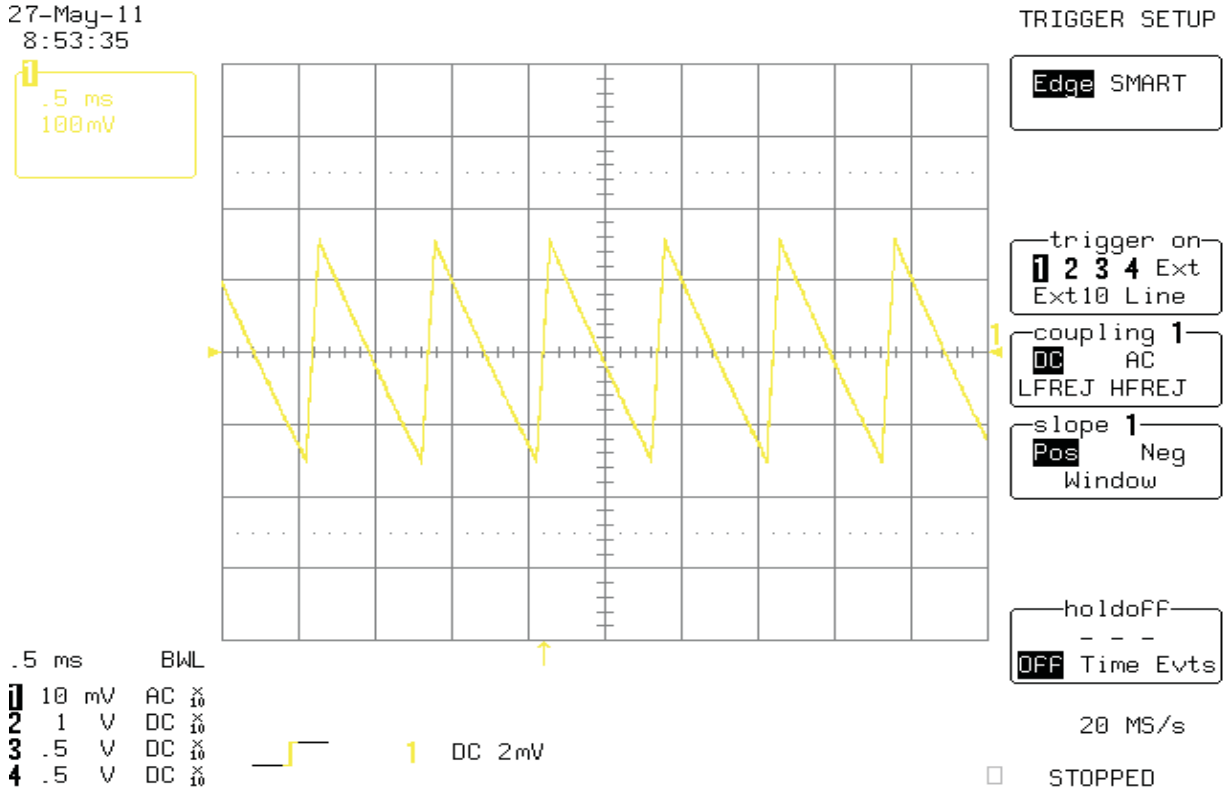

Figure 2. Boost Output Ripple : Vbat = 3.2 V and 1 mA Load on Boost

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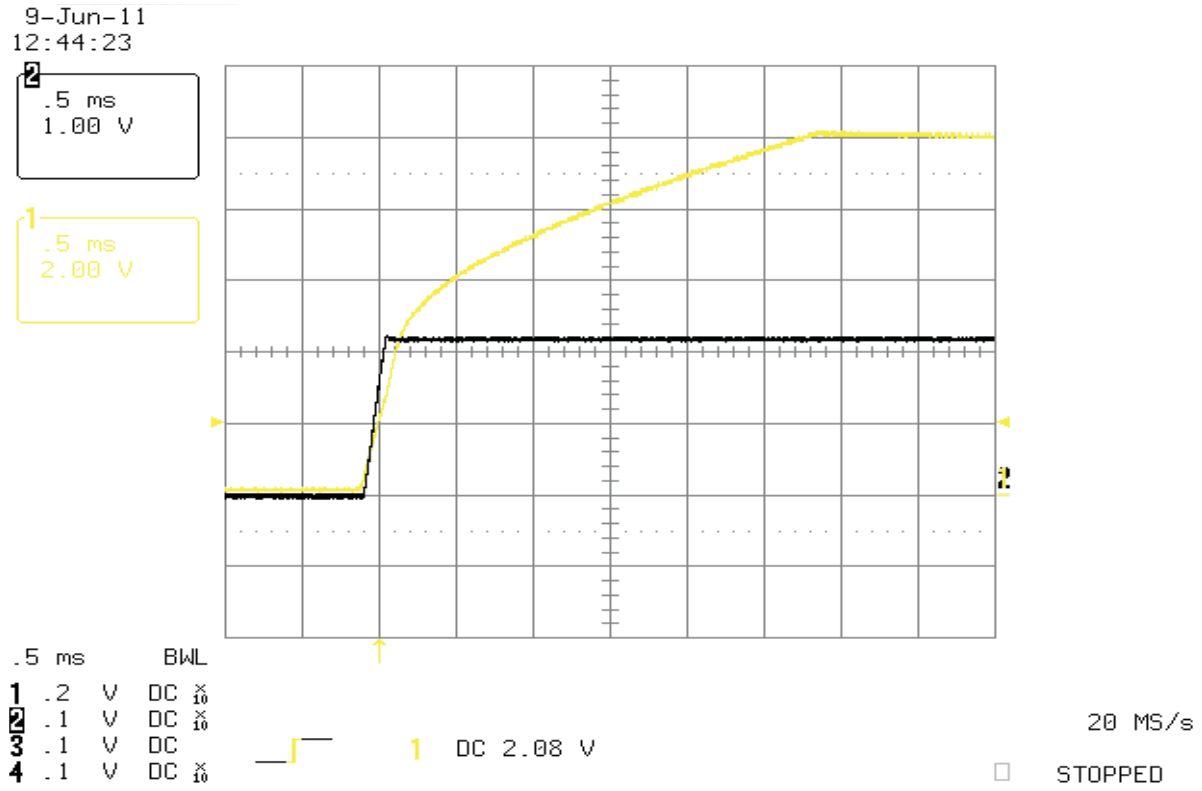

Figure 3. Startup : Vin = 5 V, 1 mA Load on Boost, and 15 mA Load on LDO

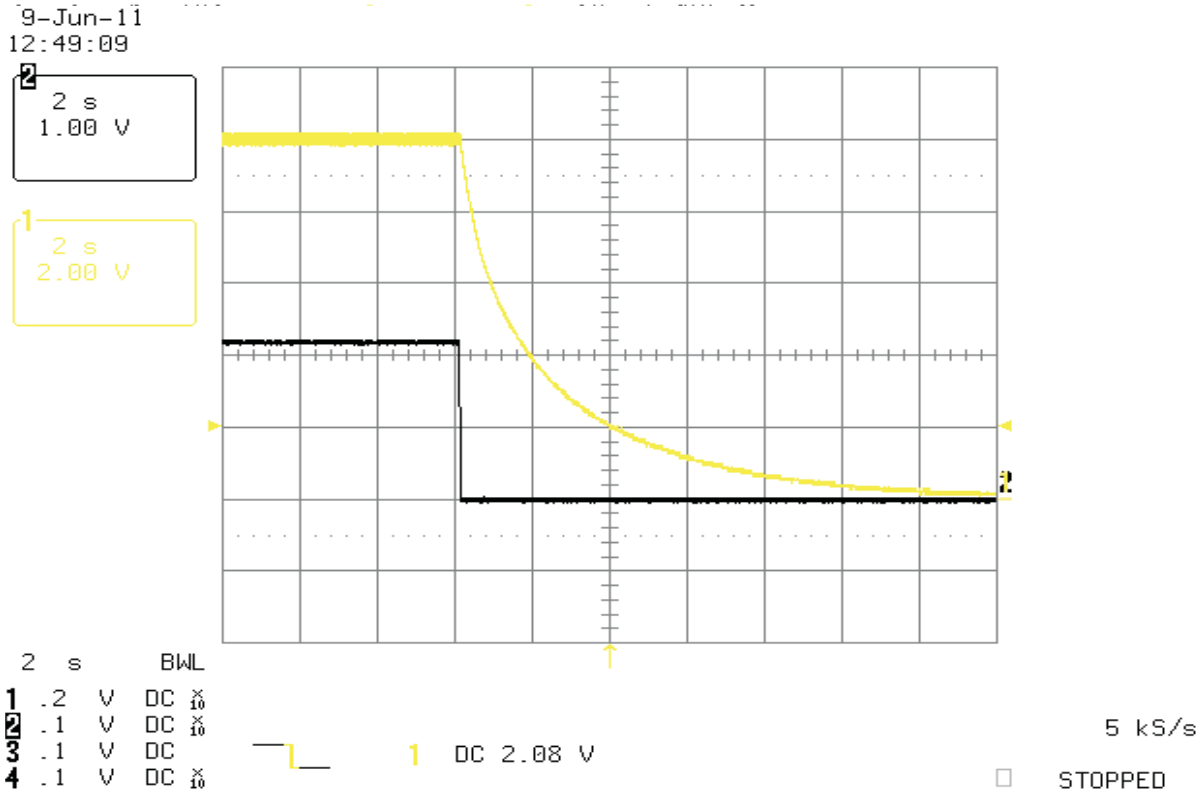

Figure 4. Shutdown : Vin = 5 V, 1 mA Load on Boost, and 15 mA Load on LDO

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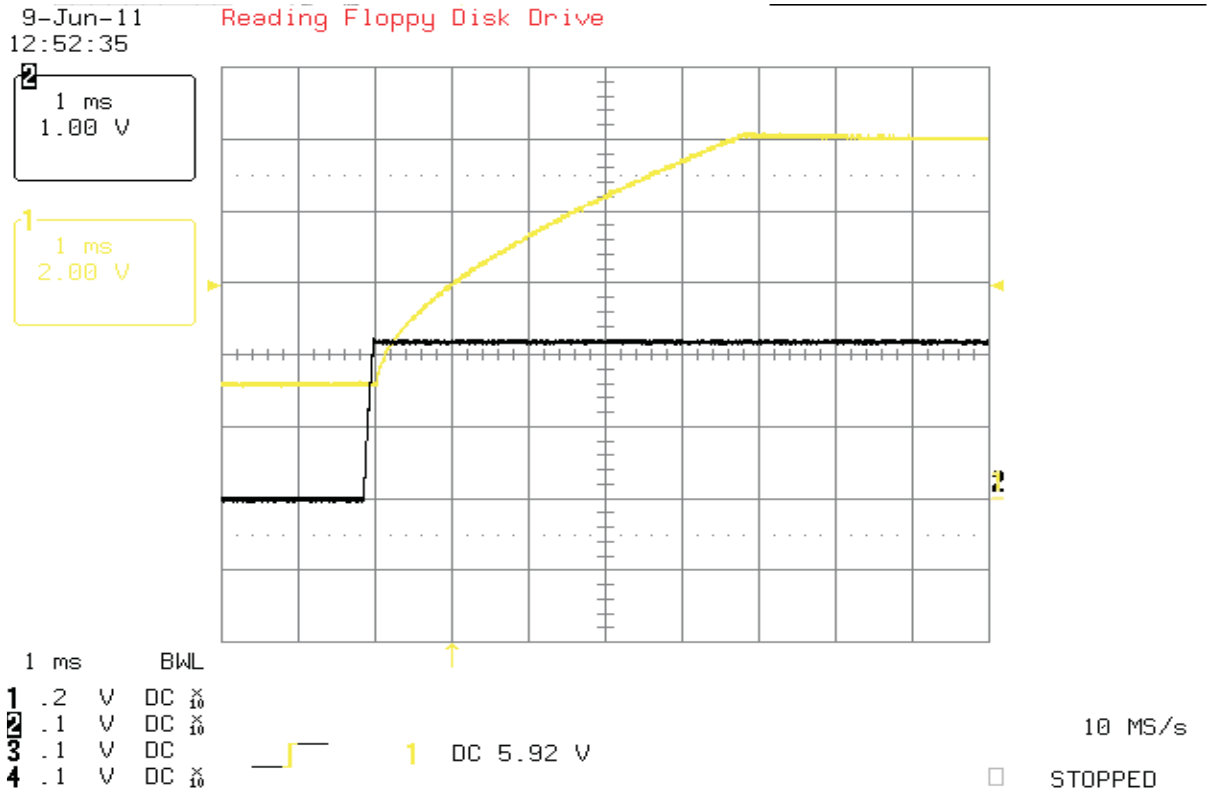

Figure 5. Startup : Vbat = 3.6 V, 1 mA Load on Boost, and 15 mA Load on LDO

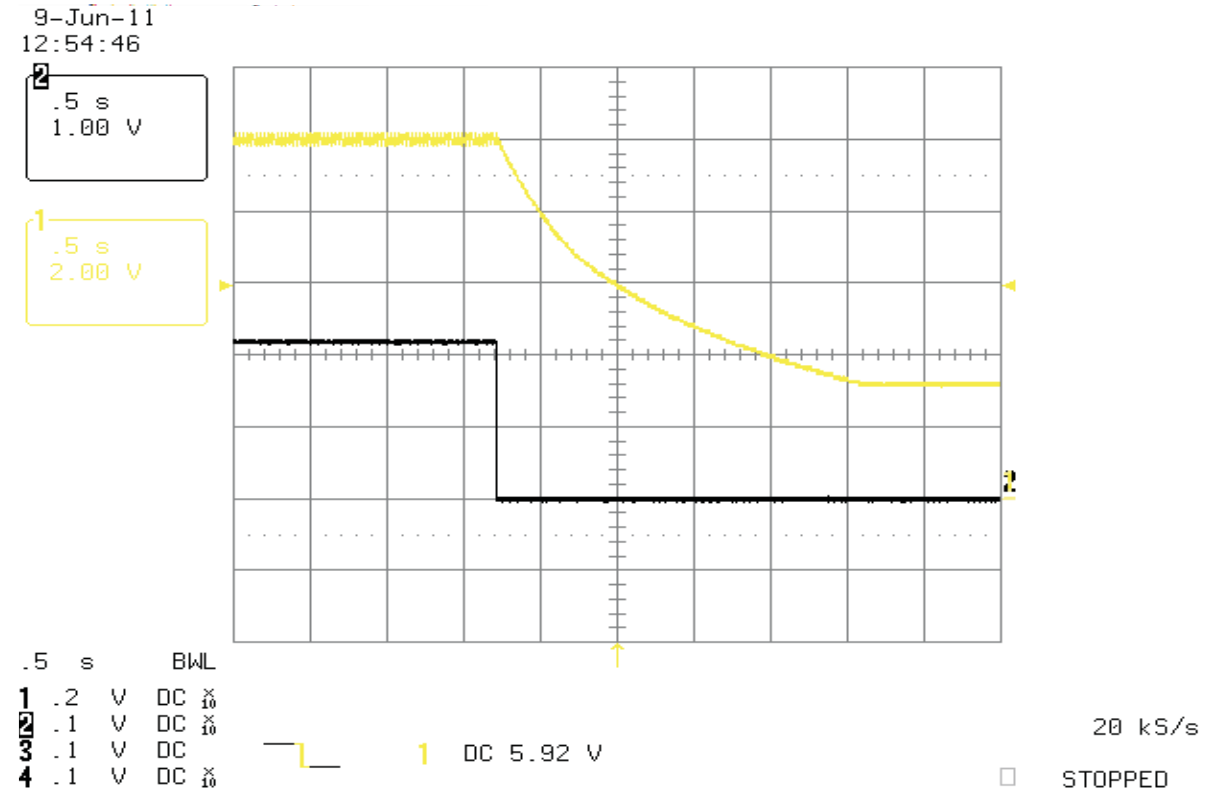

Figure 6. Shutdown : Vbat = 3.6 V, 1 mA Load on Boost, and 15 mA Load on LDO

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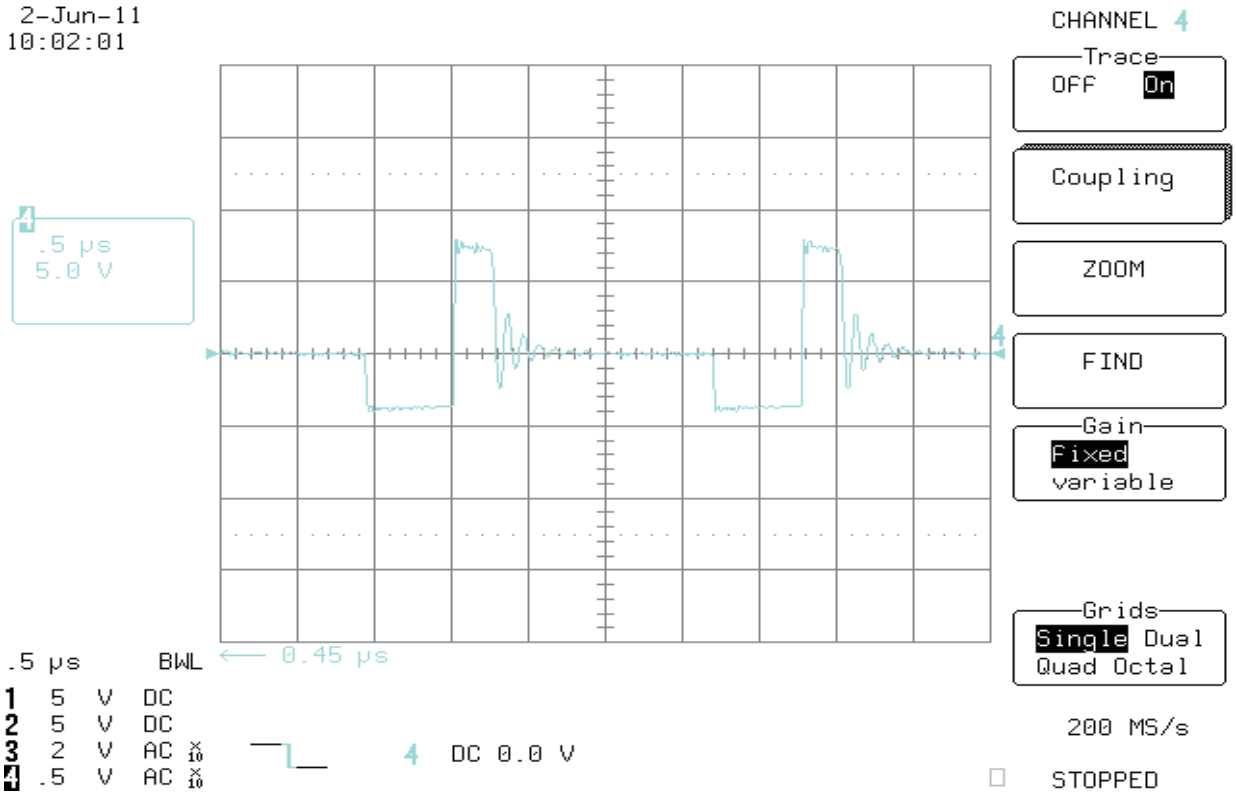

Figure 7. Switchnode : Vbat = 3.6 V, No Load, 0.5µs/div

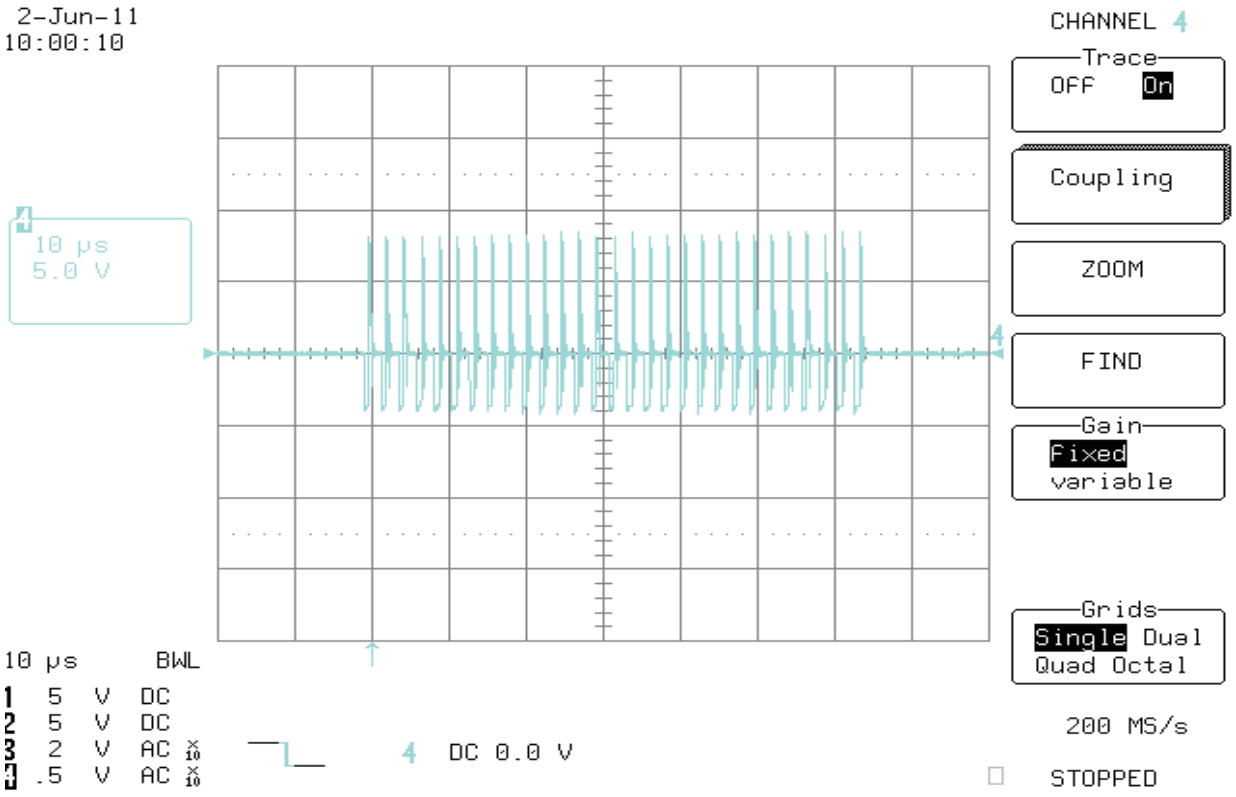

Figure 8. Switchnode : Vbat = 3.6 V, No Load, 10 µs/div

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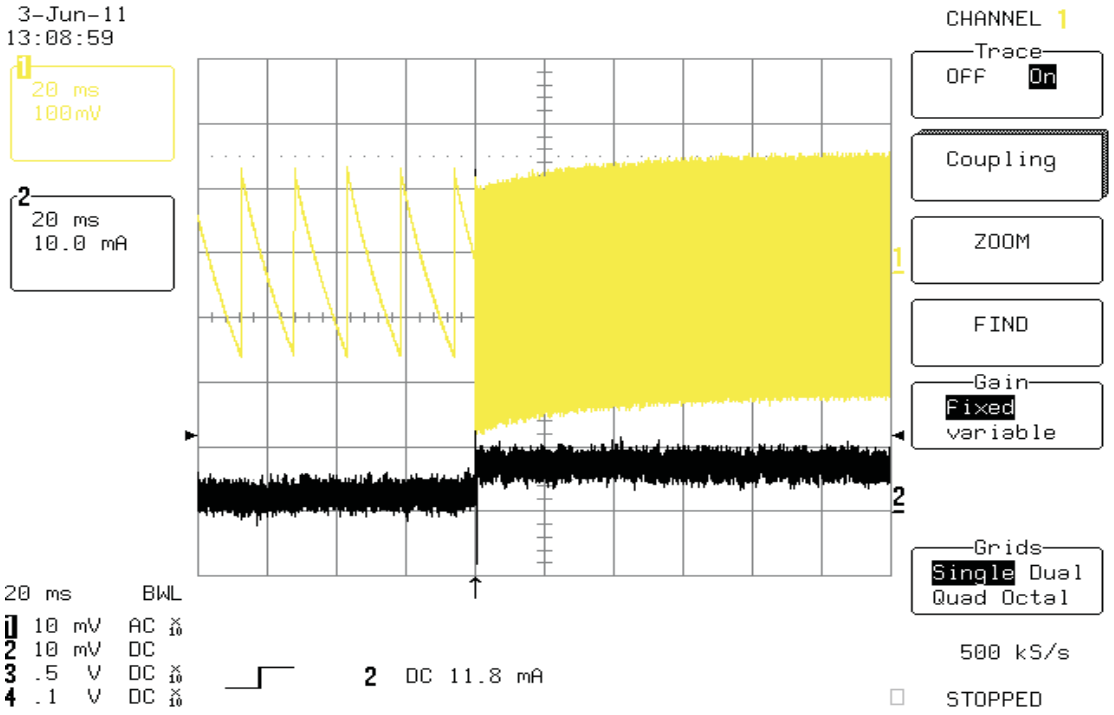

Figure 9. Load Transient, Boost : Vbat = 3.6 V with 0 mA to 5 mA Transient, Constant 15 mA Load on LDO. CH3 Bstout CH4 IBOOST

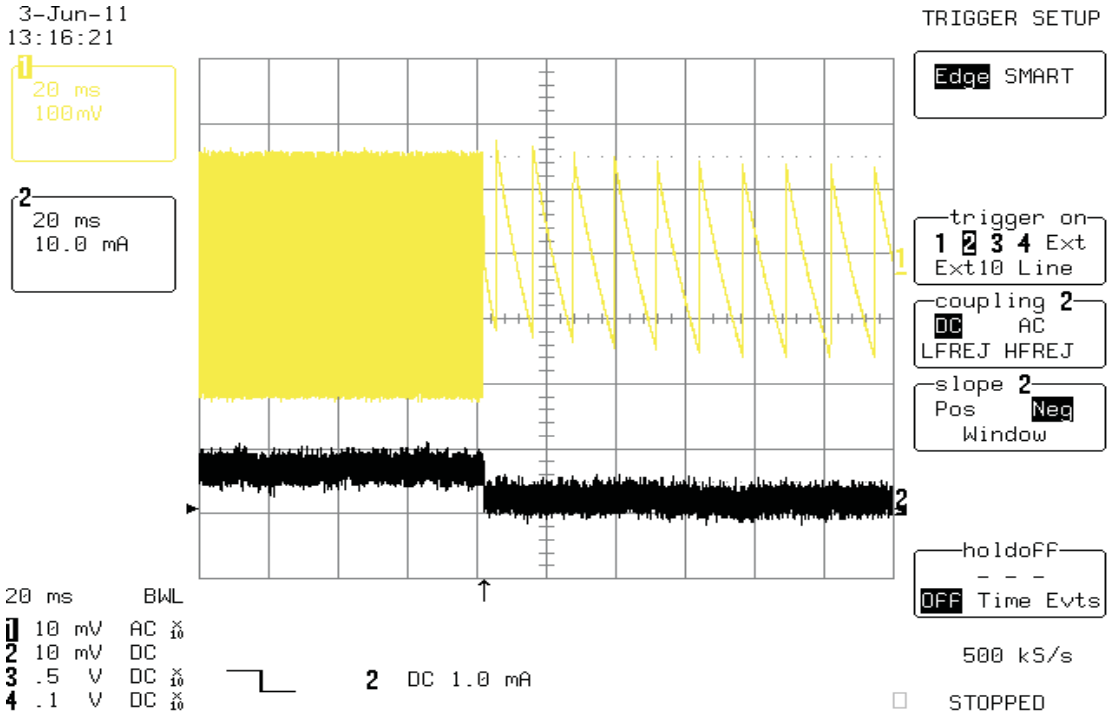

Figure 10. Load Transient, Boost : Vbat = 3.6 V with 5 mA to 0mA Transient, Constant 15 mA Load on LDO. CH3 Bstout CH4 IBOOST

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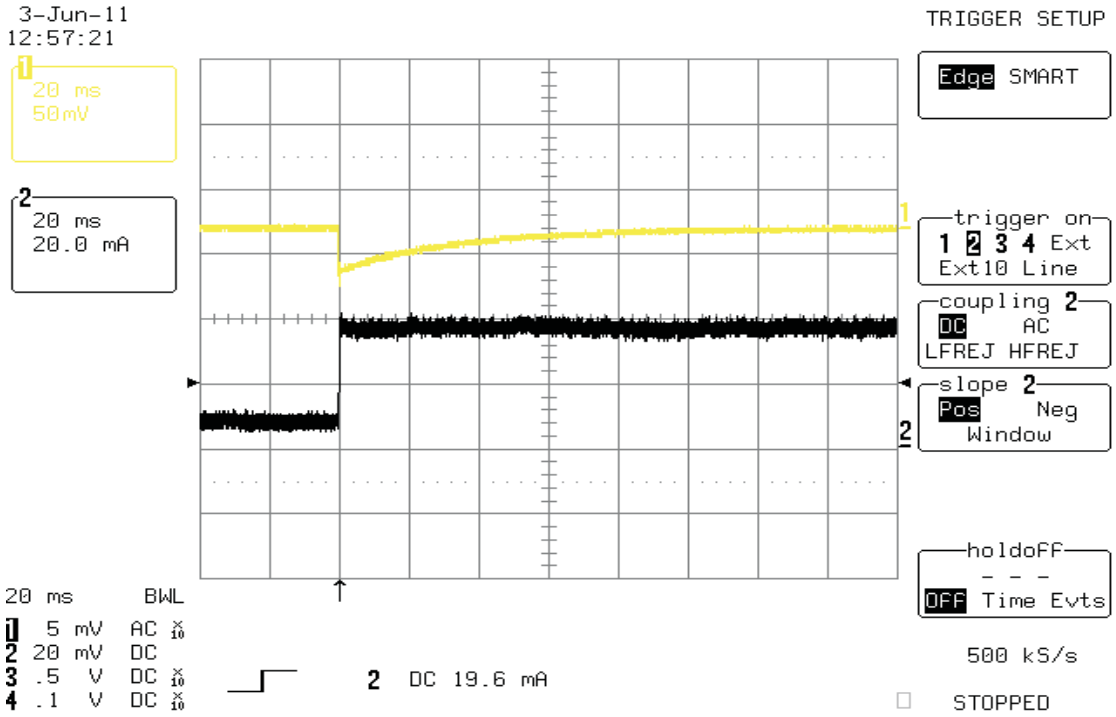

Figure 11. Load Transient, LDO : Vbat = 3.6 V with 0 mA to 30 mA Transient. CH3 VLDO, CH4 IVLDO

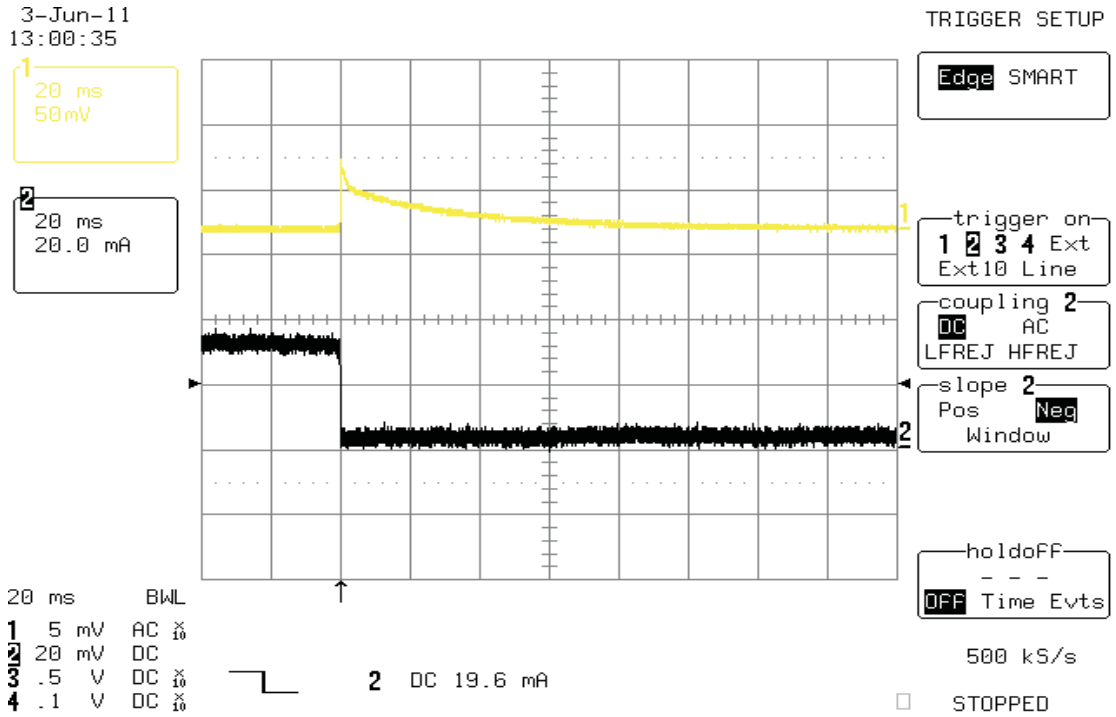

Figure 12. Load Transient, LDO : Vbat = 3.6 V with 30 mA to 0 mA Transient. CH3 VLDO, CH4 IVLDO

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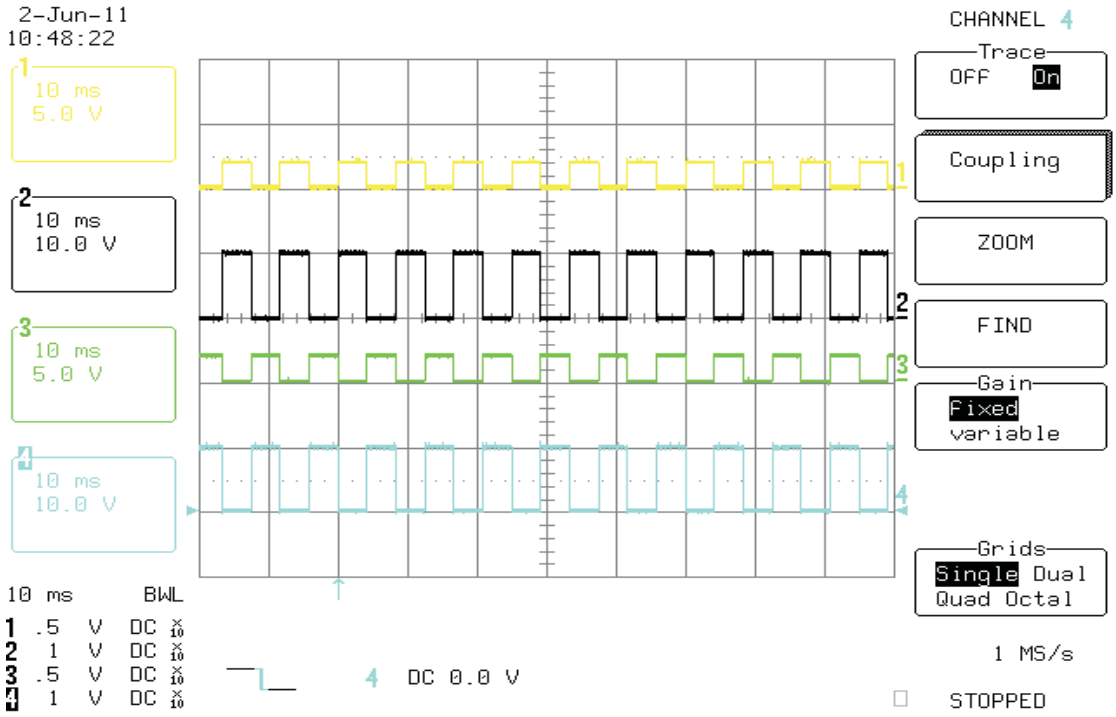

Figure 13. H-Bridge Operation : Ch. 1 - Function Generator Input to HBR1, Ch. 2 - LCRP output, Ch. 3 - Function Generator Input to HBR2, Ch. 4 - LCRN output

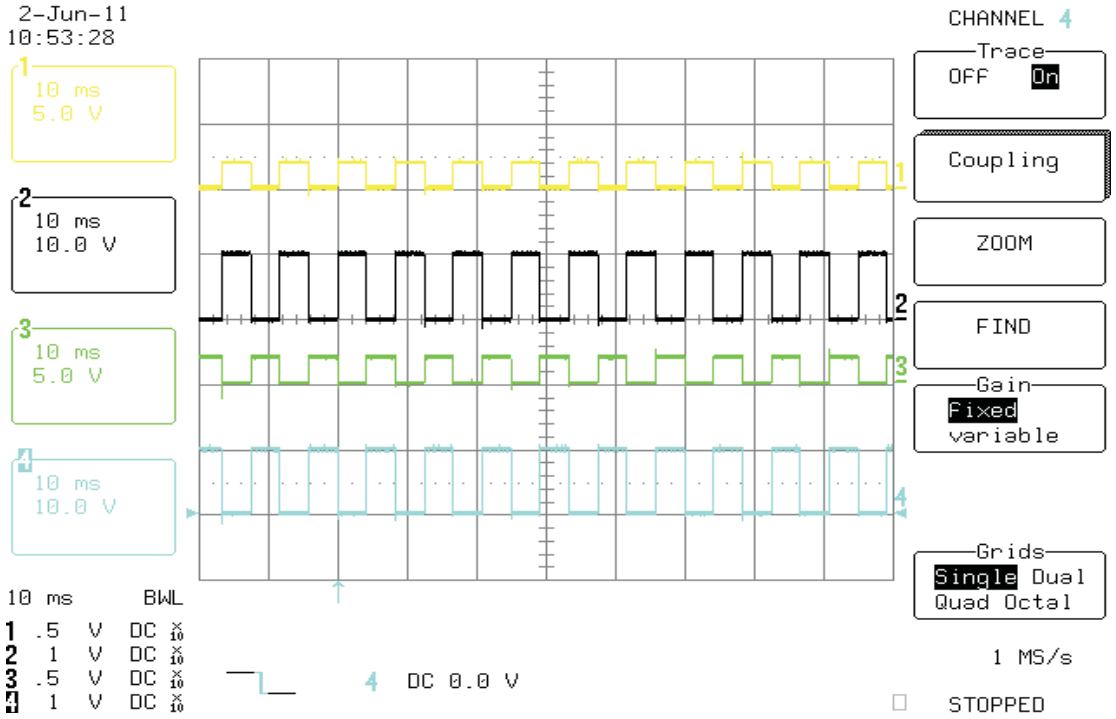

Figure 14. H-Bridge Operation : Ch. 1 - Function Generator Input to HBL1, Ch. 2 - LCLP output, Ch. 3 - Function Generator Input to HBL2, Ch. 4 - LCLN output

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6.2 Measured Data

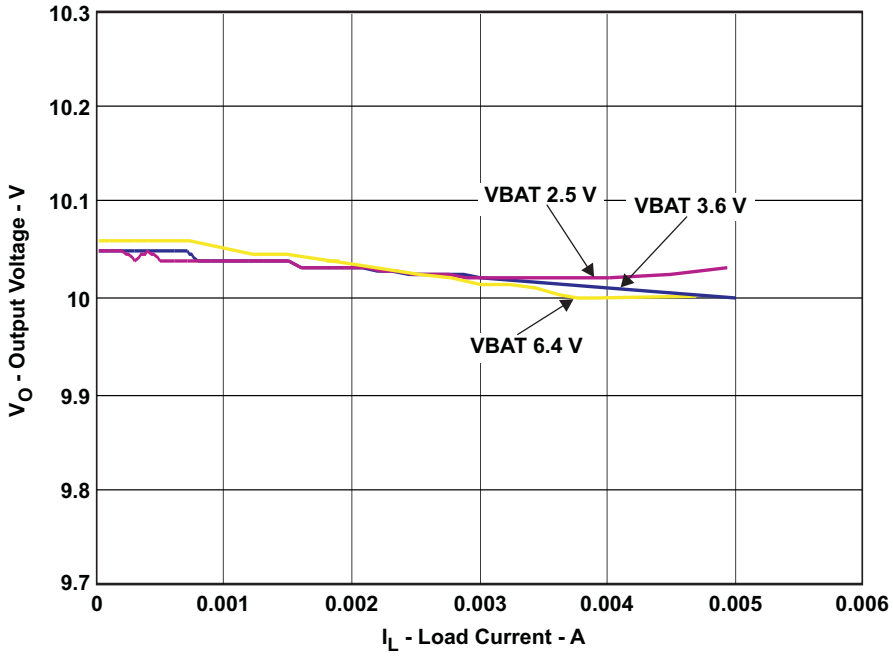

Figure 15. Load Regulation

6.3 Thermal Performance

Figure 16 and Figure 17 show the typical thermal performance for the TPS826xx for both the top side and the bottom side, respectively

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6.3.1 Top Side

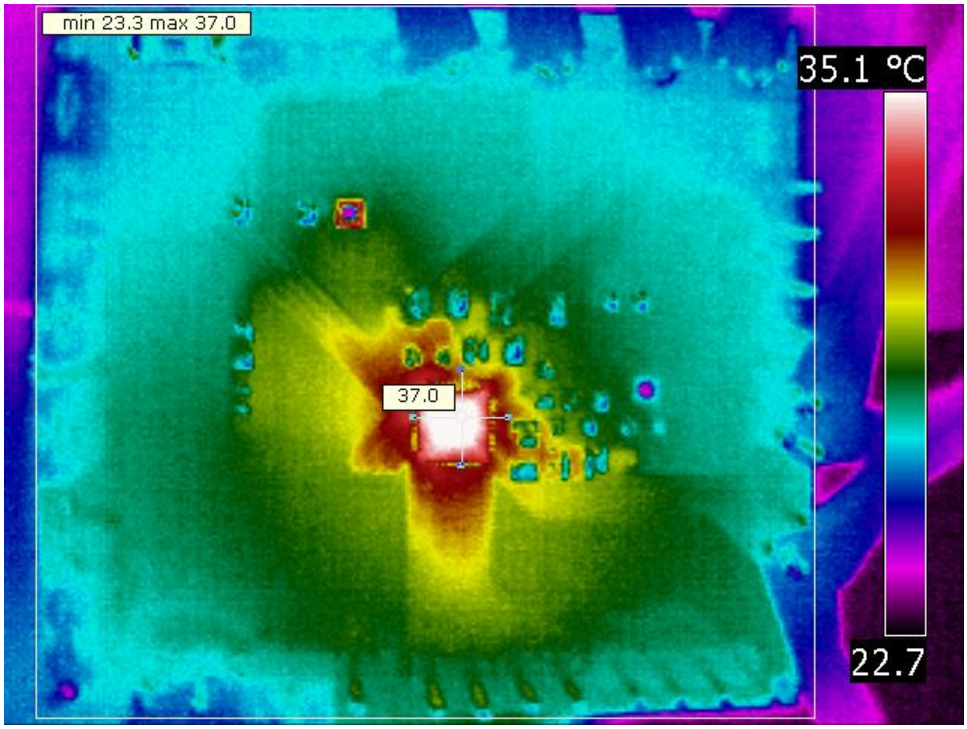

Figure 16. Thermal Performance – Top Side

6.3.2 Bottom Side

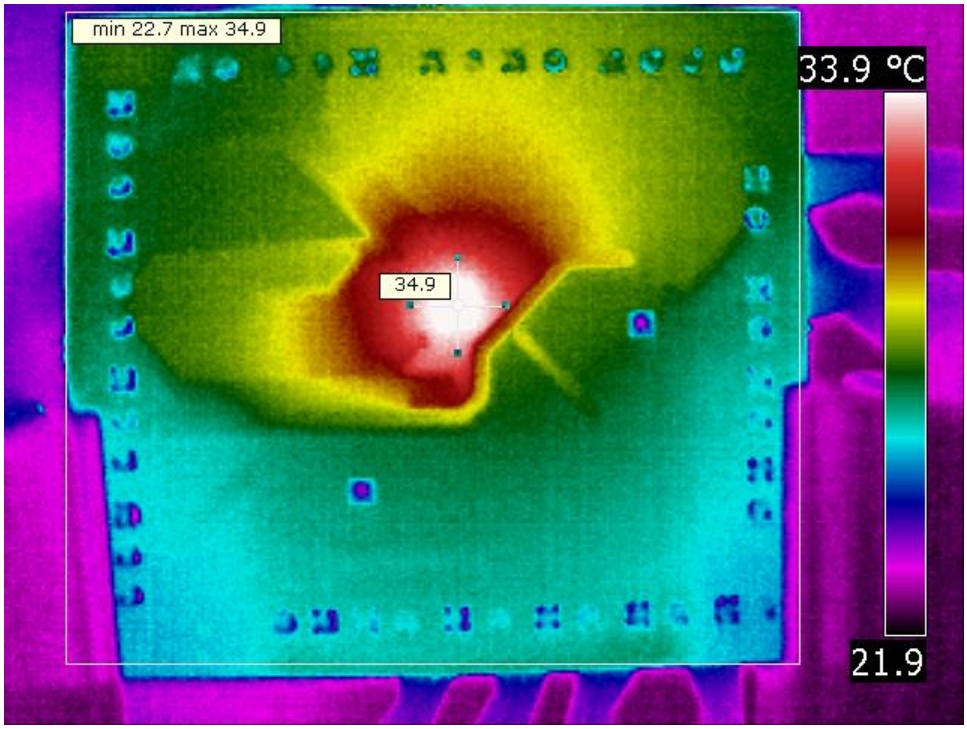

Figure 17. Thermal Performance – Bottom Side

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7 EVM Assembly Drawings and Layout

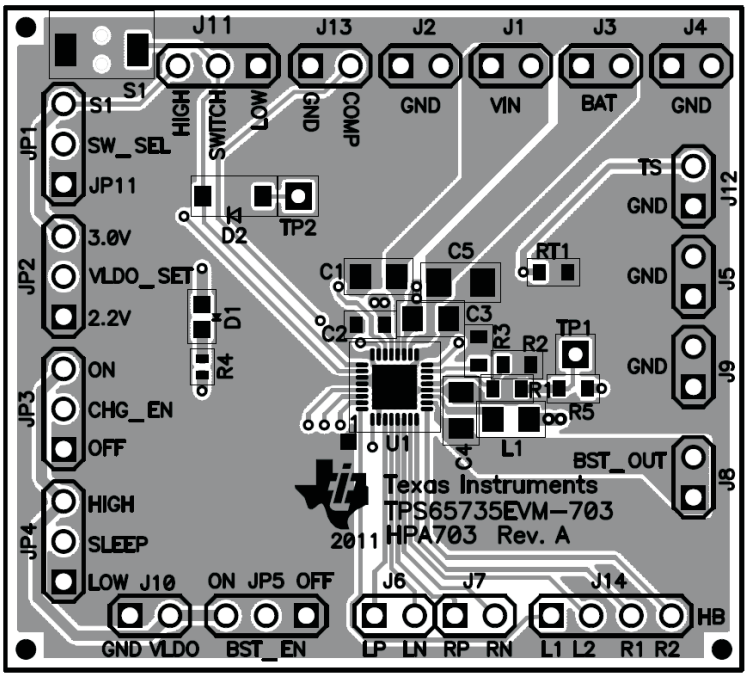

Figure 18. Top Assembly – Silkscreen

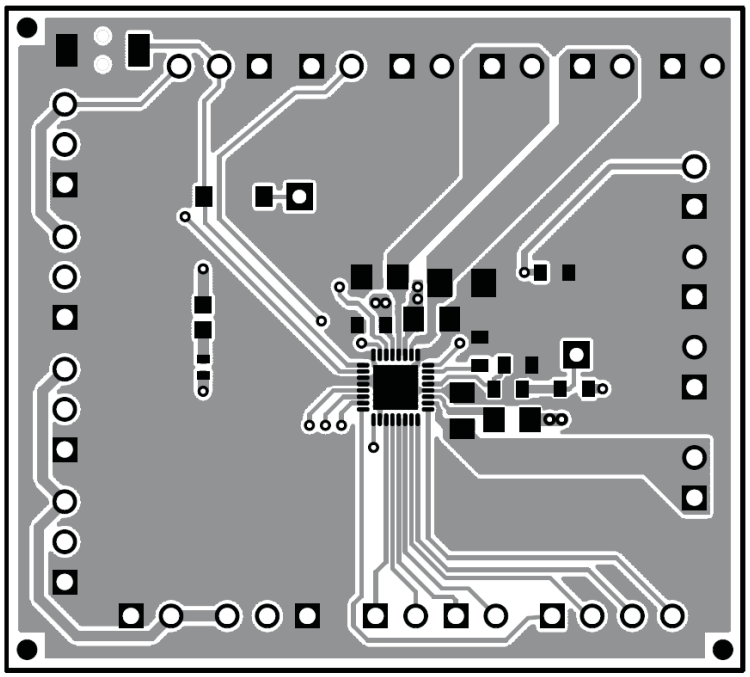

Figure 19. Top Layer

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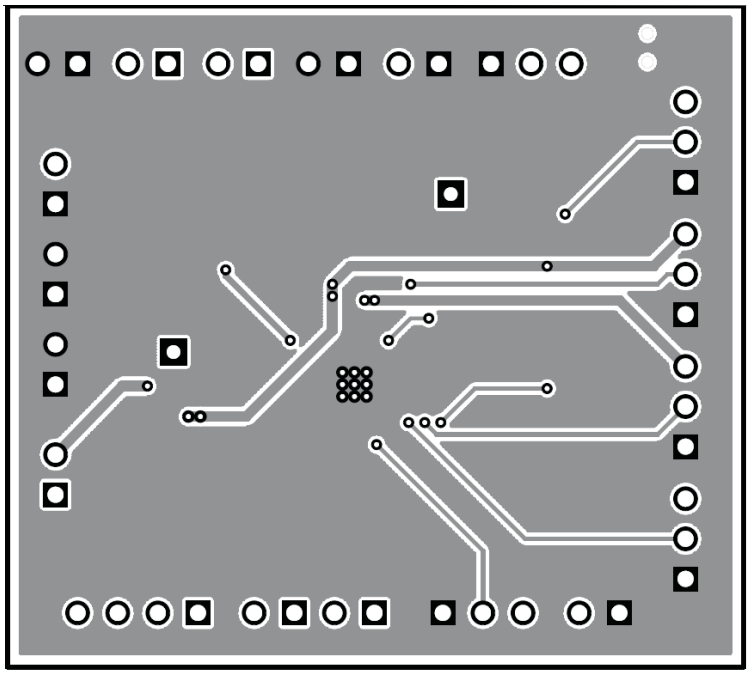

Figure 20. Bottom Layer

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8 Bill of Materials

Table 1. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	2.2 µF	Capacitor, Ceramic, 25V, X5R, 10%	0805	GRM219R61E225KA12D	Murata
1	C2	2.2 µF	Capacitor, Ceramic, 10V, X7R, 10%	0603	GRM188R71A225KE15D	Murata
1	C3	4.7 µF	Capacitor, Ceramic, 10V, X7R, 20%	0805	C2012X7R1A475M	TDK
1	C4	4.7 µF	Capacitor, Ceramic, 25V, X5R, 10%	0805	Std	STD
1	C5	10 µF	Capacitor, Ceramic, 16V, X5R, 20%	1206	Std	STD
1	L1	10uH	Inductor, 1.066Ohm , 350mA, 20%	0805	CBC2016T100M	Taiyo Yuden
1	R1	1.82M	Resistor, Chip, 1/16W, 1%	0603	Std.	STD
1	R2	243k	Resistor, Chip, 1/16W, 1%	0603	Std.	STD
1	R3	6.49K	Resistor, Chip, 1/16W, 1%	0603	Std	STD
1	R4	681	Resistor, Chip, 1/16W, 5%	0402	Std	STD
1	S1	SKRELDE010	Switch, SPST, PB Momentary,	0.140 X 0.173 inch	SKRELDE010	Alps
1	U1	TPS65735RSN	IC, PMU for Active Shutter 3D Glasses	QFN-32	TPS65735RSN	TI

Table 2. Evaluation Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	D1	LTST-C190CKT	Diode, LED, Red, 2.1-V, 20-mA, 6-mcd	0603	LTST-C190CKT	Lite On
0	D2	Open	Diode, Zener	SOD-123	STD	STD
12	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J12, J13	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
1	J11	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
1	J14	PEC04SAAN	Header, Male 4-pin, 100mil spacing,	0.100 inch x 4	PEC04SAAN	Sullins
5	JP1, JP2, JP3, JP4, JP5	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
1	R5	0	Resistor, Chip, 1/16W, 1%	0603	Std.	STD
0	RT1	Open	Thermistor, NTC, 10kOhms	0603	NCP18W103J03RC	Murata
2	TP1, TP2	STD	Test Point, O.032 Hole		STD	STD
5	—		Shunt, 100-mil, Black	0.100	929950-00	3M
1	—		PCB, 1.84" x 1.65" x 0.031"		HPA703	Any

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2.5 V to 6.4 V and the output voltage range of 8 V to 16 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50° C. The EVM is designed to operate properly with certain components above 50° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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