Multi-Rail Power Supply for Microcontrollers in Safety-Critical Applications

Check for Samples: TPS65381-Q1

FEATURES

- Multi-Rail Power Supply Supporting Among Others:
  - Texas Instruments TMS570LS Series 16/32-Bit RISC Flash Microcontroller
- Supply Rails:
  - Input voltage range:
    - 5.8 V to 36 V (CAN, I/O, MCU Core, and Sensor Supply Regulators Functional)
    - 4.5 V to 5.8 V (3.3-V I/O and MCU Core Voltage Functional)
  - 6-V Asynchronous Switch-Mode Pre-Regulator With Internal FET, 1.5-A Current Limit, and Temperature Protection
  - 5-V (CAN) Supply Voltage, Linear Regulator With Internal FET, and Temperature Protection
  - 3.3-V or 5-V MCU I/O Voltage, Linear Regulator With Internal FET, and Temperature Protection
  - 0.8-V to 3.3-V Adjustable MCU Core Voltage, Linear Regulator Controller With External FET
  - Sensor Supply: Linear Tracking Regulator With Tracking Input, 300-mA Current Limit, Temperature Protection, and Protection Against Short to Battery and Short to Ground
  - Reverse Battery Protection With External FET Allowing for Low-Voltage Operation Down To 4.5 V
  - Charge Pump: Typ. 12 V Above Battery Voltage
- Power Supply / System Monitoring:
  - Under- and Overvoltage Monitoring on All Regulator Outputs, Battery Voltage, and Internal Supplies
  - Self-Check on All Voltage Monitoring (During Power Up and After Power Up Initiated by External MCU)
  - Independent Voltage References for Regulator References and Voltage Monitoring. Voltage-Monitoring Circuitry With Separate Battery Voltage Input
  - Wake-Up Through Deglitched Ignition Signal
  - Wake-Up Through CAN WAKEUP Pin
  - Enable Circuit for Peripheral Device Wake-Up Circuitry or Power Stages
  - Junction Temperature Sensing With Shutdown Thresholds
- Microcontroller Interface
  - Open/Close Window or Question-Answer Watchdog Function
  - MCU Error-Signal Monitor (Supports TI TMS570 MCU Mode or Other MCUs with PWM-Like Signaling)
  - DIAGNOSTIC State for Performing Device Self-Tests, Diagnostics, and External Interconnect Checks.
  - Safe-State for Device and System Protection on Error Event Detection
  - Clock Monitor for Internal Oscillators
  - Self-Tests for Analog and Digital Critical Circuits Executed With Every Device Power Up or Activated by External MCU in DIAGNOSTIC State
  - CRC on Non-Volatile Memory and Device/System Configuration Registers
  - Reset circuit for MCU
- SPI Interface
  - Configuring IC Registers
  - Watchdog Question-Answering
  - Diagnostic Readout
  - Compliant With 3.3-V and 5-V Logic Levels
- Package: 32-Pin HTSSOP PowerPAD™ Package

APPLICATIONS

- Safety Critical Automotive Applications
  - Electrical Power Steering (EPS, EHPS)
  - Braking
  - Suspension
  - Airbag
- Industrial Safety Applications

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DESCRIPTION

The TPS65381-Q1 is a multi-rail power supply designed to supply microcontrollers in safety-critical applications, such as those found in automotive. The devices supports Texas Instruments' TMS570LS series 16/32-bit RISC flash MCU and other microcontrollers with dual-core lockstep (LS) or loosely coupled architectures (LC).

The TPS65381-Q1 integrates multiple supply rails to power the MCU, CAN or FlexRay, and an external sensor. An asynchronous buck switch-mode power-supply converter with internal FET converts the input battery voltage to a 6-V pre-regulator output. This 6 V is used to supply the other regulators.

A fixed 5-V linear regulator with an internal FET is integrated to be used as, for example, a CAN supply. A second linear regulator, also with an internal FET, regulates the 6 V to a selectable 5-V or 3.3-V MCU I/O voltage.

The TPS65381-Q1 comprises a linear regulator controller with external FET and resistor divider, regulating the 6 V to an externally adjustable core voltage of between 0.8 V and 2.6 V.

The device comprises a sensor supply with short-to-ground and short-to-battery protection. This supply can thus be used to power a sensor outside the electronic control unit (ECU).

The device has an integrated charge pump to provide overdrive voltage for the internal regulators. Reverse-battery protection can be obtained by using the charge pump output to control an external NMOS transistor. This solution allows for a lower minimum-battery-voltage operation compared to a traditional reverse-battery blocking diode.

The device monitors under- and overvoltage on all regulator outputs, battery voltage, and internal supply rails. A second band-gap reference, independent from the main band-gap reference, is used for the under- and overvoltage monitoring, to avoid any drifts in the main band-gap reference from being undetected. In addition, regulator current limits and temperature protections are implemented.

The TPS65381-Q1 functional safety architecture features a question-answer watchdog, MCU error-signal monitor, clock monitoring on internal oscillators, self-check on clock monitor, CRC on non-volatile memory, and a reset circuit for the MCU. A built-in self-test (BIST) allows for monitoring the device functionality at start-up. A dedicated DIAGNOSTIC state allows the MCU to check TPS65381-Q1 safety functions.

The TPS65381-Q1 is offered in an HTSSOP-32 PowerPAD package.

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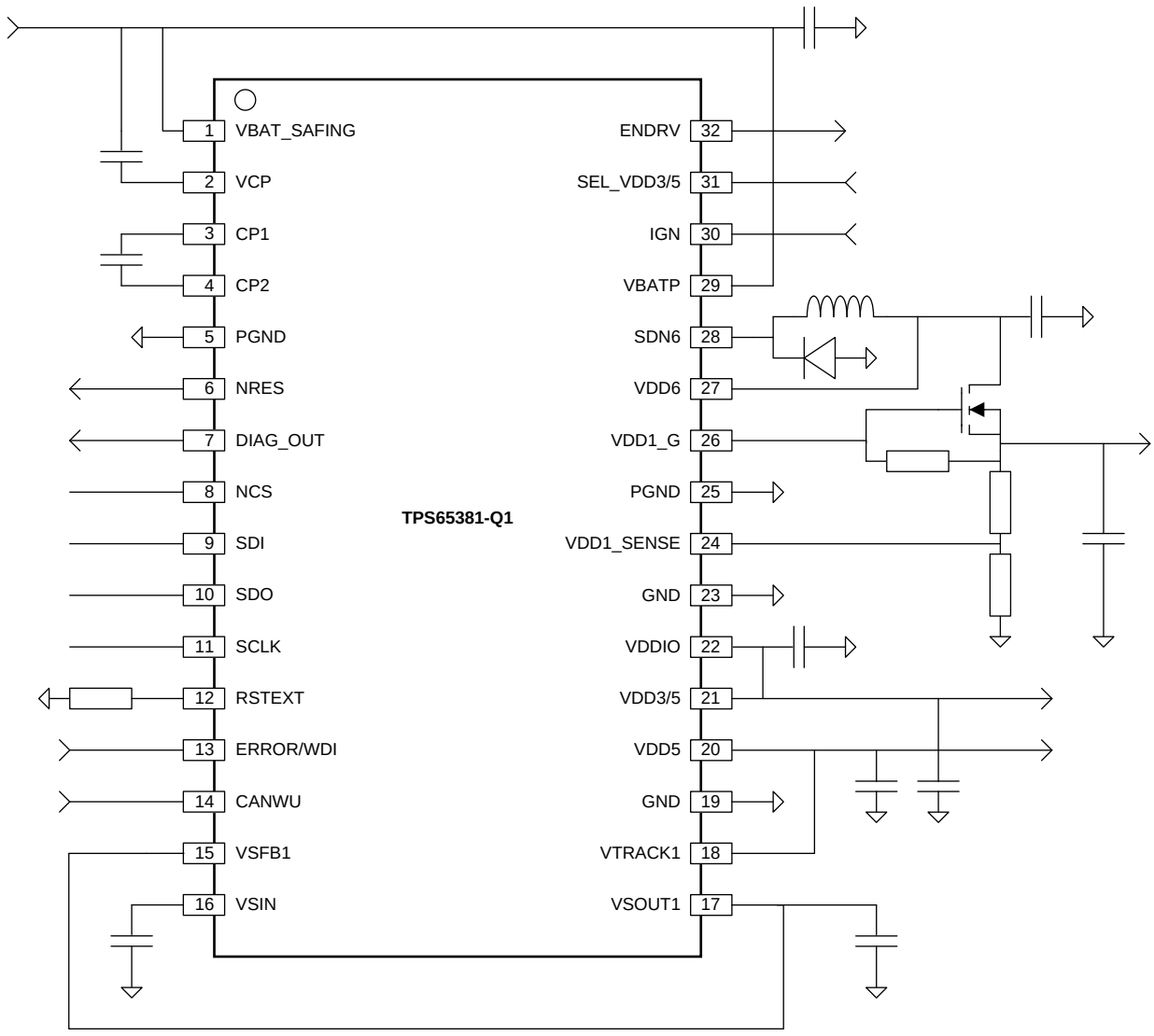


Figure 1. Typical Application Diagram

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

POS			VALUE	UNIT
M1.1	Protected battery voltage	VBATP, VBAT_SAFING, VSIN	–0.3 to 40	V
M1.2	Charge-pump voltages	VCP, CP1	–0.3 to 50	V
M1.3	Charge-pump pumping capacitor voltage	CP2	–0.3 to 40	V
M1.4	VDD6 switching-node voltage	SDN6	–0.3 to 40	V
M1.5	VDD6 output voltage	VDD6	–0.3 to 40	V
M1.6	VDD5 output voltage	VDD5	–0.3 to 7	V
M1.7	VDD3/5 output voltage	VDD3/5	–0.3 to 7	V
M1.8	VDD1_G voltage	VDD1_G	–0.3 to 15	V
M1.10	VDD1_SENSE voltage	VDD1_SENSE	–0.3 to 7	V
M1.11	Sensor supply tracking voltage	VTRACK1	–0.3 to 40	V
M1.12	Sensor supply feedback voltage	VSFB1	–2 to 40	V
M1.13	Sensor supply output voltage	VSOUT1	–2 to 40	V
M1.14	Analog/digital ref. output voltage	DIAG_OUT	–0.3 to 7	V
M1.15	Logic I/O voltage	VDDIO, ERROR/WDI, ENDRV, NRES, NCS, SDI, SDO, SCLK, DMUXO, SEL_VDD3/5, RSTEXT	–0.3 to 7	V
M1.16	IGN wake-up	IGN	–7 to 40	V
M1.17	CAN wake-up	CANWU	–0.3 to 40	V
M1.18	Operating virtual junction temperature range	T_J	–40 to 150	°C
M1.19	ESD	HBM on sensor supply pins VSOUT1 and VSFB1	±4	kV
M1.20		HBM on all other pins	±2	
M1.21		CDM on corner pins	±750	
M1.22		CDM on all other pins	±500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

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THERMAL INFORMATION

THERMAL METRIC(1)		TPS65381 HTSSOP-DAP 32 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	31.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	14.3	
θ_{JB}	Junction-to-board thermal resistance(4)	15.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.3	
ψ_{JB}	Junction-to-board characterization parameter(6)	15.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating temperature range (unless otherwise noted)

Pos		MIN	TYP	MAX	UNIT
R1.1	Input supply-voltage range on VBATP pins for initial power up	5.8			V
R1.2	Input supply voltage range on VBATP – VDD5, VDD3/5, VDD1 outputs functional (no undervoltage)	5.8	12	36	V
R1.3	Input supply-voltage range on VBATP – VDD6, VDD5 regulators in low dropout, VDD3 and VDD1 regulator outputs functional (no undervoltage). VSOUT1 either functional or in low dropout, depending on configuration.	4.5			V
R1.3a	Input supply voltage for VBAT_SAFING (when below minimum, device does not start up and NRES, ENDRV is pulled low.)	4.2		40	V
R1.4	VDDIO supply-voltage range (Note: VDDIO has internal pullup diode to VDD3/5.)	3.3		5	V
R1.5	Current consumption in standby mode (all regulator outputs disabled)			75	µA

ELECTRICAL CHARACTERISTICS

Over operating ambient temperature T_J = –40°C to 150°C and operating VBATP range 6 V to 36 V (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD6-BUCK With Internal FET							
AN	C_{VDD6}	Value of output ceramic capacitor	ESR range 100 mΩ to 300 mΩ	22		47	µF
AN	L_{VDD6}	Value of inductor		22	33		µH
A1.1	VDD6	VDD6 output voltage	Average dc value excl. ripple and load transients, VBAT > 7 V, 0 < I_{VDD6} < 1.3 A, inclding dc line and load regulation, temperature drift, and long-term drift	–10%	6	10%	V
A1.2	I_{VDD6}	I_{VDD5} + I_{VDD3} + I_{VDD1}+ I_{VSOUT1}	Load currents from VDD5, VDD3_5, VDD1 and VSOUT1; VDD6 not recommended to be loaded directly			1.3	A
A1.3	Vdropout6	VDD6 output dropout voltage Vdropout6 = (VBATP – SDN6)	I_{VDD6} = 1.3 A			0.6	V
A1.4	I_{VDD6_limit}	Current limit		1.5		2.5	A
VDD6-BUCK With Internal FET							

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ELECTRICAL CHARACTERISTICS (continued)

Over operating ambient temperature T_J = –40°C to 150°C and operating VBATP range 6 V to 36 V (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A1.5	F_{sw_VDD6}	Switching frequency	In continuous mode and steady state	–10%	440	10%	kHz
A1.6	DC_{VDD6}	Ton/Tperiod	VBATP > 7 V	7%		100%	
A1.7	$Tprot_{VDD6}$	Temperature protection threshold	Global shutdown	175		210	°C
VDD5 – LDO With Internal FET							
AN	C_{VDD5}	Value of output ceramic capacitor	ESR range 0 mΩ to 100 mΩ	1		5	µF
2.1	VDD5	VDD5 output voltage	0 < I_{VDD}5 < 300 mA, including line and load regulation, temperature drift, and long-term drift	–2%	5	2%	V
2.2	I_{VDD5}	VDD5 output current	Min. load with internal resistor of typ. 660 Ω			300	mA
2.3	$VDD5_{dyn}$	VDD5 output voltage dynamic	Load step 10% to 90% in 1 µs, with 5-µF C_{VDD5}	4.85	5	5.15	V
2.4	$VDD5_{max}$	Maximum VDD5 output voltage during VBATP step from 5.5 V to 13.5 V within 10 µs	C_{VDD5} = 5 µF, I_{VDD5} < 300 mA			5.5	V
2.5	Vdropout5	VDD5 output dropout voltage Vdropout5 = (VDD6-VDD5)	I_{VDD5} < 300 mA			0.30	V
2.6	$PSRR_{VDD5}$	Power supply rejection ratio	50 < f < 20 kHz,VBATP = 10 V, U = 4 Vpp C_{VDD5} = 5 µF, 0 < I_{VDD5} < 300 mA	40			dB
2.7	$LnReg_{VDD5}$	Line regulation (I_{VDD5} constant)	0 < I_{VDD5} < 300 mA, 8 V < VBATP < 19 V	–25		25	mV
2.8	$LdReg_{VDD5}$	Load regulation (VDD6 constant)	0 < I_{VDD5} < 300 mA, 8 V < VBATP < 19 V	–25		25	mV
2.9	$TmpCo_{VDD5}$	Temperature drift	Normalized to 25°C value	–0.5		0.5	%
			Empty				
2.11	dVDD5/dt	dV/dt at VDD5 at startup		5		50	V/ms
2.12	$t_{delayVDD5}$	VDD5 voltage stabilization delay	Maximum delay between rising edge on CANWU pin till VDD5 reaching end-value within 2%			2.5	ms
2.13	$Tprot_{VDD5}$	Temperature protection threshold	VDD5 switch-off	175		210	°C
2.14	I_{VDD5_limit}	Current limit		350		650	mA
VDD3/5 – LDO With Internal FET							
AN	$C_{VDD3/5}$	Value of output ceramic capacitor	ESR range 0 mΩ to 100 mΩ	1		5	µF
3.1	VDD3/5	VDD3/5 output voltage	SEL_VDD3/5 pin open: 3.3 V SEL_$V_{DD3/5}$ to ground: 5 V 0 < $I_{VDD3/5}$ < 300 mA, inclusive of line and load regulation, temperature drift	–2%	3.35	+2%	V
3.2	$I_{VDD3/5}$	VDD3/5 output current	Min. load with internal resistor: 440 Ω for 3.3-V setting 660 Ω for 5-V setting			300	mA
3.3	$VDD3/5_{dyn}$	VDD3/5 output voltage dynamic	Depending on 3.3 V/5 V setting Load step 10% to 90% in 1 µs, with 5 µF CVDD3/5	3.17 4.85	3.3 5.0	3.43 5.15	†
3.4	$VDD3/5_{max}$	Maximum VDD3/5 output voltage during VBATP step from 5.5 V to 13.5 V within 10 µs	Depending on 3.3 V/5 V setting $C_{VDD3/5}$ = 5 µF, $I_{VDD3/5}$ < 300 mA			3.6 5.5	V
3.5	Vdropout3/5	VDD3/5 output dropout voltage Vdropout3/5= (VDD6-VDD3/5)	$I_{VDD3/5}$ < 300 mA			0.3	V
3.6	$PSRR_{VDD3/5}$	Power-supply rejection ratio	50 < f < 20 kHz, VBATP = 10 V, U = 4 Vpp $C_{VDD3/5}$ = 5 µF, 0 < $I_{VDD3/5}$ < 300 mA	40			dB
3.7	$LnReg_{VDD3/5}$	Line regulation (I_{VDD3} constant)	0 < $I_{VDD3/5}$ < 300 mA, 8 V < VBATP < 19 V	–25		25	mV
3.8	$LdReg_{VDD3/5}$	Load regulation (VDD5 constant)	0 < $I_{VDD3/5}$ < 300 mA 8 V < VBATP < 19 V	–25		25	mV
3.9	$TmpCo_{VDD3/5}$	Temperature drift	Normalized to 25°C value	–0.5%		0.5%	
			Empty				

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ELECTRICAL CHARACTERISTICS (continued)

Over operating ambient temperature T_J = –40°C to 150°C and operating VBATP range 6 V to 36 V (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.11	dVDD35/dt	dV/dt at VDD3/5 at start-up	Depending on 3.3 V/5 V setting	3 5		30 50	V/ms
3.12	$t_{VDD3/5}$	VDD3/5 voltage stabilization delay	Maximum delay after CAN wake-up for VDD3/5 output to settle			2.5	ms
3.13	$Tprot_{VDD3/5}$	Temperature protection threshold	Global shutdown	175		210	°C
3.14	$I_{VDD3_5_limit}$	Current limit		350		650	mA
3.15	$I_{pu_SEL_VDD3/5}$	Pullup current on SEL_VDD3/5 pin				20	µA
VDD1 – LDO With External FET							
AN	Vgs(th)	Gate threshold voltage, external FET	ID = 1 mA	0.3		3	V
AN	Ciss	Gate capacitance, external FET	VGS = 0 V			3200	pF
AN	Qgate	Gate Charge ext. FET	VGS = 0 V to 10 V			70	nC
AN	gfs	Forward transconductance, external FET	ID = 50 mA	0.4			S
AN	C_{VDD1}	Value of output ceramic capacitor	ESR range 0 mΩ to 100 mΩ	5		40	µF
A4.1	VDD1	VDD1 output voltage	Depends on external resistive divider	0.8		3.3	V
A4.2	$VDD1_{SENSE}$	VDD1 reference voltage	10 mA < I_{VDD1} < 600 mA, including line and load regulation, temperature drift and long-term drift	–2%	0.8	2%	V
A4.3	I_{VDD1}	VDD1 output current	Minimum current realized with external resistive divider	10		600	mA
A4.4	$VDD1_G$	VDD1_G output voltage	Referred to GND			15	V
A4.5	$VDD1_{G_off}$	VDD1_G voltage in OFF condition	Test condition: 20 µA into VDD1_G pin			0.3	V
A4.6	I_VDD1_G	VDD1_G DC load current				200	µA
A4.7	$VDD1_{dyn}$	VDD1 output voltage dynamic	Load step 10% to 90% in 1 µs, with 40 µF C_{VDD1}	–4%		4%	V
A4.8	$VDD1_{max}$	Maximum VDD1 output voltage during VBATP step from 5.5 V to 13.5 V within 10 µs	C_{VDD1} > 6 µF, I_{VDD1}< 600 mA			10%	V
A4.9	$PSRR_{VDD1}$	Power-supply rejection ratio	50 < f < 20 kHz, VBATP = 10 V, U = 4 Vpp, C_{VDD1} = 10 µF, 10 mA < I_{VDD1} < 600 mA	40			dB
A4.10	$LnReg_{VDD1}$	Line regulation on VDD1_SENSE (I_{VDD1} constant)	10 mA < I_{VDD1}< 600 mA, 8 V < VBATP < 19 V	–7		7	mV
A4.11	$LdReg_{VDD1}$	Load regulation on VDD1_SENSE (VBATP constant)	10 mA < I_{VDD}1 < 600 mA, 8 V < VBATP < 19 V	–7		7	mV
A4.12	$TmpCo_{VDD1}$	Temperature drift	Normalized to 25°C value	–0.5%		0.5%	
			Empty				
A4.14	dVDD1/dt	dV/dt at VDD1_SENSE at start-up		0.8		8	V/ms
A4.15	$t_{delayVDD1}$	VDD1 voltage stabilization delay	Maximum delay after CAN wake-up for VDD1 output to settle			2.5	ms
VSOUT1 – LDO With Protected Internal FET							
AN	C_{VSOUT1}	Value of output ceramic capacitor	ESR range 0 mΩ to 100 mΩ	0.5		10	µF
5.1	VSOUT1	VSOUT1 output voltage	Depends on extal resistive divider.	3.3		9.5	V
5.2	MVVSOUT1	For tracking mode: Matching output errorMV_{VSOUT1} = (VTRACK1 – VSFB1)	0 < I_{VSOUT1} < 100 mA For specified IV_{SOUT} range, referenced to VTRACK1 input, including long-term and temperature drift.	–15		15	mV
5.3	VSFB1	For non-tracking mode: VSOUT1 reference voltage	10 mA < IV_{SOUT} < 100 mA, including line and load regulation, temperature drift and long-term drift	–2%	2.5	2%	V
5.3a	$VTRACK1_{th}$	Threshold for tracking/non-tracking	VTRACK1 > 1.2 V; VSOUT1 in tracking mode VTRACK1 < 1.2 V; VSOUT1 in non-tracking mode		1.2		V

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ELECTRICAL CHARACTERISTICS (continued)

Over operating ambient temperature T_J = –40°C to 150°C and operating VBATP range 6 V to 36 V (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.3b	$VTRACK1_{pd}$	Internal pulldown resistance on VTRACK1 pin			100		kΩ
5.4	IVSOUT1	VSOUT1 output current	internal resistor to dissipate min current			100	mA
5.5	VdrS1	VSOUT1 dropout voltage VdrS1 = (VSIN-VSOUT1)	T_J = –40°C to 165°C 0 < I_{VSOUT1} < 100 mA			0.75	V
5.6	$PSRR_{VSOUT1}$	Power-supply rejection ratio	With stable VTRACK1 input voltage 50 < f < 20 kHz, VBATP = 10 V, U = 4 Vpp C_{VSOUT1} = 1 µF, 0 < I_{VSOUT1} < 100 mA	40			dB
5.7	$LnReg_{VSOUT1}$	Line regulation I_{VSOUT1} constant)	0 < IVSOUT1 < 100 mA, 8 V < VBATP < 19 V	–25		25	mV
5.8	$LdReg_{VSOUT1}$	Load regulation (VSIN constant)	0 < IVSOUT1 < 100 mA, 8 V < VBATP < 19 V	–25		25	mV
5.9	$TmpCo_{VSOUT1}$	Temperature drift	Normalized to 25°C value	–0.5%		0.5%	
			Empty				
5.11	$VSOUT1_{SH}$	Output short circuit voltage range		–2		40	V
5.12	$–I_{VSIN}$	Output reverse current	VSOUT1 = 14 V and VBATP = 0 V, regulator switched off			20	mA
5.13	TprotVSOUT1	Temperature protection threshold	VSOUT1 switch-off	175		210	°C
5.14	I_{VSOUT1_limit}	Current limit		100		500	mA
VOLTAGE MONITORING							
6.1	VBATP_UVoff	VBATP level for switching off VDDx		4.2		4.5	V
6.2	VBATP_UVon	VBATP level for switching on VDDx		5.4		5.8	V
6.3	VBATP_UVhys	Undervoltage hysteresis		1.1		1.4	V
6.4	VBATP_OVrise	VBATP level for setting VBAT_OV flag		29.5		32.5	V
6.5	VBATP_OVfall	VBATP level for clearing VBAT_OV flag		29		32	V
6.6	VBATP_OVhys	Overvoltage hysteresis		0.2		0.9	V
6.7	VBATP_deglitch	VBATP under/overvoltage monitor deglitch time			200		µs
6.8	VDD5_UV	VDD5 undervoltage level		4.5		4.85	V
6.9	VDD5_UVhead	VDD5 undervoltage headroom (VDD5act – VDD5_UVact)		200			mV
6.10	VDD5_OV	VDD5 overvoltage level		5.2		5.5	V
6.11	VDD5_OVhead	VDD5 overvoltage headroom (VDD5_OVact – VDD5act)		200			mV
6.12	VDD3/5_UV	VDD3/5 undervoltage level 3.3-V setting 5-V setting		 2.97 4.5		 3.17 4.8	V
6.13	VDD3/5_UVhead	VDD3/5 undervoltage headroom (VDD3/5act – VDD3/5_UVact) 3.3-V setting 5-V setting		 170 200			mV
6.14	VDD5_3_OV	VDD5_3 overvoltage level 3.3-V setting 5-V setting		 3.43 5.2		 3.63 5.5	V
6.15	VDD3/5_UVhead	VDD3/5 undervoltage headroom (VDD3/5_OVact – VDD3/5act) 3.3-V setting 5-V setting		 170 200			mV
6.16	VDD1_UV	VDD1 undervoltage level	Sensed on VDD1_SENSE pin	0.94		0.97	VDD1
6.17	VDD1_OV	VDD1 overvoltage level	Sensed on VDD1_SENSE pin	1.03		1.06	VDD1
6.18	VDDx_deglitch	VDDx under/overvoltage monitor deglitch time		10		40	µs
6.19	VSOUT1_UV	VSOUT1 undervoltage level	Sensed on VSFB1 pin	0.88		0.94	VSOUT 1
6.20	VSOUT1_OV	VSOUT1 overvoltage level	Sensed on VSFB1 pin	1.06		1.12	VSOUT 1
6.21	VSOUT1_deglitch	VSOUT1 under/overvoltage monitor deglitch time		10		40	µs

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ELECTRICAL CHARACTERISTICS (continued)

Over operating ambient temperature T_J = –40°C to 150°C and operating VBATP range 6 V to 36 V (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.22	VDD6_UV	VDD6 undervoltage level		5.2		5.4	V
6.23	VDD6_OV	VDD6 overvoltage level		7.8		8.2	V
IGNITION and CAN WAKE-UP							
7.1	IGN_WUP	IGN wake-up threshold		2		3	V
7.2	CAN_WUP	CAN wake-up threshold		2		3	V
7.3	WUP_hyst	Wake-up hysteresis		50		200	mV
7.4	I_IGN	IGN forward leakage current				50	µA
7.5	I_IGN_rev	IGN current at –7 V				–1	mA
7.6	IGN_deg	IGN deglitch filter time		7.5		22	ms
7.7	I_CAN	CAN forward leakage current				50	µA
7.8	I_CAN_rev	CAN current at –0.3 V				1	mA
7.9	CAN_deg	CAN deglitch filter time		100		350	µs
Charge Pump							
AN	C_{pump}	Pumping capacitor			10		nF
AN	C_{store}	Storage capacitor			100		nF
8.1	VCP_{on}	VCP output voltage in on-state	VBATP > 5.8 V	VBATP + 4		VBATP + 15	V
8.2	I_{CP}	External load				100	µA
8.3	f_{CP}	Charge-pump switching frequency			250		kHz
Reset and Enable Outputs							
9.1	$V_{NRES_ENDRV_L}$	NRES / ENDRV low output level	With external 5-mA open-drain current			0.2	V
9.2	$R_{NRES_ENDRV_PULLUP}$	NRES / ENDRV internal pullup resistance		3		6	kΩ
9.2a	$R_{dson_ENDRV_NRES}$	$r_{ds(on)}$ NRES/ENDRV pulldown transistor		11		86	Ω
9.3	R_{RSTEXT}	Value of external reset extension resistor(1)	In case of open-connect, device stays in RESET state.	0	22		kΩ
9.4	$t_{RSTEXT(22k\Omega)}$	Reset extension delay		4.05	4.5	4.95	ms
9.4a	$t_{RSTEXT(0k\Omega)}$	Reset extension delay			1.4		ms
9.5	$V_{ENDRV_NRES_TH}$	ENDRV and NRES readback threshold	Read-back muxed to DIAG_OUT pin	300	400	500	mV
Digital Input / Output							
10.1	V_{DIGIN_HIGH}	Digital input, high level		2			V
10.2	V_{DIGIN_LOW}	Digital input, low level				0.8	V
10.3	V_{DIGIN_HYST}			0.1			V
10.4			Empty				
10.5	V_{DIGOUT_HIGH}	Digital output, high level	Iout = –2 mA (out of pin)	VDDIO – 0.2			V
10.6	V_{DIGOUT_LOW}	Digital output, low level	Iout = 2 mA (into pin)			0.2	V
Internal System Clock							
11.1	f_{Sysclk}	System clock frequency		3.8	4	4.2	MHz
Window Watchdog							
12.1	$t_{ERROR_WDI_deglitch}$	Deglitch time on ERROR/WDI pin		14.25	15	15.75	µs
Serial Peripheral Interface Timing							
13.1	f_{SPI}	SPI clock (SCLK) frequency				8(2)	MHz
13.2	t_{SPI}	SPI clock period		125			ns
13.3	t_{high}	High time: SCLK logic high duration		45			ns
13.4	t_{low}	Low time: SCLK logic low duration		45			ns
13.5	t_{sucs}	Setup time NCS: time between falling edge of NCS and rising edge of SCLK		45			ns

(1) In case of open-connect, device stays in RESET state.
(2) MAX SPI Clock tolerance is ±10%

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ELECTRICAL CHARACTERISTICS (continued)

Over operating ambient temperature T_J = –40°C to 150°C and operating VBATP range 6 V to 36 V (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
13.6	t_{d1}	Delay time: time delay from falling edge of NCS to data valid at SDO				30	ns
13.7	t_{susi}	Setup time at SDI: setup time of SDI before the rising edge of SCLK				15	ns
13.8	t_{d2}	Delay time: time delay from falling edge of SCLK to data valid at SDO		0		30	ns
13.9	t_{hcs}	Hold time: time between the falling edge of SCLK and rising edge of NCS		45			ns
13.10	t_{hlcs}	SPI transfer inactive time (time between two transfers)		250			ns
13.11	t_{tri}	Hi-Z state delay time: time between rising edge of NCS and SDO in Hi-Z state				15	ns
13.12	R_{PULL_UP}	Internal pullup resistor on NCS input pin		40	70	100	kΩ
13.13	R_{PULL_DOWN}	Internal pulldown resistor on SDI and SCLK input pins		40	70	100	kΩ
NOTE: Capacitance at C_{SDO} = 100 pF							

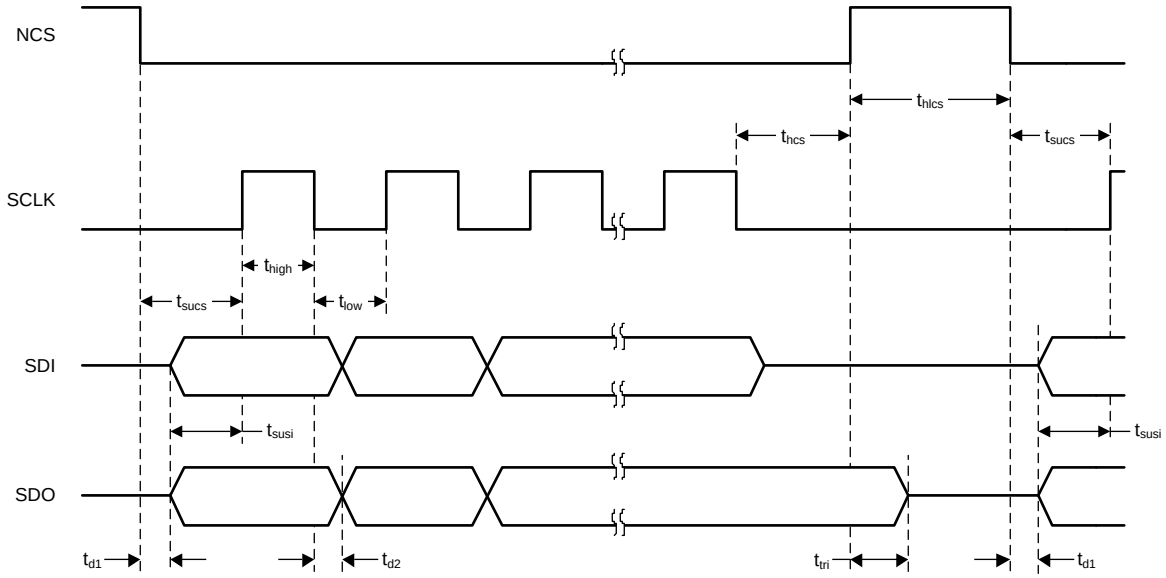


Figure 2. SPI Timing Parameters

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PIN ASSIGNMENT

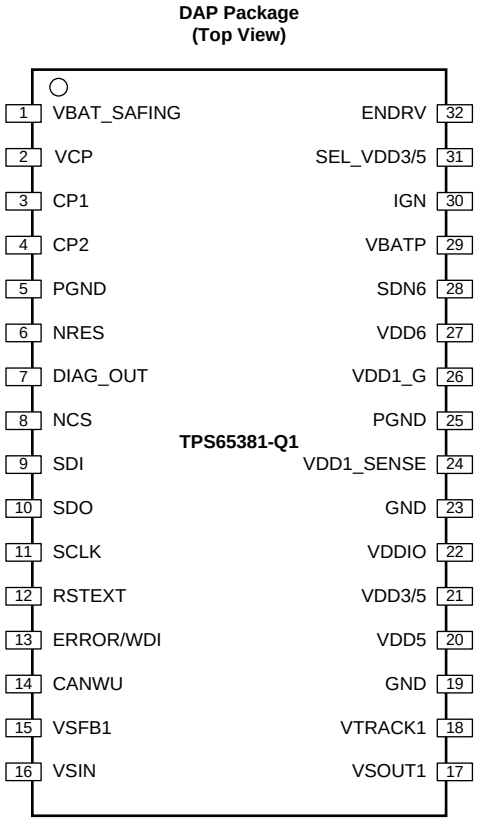


Figure 3. HTSSOP-32 Package (DAP)

PIN FUNCTIONS

PIN		I/O/ PWR/GND	DESCRIPTION
NAME	NO.		
CANWU	14	I	Wake-up input signal from CAN tranceiver
CP1	3	PWR	Charge-pump external capacitor, high-voltage side
CP2	4	PWR	Charge-pump extenal capacitor, low-voltage side
DIAG_OUT	7	O	Analog MUX output for MCU ADC
ENDRV	32	O	Enable output signal for peripherals (for example, motor-driver IC).
ERROR/WDI	13	I	Error input signal from MCU / window watchdog input trigger
GND	19, 23	GND	Ground (analog)
IGN	30	I	Wake-up signal from ignition key
NCS	8	I	SPI chip select (active-low)
NRES	6	O	Cold-reset (NPOR_RST) output signal for µC
PGND	5, 25	I	Ground (power)
RSTEXT	12	I	Configuration pin for reset extension
SCLK	11	I	SPI clock
SDI	9	I	SPI serial data IN
SEL_VDD3/5	31	I	Select input for VDD3/5 regulator
SDN6	28	PWR	Switching node for VDD6 switch-mode regulator
SDO	10	O	SPI serial data OUT
VBATP	29	PWR	Battery voltage (reverse protected)
VBAT_SAFING	1	PWR	Battery voltage (reverse protected) for safety functions

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PIN FUNCTIONS (continued)

PIN		I/O/ PWR/GND	DESCRIPTION
NAME	NO.		
VCP	2	PWR	Charge-pump output voltage
VDD1_G	26	O	Gate of external FET for VDD1 regulator
VDD1_SENSE	24	I	Input reference for VDD1 regulator
VDD3/5	21	I	VDD3/5 regulator output voltage
VDD5	20	PWR	VDD5 regulator output voltage
VDD6	27	PWR	VDD6 switch-mode regulator output voltage
VDDIO	22	PWR	I/O-level for pins from/to MCU
VSFB1	15	I	Feedback input reference for sensor supply regulator
VSIN	16	PWR	Sensor supply regulator input supply voltage
VSOUT1	17	PWR	Sensor supply regulator output voltage
VTRACK1	18	I	Tracking input reference for sensor supply regulator
Thermal pad	–		Connected to GNDIO. Place thermal vias to large ground plane and connect to AGND and GNDIO pin.

FUNCTIONAL BLOCK DIAGRAM

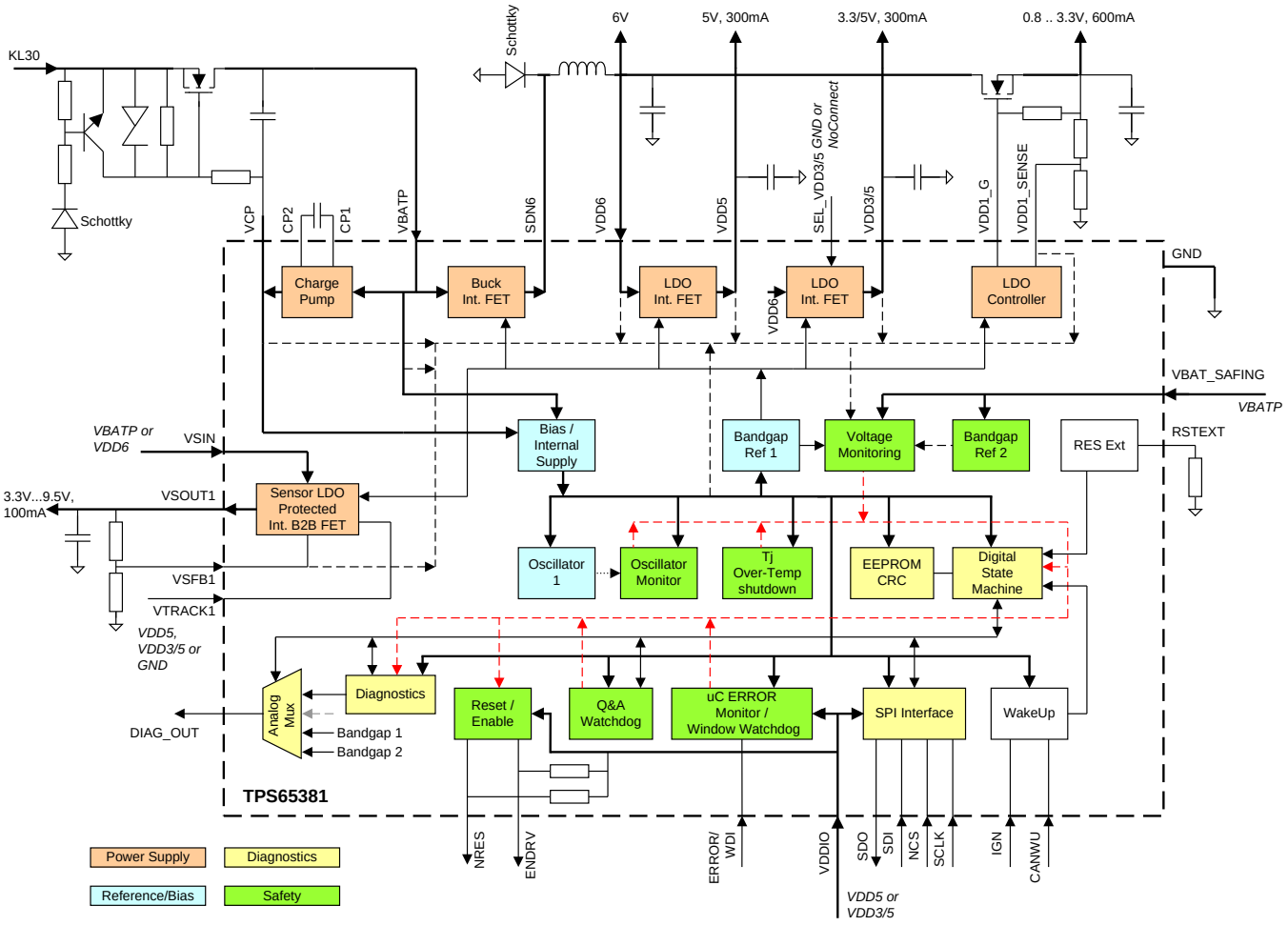


Figure 4. TPS65381-Q1 Functional Block Diagram

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DETAILED DESCRIPTION

VDD6 Buck Switch-Mode Power Supply

The purpose of the VDD6 buck switch-mode power supply is to reduce the power dissipation inside the IC. It converts the ingoing power for VDD5, VDD3/5, VDD1 and VSOUT1 from the battery-voltage domain to the 6-V voltage domain. Hence, VDD6 is intended to be used as pre-regulator only; its output voltage is less accurate compared to VDD5, VDD3/5, VDD1, and VSOUT1. The VDD6 output-current capability is dimensioned to supply VDD5, VDD3/5, VDD1, and VSOUT1 at their respective maximum output currents.

This switch-mode power supply (SMPS) operates with fixed-frequency adaptive on-time control pulse-width modulation (PWM). Its control loop is based on a hysteretic comparator. The internal N-channel MOSFET is turned on at the beginning of each cycle. This MOSFET is turned off when the hysteretic PWM comparator resets the latch. Once this internal MOSFET is turned OFF, the external Schottky diode recirculates the energy stored in the inductor for the remainder of the switching period. In order to preserve sufficient headroom for the VDD5 regulator at low battery voltage, the VDD6 regulator is put in dropout mode for battery voltage below 7 V.

The internal MOSFET is protected from excess power dissipation with a current-limit circuit, and junction overtemperature protection shared with VDD3/5. In case of an overtemperature condition in VDD6 detected by the VDD3/5 overtemperature protection, the TPS65381-Q1 goes to the STANDBY state (all regulators switched off).

VDD5 Linear Regulator

This is a regulated supply of 5 V ±2% over temperature and battery supply range. A low-ESR ceramic capacitor is required for loop stabilization; this capacitor must be placed close to the pin of the IC. This output is protected against shorts to ground by a current limit, and limits output voltage overshoot during power up, or during line or load transients.

On an initial IGN or CANWU power cycle, the soft-start circuit on this regulator is initiated. This is typically in the 1-ms to 2-ms range. This output may require a larger output capacitor to ensure that during load transients the output does NOT drop below the required regulation specifications.

The internal MOSFET is protected from excess power dissipation with junction overtemperature protection. In case of an overtemperature condition in VDD5, only the VDD5 regulator is be switched off by clearing bit 4 in the SENS_CTRL register. In order to re-enable VDD5, first bit 1 in SAFETY_STAT 1 must be cleared on readout, and after that bit 4 in the SENS_CTRL register must be set again.

VDD3/5 Linear Regulator

This is a regulated supply of 3.3 V or 5 V ±2% over temperature and battery supply range. The output voltage level can be selected with the SEL_VDD5/3 pin (open pin selects 3.3 V, grounded pin selects 5 V). The state of this selection pin is sampled and latched directly at the first initial IGN or CANWU power cycle. Once latched, any change in the state of this selection pin after the first initial IGN or CANWU power cycle does not change the initially selected state of the VDD3/5 regulator.

A low-ESR ceramic capacitor is required for loop stabilization; this capacitor must be placed close to the pin of the IC. This output is protected against shorts to ground by a current limit, and limits output-voltage overshoot during power up or during line or load transients.

On an initial IGN or CANWU power cycle, the soft-start circuit on this regulator is initiated. This is typically in the 1-ms to 2-ms range. This output may require a larger output capacitor to ensure that during load transients the output does NOT drop below the required regulation specifications.

The internal MOSFET is protected from excess power dissipation with a current-limit circuit and junction overtemperature protection. In case of an over-temperature in VDD3/5, the TPS65381-Q1 goes to STANDBY state (all regulators switched-off)

VDD1 Linear Regulator

This is an adjustable supply between 0.8 V and 3.3 V ±2% over temperature and battery supply range.

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In order to reduce on-chip power consumption, an external power NMOS is used. The regulation loop and the command gate drive are integrated. It is recommended to apply a resistor in the range of 100 kΩ to 1 MΩ between the gate and source of the external power NMOS. The VDD1 gate output is limited to prevent gate-source overvoltage stress during power up or during line or load transients.

On an initial IGN or CANWU power cycle, the soft-start circuit on this regulator is initiated. This is typically in the 1-ms to 2-ms range. This soft-start is meant to prevent any voltage overshoot at start-up. The VDD1 output may require larger output capacitor to ensure that during load transients the output does not drop below the required regulation specifications.

The VDD1 LDO itself does not have a current limit and no overtemperature protection for the external NMOS FET. Therefore, it is recommended to supply VDD1 from VDD6 (see Figure 4). In this way, VDD6 current limit acts as current limit for VDD1 and the power dissipation is limited as well. In order to avoid damage in the external NMOS FET, it is recommended to choose its current rating well above the maximum specified VDD6 current limit.

If the VDD1 regulator is not being used, leave the VDD1_G and VDD1_SENSE pins open. An internal pullup device on VDD1_SENSE detects the open connection and pulls up VDD1_SENSE. This forces the regulation loop to bring the VDD1_G output down. A VDD1 overvoltage is detected, which would normally prohibit assertion of ENDRV pin. In case the VDD1 regulator is not being used, the MCU can configure the TPS65381-Q1 to ignore the VDD1 overvoltage flag. This allows the assertion of the ENDRV pin in that case.

This internal pullup device on the VDD1_SENSE pin also prevents a real VDD1 overvoltage on the MCU core supply in case of an open connection to the VDD1_SENSE pin, as it brings the VDD1_G pin down. So in this situation, the VDD1 output voltage is 0 V, but internally the TPS65381-Q1 reports an overvoltage flag.

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VSOUT1 Linear Regulator

This is a regulated supply with two separate modes: tracking mode and non-tracking mode. The mode selection occurs with the VTRACK1 pin. When the voltage applied on the VTRACK1 pin is above 1.2 V, VSOUT1 is in tracking mode. When the VTRACK1 pin is shorted to ground, VSOUT1 is in non-tracking mode. This mode selection occurs during the first ramp-up of the VDDx rails, and is latched after the first VDDx ramp-up is completed.

In tracking mode, VSOUT1 tracks the input reference voltage on the VTRACK1 pin with a gain factor determined by the external resistive divider. The tracking offset between VTRACK1 and VSFB1 is ±15 mV over temperature and battery supply range. This mode allows, for instance, VSOUT1 to be 5 V while tracking the VDD3 (3.3-V) supply. In unity-gain feedback, VSOUT1 can directly follow VDD5 or VDD3.

In non-tracking mode, the VSOUT1 output voltage proportional to a fixed reference voltage of 2.5 V at the VSFB1 pin, with a gain factor determined by the external resistive divider. This mode allows VSOUT1 to be any factor of the internal reference voltage.

Both in tracking and non-tracking mode, the VSOUT1 output voltage must 3.3 V or higher. VSOUT1 can track VDD3/5 in 3.3-V setting within the specified limits.

VSOUT1 has a separate input supply to reduce the internal power dissipation. For an output voltage of 3.3 V or 5 V, for instance, VDD6 can be used as the input supply. For an output voltage of >5 V, VBATP can be used as the input supply. Here, the maximum power dissipation for the internal FET should not exceed 0.6 watt to avoid thermal shutdown.

A low-ESR ceramic capacitor is required for loop stabilization; this capacitor must be placed close to the pin of the IC. This output is intended for going outside the ECU; hence, it is protected against shorts to external chassis ground by a current limit. Furthermore, in case of output shorted to battery voltage, any potential reverse current going back inside the ECU is blocked, hence preventing any unintended supplying of the ECU by this VSOUT1 output. This regulator also limits output-voltage overshoot during power up or during line or load transients.

VSOUT1 is disabled by default on start-up. After NRES release, the MCU can enable VSOUT1 via SPI command. After this SPI command, the soft-start circuit on this regulator is initiated. This is typically in the 1-ms to 2-ms range. This output may require a larger output capacitor to ensure that during load transients the output does NOT drop below the required regulation specifications. Regardless of tracking or non-tracking mode, the VSFB1 is ramped to its desired value after completion of the soft start.

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The internal MOSFET is protected from excess power dissipation with a current-limit circuit and junction over-temperature protection. In case of an overtemperature condition in VSOUT1, only the VSOUT1 regulator is switched off by clearing bit 0 in the SENS_CTRL register. In order to re-enable VSOUT1, first bit 2 in SAFETY_STAT 1 must be cleared on read-out, and after that bit 0 in SENS_CTRL register must be set again.

The VSFB1 pin can be observed at an ADC input of the MCU through the DIAG_OUT pin. This allows the detection of a short to any other supply prior to enabling the VSOUT1 LDO.

Charge Pump

The charge pump is configured to supply an overdrive voltage of typically 12 V to the supply voltage. This overdrive voltage is needed for driving the gate voltages of the internal NMOS-FETs of the VDDx and VSOUT1 supply rails. Furthermore, this overdrive voltage can be used to drive the gate of an external NMOS power FET acting as reverse-battery protection. Such reverse-battery protection allows for lower minimum-battery-voltage operation compared to a traditional reverse-battery blocking diode. If such reverse battery protection is used, a series resistance of about 10 kΩ must be connected between the VCP pin and the gate of the NMOS power FET (see Figure 4). This series resistance is needed to limit any current out of the VCP pin when the gate of the NMOS power FET is driven to negative voltage, because the absolute-maximum rating of the VCP pin is limited to –0.3V due to a parasitic reverse diode to the substrate, that is, ground.

The charge pump requires two external capacitors, one bucket capacitor and one buffer capacitor. In order to have sufficient overdrive voltage out of the charge pump even at low battery voltage, the external load current on the VCP pin should be less than 100 µA.

Wake-Up

The TPS65381-Q1 has two wake-up pins: IGN and CANWU. Both pins have a wake-up threshold level between 2 V and 3 V, and a hysteresis between 50 mV and 200 mV.

The IGN wake-up pin is level-sensitive, and has a deglitch (filter) time between 7.5 ms and 22 ms. The TPS65381-Q1 provides a power-latch function (POST_RUN) for this IGN pin, allowing the MCU to decide when to power down the TPS65381-Q1 through SPI. For this, the MCU must set the IGN power-latch bit 4 (IGN_PWRL) in the SPI SAFETY_FUNC_CFG register, and it can read the unlatched status of the deglitched (filtered) IGN pin on SPI register DEV_STAT, bit 0 (IGN). To go to the STANDBY state, the MCU must clear the IGN_PWRL bit. The IGN_PWRL bit is also cleared after a detected CANWU wake-up event. Furthermore, the TPS65381-Q1 provides an optional transition to the RESET state after a detected IGN wake-up during the POST_RUN (see Figure 6)

The CANWU pin is edge-sensitive; a minimum 350-µs pulse duration is needed for wake-up. The CANWU wake-up is latched, allowing the MCU to decide when to power down the TPS65381-Q1 through SPI command WR_CAN_STBY.

Reset Extension

The TPS65381-Q1 releases the reset to the external MCU through the NRES pin with a certain delay time (reset extension time) after the VDD3/5 and VDD1 have crossed their respective undervoltage thresholds. This reset extension time is externally configurable with a resistor between RESEXT pin and ground. When shorting this RESEXT pin to ground, the minimum reset extension time is typically 1.4 ms. For a 22-kΩ external resistor, the typical reset extension time is 4.5 ms. For an open-connect on the RSTEXT pin, the TPS65381-Q1 remains in the RESET state, keeping the NRST pin low all the time.

POWER-UP / POWERDOWN Behavior

The power-up / power-down behavior is illustrated in Figure 5.

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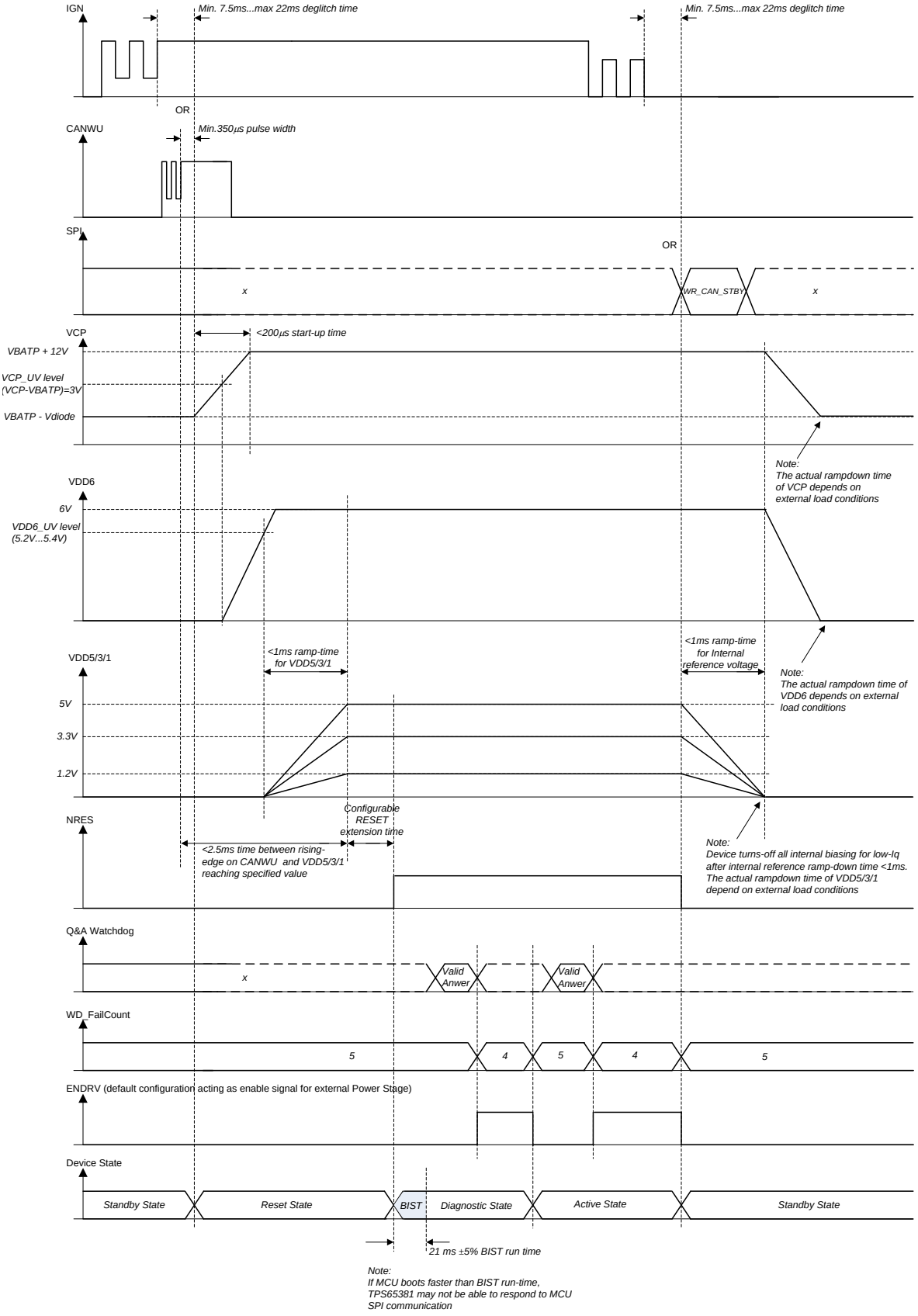


Figure 5. Power-Up / Power-Down Behavior

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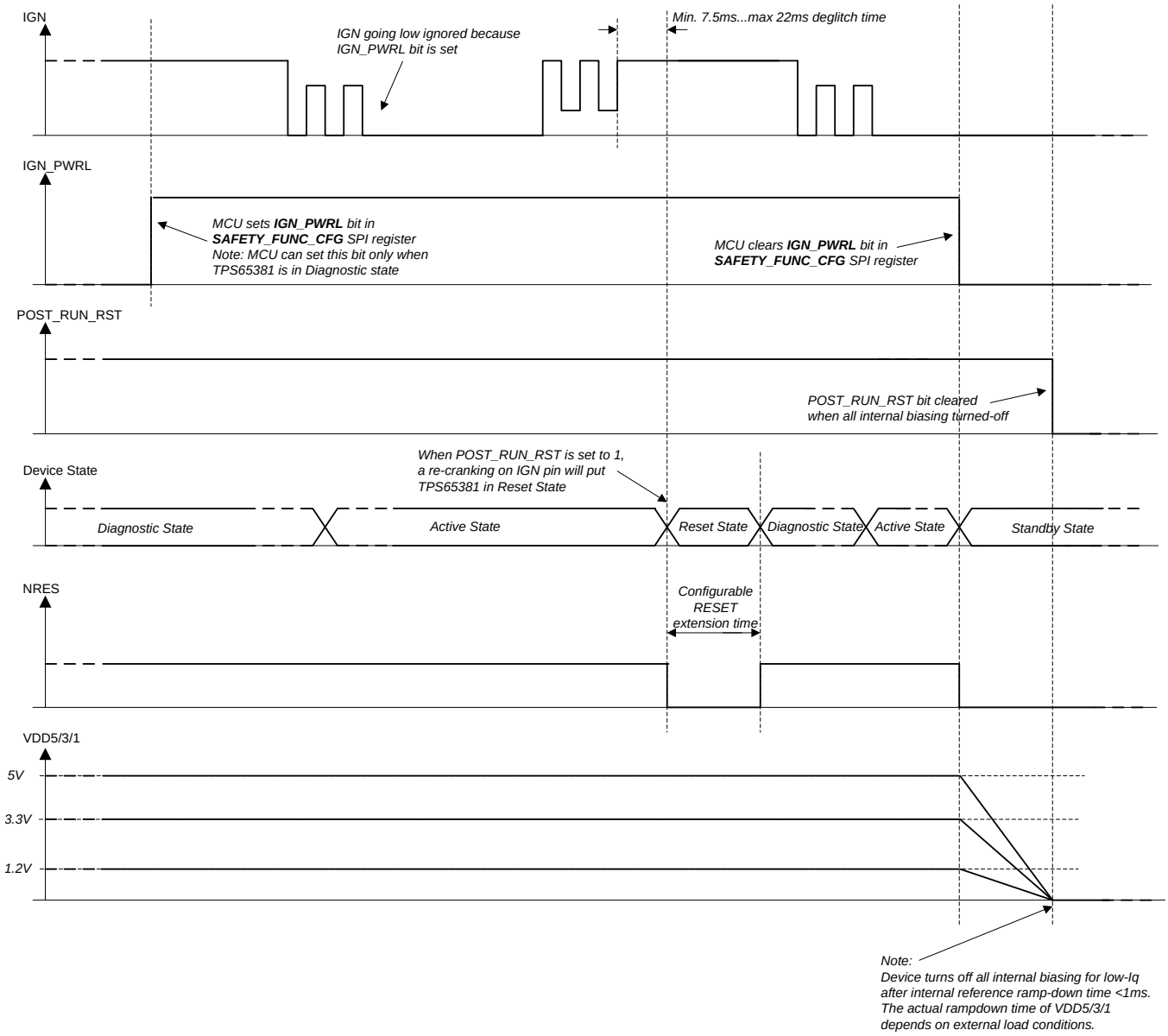


Figure 6. IGN Power Latch and POST-RUN Reset

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Safety Functions and Diagnostics Overview

The IC is intended to be used in safety-critical automotive applications. The following diagnostic blocks are implemented in order to achieve a better diagnostic coverage or a lower rate of dangerous undetected faults.

- Voltage monitor (VMON)
- Analog built-in self-test (ABIST) diagnostics for safety-critical analog blocks
- Loss of clock monitor (LCMON)
- Junction temperature monitoring for all power supplies with internal FET
- Current limit for all power supplies
- Analog MUX (AMUX) for externally monitored diagnostics/debug
- Digital MUX (DMUX) for externally monitored diagnostics/debug
- Logic built-in self-test (LBIST) for safety-critical controller functions
- Configurable open/close window or question-answer watchdog timer (WDT)

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- MCU error signal monitor (ESM)
- Controlled and protected enable output (ENDRV) for external power stages or peripheral wake-up, also configurable as MCU warm reset driver
- Device configuration register CRC protection
- SPI command decoder with parity check
- SPI data output feedback check
- Reset circuit for initializing external MCU
- EEPROM analog trim content CRC protection
- Device state controller with SAFE state in case of detected error event

Voltage Monitor (VMON)

The VBAT supply voltage, all regulator outputs and internally generated voltages are supervised by a voltage monitor module (VMON). An undervoltage or overvoltage condition is indicated by the corresponding VMON register status flag bits:

- VMON flag bit set to 1 when power supply is within specification
- VMON flag bit set to 0 when power supply is outside tolerance band

The monitoring is done by undervoltage and overvoltage comparators. The reference voltage (BANDGAP_REF2) for the VMON module is independent of the system reference voltage (BANDGAP_REF1) used by the regulators. A glitch-filtering function ensures reliable monitoring without false setting of the VMON status flag bits. The complete VMON block is supplied by a separate supply pin, VBAT_SAFING.

VMON comparator diagnostics are covered by analog built-in self-test (ABIST) executed during device start-up/power up or activated by the external MCU SPI request when the device is in the DIAGNOSTIC or ACTIVE state. Each monitored voltage rail is emulated for undervoltage and overvoltage conditions on the corresponding comparator inputs, hence forcing the corresponding comparator to toggle multiple times (in a toggling pattern observed and checked by the ABIST controller). The monitored voltage rails themselves are not affected during this self-test, so no real under- or overvoltage occurs on any of these rails due to this self-test.

Loss-of-Clock Monitor (LCMON)

Clock monitor detects internal oscillator failures:

- Oscillator clock stuck high or stuck low
- Reduced clock frequency

It is enabled during a power-up event after power-on reset is released (driven high). It remains active during device normal operation (STANDBY, RESET, DIAGNOSTIC, ACTIVE, and SAFE states). In case of a clock failure:

- The device transitions to the STANDBY state.
- All regulators are disabled.
- The digital core is reinitialized.
- Reset to the external MCU is asserted low.
- The failure condition is latched outside the digital core.
  - NOTE: Only loss of power can clear this latch.
- Once this latch is cleared, a new start-up event following a clock failure event will again set this latch.

The loss-of-clock monitor has its own self-test structure that is activated and monitored by analog BIST (ABIST). The external MCU can re-check the clock monitor any time when the device is in the DIAGNOSTIC or ACTIVE state. The enabled diagnostics emulate a clock failure that causes the clock-monitor output to toggle. The clock-monitor toggling pattern is checked by ABIST, while the external MCU can check that the loss-of-clock status bit is being set during active test. During this self-test, the actual oscillator frequency (4 MHz) is not changed due to this self-test.

Analog Built-In-Self-Test (ABIST)

ABIST is the controller and monitor circuit for performing self-checking diagnostics on critical analog functions:

- VMON under- and overvoltage comparators

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- Clock monitor (LCMON)
- EEPROM analog trim content check (CRC protection)

During the self-test on the VMON under- and over voltage comparators, the monitored voltage rails themselves are left unchanged, so no real under- or overvoltage occurs on any of these rails due to these self-tests. Furthermore, also during the self-check on the clock monitor, the actual oscillator frequency (4 MHz) is not changed due to this self-test.

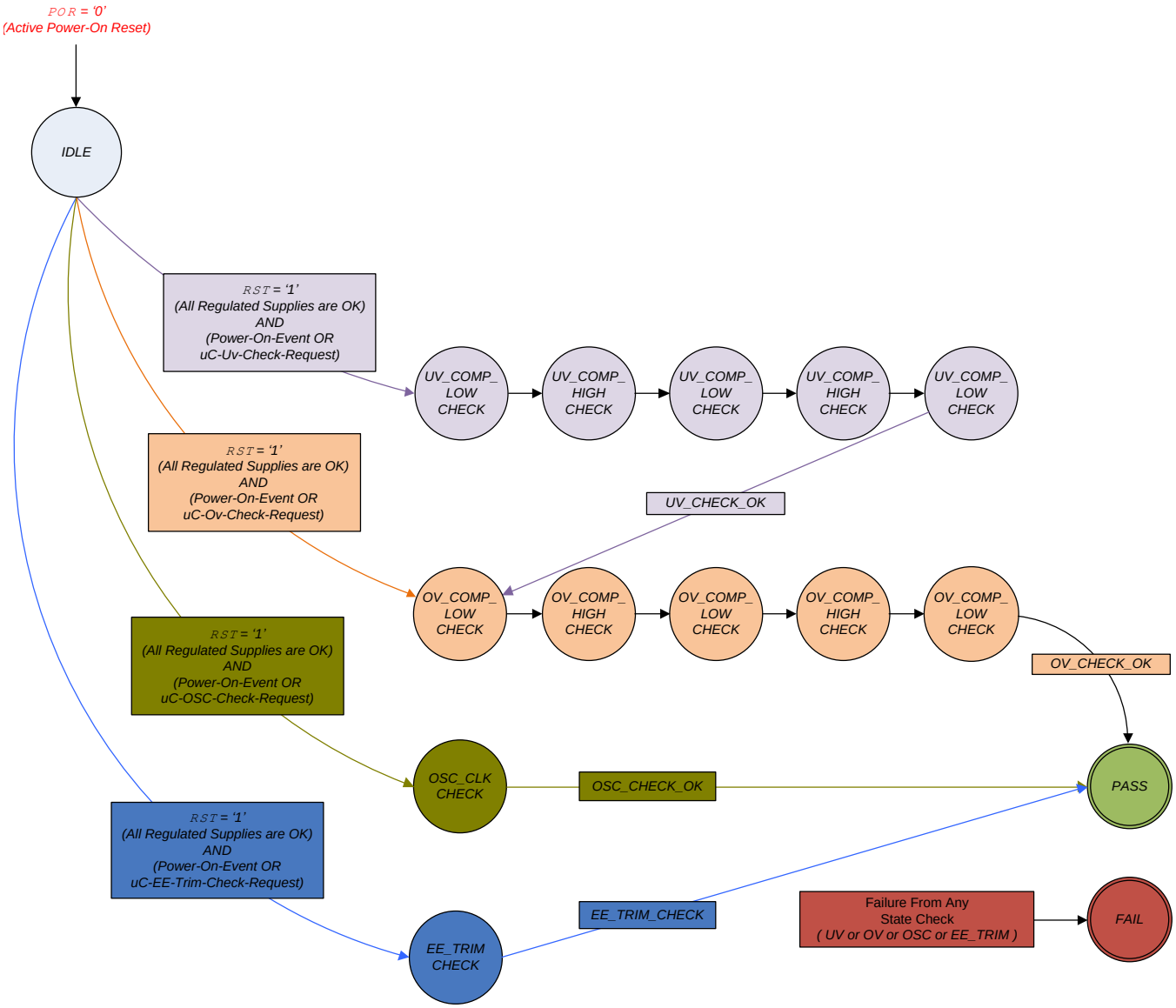


Figure 7. Analog BIST Run States

In case of ABIST failure, the device enters the SAFE state, reset to the external MCU (NRST_EXT on the NRES pin) is asserted low, while all ABIST status flag bits remain latched in the digital core. On a new start-up event (IGN or CANWU event), the TPS65381-Q1 transitions via the RESET state to the DIAGNOSTIC state. In the DIAGNOSTIC state, the external MCU can detect the reason for a previous reboot, and the ABIST failure root cause, by reading the ABIST status register.

In the DIAGNOSTIC state, the external MCU can activate any ABIST check. During active ABIST run, the device cannot monitor the state of regulated supplies. Full ABIST run time is approximately 2 ms. The ABIST can also be performed in the ACTIVE state on MCU request, depending on system safety requirements (that is, system fault-response time requirement).

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Junction Temperature Monitoring and Current Limiting

Each LDO with an internal power FET has junction temperature monitoring with thermal shutdown protection. In case of thermal shutdown, a regulated supply can be enabled only after the thermal shutdown condition is removed. For VDD5 and VSOUT1 supplies, the thermal shutdown event clears an enable bit, and the external MCU must set the enable control bit again in order to re-enable the regulator.

For the configurable VDD3/5 regulator, a thermal shutdown event puts the device in the STANDBY state with all regulators turned off, and reset to the external MCU (NRES) asserted low. The VDD6 buck pre-regulator shares its thermal protection with the VDD3/5 thermal shutdown.

For the VDD5 regulator, thermal shutdown places device into the RESET state with reset to the external MCU (NRES) asserted low, while all other regulators remain enabled.

The VDD3/5, VDD5, and VSOUT regulators include a current-limit circuit for additional protection against excessive power consumption and thermal overstress. Respective status bits are set in the SAFETY_STAT_1 register when a current limit is detected on any of these rails.

Diagnostic Output Pin DIAG_OUT

Analog and digital critical signals, which are not directly connected to the MCU, are switched by a multiplexer to the external DIAG_OUT pin. The programming of the multiplexer is done via SPI register DIAG_MUX_SEL. The digital signals are buffered in order to have sufficient drive capabilities.

This multiplexer facilitates external pin interconnect tests by feeding back the input pin state or feeding back internal module self-test status or safety-critical comparator outputs.

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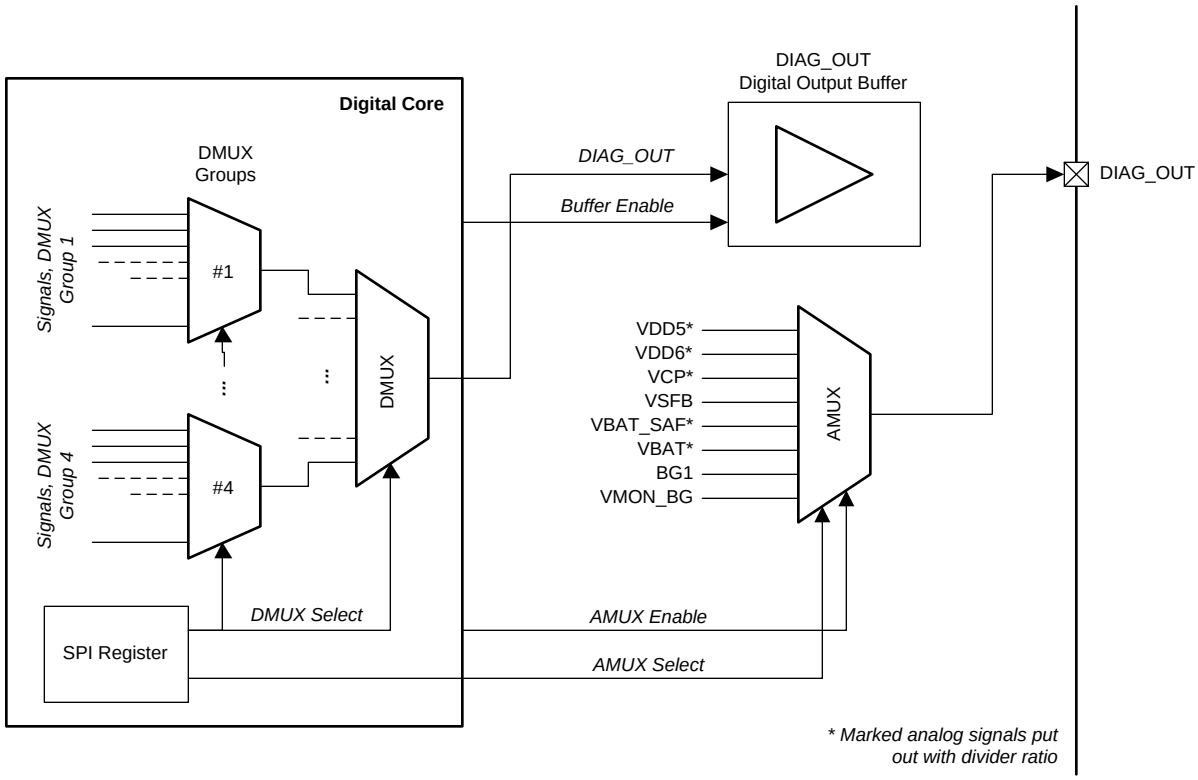


Figure 8. Diagnostic Output Pin DIAG_OUT

In case the DIAG_OUT pin is connected to a mixed analog/digital input pin of the MCU, it is recommended to configure this MCU input pin and the DIAG_OUT pin simultaneously in accordance with the desired kind of signal (analog or digital). The kind of signal (analog or digital) on the DIAG_OUT1 pin can be configured with the MUX_CFG bits in the DIAG_CFG_CTRL register. The DIAG_OUT multiplexer can be globally enabled/disabled with bit 7 in the DIAG_CFG_CTRL register

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Analog MUX (AMUX)

Table 1 describes the selectable analog internal signals on the DIAG_OUT pin. In the DIAG_CFG_CTRL register, the MUX_CFG bits must be set to 10 for the analog MUX mode.

Table 1. Analog MUX Selection Table

SIGNAL NUMBER	VOLTAGE RAIL/ SIGNAL NAME	DESCRIPTION	DIVIDE RATIO	VOLTAGE RANGE	DIAG_MUX_SEL[3:0]
A.1	VDD5	Linear VDD5 regulator output	2	2.5 V ±2%	0000
A.2	VDD6	Switch-mode pre-regulator	3	2 V ±5%	0001
A.3	VCP	External charge pump	13.5	0.8 V to 5.5 V	0010
A.4	VSFB1	Sensor supply feedback voltage	1	1.226 V to 5 V ±2%	0011
A.5	VBAT_SAFING	Safing battery supply	10	0.4 V to 4 V	0100
A.6	VBAT	Battery supply	10	0.4 V to 4 V	0101
A.7	BG1	Regulators band-gap reference	1	1.226 V ±2%	0110
A.8	VMON_BG	Voltage-monitor band gap	1	1.226 V ±2%	0111

In case one of these analog signals comes to a voltage above VDDIO, a clamp becomes active to avoid any voltage level higher than VDDIO on the DIAG_OUT pin.

Digital MUX (DMUX)

The following tables describe the selectable digital internal signals on the DIAG_OUT pin. In the DIAG_CFG_CTRL register, the MUX_CFG bits must be set to 01 for the digital MUX mode.

Table 2. Digital MUX Selection Table – Group 1

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D1.1	RSV	Reserved, logic 0	000	0000
D1.2	AVDD_UVN	AVDD undervoltage comparator output	000	0001
D1.3	BG_ERR1	VMON or main band gap is OFF	000	0010
D1.4	BG_ERR2	VMON or main band gap is OFF	000	0011
D1.5	VCP12_NUV	VCP12 charge-pump undervoltage comparator	000	0100
D1.6	VCP12_OV	VCP12 charge-pump overvoltage comparator	000	0101
D1.7	VCP17_OV	VCP17 charge-pump overvoltage comparator	000	0110
D1.8	VDD6_NUV	VDD6 undervoltage comparator	000	0111
D1.9	VDD6_OV	VDD6 overvoltage comparator	000	1000
D1.10	VDD5_NUV	VDD5 undervoltage comparator	000	1001
D1.11	VDD5_OV	VDD5 overvoltage comparator	000	1010
D1.12	VDD3/5_NUV	VDD3/5 undervoltage comparator	000	1011
D1.13	VDD3/5_OV	VDD3/5 overvoltage comparator	000	1100
D1.14	VDD1_NUV	VDD1 undervoltage comparator	000	1101
D1.15	VDD1_OV	VDD1 overvoltage comparator	000	1110
D1.16	LOCLK	Loss-of-system-clock comparator	000	1111

Table 3. Digital MUX Selection Table – Group 2

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D2.1	RSV	Reserved, logic 0	001	0000

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Table 3. Digital MUX Selection Table – Group 2 (continued)

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D2.2	SYS_CLK	System clock source	001	0001
D2.3	DFT	Signal reserved for production test	001	0010
D2.4	WDT_CLK	Watchdog clock reference (0.55-ms period time)	001	0011
D2.5	RST_EXT_CLK	Reset extension oscillator output	001	0100
D2.6	T_5US	5-µs time reference	001	0101
D2.7	T_15US	15-µs time reference	001	0110
D2.8	T_40US	40-µs time reference	001	0111
D2.9	T_2MS	2-ms time reference	001	1000
D2.10	UC_ERROR/WDI	External MCU ERROR/WDI input pin	001	1001
D2.11	SPI_NCS	SPI chip-select input pin	001	1010
D2.12	SPI_SDI	SPI slave-data input pin	001	1011
D2.13	SPI_CLK	SPI clock input pin	001	1100
D2.14	SDO_RDBCK	SPI slave-data output-pin readback	001	1101
D2.15	UC_ERROR/WDI	Same signal as 2.10	001	1110
D2.16	NRST_EXT_IN	NRES pin readback (reset to external MCU)	001	1111

Table 4. Digital MUX Selection Table – Group 3

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D3.1	RSV	Reserved, logic 0	010	0000
D3.2	DFT	Signal reserved for production test	010	0001
D3.3	DFT	Signal reserved for production test	010	0010
D3.4	CP_OV	Charge-pump overvoltage comparator	010	0011
D3.5	CP_UVN	Charge-pump undervoltage comparator	010	0100
D3.6	CP_PH1	Charge-pump switching phase 1	010	0101
D3.7	CP_PH2	Charge-pump switching phase 2	010	0110
D3.8	CP_DIFF3V	Indicates VCP-VBATP > 3 V	010	0111
D3.9	DFT	Signal reserved for production test	010	1000
D3.10	VBAT_UVN	VBAT undervoltage comparator	010	1001
D3.11	VBATP_OV	VBAT overvoltage comparator	010	1010
D3.12	VDD5_OT	VDD5 overtemperature	010	1011
D3.13	VDD3_5_OT	VDD3/5 overtemperature	010	1100
D3.14	VSOUT_OT	VSOUT overtemperature	010	1101
D3.15	VDD5_CL	VDD5 current limit	010	1110
D3.16	VDD3_CL	VDD3 current limit	010	1111

Table 5. Digital MUX Selection Table – Group 4

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D4.1	RSV	Reserved, logic 0	011	0000
D4.2	VSOUT_ILIM	VSOUT1 current limit	011	0001
D4.3	VSOUT_UVN	VSOUT1 undervoltage comparator	011	0010

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Table 5. Digital MUX Selection Table – Group 4 (continued)

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D4.4	VSOUT_OV	VSOUT1 overvoltage comparator	011	0011
D4.5	DVDD_UV	DVDD undervoltage comparator	011	0100
D4.6	DVDD_OV	DVDD overvoltage comparator	011	0101
D4.7	RSV	Reserved	011	0110
D4.8	VS_TRK_MODE	VSOUT1 in track-mode indication	011	0111
D4.9	VMON_TRIM_ERR	VMON trim error	011	1000
D4.10–16	RSV	Reserved	011	1001–1111

Table 6. Digital MUX Selection Table – Group 5

SIGNAL NUMBER	SIGNAL NAME	DESCRIPTION	CHANNEL GROUP DIAG_MUX_SEL [6:4]	CHANNEL NUMBER DIAG_MUX_SEL [3:0]
D5.1	RSV	Reserved, logic 0	111	0000
D5.2	TI_TEST_MODE	TI production test mode indication	111	0001
D5.3 – 16	DFT	Signal reserved for production test	111	0010–1111

Logic Built-In Self-Test (LBIST)

The logic BIST (LBIST) is used to test the digital-core safety-critical functions.

- Includes an application-controllable logic BIST engine which applies test vectors to the digital core
- LBIST engine provides at least 95% stuck-at fault grade to logic blocks under test.
- LBIST run time is typically 4.2 ms (±5%). After the LBIST, there is a typical 16-ms wait period to fill the digital filters covered by the LBIST. During this time, the ABIST is performed. So total BIST time is appriximately 21 ms.
- LBIST engine has a time-out counter as a fail-safe feature.

LBIST is activated with every device power-up event or by the external MCU when the device is in the DIAGNOSTIC state (by writing to the SAFETY_BIST_CTL register; note that this register is SW WRITE PROTECT). It can also be run in the ACTIVE state (together with ABIST), depending on whether system-safety timing requirements can allow the total 21-ms BIST time. During an active LBIST run, the device cannot monitor the state of regulated supplies, and cannot monitor state of the MCU through the watchdog timer.

Watchdog Timer (WDT)

For monitoring proper function of the external MCU, the TPS65381-Q1 includes a closed-loop digital watchdog. This watchdog requires specific trigger messages to be passed between the MCU and the TPS65381-Q1 at specific timing intervals in order to enable operation of the safing path / external power stages through the ENDRV pin. This function is consequently referred to as the watchdog-enabled function. When improper MCU operation is detected, the ENDRV pin is pulled low to disable the safing path / external power stages.

Normal MCU operation is indicated when the MCU periodically sends a watchdog trigger which is received by the watchdog timer within a defined time window. The TPS65381-Q1 has two different watchdog timer configurations for the external MCU to send the watchdog trigger:

- Watchdog trigger input configuration (WDTI Configuration): The MCU sends watchdog triggers by asserting the ERROR/WDI input pin.
- Question-answer configuration (Q&A configuration): The MCU sends watchdog triggers through SPI.

The WDT configuration is controlled by the WD_CFG bit in the safety-function configuration register (SAFETY_FUNC_CFG, bit 5). Default configuration is the WDTI configuration.

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WDT Fail Counter, WDT Status, and WDT Fail Event

The watchdog function includes a watchdog fail counter which increments and decrements due to *good* and *bad* events, respectively. When the value of the watchdog fail counter is 5 or more, the watchdog status is out-of-range, and the watchdog-enabled function is disabled. (ENDRV pin low).

When the watchdog fail counter is 4 or less, the watchdog status is in-range, and the closed-loop watchdog no longer disables the watchdog-enabled function (ENDRV pin high). Note that this function can still be disabled by its individual control methods (through ENABLE_DRV control bit in the SAFETY_CHECK_CTRL register).

The watchdog fail counter operates independently of the state of the WD_EN bit (in the SAFETY_FUNC_CFG register). The internal WD_EN bit and watchdog status signals are ANDed together in order to disable the watchdog-enabled function when the watchdog fail counter is above the count of 4 and the ENABLE_DRV control bit (in the SAFETY_CHECK_CTRL register) is set.

The watchdog fail counter responds as follows:

- A *good event* decrements the fail counter by 1.
- A *bad event* increments the fail counter by 1.
- A *time-out event* increments the fail counter by 1 and sets the TIME_OUT flag (register WDT_STATUS, bit 1)

The definitions of *good event*, *bad event* and *time-out event* are given in the sections describing the WDTI configuration and Q&A configuration.

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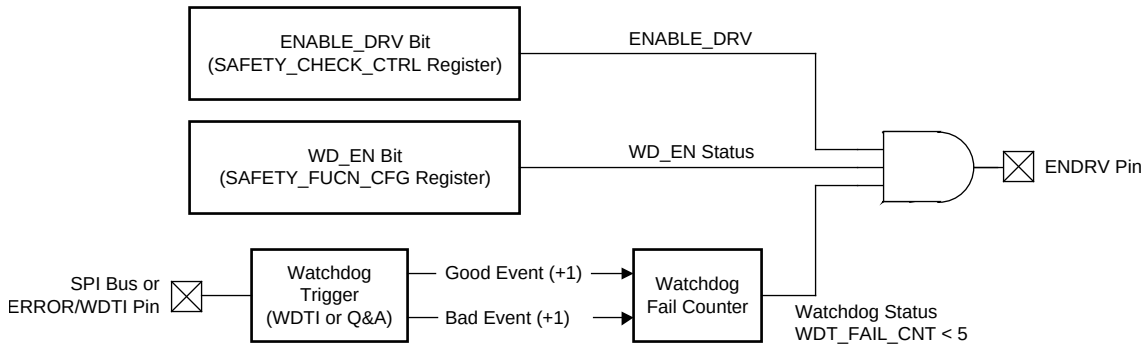


Figure 9. Watchdog Enable Function

Table 7. Watchdog Status for Fail Counter Value Range

Watchdog Fail Counter *WDT_FAIL_CNT[2:0]*	**0b000–0b100**	**0b101–0b111**	**0b111**
Watchdog status	Closed-loopis watchdog in-range.	Closed loop watchdog is out-of-range.	NRES pulled low

When the watchdog fail counter reaches a count of 7, depending on device configuration, an external reset to the MCU is asserted by pulling the NRES pin low.

WDTI Configuration with External Trigger Input (Default Mode)

After a power-on event, the reset output at the NRES pin is kept low for the reset extension time (externally configurable with a resistor between the RESEXT pin and ground, minimum time is 1.44 ms). After a low-to-high transition on the NRES output pin (re-boot of MCU), the watchdog function starts with the default CLOSE window duration t_{WCW}. A received WD trigger interrupt (WDTI) within this CLOSE window interval is interpreted as a *bad event*.

The OPEN window with duration t_{WOW} is started after the CLOSE window. The OPEN window lasts at minimum until a WD interrupt is received, at maximum the programmed t_{WOW} time. A received WD trigger interrupt (WDTI) within this OPEN window interval is interpreted as a *good event*.

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When the MCU suspends sending trigger events to the ERROR/WDI pin during the CLOSE/OPEN window, the watchdog consider this as a *no-response event*. This sets the TIME_OUT flag (register WDT_STATUS, bit 1), which is useful for the MCU software in order to synchronize the watchdog trigger events on the required watchdog timing. In order to do so, MCU should not send any trigger event on the ERROR/WDI pin directly after reboot or after reconfiguring watchdog timer, until this TIME_OUT flag is set.

t_{WOW} and t_{WCW} can be programmed through the SPI registers. For the WDTI configuration, this can be done as follows:

t_{WOW} (WDTI) = (RW[4:0] + 1) × 0.55 ms. Bits RW[4:0] are located in SPI register WDT_WIN2_CFG.
t_{WCW} (WDTI) = (RT[4:0] + 1) × 0.55 ms. Bits RT[4:0] are located in SPI register WDT_WIN1_CFG

The watchdog function uses an internal 4-MHz (with ±5% accuracy) system clock as a time reference for creating the 0.55-ms time step. Any CLOSE window duration (t_{WCW}) update takes effect during the next active watchdog OPEN window. Any OPEN window duration (t_{WOW}) update takes effect during the next watchdog CLOSE window.

A WD trigger interrupt (WDTI) rising edge on the ERROR/WDI input pin, followed by a WD trigger interrupt (WDTI) falling edge on the ERROR/WDI input pin, is considered to be a watchdog trigger event. The watchdog trigger event is considered valid (that is, a *good event*) if received during a watchdog OPEN window (WOW).

The valid watchdog trigger event or power-up/power-down event resets the watchdog window sequence. This is always followed by starting a watchdog CLOSE window (WCW).

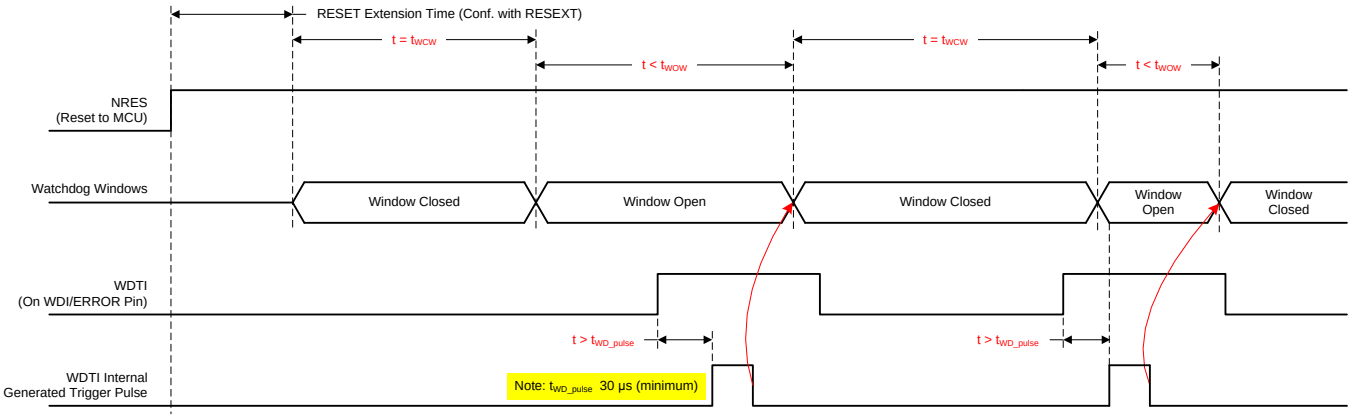


Figure 10. Possible Cases for *Good* Watchdog Events in WDTI Configuration

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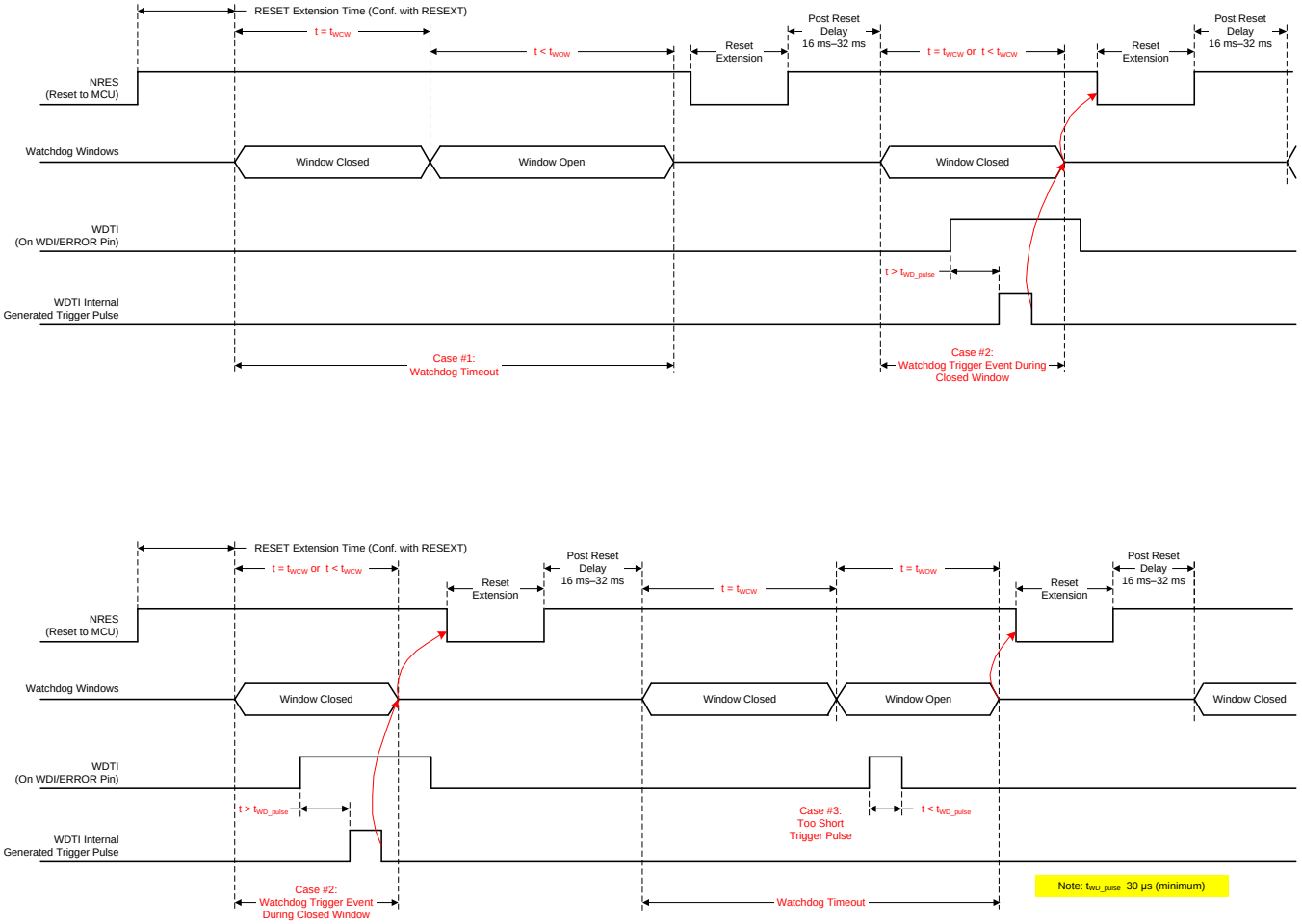


Figure 11. Possible Cases for *Bad* Watchdog Events in WDTI Configuration

WD Question / Answer Configuration Through SPI

The TPS65381-Q1 watchdog can be configured in question/answer (Q&A) mode by setting bit WD_CFG in SAFETY_FUNC_REG to 1. In question/answer configuration, upon an MCU request, the TPS65381-Q1 provides a *token* (or *question*) to the MCU over SPI (latched in WDT_TOKEN register). The MCU performs a fixed series of arithmetic operations on the token value and returns the resulting token value *answers* to the ASIC over SPI (by writing to the WDT_ANSWER register). The TPS65381-Q1 verifies that the MCU returns the token value results (answers) within the specified timing windows, and that the token value responses (answers) are correct.

When the MCU performs the watchdog-related SPI communications within the correct timing windows, and returns the correctly calculated token (question) responses (answers), the watchdog considers these *good events*.

When the MCU performs the watchdog-related SPI communications outside of the correct timing windows, or returns an incorrectly calculated token (question) responses (answers), or returns the correct answers in the wrong sequence, the watchdog considers these *bad events*.

When the MCU suspends watchdog-related SPI communications for the duration of the watchdog time-out window, the watchdog considers this as a *no-response event*. This sets the TIME_OUT flag (register WDT_STATUS, bit 1), which is useful for the MCU software in order to synchronize the watchdog trigger events on the required watchdog timing. In order to do so, MCU should not send any trigger event on ERROR/WDI pin directly after reboot or after reconfiguring the watchdog timer or after configuring watchdog from WDTI to Q&A, until this TIME_OUT flag is set.

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WDT-Related SPI Event Definitions

- **WD Token Request (*Question*)**
  - This event occurs when MCU requests a read of the *Watchdog Token Value SPI* register.
  - If the SPI frame is not successfully transmitted (that is, there is a SPI fault detected), the WD token request event does not occur.
  - The MCU can request each new generated token at the start of the OPEN Window, but this is not a required condition for getting a *good event*. The MCU can also generate the TOKEN by itself by mimicking the TOKEN generation circuit as given in Figure 13. Nevertheless, the valid responses (*answers*) are always based on the TOKEN generated inside the TPS65381-Q1. So if the MCU generates a wrong TOKEN and gives responses (*answers*) based on its own (wrong) TOKEN, a *bad event* is detected in the TPS65381-Q1.
- **WDT Token Response (*Answer*)**
  - This event occurs when the MCU writes to the watchdog answer register.
  - Each WD token request requires four WD token responses (three responses during an OPEN window and one response during a CLOSED window).

WDT Token Value Generation (or WDT Question Generation)

The TPS65381-Q1 generates a new 4-bit token value only after valid and complete WD token responses.

- Three correct SPI WD token responses received during a WD open window, followed by
- One correct SPI WD token response received during a WD close window
- In addition to the above timing, the sequence of four responses must be correct.

The *Watchdog Token Value* is latched in the *Watchdog Token Value* SPI register and can be read at any time.

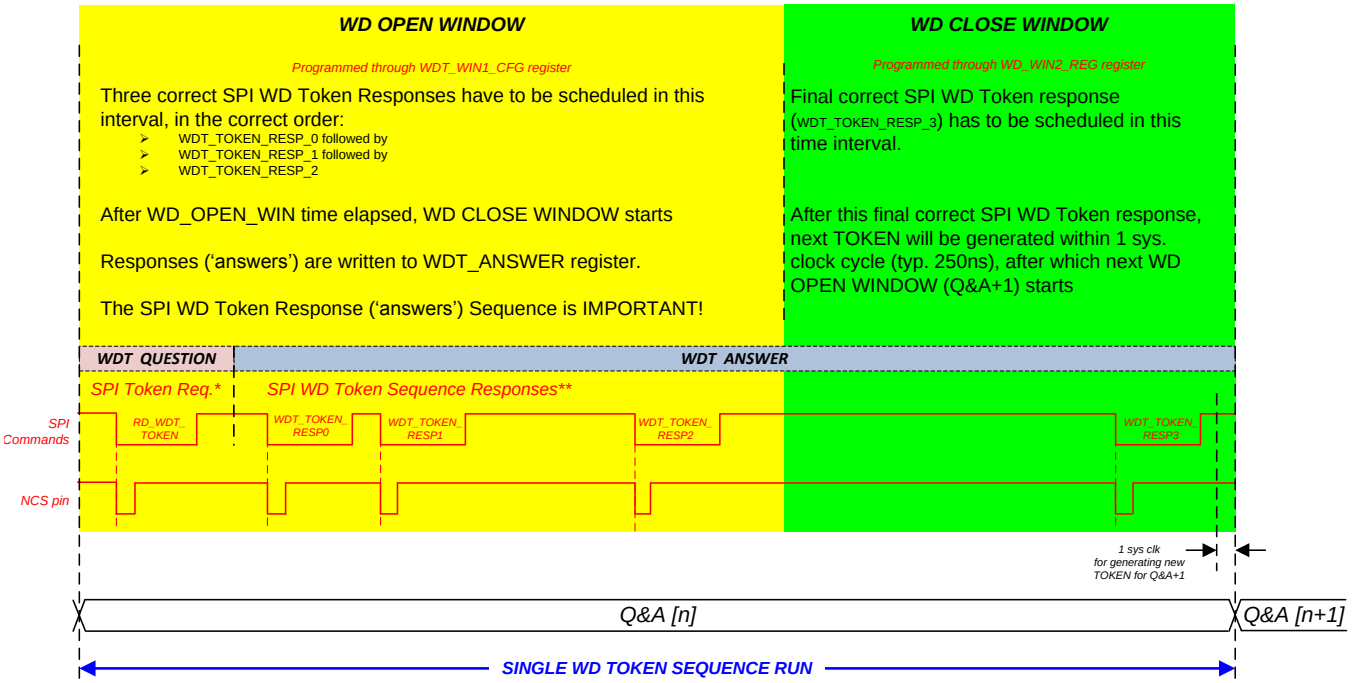
Watchdog Timer Configuration for Question/Answer Configuration

Similarly as for WDTI configuration, the WD question/answer configuration, the t_{WOW} and t_{WCW}, can be programmed through SPI registers. For the WD question/answer configuration, this can be done as follows:

t_{WOW} (QA) = (RW[4:0] + 1) x 0.55 ms. Bits RW[4:0] are located in SPI register WDT_WIN1_CFG.
t_{WCW} (Q&A) = (RT[4:0] + 1) x 0.55 ms. Bits RT[4:0] are located in SPI register WDT_WIN2_CFG.

The watchdog function uses the internal 4-MHz (with ±5% accuracy) system clock as a time reference for creating the 0.55-ms time step. Any open-window duration (t_{WOW}) update and/or close-window duration (t_{WCW}) update takes effect during the next active watchdog open window and/or watchdog close window.

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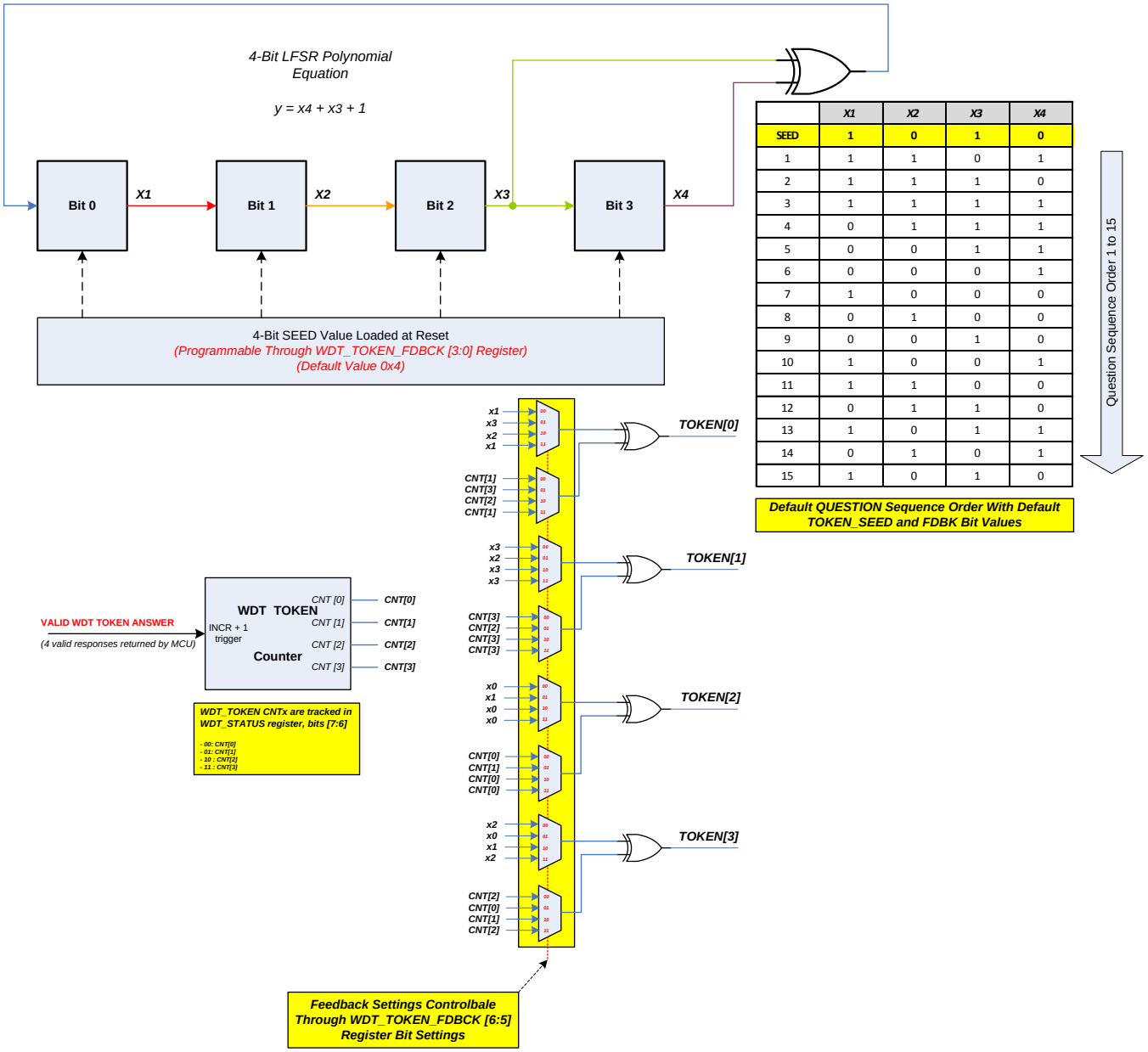
** It is not mandatory for MCU to request the TOKEN: MCU can start given the correct answers WDT_TOKEN_RESP0..2 anywhere within the OPEN WINDOW. The new TOKEN will always be generated within 1 sys. Clock cycle after the final WDT_TOKEN_RESP3*

*** MCU can put any other SPI Commands in-between the WDT_TOKEN_RESPx answers (even re-requesting the TOKEN) without any influence on the Watchdog function, as long as the WDT_TOKEN_RESP0..2 are given within the OPEN Window and WDT_TOKEN_RESP3 is given within the CLOSE Window*

Figure 12. WDT Token / Response Sequence Run

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	X1	X2	X3	X4
SEED	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

Figure 13. TOKEN Generation

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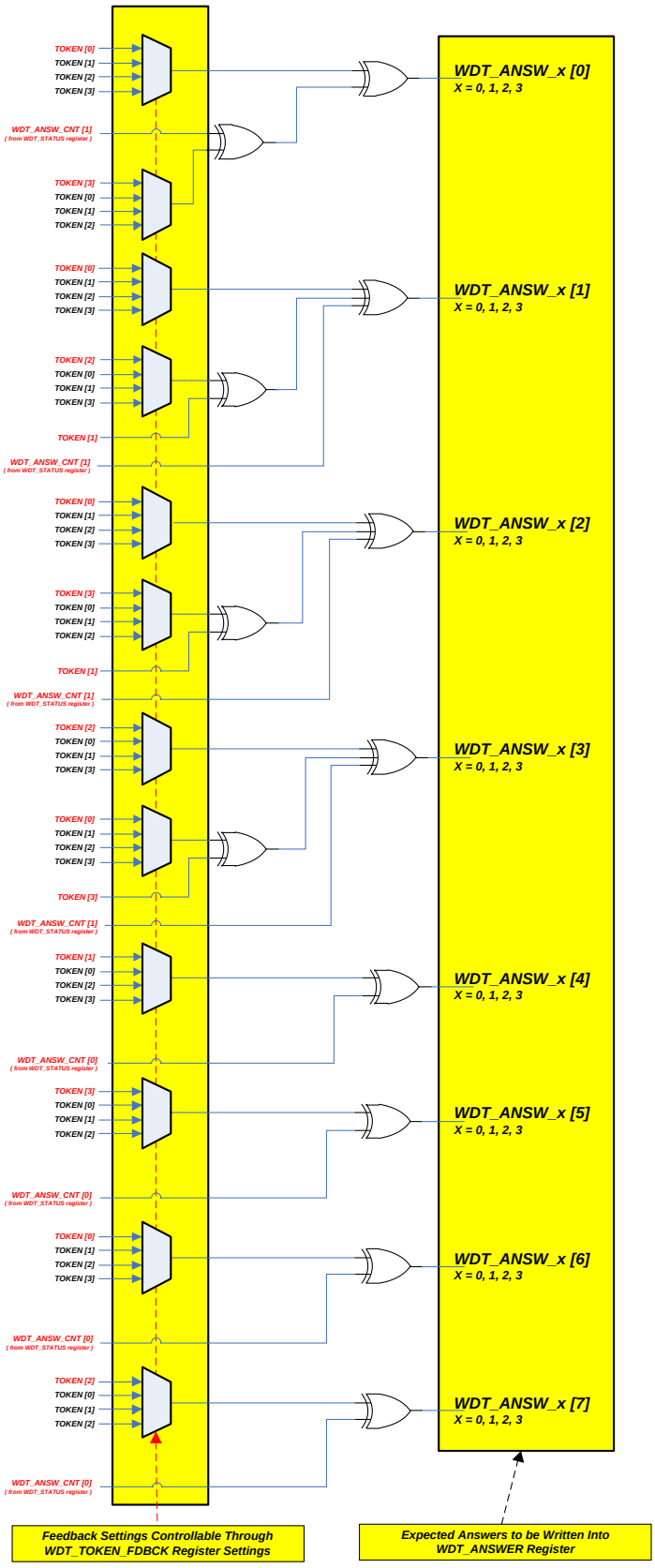


Figure 14. Watchdog Token Value Response Calculation (or Watchdog Answer Calculation)

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Table 8. Set of 4-Bit WD Token Values and Corresponding 8-Bit Responses

4-Bit WDT TOKEN	WDT Answer (to be written into WDT_ANSW register)			
	8-Bit WDT TOKEN RESPONSE 0	8-Bit WDT TOKEN RESPONSE 1	8-Bit WDT TOKEN RESPONSE 2	8-Bit WDT TOKEN RESPONSE 3
WDT_TOKEN Register	*WDT_ANSW_CNT [1:0] = 00*	*WDT_ANSW_CNT [1:0] = 01*	*WDT_ANSW_CNT [1:0] = 10*	*WDT_ANSW_CNT [1:0] = 11*
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3
0x8	D2	22	DD	2D
0x9	9D	6D	92	62
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

MCU Error Signal Monitor (MCU ESM)

This block monitors the external MCU error conditions signaled over ERROR/WDI input pin. It is configurable to monitor two different signaling options:

- Detecting a low pulse signal with programmable low pulse-duration threshold (TMS570 mode)
- Detecting the PWM signal with programmable frequency and duty cycle (PWM mode) (1).

The operating mode is controlled through the ERROR_CFG bit in the SAFETY_FUNC_CFG register. Low signaling duration threshold (for TMS570 mode) or expected PWM low pulse duration (for PWM mode) is set through the SAFETY_ERR_PWM_L register, and expected PWM high pulse duration (for PWM mode) is set through the SAFETY_ERR_PWM_H register.

The module is covered by logic BIST and is activated at a device power-up event or by the external MCU when the device is in the DIAGNOSTIC or ACTIVE or SAFE state.

TMS570 Mode

An error condition is detected when the ERROR/WDI pin remains low for a programmed amount of time set by the SAFETY_ERR_PWM_L register. The programmable time range is 5 µs to 1.28 ms, with 5-µs steps.

The SAFETY_ERR_PWM_L register must be set to the desired value based on the maximum required time for the TMS570 MCU to detect an error/fault and potentially recover from it (or correct it). Figure 15 gives the error-detection case scenarios.

The ERROR_PIN_FAIL bit in the SAFETY_ERR_STAT register is set when an error-pin signaling failure is detected.

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(1) PWM mode can be used as an external clock-monitor function.

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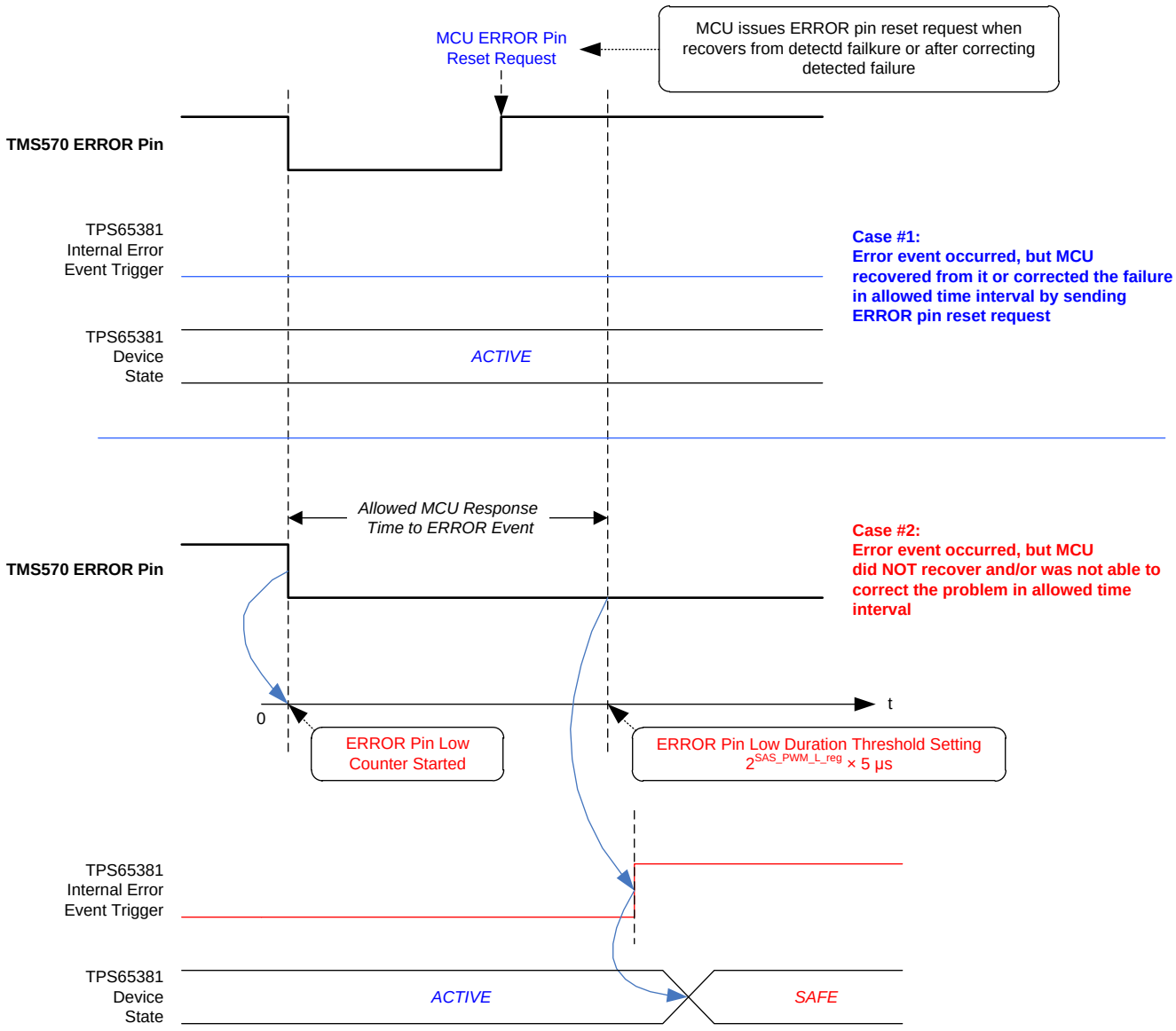


Figure 15. Error-Detection Case Scenarios for the TMS570 MCU

PWM Mode

An error condition is detected when the ERROR/WDI, the monitored input pin signal frequency, and/or the duty cycle is outside its programmed range. The expected signal high pulse duration is set by the SAFETY_ERR_PWM_H register and the expected signal low pulse duration is set by the SAFETY_ERR_PWM_L register.

The programmable time range for the expected HIGH and LOW pulse duration is 5 µs to 1.28 ms, with 5-µs resolution steps.

The ERROR_PIN_FAIL bit in the SAFETY_ERR_STAT register is set when an error-pin signaling failure is detected.

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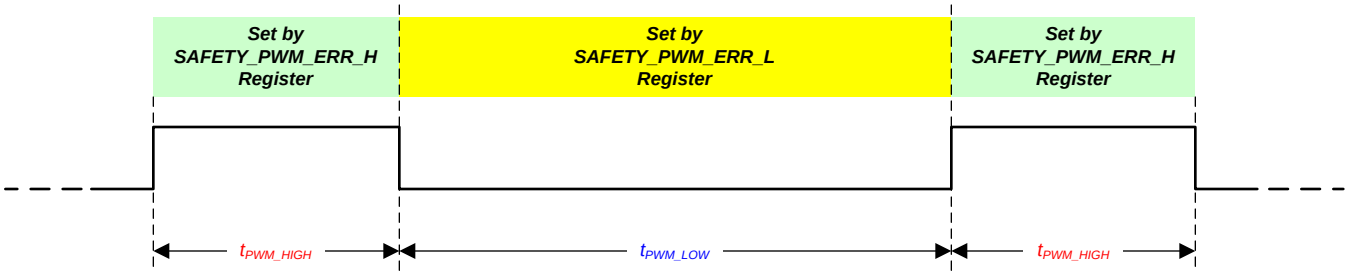


Figure 16. ERROR Pin Monitor – PWM Mode

Device Configuration Register Protection

This function offers a mechanism to protect safety-critical SPI-mapped registers by means of SPI write-access protection and CRC check.

The register access protection includes two distinctive features:

- A register cannot be written once write-access lock protection is set. The lock can be cleared by software or by a power-on reset.
- CRC protection for configuration registers

A CRC is done on safety-critical data after SPI write updates to verify the SPI register contents are correctly programmed. The CRC controller is a diagnostic module which is used to perform CRC to verify the integrity of the SPI mapped register space. A signature representing the content of the safety-critical registers is obtained when its content is read into the CRC controller. The responsibility of the CRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a predetermined good signature value. The predetermined CRC signature value is stored in the SAFETY_CFG_CRC register. The external MCU uses the SAFETY_CHECK_CTL register to enable a CRC check and the SAFETY_STAT_2 register to monitor its status.

A standard CRC-8 polynomial is used: X8 + X7 + X6 + X4 + X2 + 1

The CRC monitor test is covered by logic BIST.

Enable and Reset Driver Circuit

Figure 17 illustrates the Enable and Reset Circuit:

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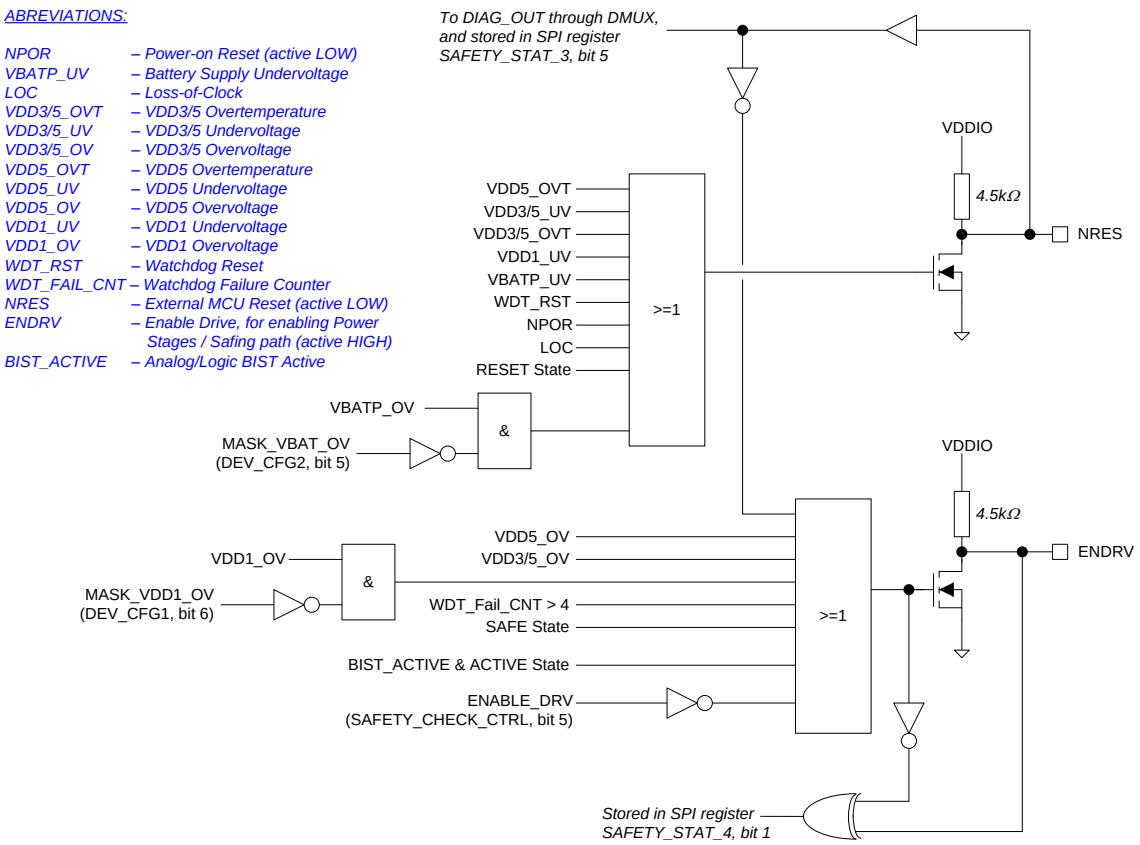


Figure 17. Reset and Enable Circuit

The ENDRV pin features a read-back circuit to compare the external ENDRV level with the internally applied ENDRV level. This is to detect any possible failure in the ENDRV pullup or pulldown components. A failure can be detected by the MCU through the SPI register SAFETY_STAT_4, bit 1.

The NRES pin features a readback of the external NRES level. The value can be read on the DIAG_OUT pin, and in the SPI register SAFETY_STAT_3, bit 5.

For both ENDRV and NRES, the logic readback threshold level is typically 400 mV.

The timing-response diagram for the NRES and ENDRV pins to any RESET condition is given in the next timing diagram.

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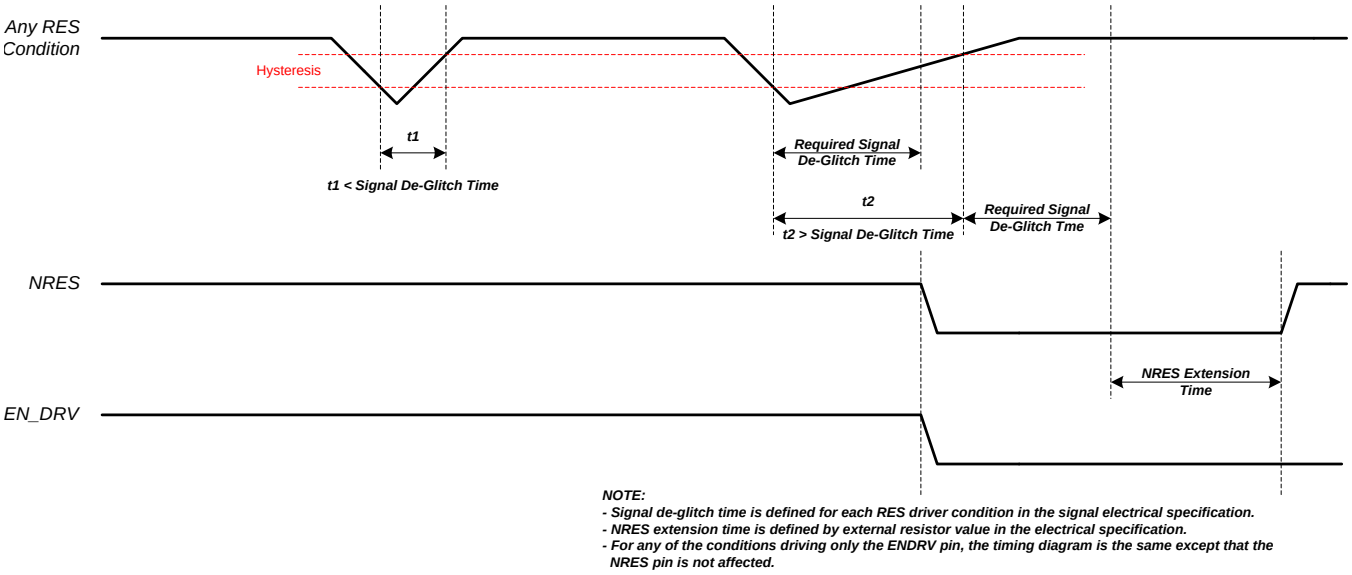


Figure 18. Timing-Response Diagram for NRES and ENDRV Pins to Any RESET Condition

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Device Controller State Diagram

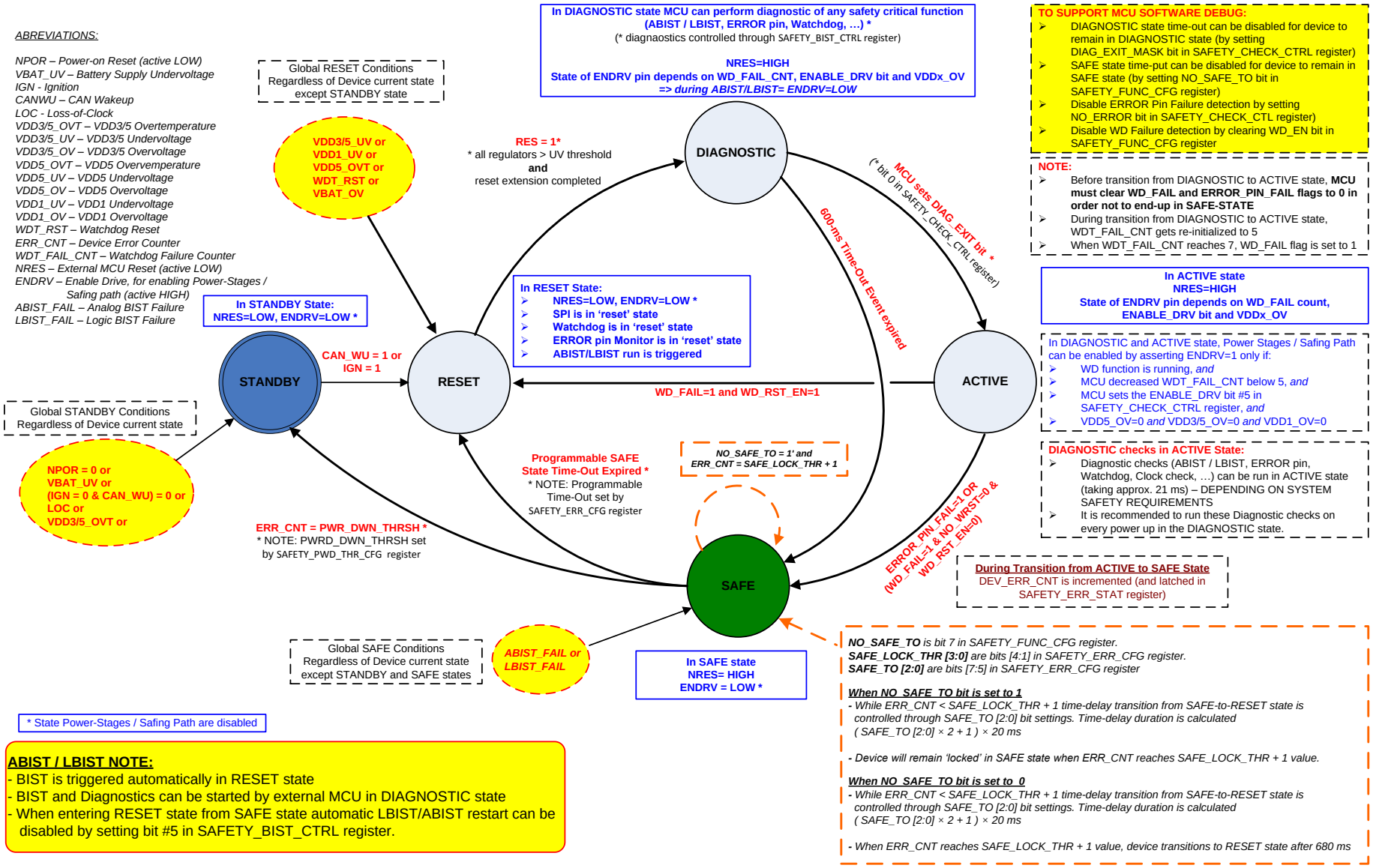


Figure 19. Device Controller State Diagram

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STANDBY STATE

- Default state at power up
- All regulators are disabled, ENDRV is disabled, and NRES to the external MCU is driven low.
- Device transition to the STANDBY state from any state due to:
  - VBATP undervoltage event
  - IGN and CANWU driven low
  - VDD3/5 overtemperature event
  - Loss-of-clock detection
  - Error count reached programmed power-down threshold

RESET STATE

- Enters from the STANDBY state after an IGN or CANWU event
- Enters from the SAFE state after a reset delay time-out expires
- Enters from the ACTIVE state after a WDT failure when WDT_RST_EN = 1
- Device transitions to the RESET state from any other state due to:
  - VDD3/5 undervoltage event
  - VDD1 undervoltage event
  - VBATP overvoltage event
  - Watchdog reset

DIAGNOSTIC STATE

- Enters from the RESET state after all regulators are ramped-up and the MCU reset (NRES pin) extension is completed
- State used to perform all device self-tests and diagnostics by the MCU (failures are induced to emulate internal failures and confirm their detection)

  NOTE: if the DIAG_EXIT_MASK or DIAG_EXIT bit is not set to 1 within 600 ms, the DIAGNOSTIC state time-out interval expires, causing a transition to the SAFE state (both the ERROR_PIN failure and WDT failure status bits are set to 1 in the SAFETY_ERR_STATUS register, and the error count is incremented. When setting the DIAG_EXIT_MASK bit to 1 (only recommended for software debug), device stays in the DIAGNOSTIC state until the DIAG_EXIT bit is set. Setting the DIAG_EXIT bit to 1 causes a controlled transition to the ACTIVE state.

ACTIVE STATE

- Enters from the DIAGNOSTIC state after the external MCU sets the DIAG_EXIT bit in the SAFETY_CHECK_CTRL register (controlled transition) or DIAGNOSTIC state time-out interval expired (uncontrolled transition in case of an error in the MCU. This sets the ERROR_PIN failure and WDT failure status bits in the SAFETY_ERR_STATUS register, causing a transition to the SAFE state, and the error count is incremented).
- Watchdog and ERROR/WDI pin monitoring functions are running.

SAFE STATE

- Enters from the ACTIVE state after an ERROR/WDI pin or WDT failure when WDT_RST_EN = 0 and NO_WRST = 0
- Enters from the DIAGNOSTIC state after a 600 ms time-out event expires when the DIAG_EXIT_MASK is not set to 1
- Enters from RESET, DIAGNOSTIC, or ACTIVE state after ABIST or LBIST failure
- Every transition to the SAFE state increments the error count.

SPI Interface

The primary communication between the IC and the external the MCU is via a SPI bus, which provides full-duplex communications in a master-slave configuration. The external MCU is always a SPI master, sending command requests on the SDI pin, and receiving device responses on the SDO pin. The TPS65381-Q1 is always a SPI slave device, receiving command requests and sending responses (status, measured values) to the external MCU over the SDO line.

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- SPI is a 4-pin interface.
  - NCS - SPI chip select (active-low)
  - SCLK - SPI clock
  - SDI - SPI slave-in / master-out (SIMO)
  - Enters from RESET, DIAGNOSTIC, or ACTIVE state after ABIST or LBIST failure
  - SDO - SPI slave-out / master-in (SOMI, three-state output)
- Frame size is 16 bits.
- Speed is up to 10 Mbit/s.
- Commands and data are shifted MSB first, LSB last.
- The SDI line is sampled on the falling edge of SCLK.
- The SDO line is shifted out on the rising edge of SCLK.

The SPI communication starts with the NCS falling edge, and ends with NCS rising edge. The NCS high level keeps the SPI slave interface in the reset state, and the SDO output is in the high-impedance state.

SPI Command Transfer Phase

The following table shows the SPI command-transfer frame during a command or read access.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	PARITY

CMD[6:0]	Register WR or RD command
PARITY	Parity bit for 7-bit command filed

The SPI Interface does not support back-to-back SPI frame operation: after each SPI command or read access, the NCS pin must go from low to high before the next SPI transfer can be started.

SPI Data-Transfer Phase

The table below shows the SPI data-transfer frame format during a write access:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

DATA[7:0]	Data value for write access (8-bit)

It is possible to mix the two access modes (write and read access) during one SPI communication sequence (NCS = 0). The SPI communication can be terminated after a single 8-bit SPI transfer by asserting NCS = 1. The device returns status flag bits (for the very first SPI transfer after power up) or the current register value that was addressed during the SPI transfer-address phase.

The SPI interface does not support back-to-back SPI frame operation: after each SPI transfer, the NCS pin must go from low to high before the next SPI transfer can be started.

Device Status Flag Byte Response

The following table shows the SPI data status response frame format during a command, read or write access:

Bit	R7	R6	R5	R4	R3	R2	R1	R0
Function	STAT[7]	STAT[6]	STAT[5]	STAT[4]	STAT[3]	STAT[2]	STAT[1]	STAT[0]

- STAT[7]: 1
- STAT[6]: 0
- STAT[5]: 1
- STAT[4]: 0
- STAT[3]: SPI WR access (during previous SPI frame-command phase)
- STAT[2]: SPI SDO error (during previous SPI frame)
- STAT[1]: Data-phase parity (during previous SPI frame)
- STAT[0]: Invalid SPI transfer

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Device SPI Data Response

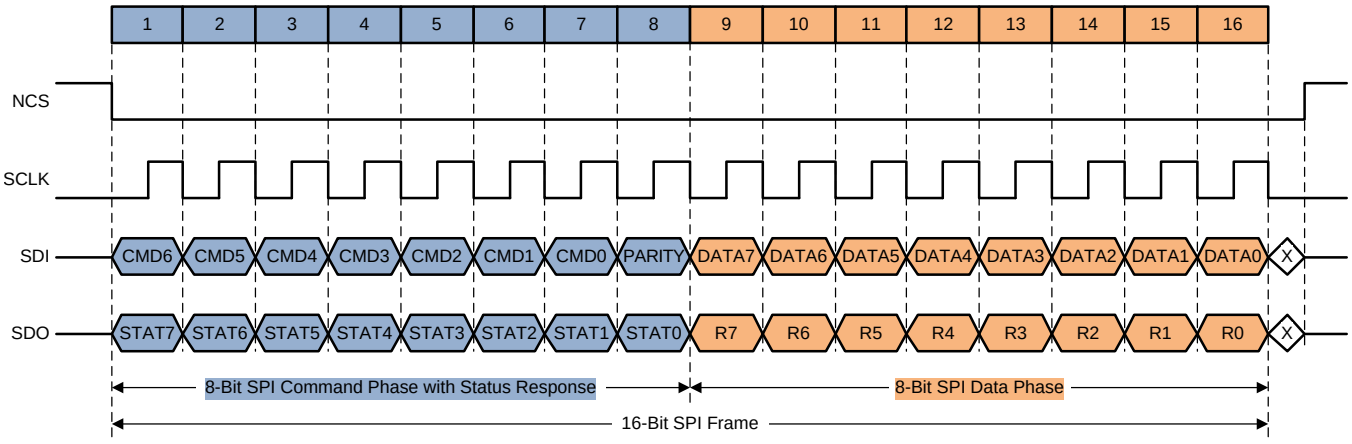
The following table shows the device SPI data-response frame format during a read access:

Bit	R7	R6	R5	R4	R3	R2	R1	R0
Function	R7	R6	R5	R4	R3	R2	R1	R0

- R[7:0] Internal register value. All unused bits are set to zero.

SPI Frame Overview

Figure 20 shows an overview of a complete 16-bit SPI Frame:



NOTE: SPI Master (MCU) and SPI Slave (TPS6538x) sample received data on the falling SCLK edge, and transmit on rising SCLK edge

Figure 20. 16-Bit SPI Frame

Device SPI Mapped Response

The following tables show the available SPI registers. For each SPI register, the bit names are given, with the default values (values after internal logic reset). These default values apply after each wake-up from IGN or CANWU. The explanation of each bit function is given following the tables.

Device Revision and ID

DEV_REV Register — *Read command: RD_DEV_REV*

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]
0	0	0	1	0	0	0	1

D[7:0] ***REV[7:0] – Device Revision***

– REV[3:0]: Device minor revision

– REV[7:4]: Device major revision

DEV_ID Register — *Read command: RD_DEV_ID*

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]
0	0	0	0	0	0	0	0

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Device Status

DEV_STATE Register — *Read command: RD_DEV_STAT*

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	RSV	RSV	CANWU_L	IGN
0	0	0	0	0	0	0	0

D[7:2] RSV

D[1] CANWU_L – Latched CAN wake-up event

D[0] IGN – Deglitched IGN pin (7.7-ms to 22-ms deglitch time)

Device Configuration

DEV_CFG1 Register

Read command: ***RD_DEV_CFG1*** *Write command:* ***WR_DEV_CFG1***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	MASK_VDD1_OV	RSV	RSV	RSV	RSV	RSV	RSV
1	1	0	0	0	0	0	0

D[7] VDD_3_5_SEL – Status bit of VDD3/VDD5 selection at power up

– SEL_VDD3/5 input pin is sampled and latched at power up

- 0: 5-V setting
- 1: 3.3-V setting

(NOTE: Same as SAFETY_FUNC_CFG bit D0)

D[6] MASK_VDD1_OV

– Set to 1 per default: VDD1_OV is masked in the state machine and ENDRV condition. This setting can be used in case VDD1 is not used in an application.

If VDD1 is used in an application, it is recommended to clear this bit to 0 when the device is in the DIAGNOSTIC state.

D[5:0] RSV

DEV_CFG2 Register

Read command: ***RD_DEV_CFG2*** *Write command:* ***WR_DEV_CFG2***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
EN_VDD3/5_OT	EN_VDD5_OT	POST_RUN_RST	MASK_VBAT_OV	RSV	RSV	RSV	RSV
1	1	0	0	0	0	0	0

D[7] EN_VDD3/5_OT

– Set to 1 per default. Clearing this bit to 0 disables the VDD3/5 overtemperature shutdown. The VDD3_5_OT flag is still present in SAFETY_STAT_REG1 bit D0.

D[6] EN_VDD5_OT

– Set to 1 per default. Clearing this bit to 0 disables the VDD5 overtemperature shutdown. The VDD5_OT flag is still present in SAFETY_STAT_REG1 bit D1.

D[5] POST_RUN_RST – Set to 0 per default. If this bit is set to 1 when using the IGN_PWRL function, a re-cracking on the IGN pin causes the device to go to the RESET state.

D[4] MASK_VBATP_OV

– Set to 0 per default. When set 1, VBATP_OV is masked from the RESET condition.

D[3:0] RSV, not read/writable

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Safety-Related Status and Control Registers

VMON_STAT_1 Register

Read command: ***RD_VMON_STAT_1***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
VBATP_OV	VPATP_UV	VCP17_OV	VCP12_OV	VCP12_UV	AVDD_VMON_ERR	BG_ERR2	BG_ERR1
0	0	0	0	0	0	0	0

D[7] VBATP_OV – VBATP overvoltage status bit
- Set to 1 when VBATP overvoltage is detected
- Cleared to 0 after SPI read access and if overvoltage condition is no longer present

D[6] VBATP_UV – VBATP undervoltage status bit
- Set to 1 when VBATP undervoltage is detected
- Cleared to 0 after SPI read access and if undervoltage condition is no longer present

D[5] VCP17_OV – VCP17 overvoltage status bit
- Set to 1 when VCP17 overvoltage is detected
- Cleared to 0 after SPI read access and if overvoltage condition is no longer present

D[4] VCP12_OV – VCP12 overvoltage status bit
- Set to 1 when VCP12 overvoltage is detected
- Cleared to 0 after SPI read access and if overvoltage condition is no longer present

D[3] VCP12_UV – VCP12 undervoltage status bit
- Set to 1 when VCP12 undervoltage is detected
- Cleared to 0 after SPI read access and if undervoltage condition is no longer present

D[2] AVDD_VMON_ERR – voltage-monitor power-supply error status
- Set to 1 when voltage-monitor power supply is not OK. Cleared to 0 after SPI read access and if error condition is no longer present

D[1] BG_ERR2 – Reference band-gap 2 error
- Set to 1 when band-gap 2 error is detected
- Cleared to 0 after SPI read access and if error condition is no longer present

D[0] BG_ERR1 – Reference band-gap 1 error
- Set to 1 when band-gap 1 error is detected
- Cleared to 0 after SPI read access and if error condition is no longer present

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VMON_STAT_2 Register

Read command: ***RD_VMON_STAT_2***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
VDD6_OV	VDD6_UV	VDD5_OV	VDD5_UV	VDD3/5_OV	VDD3/5_UV	VDD1_OV	VDD1_UV
0	0	0	0	0	0	0	0

D[7] VDD6_OV – VDD6 overvoltage status bit
- Set to 1 when VDD6 overvoltage is detected
- Cleared to 0 after SPI read access and if overvoltage condition is no longer present

D[6] VDD6_UV – VDD6 undervoltage status bit
- Set to 1 when VDD6 undervoltage is detected
- Cleared to 0 after SPI read access and if undervoltage condition is no longer present

D[5] VDD5_OV – VDD5 overvoltage status bit
- Set to 1 when VDD5 overvoltage is detected
- Cleared to 0 after SPI read access and if overvoltage condition is no longer present

D[4] VDD5_UV – VDD5 undervoltage status bit
- Set to 1 when VDD5 undervoltage is detected
- Cleared to 0 after SPI read access and if undervoltage condition is no longer present

D[3] VDD3/5_OV – VDD3/5 overvoltage status bit
- Set to 1 when VDD3/5 overvoltage is detected
- Cleared to 0 after SPI read access and if overvoltage condition is no longer present

D[2] VDD3/5_UV – VDD3/5 undervoltage status bit
- Set to 1 when VDD3/5 undervoltage is detected
- Cleared to 0 after SPI read access and if undervoltage condition is no longer present

D[1] VDD1_OV – VDD1 overvoltage status bit
- Set to 1 when VDD1 overvoltage is detected
- Cleared to 0 after SPI read access and if overvoltage condition is no longer present

D[0] VDD1_UV – VDD1 undervoltage status bit
- Set to 1 when VDD1 undervoltage is detected
- Cleared to 0 after SPI read access and if undervoltage condition is no longer present

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SAFETY_STAT_1 Register

Read command: ***RD_SAFETY_STAT_1***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
VDD5_ILIM	VDD3_ILIM	VSOUT1_UV	VSOUT1_OV	VSOUT1_ILIM	VSOUT1_OT	VDD5_OT	VDD_3_5_OT
0	0	0	0	0	0	0	0

D[7] VDD5_ILIM – VDD5 current-limit status bit
- Set to 1 when VDD5 current limit is exceeded
- Cleared to 0 after SPI read access and if current-limit condition is no longer present

D[6] VDD3_ILIM – VDD3 current-limit status bit
- Set to 1 when VDD3 current limit is exceeded
- Cleared to 0 after SPI read access and if current-limit condition is no longer present

D[5] VSOUT1_UV – Sensor-supply undervoltage status bit
- Set to 1 when VSOUT1 undervoltage is detected
- Cleared to 0 after SPI read access and if undervoltage condition is no longer present

D[4] VSOUT1_OV – Sensor-supply overvoltage status bit
- Set to 1 when VSOUT1 overvoltage is detected
- Cleared to 0 after SPI read access and if overvoltage condition is no longer present

D[3] VSOUT1_ILIM – VSOUT1 sensor-supply current-limit status bit
- Set to 1 when VSOUT current limit is exceeded
- Cleared to 0 after SPI read access and if current-limit condition is no longer present

D[2] VSOUT1_OT – Sensor-supply overtemperature status bit
- Set to 1 when VSOUT overtemperature is exceeded. It clears VSOUT enable control bit.
- Cleared to 0 after SPI read access and if overtemperature condition is no longer present

D[1] VDD5_OT – VDD5 overtemperature status bit
- Set to 1 when VDD5 overtemperature is exceeded. It keeps VDD5 regulator disabled as long as bit is set.
- Cleared to 0 after SPI read access and if overtemperature condition is no longer present

D[0] VDD_3_5_OT – VDD3/5 overtemperature status bit
- Set to 1 when VDD3/5 overtemperature is exceeded. It keeps VDD3/5 regulator disabled as long as bit is set to 1.
- Cleared to 0 after SPI read access and if overtemperature condition is no longer present

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SAFETY_STAT_2 Register

Read command: ***RD_SAFETY_STAT_2***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	CFG_CRC_ERR	EE_CRC_ERR	RSV	WDT_FAIL_CNT[2]	WDT_FAIL_CNT[1]	WDT_FAIL_CNT[0]
0	0	0	0	0	1	0	1

D[7:6] RSV

D[5] CFG_CRC_ERR – CRC Error status bit for safety configuration registers

- Safety configuration registers are protected by CRC8.
- This bit is set to 1 when the calculated CRC8 value for safety configuration registers does not match the expected CRC8 value stored in the SAFETY_CFG register.
- Cleared to 0 after SPI read access and CRC8 mismatch is no longer present.

D[4] EE_CRC_ERR – EPROM CRC error status bit

- EEPROM content is protected by CRC8.
- This bit is set to 1 when the calculated CRC8 value does not match the expected CRC8 value stored in the EEEPROM DFT register.
- Cleared to 0 after SPI read access and CRC8 mismatch is no longer present.

D[3] RSV

D[2:0] WDT_FAIL_CNT[2:0] – Watchdog failure counter state

- The default value is 5.
- Watchdog failure counter is incremented every time the device watchdog response failure is detected and decremented each time the correct response is received.
- Watchdog failure counter must be decremented below 5 in order to enable the ENABLE_DRV output pin.
- Watchdog failure is detected when the watchdog failure counter reaches the count of 7 and the WD_FAIL status bit is set to 1 in the SAFETY_ERR_STAT register (setting the WD_FAIL bit to 1 in the SAFETY_ERR_STAT register).

SAFETY_STAT_3 Register

Read command: ***RD_SAFETY_STAT_3***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	NRES_IN	LBIST_ERR	ABIST_UVOV_ERR	ABIST_UVOV_ERR	LBIST_RUN	ABIST_RUN
0	0	0	0	0	0	0	0

D[7:6] RSV

D[5] NRES_IN – Reset input status

- This bit reflects the read-back state of the NRES pin.

D[4] LBIST_ERR – Logic BIST error-status bit

- This bit is set to 1 when logic BIST fails
- Cleared to 0 after SPI read access.
- Only valid when the LBIST_RUN bit is 0

D[3] ABIST_UVOV_ERR – Analog BIST under- and overvoltage BIST error-status bit

- This bit is set to 1 when analog under- and overvoltage BIST fails.
- Cleared to 0 after SPI read access
- Only valid when the ABIST_RUN bit is 0

D[2] ABIST_UVOV_ERR – Analog BIST under- and overvoltage BIST error-status bit (identical to D3)

- This bit is set to 1 when analog under- and overvoltage BIST fails.
- Cleared to 0 after SPI read access
- Only valid when the ABIST_RUN bit is 0

D[1] DBIST_RUN – Logic BIST run-status bit

- This bit is set to 1 when logic BIST is running.
- Cleared to 0 after logic BIST completes run.

D[0] ABIST_RUN – Analog BIST run-status bit

- This bit is set to 1 when analog BIST is running.
- Cleared to 0 after analog BIST completes run

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SAFETY_STAT_4 Register

Read command: ***RD_SAFETY_STAT_4***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
SPI_ERR[1]	SPI_ERR[0]	LOCLK	RSV	MCU_ERR	WD_ERR	EN_DRV_ERR	TRIM_ERR
1	1	0	0	0	0	0	0

D[7:6] SPI_ERR[1:0] – SPI error-status bits
- 00: No error
- 01: Command error
- 10: Format error (received bit count is not equal to 16)
- 11: Data output mismatch

D[5] LOCLK – Loss of clock-detection status bit
- – Set when loss-of-clock failure is detected
- Cleared 0 after SPI read access and if clock failure is no longer present.

D[4] RSV

D[3] MCU_ERR – MCU Error Monitor status bit
- – This bit is set to 1 when an ERROR pin failure is detected.
- – Cleared to 0 after SPI read access and if failure is no longer present

D[2] WD_ERR – Watchdog error-status bit
- – This bit is set to 1 when a watchdog function failure is detected.
- – Cleared to 0 after SPI read access

D[1] EN_DRV_ERR – Enable driver error
- – This bit is set to 1 when a mismatch between the EN_DRV output and EN_DRV input feedback is detected.
- – Cleared to 0 after SPI read access if failure is no longer present

D[0] TRIM_ERR – VMON trimming error-status bit
- – This bit is set to 1 when mismatch voltage-monitor trim error is detected.
- – Cleared to 0 after SPI read access if failure is no longer present

SAFETY_STAT_5 Register

Read command: ***RD_SAFETY_STAT_5***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	RSV	FSM[2]	FSM[1]	FSM[0]
0	0	0	1	0	0	0	0

D[2:0] FSM[2:0] – Current device state
- – Reflects current device state
  - ● STANDBY state: 8’h00
  - ● RESET state: 8’h03
  - ● DIAGNOSTIC state: 8’h07
  - ● ACTIVE state: 8’h05
  - ● SAFE state: 8’h04

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SAFETY_ERR_CFG Register

Read command: ***RD_SAFETY_ERR_CFG*** *Write command:* ***WR_SAFETY_ERR_CFG***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
SAFE_TO [2]	SAFE_TO [1]	SAFE_TO [0]	SAFE_LOCK_TH [3]	SAFE_LOCK_TH [2]	SAFE_LOCK_TH [1]	SAFE_LOCK_TH [0]	CFG_LOCK
1	1	0	0	0	0	0	0

D[7:5] SAFE_TO[2:0] – SAFE state time-out settings

- Duration of SAFE state is time-limited to protect against potential MCU *locked* state.
- Time-out duration = (2 × SAFE_TO[2:0] + 1) × 20 ms
- Minimum duration is 20 ms
- Maximum duration is 300 ms
- 20-ms time reference has 5% accuracy coming from 4-MHz internal oscillator)

D[4:1] SAFE_LOCK_THR[3:0]

- Sets corresponding device ERR_CNT threshold at which device remains in SAFE state regardless of time-out event
- When NO_SAFE_TO bit (SAFETY_FUNC_CFG register, bit 7) is set to 1:
  - While ERR_CNT < SAFE_LOCK_THR + 1, time-delay transition from SAFE-to-RESET state is controlled through SAFE_TO[2:0] bit settings. Time-delay duration is calculated (SAFE_TO[2:0] × 2 + 1) × 20 ms
  - Device remains *locked* in SAFE state when ERR_CNT reaches SAFE_LOCK_THR + 1 value.
- When NO_SAFE_TO bit (SAFETY_FUNC_CFG register, bit 7) is set to 0:
  - While ERR_CNT < SAFE_LOCK_THR + 1, time-delay transition from SAFE-to-RESET state is controlled through SAFE_TO[2:0] bit settings. Time-delay duration is calculated (SAFE_TO[2:0] × 2 + 1) × 20ms
  - When ERR_CNT reaches SAFE_LOCK_THR + 1 value, device transitions to RESET state after 680 ms.
- Intended to support software debug/development and NOT recommended for normal functional operation.
- 0000 setting is default setting, and has same effect as 1111 setting. Both settings give the maximum threshold.

D[0] CFG_LOCK

- Register lock access control
- When set to 1, the register content cannot be updated by SPI WR access.

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SAFETY_BIST_CTRL Register

Read command: ***RD_SAFETY_BIST_CTRL*** *Write command:* ***WR_SAFETY_BIST_CTRL***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
BIST_DEG_CNT[1]	BIST_DEG_CNT[0]	AUTO_BIST_DIS	EE_CRC_CHK	LOCLK_EN	LBIST_EN	ABIST_EN	ABIST_EN
1	1	0	0	0	0	0	0

D[7:6] BIST_DEG_CNT[1:0] – Deglitch filter duration setting during active analog BIST
- It controls deglitch filter duration for every safety-critical monitored voltage.
- Resolution is 15 µs (with MIN setting at 15 µs and MAX setting at 60 µs): bist_deglitch = (BIST_DEG_CNT[1:0] + 1) × 15 µs)
- 15-µs time reference has 5% accuracy coming from 4-MHz internal oscillator.

D[5] AUTO_BIST_DIS
- It controls automatic BIST start-up in RESET state ONLY when device enters RESET sate from SAFE state.
- When set to 1, automatic BIST start-up is disabled.

D[4] EE_CRC_CHK – Recalculate EEPROM CRC8
- It controls EEPROM CRC8 check function
- When set to 1, EEPROM content is reloaded and CRC8 re-calculated and compared against expected value stored in EEPROM DFT register.
- NOTE: With every power-up event, EEPROM content is reloaded and its CRC8 re-calculated.
- The self-test status is checked through bit 4 in SAFETY_STATUS_2 register.

D[3] LOCLK_EN - Enable LOC BIST separately, without the analog UV, OV BIST

D[2] LBIST_EN – Enable digital BIST run
- It controls the logic BIST run
- The self-test status is monitored through bits D1 and D4 in the SAFETY_STAT_3 register.
- LBIST_EN clears the DIAG_EXIT_MASK bit to 0. The time-out counter only stops during the running of LBIST. After LBIST completes, the time-out counter continues from last value. To stay in the DIAGNOSTIC state, the DIAG_EXIT_MASK bit must be set to 1 after LBIST completion. For transition from the DIAGNOSTIC state to the ACTIVE state, the DIAG_EXIT bit must be set to 1.

D[1] ABIST_EN – Enable analog BIST run (same as D[0])
- It controls the analog UV,OV and LOC BIST run.
- The self-test status is monitored through bits D0, D2, and D3 in the SAFETY_STAT_3 register, and bit D4 in the SAFETY_STAT4 register.

D[0] ABIST _EN – Enable analog BIST run (same as D[1])
- It controls the analog UV, OV, and LOC BIST run.
- The self-test status is monitored through bits D0, D2, and D3 in the SAFETY_STAT_3 register, and bit D4 in the SAFETY_STAT4 register.

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SAFETY_CHECK_CTRL Register

Read command: ***RD_SAFETY_CHECK_CTRL*** *Write command:* ***WR_SAFETY_CHECK_CTRL***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
CFG_CRC_EN	RSV	ENABLE_DRV	NO_WRST	RSV	NO_ERROR	DIAG_EXIT_MASK	DIAG_EXIT
0	0	0	1	0	1	0	0

D[7] CFG_CRC_EN
- Controls enabling CRC8 protection for device configuration registers.
- When set to 1, CRC8 is calculated for all device configuration registers and compared with the CRC8 value stored in the SAFETY_CFG_CRC register.
- It is recommended first to set the desired device configuration, followed by updating the SAFTY_CFG_CRC register before setting this bit to 1.
- The following registers are protected:
  - SAFETY_FUNC_CFG register
  - REG_REV (device revision) register
  - SAFETY_PWD_THR_CFG register
  - SAFETY_ERR_CFG register
  - WDT_TOKEN_CFG register
  - WDT_OPEN_WIN_CFG register
  - WDT_CLOSE_WIN_CFG register
  - SAFETY_ERR_PWM_L register

D[6] RSV, read/writeable with no effect

D[5] ENABLE_DRV
- Controls enabling ENDRV output
- In addition to setting this bit to 1, the watchdog failure counter must be decremented below its default count value of 5 in order to enable the ENDRV output.

D[4] NO_WRST - Watchdog reset enable
- When set to 1, this bit masks the transition from the ACTIVE to the SAFE state caused by watchdog failure count >7 (for debugging purposes)
- When set to 0, depending on the setting of the WD_RST_EN bit (bit D3) in the SAFETY_FUNC_CFG register, transition from the ACTIVE to the SAFE state caused by WD_FAIL_CNT = 7 (for debugging purpose)
  - The WD_RST bit has the higher priority, so when WD_RST_EN = 1, transition from ACTIVE to RESET has the higher priority when WD_FAIL_CNT = 7.

D[3] RSV, not read/writable

D[2] NO_ERROR
- Controls enabling the MCU_ERROR pin-monitor function (through the device ERROR/WDI pin) and transition from the ACTIVE state to the SAFE state when an MCU_ERROR pin failure is detected.
  - 1: MCU_ERROR pin failure is monitored, but a detected failure in the ACTIVE state does not cause a transition to the SAFE state.
  - 0: MCU_ERROR pin failure is monitored, and a detected failure in the ACTIVE state causes a transition to the SAFE state.
- If an MCU_ERROR pin failure is detected, the ERROR_PIN_FAIL status bit in the SAFETY_ERR_STAT register is set, only for setting NO_ERROR = 0.

D[1] DIAG_EXIT_MASK
- Controls exit from the DIAGNOSTIC state
- When set to 1, exit from the DIAGNOSTIC state is disabled regardless if a time-out event occurs or if the DIAG_EXIT bit is set.
- This feature is only recommended for software debug/development and should not be activated in functional mode.

D[0] DIAG_EXIT
- Controls exit from the DIAGNOSTIC state.
- When set to 1 and the DIAG_EXIT_MASK bit is 0, the device transitions from the DIAGNOSTIC to the ACTIVE state.

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SAFETY_FUNC_CFG Register

Read command: ***RD_SAFETY_FUNC_CTRL*** *Write command:* ***WR_SAFETY_FUNC_CTRL***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
NO_SAFE_TO	ERROR_CFG	WD_CFG	IGN_PWRL	WD_RST_EN	RSV	RSV	VDD_3_5_SEL
0	0	0	1	0	1	0	0

D[7] NO_SAFE_TO
- Controls enabling/disabling the SAFE state time-out function
- When set to 1, SAFE state time-out is disabled. Device remains *locked* in the SAFE state when ERR_CNT reaches the SAFE_LOCK_THR + 1 value. When set to 0, SAFE state time-out is enabled. The device transitions to the RESET state after 680 ms when ERR_CNT reaches the SAFE_LOCK_THR + 1 value.

D[6] ERROR_CFG – MCU error-pin configuration bit
- When set to 0, PWM monitoring is enabled (can be used as an external clock monitor). Expected ERROR/WDI pin LOW and HIGH durations are controlled by the SAFETY_ERR_PWM_H and SAFETY_ERR_PWM_L registers.
- When set to 1, the TMS570 ERROR pin mode is enabled. The ERROR pin low-duration threshold is set by the SAFETY_ERR_PWM_L register.
- Only valid when the watchdog is set in Q&A configuration (WD_CFG = 1)

D[5] WD_CFG – Watchdog function configuration bit
- 0: WDTI configuration enabled (default) – watchdog trigger input through ERROR/WDTI pin

  : Q&A WD configuration enabled – watchdog trigger input through SPI

D[4] IGN_PWRL – Ignition-power latch control bit
- Controls enabling the ignition-power latch
- When set to 1, user can pull ignition input LOW, but device remains powered up.
- Cleared by CANWU event

D[3] WD_RST_EN
- Controls enabling/disabling the watchdog failure function detection
- 1: Watchdog failure is detected when WD_FAIL_CNT[1:0] reaches the count of 7 (in the SAFETY_STAT_2 register), leading to a transition to the RESET state.
- 0: Watchdog failure-event detection depends on the setting of the NO_WRST bi (bit D4)t in the SAFETY_CHECK_CTRL register.

D[2:1] RSV, not read/writable

D[0] VDD_3_5_SEL – Status bit of VDD3/VDD5 selection at power up
- SEL_VDD3/5 input pin is sampled and latched at power up
  - 0: 5-V setting
  - 1: 3.3-V setting

  (NOTE: Same as DEV_CFG1 bit D7)

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SAFETY_ERR_STAT Register

Read command: ***RD_SAFETY_ERR_STAT*** *Write command:* ***WR_SAFETY_ERR_STAT***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	ERROR_PIN_FAIL	WD_FAIL	DEV_ERR_CNT[3]	DEV_ERR_CNT[2]	DEV_ERR_CNT[1]	DEV_ERR_CNT[0]
0	0	0	0	0	0	0	0

D[7:6] RSV

D[5] ERROR_PIN_FAIL

- It is set to 1 when an ERROR pin failure is detected.
- It is cleared to 0 after SPI WR access.

D[4] WD_FAIL

- It is set to 1 when the watchdog function failure counter reaches the count of 7 (WD_FAIL_CNT[1:0] in the SAFETY_STATUS_2 register).
- It is cleared to 0 after SPI WR access.

D[3:0] DEV_ERR_CNT[3:0]

- It tracks the current device error count.
- It can be overwritten by SPI WR access, but ONLY in the DIAGNOSTIC mode.

SAFETY_ERR_PWM_H Register

Read command: ***RD_SAFETY_ERR_PWM_H*** *Write command:* ***WR_SAFETY_PWM_H***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
PWMH[7]	PWMH[6]	PWMH[5]	PWMH[4]	PWMH[3]	PWMH[2]	PWMH[1]	PWMH[0]
1	0	1	0	1	0	0	0

D[7:0] PWMH[7:0] – ERROR pin high -hase duration in PWM mode (15 µs resolution)

- Controls expected high-phase duration with 15 µs resolution

SAFETY_ERR_PWM_L Register

Read command: ***RD_SAFETY_ERR_PWM_L*** *Write command:* ***WR_SAFETY_PWM_L***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
PWML[7]	PWML[6]	PWML[5]	PWML[4]	PWML[3]	PWML[2]	PWML[1]	PWML[0]
0	0	1	0	1	0	0	0

D[7:0] PWML[7:0] – ERROR pin low-phase duration

- Controls expected low-phase duration
  - When ERR_CFG bit is 0 (in PWM mode): ERR PWM low-phase duration with 15-µs resolution
  - When ERR_CFG bit is 1 (TMS570 mode): ERR low duration with 5-µs resolution

SAFETY_PWD_THR_CFG Register

Read command: ***RD_SAFETY_PWD_THR_CFG*** *Write command:* ***WR_SAFETY_PWD_THR_CFG***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RSV	PWD[3]	PWD[2]	PWD[1]	PWD[0]
0	0	0	1	1	1	1	1

D[7:4] RSV

D[3:0] PWD[3:0] – Device error-count threshold to power down the device

- When error count reaches programmed threshold, device powers down.
- It recovers with new wake-up/ignition event.
- This register can be updated only in the DIAGNOSTIC mode.

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SAFETY_CFG_CRC Register

Read command: ***RD_SAFETY_CFG_CRC*** *Write command:* ***WR_SAFETY_CFG_CRC***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
CFG_CRC[7]	CFG_CRC[6]	CFG_CRC[5]	CFG_CRC[4]	CFG_CRC[3]	CFG_CRC[2]	CFG_CRC[1]	CFG_CRC[0]
1	0	1	0	1	0	0	0

D[7:0] CFG_CRC[7:0] – CRC8 value for safety configuration registers
NOTE: can be updated only in the DIAGNOSTIC state

Diagnostics

DIAG_CFG_CTRL Register

Read command: ***RD_DIAG_CFG_CTRL*** *Write command:* ***WR_DIAG_CFG_CTRL***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
MUX_EN	SPI_SDO	MUX_OUT	INT_CON[2]	INT_CON[1]	INT_CON[0]	MUX_CFG[1]	MUX_CFG[0]
0	0	0	0	0	0	0	0

D[7] MUX_EN – Enable diagnostic MUX output
0: Disabled (in high-impedance state)
1: Enabled

D[6] SPI_SDO – To control the SPI_SDO output-buffer state during an interconnect test
NOTE: With configuration 001 setting for INT_CON[2:0] bits

D[5] MUX_OUT – Diagnostic MUX output-state control bit
NOTE: When the MUX_CFG bits are set to 00 and the MUX_EN bit is set to 1

D[4:2] INT_CON[2:0] – Device interconnect-test configuration bits
000: No active interconnect test
001: ERR input state observed on diagnostic MUX output
010: SPI_NCS input state observed on diagnostic MUX output
011: SPI_SDI input state observed on diagnostic MUX output
100: SPI_SCLK input observed on diagnostic MUX output
101: N/A
110: N/A
111: The SPI_SDO bit controls the state of the SPI_SDO output buffer

D[1:0] MUX_CFG – Diagnostic MUX configuration
00: MUX output controlled by MUX_OUT bit (bit 5 in DIAG_CFG_CTRL register)
01: Digital MUX mode
10: Analog MUX mode
11: Device interconnect mode (input-pins interconnect test)
To check SDO diagnostics following sequence is needed
– DIAG_MUX configuration must be 0x1 (DIAG_CFG register bits[1:0])
=>DIGITAL MUX mode
– SPI NCS must be kept HIGH
– The state of SDO is controlled by bit 6 in the DIAG_CFG register

DIAG_MUX_SEL Register

Read command: ***RD_DIAG_MUX_SEL*** *Write command:* ***WR_DIAG_MUX_SEL***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
MUX_SEL[7]	MUX_SEL[6]	MUX_SEL[5]	MUX_SEL[4]	MUX_SEL[3]	MUX_SEL[2]	MUX_SEL[1]	MUX_SEL[0]
0	0	0	0	0	0	0	0

D[7:0] MUX_SEL[7:0] – Diagnostic MUX channel select
NOTE: MUX channel table is dependent on the MUX_CFG[1:0] bit settings in the DIAG_CFG_CTRL register

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Watchdog Timer

WDT_TOKEN_FDBCK Register

Read command: ***RD_WDT_TOKEN_FDBCK*** *Write command:* ***WR_WDT_TOKEN_FDBCK***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
FDBK[3]	FDBK[2]	FDBK[1]	FDBK[0]	TOKEN_SEED[3]	TOKEN_SEED[2]	TOKEN_SEED[1]	TOKEN_SEED[0]
0	0	0	0	0	1	0	0

D[7:4] FDBK[3:0] - WDT token FSM feedback-configuration bits

D[3:0] TOKEN_SEED[3:0] - WDT token seed value

- MCU updates TOKEN seed value to generate set of new TOKEN values
- Only for Q&A WD configuration through SPI

WDT_WIN1_CFG Register

Read command: ***RD_WDT_WIN1_CFG*** *Write command:* ***WR_WDT_WIN1_CFG***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]
0	0	0	0	0	0	0	0

D[7] RSV

D[6:0] WDT open time window duration setting (for Q&A WD configuration through SPI) **or** WDT closed-window duration setting (for WDTI configuration through the ERROR/WDI pin).

- Twow (Q&A) = Twcw (WDTI) = (RT[6:0] + 1) × 0.55 ms

  (0.55-ms time reference has 5% accuracy coming from 4-MHz internal oscillator)

WDT_WIN2_CFG Register

Read command: ***RD_WDT_WIN2_CFG*** *Write command:* ***WR_WDT_WIN2_CFG***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	RW[4]	RW[3]	RW[2]	RW[1]	RW[0]
0	0	0	0	0	0	0	0

D[7:5] RSV

D[4:0] RW[4:0] WDT closed-window duration setting (for QA WD configuration through SPI) or

–

WDT open-window duration setting (for WDTI configuration through ERROR/WDI pin).

– Twcw (QA) = Twow (WDTI) = (RW[4:0] + 1) x 0.55ms

(0.55-ms time reference has 5% accuracy coming from 4-MHz internal oscillator)

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WDT_TOKEN_VALUE Register

Read command: ***RD_WDT_TOKEN_VALUE***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
WDFAIL_TH	RSV	RSV	RSV	TOKEN[3]	TOKEN[2]	TOKEN[1]	TOKEN[0]
0	0	0	0	0	0	0	0

D[7] WDFAIL_TH
- Set to 1 when the watchdog-function failure counter reaches a count of 4 or higher (WD_FAIL_CNT[1:0] in the SAFETY_STATUS_2 register)
- Set to 0 when the watchdog-function failure counter reaches count of less than 4 (WD_FAIL_CNT[1:0] in the SAFETY_STATUS_2 register)
  - MCU must read (or calculate by itself) the current WD token value in order to generate a correct SPI response.

D[6:4] RSV

D[3:0] TOKEN[3:0] - WDT active TOKEN value (or WDT *question* value)
- Only for Q&A WD configuration through SPI

WDT_STATUS Register

Read command: ***RD_WDT_STATUS***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
WDT_ANSW_CNT [1]	WDT_ANSW_CNT [0]	TOKEN_ERR	RSV	WD_CFG_CHG	SEQ_ERR	TIME_OUT	TOKEN_ERLY
0	0	0	0	0	0	0	0

D[7:6] WDT_ANSW_CNT[1:0]: Current received WD answer count state
- Only for Q&A WD configuration through SPI

D[5] TOKEN_ERR: WD token error-status bit
- It is set to 1 when at least one received token (out of four required per single sequence) is wrong
- Only for Q&A WD configuration through SPI

D[4] RSV

D[3] WD_CFG_CHG: WD configuration-change status bit
- It is set to 1 when switching between the WDTI configuration and Q&A configuration, or
- Changing open/close window timer settings

D[2] SEQ_ERR: The last token sequence is wrong
- Incorrect timing or
- Wrong answer
- Only for Q&A WD configuration through SPI

D[1] TIME_OUT: No watchdog trigger received within OPEN/CLOSE window (no-response event)
- In WDTI configuration (default configuration): set to 1 when no trigger event has been received on the ERROR/WDTI pin during OPEN/CLOSE window
- In Q&A WD configuration: set to 1 when no ANSWERS have been received during OPEN window
- This flag is useful to synchronize the MCU Watchdog triggers on the Watchdog timer:
  - On transition from the RESET to the DIAGNOSTIC state, the MCU can poll this TIME_OUT flag directly after reboot to detect the completion of an OPEN/CLOSE window. In order to do so, the MCU should not send any trigger event on the ERROR/WDI pin directly after reboot, until this TIME_OUT flag is set.
  - After configuring the watchdog timer and/or watchdog mode (WDTI or Q&A), the MCU should not send watchdog trigger events until this TIME_OUT flag is set in order to re-synchronize with the OPEN/CLOSE timing.

D[0] TOKEN_ERLY: Token sequence completed too early
- Only for Q&A WD configuration through SPI
- Set to 1 if all 4 ANSWERs are returned during OPEN window

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WDT_ANSWER Register

Read command: ***WR_WDT_ANSWER***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
WDT_ANSW[7]	WDT_ANSW[6]	WDT_ANSW[5]	WDT_ANSW[4]	WDT_ANSW[3]	WDT_ANSW[2]	WDT_ANSW[1]	WDT_ANSW[0]
0	0	0	0	0	0	0	0

D[7:0] WDT_ANSW[7:0] – MCU watchdog answer response

- Each WDT token (question) requires four 8-bit answers
- Three 8-bit answers (SPI responses) must be returned during OPEN WDT window
- The fourth (last) 8-bit answer must be returned during CLOSE WDT window
- The number of returned answers is tracked with the WDT_ANSW_CNT[1:0] bits in the WDT_STATUS_1 register
- Only for Q&A WD configuration through SPI

Sensor Supply

SENS_CTRL Register

Read command: ***RD_SENS_CTRL*** *Write command:* ***WR_SENS_CTRL***

Data Information							
D7	D6	D5	D4	D3	D2	D1	D0
RSV	RSV	RSV	VDD5_EN	RSV	RSV	RSV	VSOUT1_EN
0	0	0	1	0	0	0	0

D[7:5] RSV

D[4] VDD5_EN – If cleared to 0, VDD5 is then turned off.

- This bit is set to 1 per default, and is cleared in case of VDD5 overtemperature (indicated by the VDD5_OT bit D1 in SAFETY_STAT1).
- NOTE: When VDD5 is disabled, bit VDD5_ILIM (bit D7 in SAFETY_STAT_1) is set to 1. Hence, it is recommended to read-out/clear this bit immediately after disabling VDD5

D[3:1] RSV

D[0] VSOUT1_EN – Sensor-supply enable bit (set to 1 to enable the VSOUT1 sensor supply)

- This bit is set to 1 by default, and is cleared in case of VSOUT1 overtemperature (indicated by the VSOUT1_OT bit D2 in SAFETY_STAT1)

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SPI Command Table

7-Bit Binary Command Code (Without Parity)	Parity	7-Bit Hex Command Code (Without Parity)	WR SW LOCK Protect	Register Command Name (NOTE: All commands have even parity.)
1011 110	1	5E	N/A	SW_LOCK with data 0x55 (to lock SPI WR access to listed registers)
1011 101	1	5D	N/A	SW_UNLOCK with data 0xAA (to unlock SPI WR access to listed registers)
0000 011	0	03	N/A	RD_DEV_ID
0000 110	0	06	N/A	RD_DEV_REV
1011 011	1	5B	YES	WR_DEV_CFG1 (SPI WR update can occur only in DIAGNOSTIC state)
1010 111	1	57	N/A	RD_DEV_CFG1
1001 010	1	4A	YES	WR_DEV_CFG2 (SPI WR update can occur only in DIAGNOSTIC state)
0100 100	0	24	N/A	RD_DEV_CFG2
0111 110	1	3E	NO	WR_CAN_STBY
0010 010	0	12	N/A	RD_SAFETY_STAT_1
1100 010	1	62	N/A	RD_SAFETY_STAT_2
1010 001	1	51	N/A	RD_SAFETY_STAT_3
1010 010	1	52	N/A	RD_SAFETY_STAT_4
1100 000	0	60	N/A	RD_SAFETY_STAT_5
0011 000	0	18	N/A	RD_SAFETY_ERR_CFG
1101 101	1	6D	YES	WR_SAFETY_ERR_CFG (SPI WR update can occur only in DIAGNOSTIC state)
1010 100	1	54	YES	WR_SAFETY_ERR_STAT (SPI WR update can occur only in DIAGNOSTIC state)
1010 101	0	55	N/A	RD_SAFETY_ERR_STAT
0011 100	1	1C	N/A	RD_SAFETY_PWD_THR_CFG
1001 100	1	4C	YES	WR_SAFETY_PWD_THR_CFG (SPI WR update can occur only in DIAGNOSTIC state)
0100 010	0	22	N/A	RD_SAFETY_CHECK_CTRL
1001 001	1	49	NO	WR_SAFETY_CHECK_CTRL
0011 110	0	1E	N/A	RD_SAFETY_BIST_CTRL
1001 111	1	4F	YES	WR_SAFETY_BIST_CTRL (SPI WR update can occur only in DIAGNOSTIC and ACTIVE states)
0010 111	0	17	N/A	RD_WD_WIN1_CFG
1110 110	1	76	YES	WR_WD_WIN1_CFG (SPI WR update can occur only in DIAGNOSTIC state)
0000 010	1	02	N/A	RD_WD _WIN2_CFG
0000 100	1	04	YES	WR_WD_WIN2_CFG (SPI WR update can occur only in DIAGNOSTIC state)
0011 011	0	1B	N/A	RD_WDT_TOKEN_VALUE
0100 111	0	27	N/A	RD_WDT_STATUS
1110 000	1	70	NO	WR_WDT_ANSWER
0001 000	1	08	N/A	RD_DEV_STAT
0001 001	0	09	N/A	RD_VMON_STAT_1
1010 011	0	53	N/A	RD_VMON_STAT_2
0101 011	0	2B	N/A	RD_SENS_CTRL
0111 101	1	3D	N/A	WR_SENS_CTRL
0011 101	0	1D	N/A	RD_SAFETY_FUNC_CFG
0011 010	1	1A	YES	WR_SAFETY_FUNC_CFG (SPI WR update can occur only in DIAGNOSTIC state)
0101 101	0	2D	N/A	RD_SAFE_CFG_CRC
0110 001	1	31	YES	WR_SAFE_CFG_CRC (SPI WR update can occur only in DIAGNOSTIC state)
1101 110	1	6E	N/A	RD_DIAG_CFG_CTRL
1100 110	0	66	NO	WR_DIAG_CFG_CTRL

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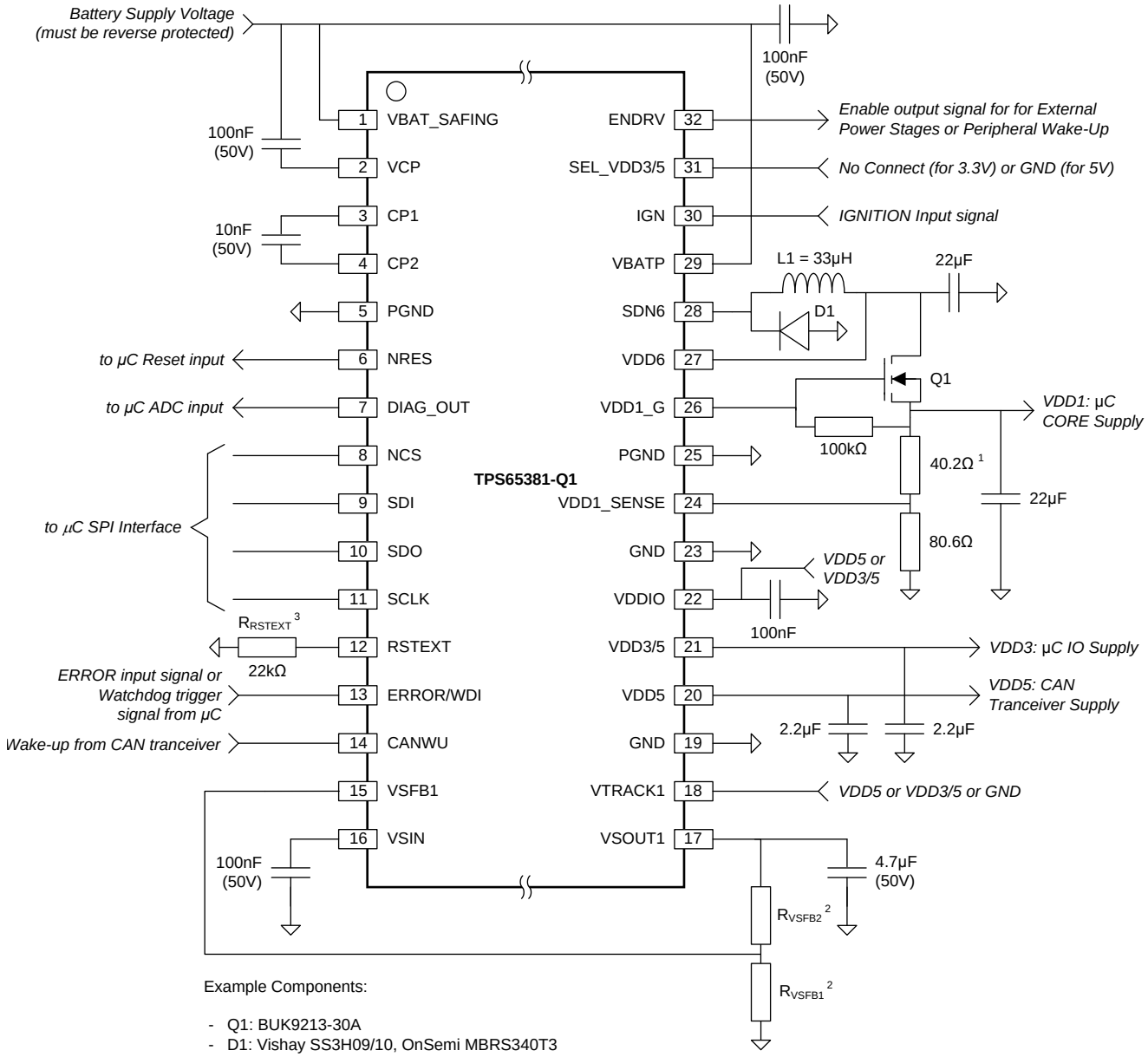
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7-Bit Binary Command Code (Without Parity)	Parity	7-Bit Hex Command Code (Without Parity)	WR SW LOCK Protect	Register Command Name (NOTE: All commands have even parity.)
1010 110	0	56	N/A	RD_DIAG_MUX_SEL
1100 100	1	64	NO	WR_DIAG_MUX_SEL
1101 011	1	6B	N/A	RD_SAFETY_ERR_PWM_H
1101 100	0	6C	YES	WR_SAFETY_ERR_PWM_H (SPI WR update can occur only in DIAGNOSTIC state)
0101 100	1	2C	N/A	RD_SAFETY_ERR_PWM_L
0111 111	0	3F	YES	WR_SAFETY_ERR_PWM_L (SPI WR update can occur only in DIAGNOSTIC state)
0111 100	0	3C	N/A	RD_WDT_TOKEN_FDBCK
0111 011	1	3B	YES	WR_WDT_TOKEN_FDBCK (SPI WR update can occur only in DIAGNOSTIC state)

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APPLICATION DIAGRAMS



Example Components:

- Q1: BUK9213-30A
- D1: Vishay SS3H09/10, OnSemi MBRS340T3
- L1: EPCOS B82464G4333M000 or COILCRAFT MSS1246T-333ML

NOTES:

1. 40.2Ω for 1.2V output voltage. Change this resistor for obtaining different VDD1 output voltage. (VDD1_SENSE = 800mV)
2. Rvsfb1 and Rvsfb2 configure the VSOUT1 voltage. See the VSOUT1 section for explanation.
3. R_{RSEXT} configures the Reset Extension time. See the Reset and Enable Outputs section of the Electrical Characteristics Table.

Figure 21. TPS65381-Q1 Typical Application Diagram

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Typical System Application Diagrams

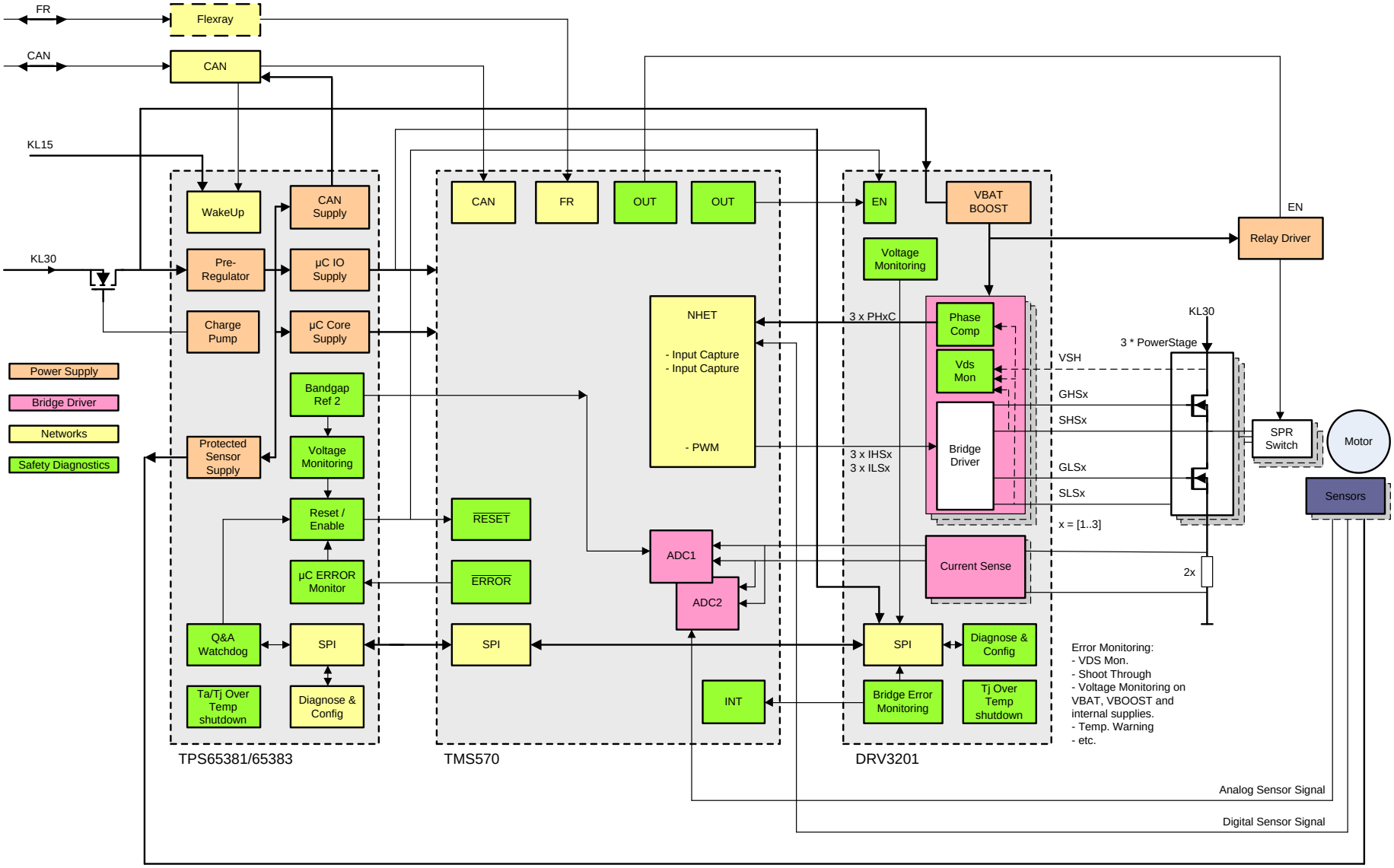


Figure 22. Electrical Power-Steering Example

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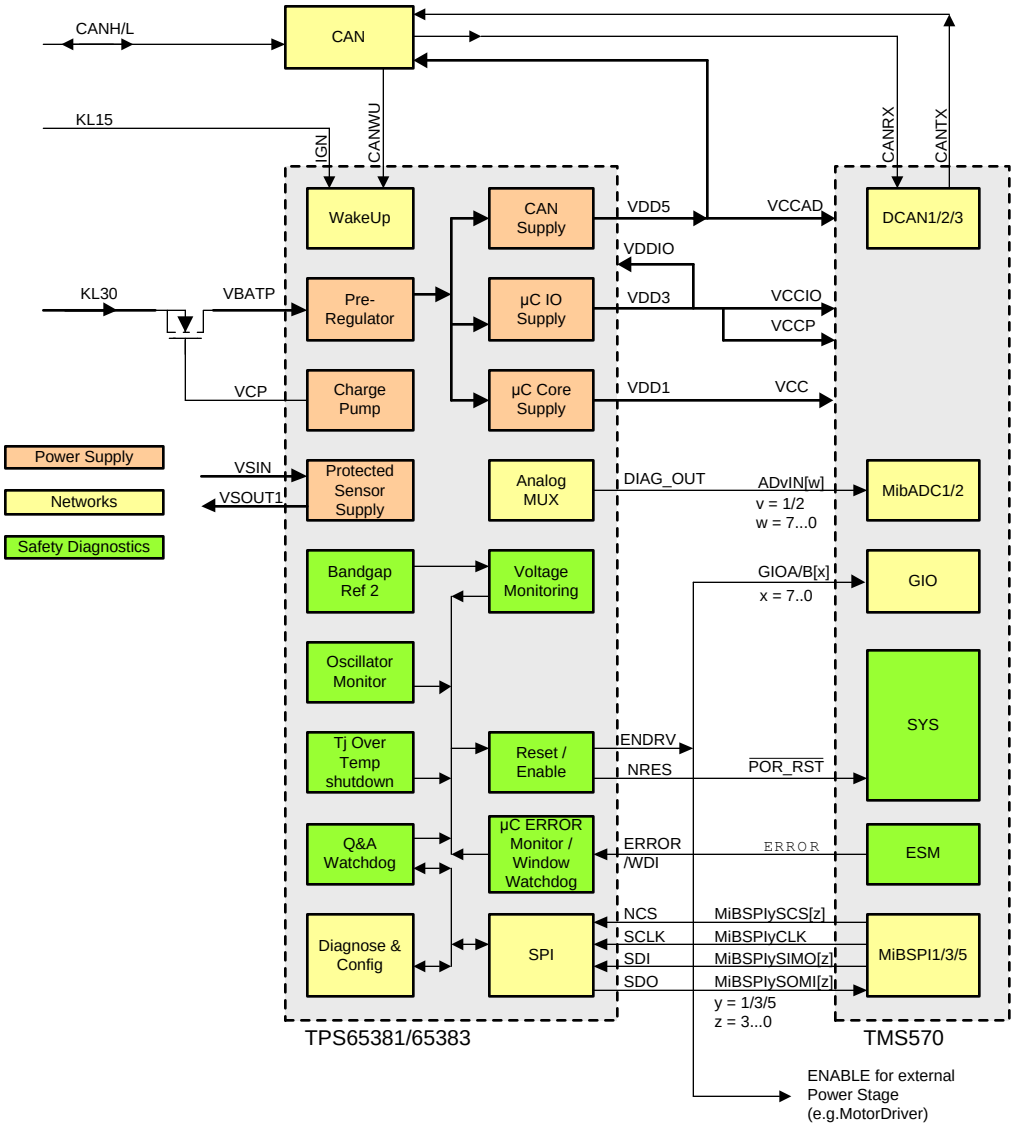


Figure 23. Example TPS65381-Q1 With Texas Instruments TMS570LS

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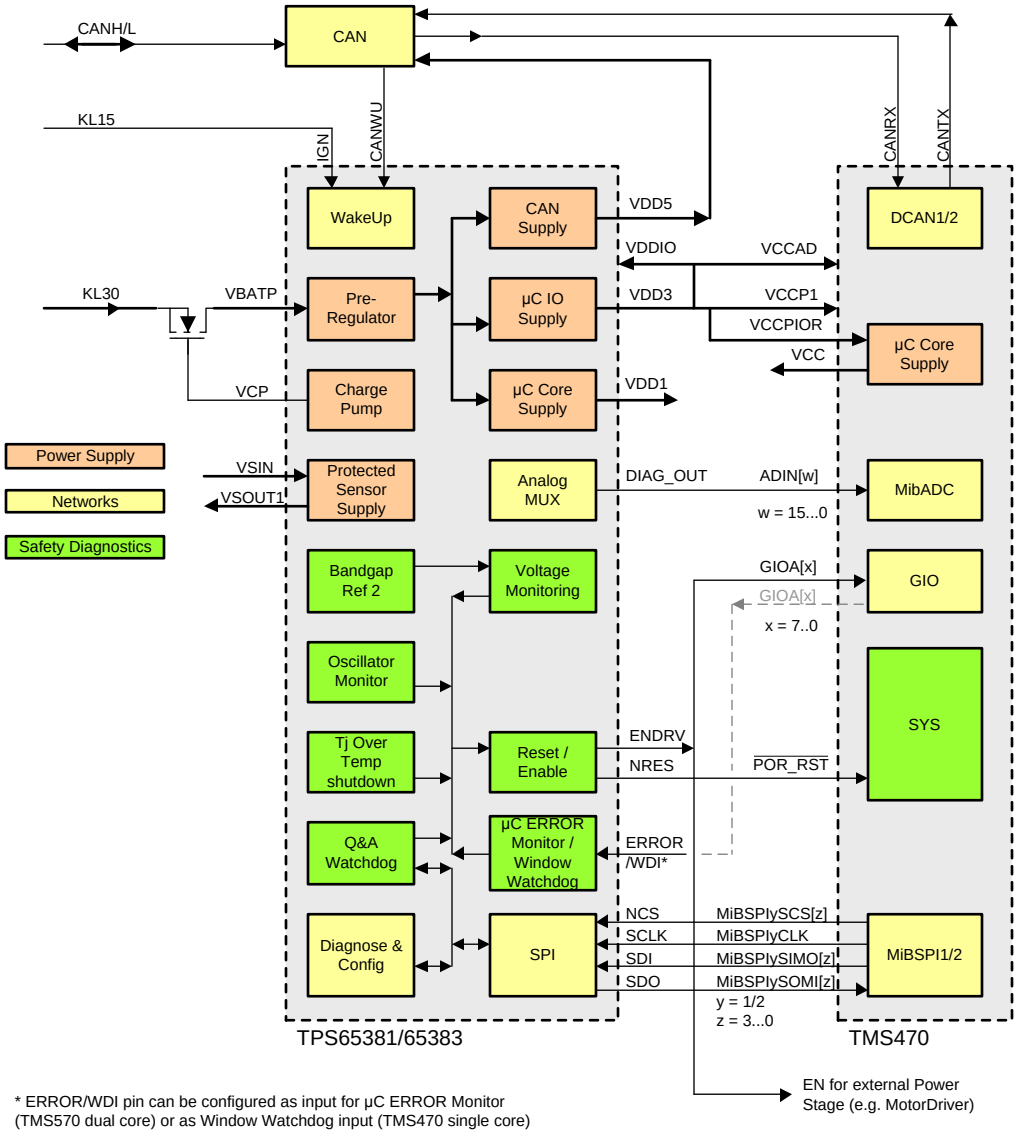


Figure 24. Example TPS65381-Q1 With Texas Instruments TMS470 (Using Internal MCU Core Supply)

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS65381QDAPRQ1	PREVIEW	HTSSOP	DAP	32	2000	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

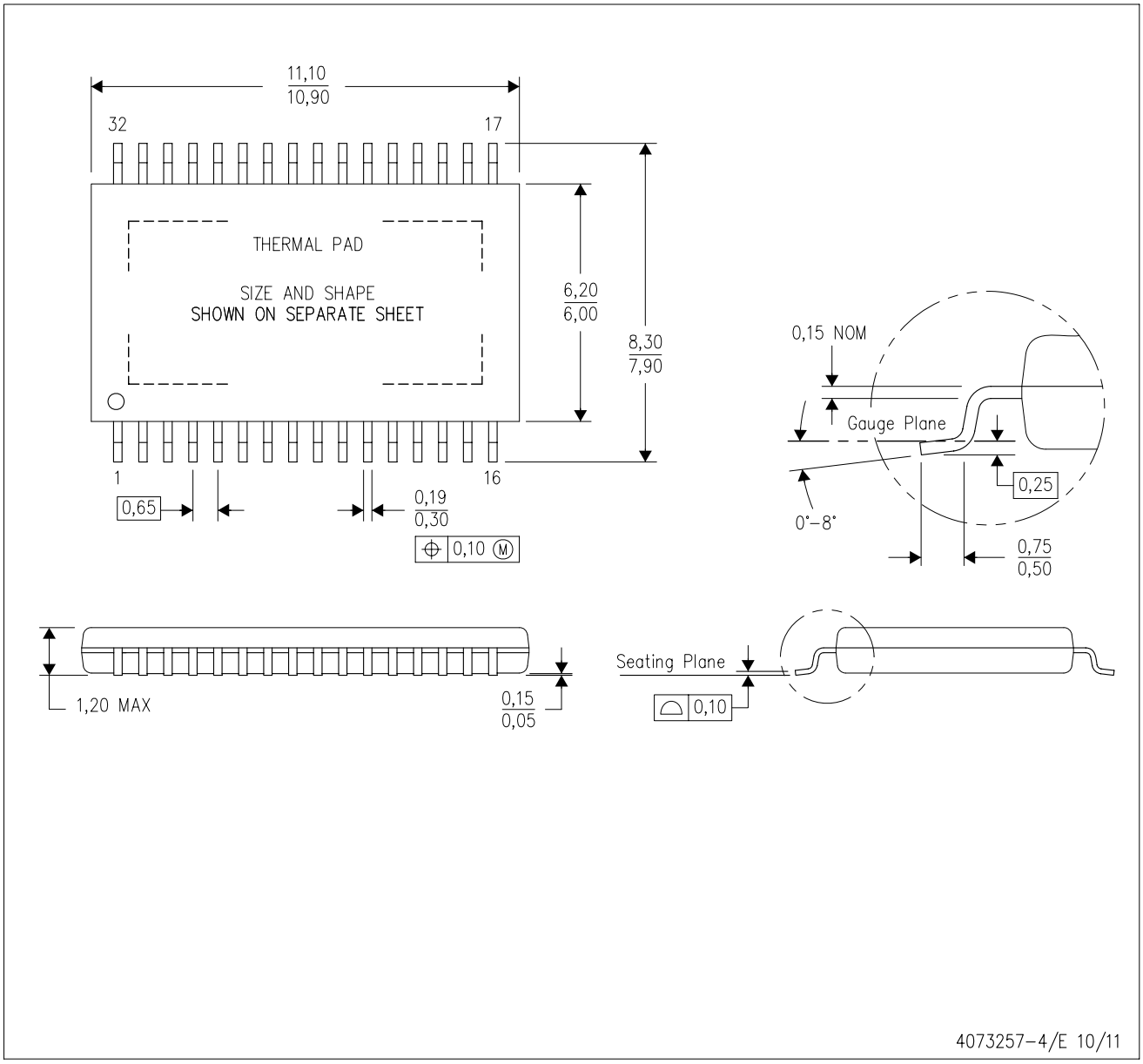
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

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