Dual Power Distribution Switches with 4.5V to 28V Input Voltage, 6A Output Current Synchronous Buck Regulator

This document presents the information required to power the TPS65286 PMIC as well as the support documentation including schematic and bill of materials

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1 Background

The TPS65286 PMIC is designed to provide 6A continuous outputs with an operational range of 4.5V to 28V and an internally switching frequency 500kHz, with automatic PFM/PWM operation. The device also features two power distribution switches.

As there are many possible options to set the converters, Table 1 presents the performance specification summary for the EVM.

Table 1. Input Voltage and Output Current Summary

EVM	TEST CONDITIONS	OUTPUT CURRENT RANGE
TPS65286EVM	VIN = 4.5V to 28V f_{SW} = 500kHz	Buck, 5V, 6A (25°C ambient)
	SW_IN1 = SW_IN2 = 5V	SW_OUT1 = SW_OUT2 = 5V, ISW_OUT1 = ISW_OUT2 = 1.2A

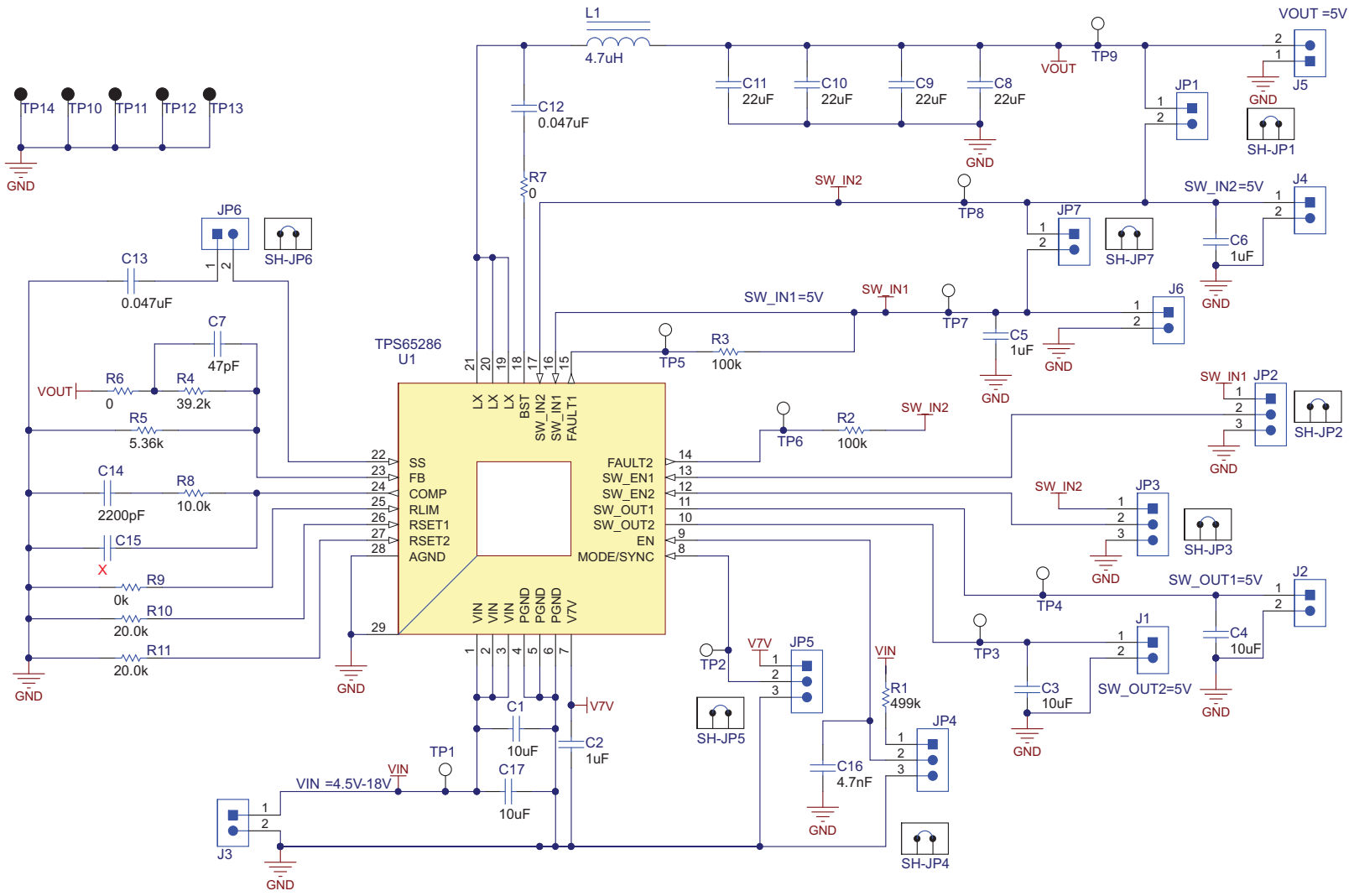
This evaluation module is designed to provide access to the features of the TPS65286. Some modifications can be made to this module to test performance at different input and output voltages, current and frequency operation. Contact TI Field Applications Group for advice on these matters.

2 Schematic

See next page.

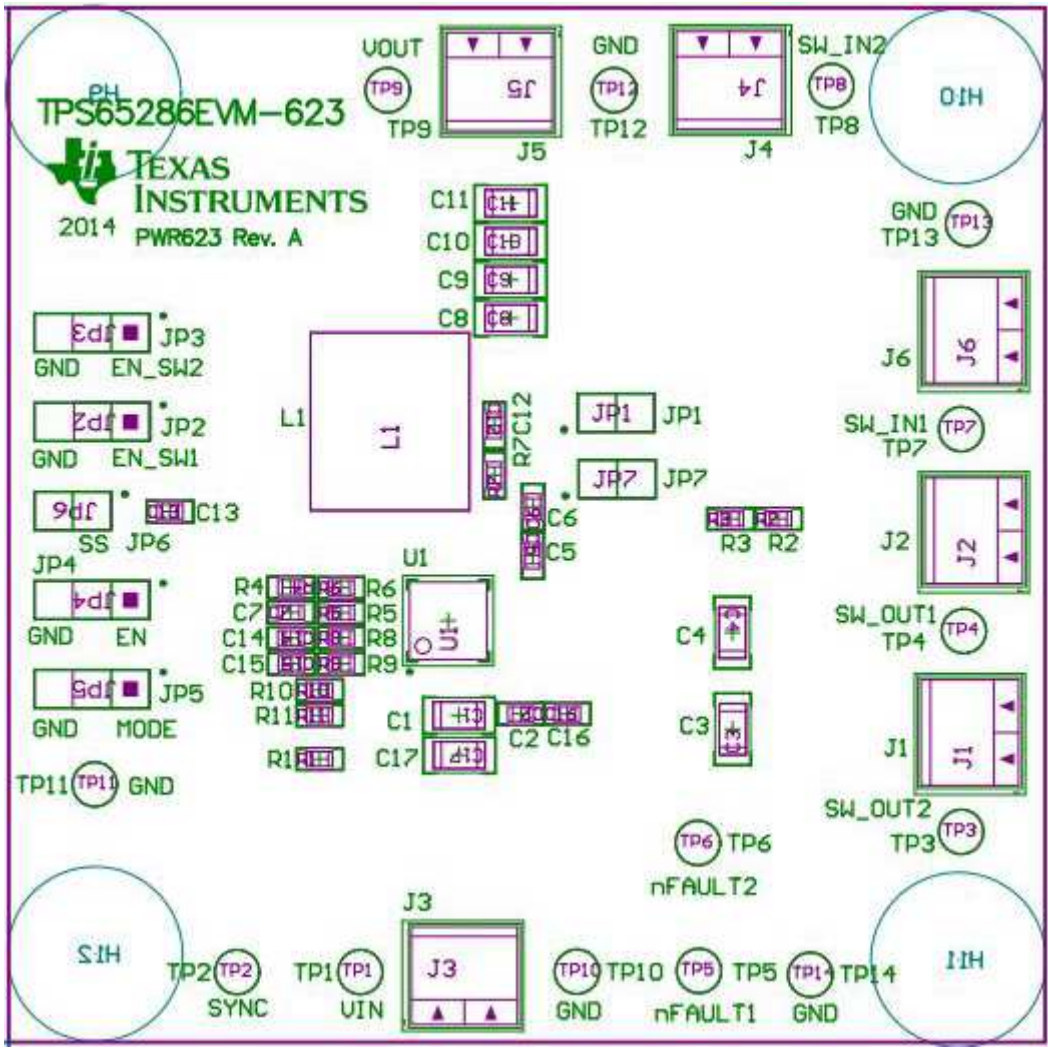
The resistor and capacitor values have been chosen according to the guidelines presented on the TPS65286 spec. Note that for the purpose of gains-phase measurements R11(zero ohm on the EVM) need to be replaced by suitable low value resistors as per the network analyzer setup required. Test points connections are provided on either end of the resistors to allow for easy measurement.

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3 Board Layout



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3.1 EVM Layout

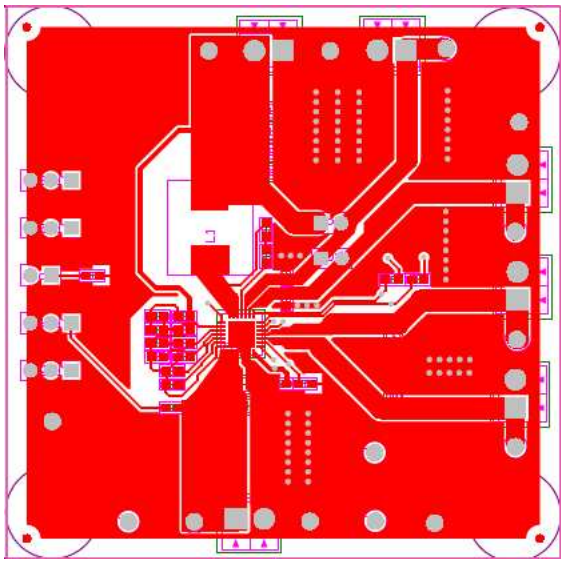


Figure 1. Top Layer

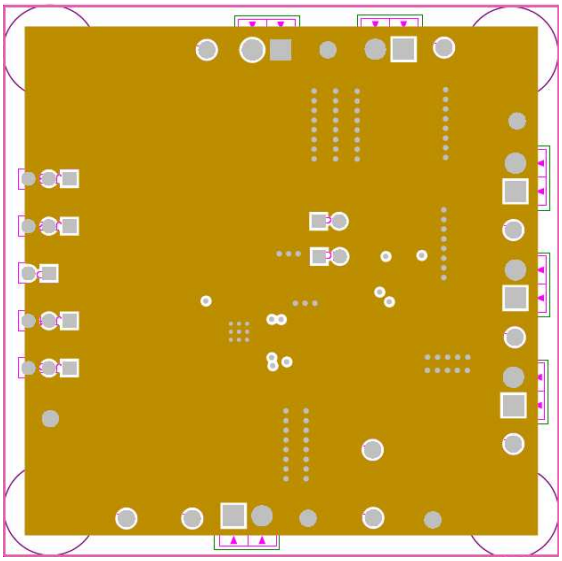


Figure 2. Middle (2nd) Layer, Solid Cu Ground

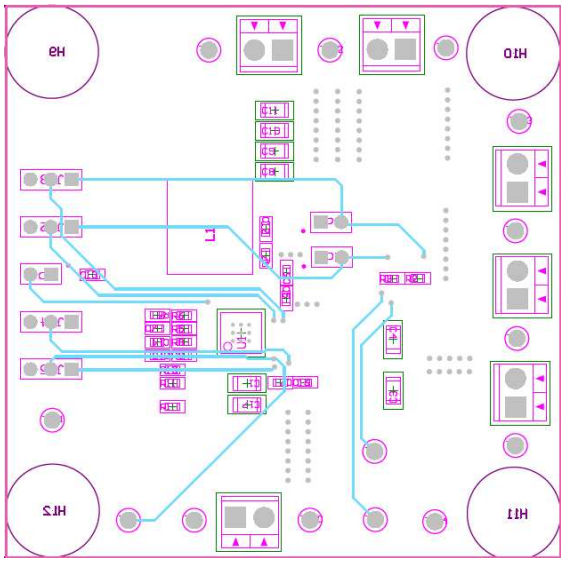


Figure 3. Mid (3rd) Layer

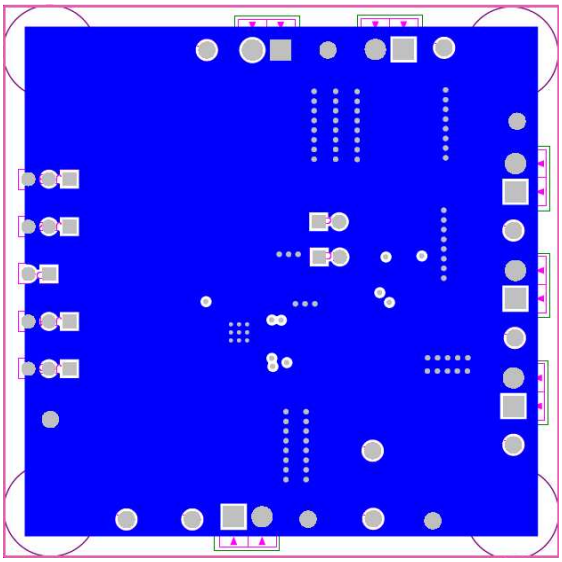
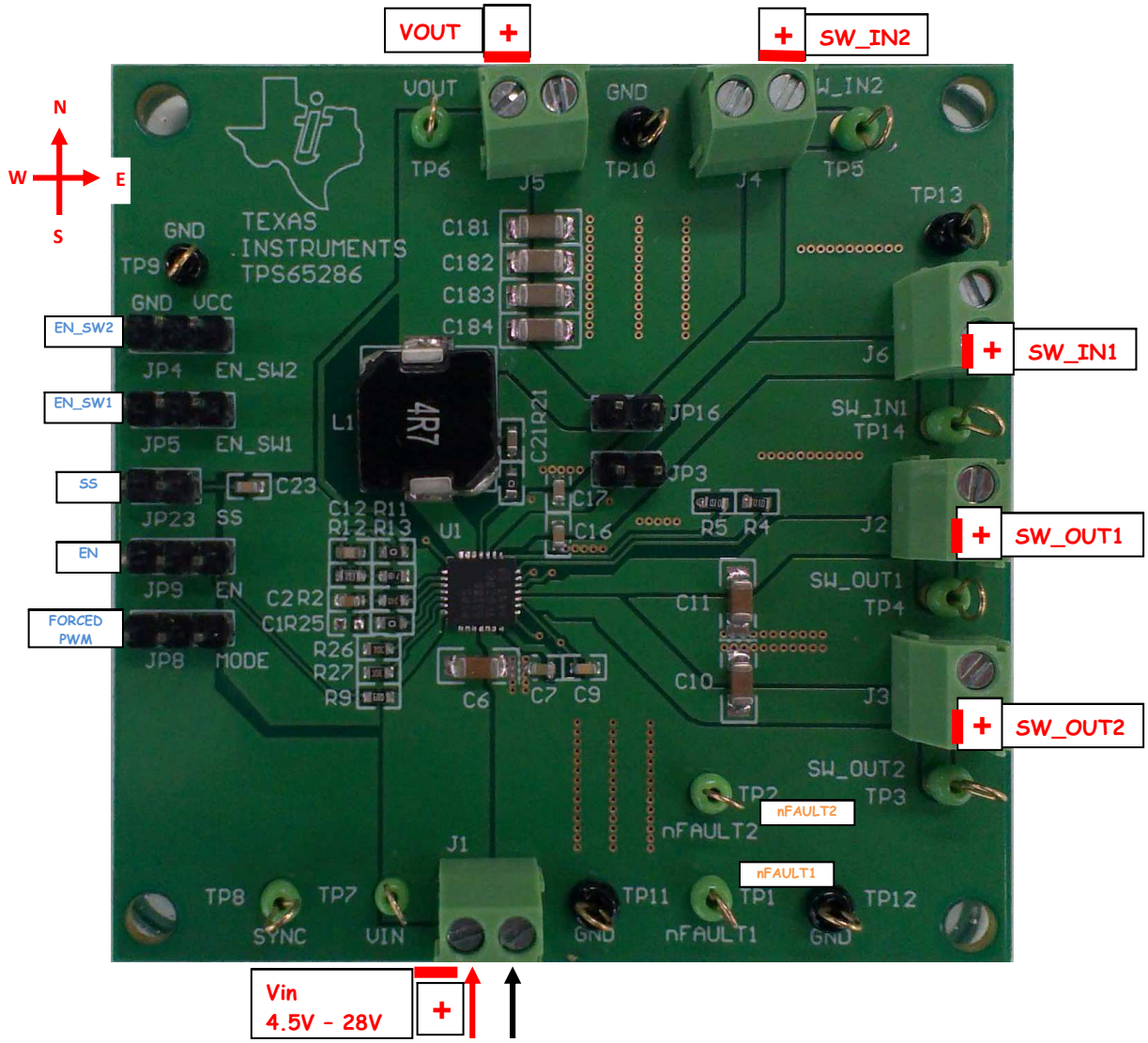


Figure 4. Bottom Layer

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4 Bench Test Setup Conditions

4.1 Headers Description and Jumper Placement



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4.2 Jumpers and Switches

No.	Function	LOC	Placement	Comment
JP1	SW_IN2 to SW_IN1	N	SW_IN1 pull to SW_IN2	Fit according to test requirement
JP2	Swtich1 enable (EN_SW1)	W	For automatic start-up fit jumper to SW_IN1. To disable SWITCH fit jumper to GND.	Fit according to test requirement
JP3	Swtich2 enable (EN_SW2)	W	For automatic start-up fit jumper to SW_IN2. To disable SWITCH fit jumper to GND.	Fit according to test requirement
JP8	BUCK enable (EN)	W	For immediate start-up fit jumper to V3V. For sequencing do not fit jumper. To disable converter fit jumper to GND.	Fit according to test requirement
JP5	Forced PWM (F_PWM)	W	For forced PWM operation fit jumper to V7V. For automatic PFM/PWM operation fit jumper to GND.	**Do not leave this header open. Use a jumper to set either forced PWM mode or automatic PFM/PWM mode.**
JP6	SS to external capacitor	W	SS pin connect to external capacitor	Fit according to test requirement
JP7	VOUT to SW_IN2	N	SW_IN2 pull to VOUT	Fit according to test requirement

4.3 Test Points and Placement

Buck converter outputs are white and have a label for easy location. Close to any of these test points there are black ground test points to allow for DVM measurement or to use a metal exposed scope probe to reduce common mode noise measurements. All test points are described in the following table:

TP	Name	Signal	Color
TP1	VIN	VIN	White
TP2	SYNC	Clock synchronization	White
TP3	SW_OUT2	Power switch2 output	White
TP4	SW_OUT1	Power switch1 output	White
TP5	nFAULT1	Power switch1 nFAULT signal indicator	White
TP6	nFAULT2	Power switch2 nFAULT signal indicator	White
TP7	SW_IN1	Power switch1 input	White
TP8	SW_IN2	Power switch2 input	White
TP9	VOUT	Output voltage Buck1	White
TP10	GND	GND	Black
TP11	GND	GND	Black
TP12	GND	GND	Black
TP13	GND	GND	Black
TP14	GND	GND	Blue

5 Power-Up Procedure

1. Define which converters are to be enabled or disabled by connecting jumpers to JP9 accordingly, or to wiring external drive signals to the ENx headers.
2. Define the strategy to enable the USB switches, either with jumpers or external drive signals to the USBENx pins
3. If nFAULTx signals are required connect JP1 and JP2 jumpers or wire the alarms pin to a pull-up supply
4. Connect loads to the output connectors.
5. Apply a DC voltage to header J1. Polarity is marked on the silk-screen.
6. To power the USB switches apply a DC voltage to J4 and J6. Enable the switches with JP4 and JP5. Check the outputs.

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6 Bill of Materials

Qty	Designator	Value	Footprint	Description	Comment
1	C1	100pF	603	CAP CERAMIC 100pF 25V X7R 0603	DNI
2	C21, C23	47nF	603	CAP CERAMIC 47pF 25V X7R 0603	
1	C9	4.7nF	603	CAP CERAMIC 4.7nF 25V X7R 0603	
1	C2	2.2nF	603	CAP CERAMIC 2.2nF 25V X7R 0603	
4	C181, C182, C183, C184	22uF	1206	CAP CERAMIC 22uF 16V X7R 1206	
1	C12	47pF	603	CAP CERAMIC 47pF 25V X7R 0603	
2	C10, C11	10uF	1206	CAP CERAMIC 10uF 25V X7R 1206	
1	C6	22uF	1206	CAP CERAMIC 22uF 35V X7R 1206	
3	C7, C16, C17	1uF	603	CAP CERAMIC 1uF 25V X7R 0603	
6	J1, J2, J3, J4, J5, J6	ED555/2DS		TERMINAL BLOCK 3.5MM 2POS PCB	
4	JP4, JP5, JP8, JP9	3 PIN	JMP0.3	CONN HEADER 50POS 0.100" SGL GOLD	
3	JP16, JP23, JP3	2 PIN	JMP0.2	CONN HEADER 50POS 0.100" SGL GOLD	
1	L1	4.7uH	IND4	Bourns power inductor	
1	R9	499K	603	RES 499K OHM 1/10W 5% 0603 SMD	
2	R4, R5	100K	603	RES 100K OHM 1/10W 5% 0603 SMD	
1	R2	10K	603	RES 10K OHM 1/10W 5% 0603 SMD	
2	R26, R27	20K	603	RES 20K OHM 1/10W 5% 0603 SMD	
3	R11, R21, R25	0	603	RES 0 OHM 1/10W 1% 0603 SMD	
1	R12	39K	603	RES 39K OHM 1/10W 1% 0603 SMD	
1	R13	5.3K	603	RES 5.3K OHM 1/10W 1% 0603 SMD	
9	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP14	Test Point White	TP	Glass Beaded Test Point	
5	TP9, TP10, TP11, TP12, TP13,	Test Point Black	TP	Glass Beaded Test Point	
1	U1	TPS65286	QFN-28		

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

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