TPS65251 4.5-V to 18-V Input, High-Current, Synchronous Step-Down Three Buck Switcher With Integrated FET

1 Features

- Wide Input Supply Voltage Range (4.5 to 18 V)
- 0.8 V, 1% Accuracy Reference
- Continuous Loading: 3 A (Buck 1), 2 A (Buck 2 and 3)
- Maximum Current: 3.5 A (Buck 1), 2.5 A (Buck 2 and 3)
- Adjustable Switching Frequency 300 kHz to 2.2 MHz Set by External Resistor
- Dedicated Enable for Each Buck
- External Synchronization Pin for Oscillator
- External Enable/Sequencing and Soft-Start Pins
- Adjustable Current Limit Set By External Resistor
- Soft-Start Pins
- Current-Mode Control With Simple Compensation Circuit
- Powergood
- Optional Low-Power Mode Operation for Light Loads
- VQFN Package, 40-Pin 6 mm × 6 mm RHA

2 Applications

- Set Top Boxes
- Blu-ray DVD
- DVR
- DTV
- Car Audio/Video
- Security Camera

3 Description

The TPS65251 features three synchronous wide input range high efficiency buck converters. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5-, 9-, 12- or 15-V systems and have integrated power transistors. The output voltage can be set externally using a resistor divider to any value between 0.8 V and close to the input supply. Each converter features enable pin that allows a delayed start-up for sequencing purposes, soft-start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIMx) pin that enables designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. The current mode control allows a simple RC compensation.

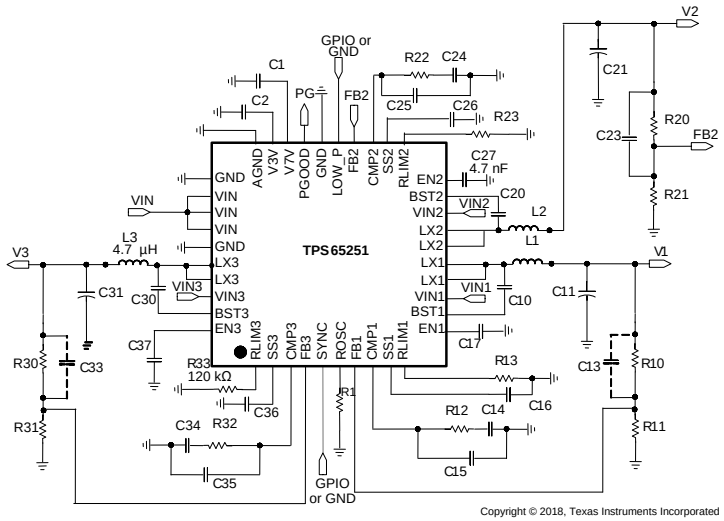
The switching frequency of the converters can either be set with an external resistor connected to ROSC pin or can be synchronized to an external clock connected to SYNC pin if needed. The switching regulators are designed to operate from 300 kHz to 2.2 MHz. 180° out of phase operation between Buck 1 and Buck 2, 3 (Buck 2 and 3 run in phase) minimizes the input filter requirements.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65251	VQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 2015) to Revision G **Page**

- Changed the values for Voltage at LX1, LX2, LX3 From: MIN = –1 V, MAX = 20 V To: MIN = –3 V, MAX = 23 V in the *Absolute Maximum Ratings* ... 5

Changes from Revision E (December 2014) to Revision F **Page**

- Changed the MAX value for Voltage at VIN1,VIN2, VIN3, LX1, LX2, LX3 From: 18 V To: 20 V in the *Absolute Maximum Ratings* ... 5
- Added *Community Resources* ... 27

Changes from Revision D (December 2012) to Revision E **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

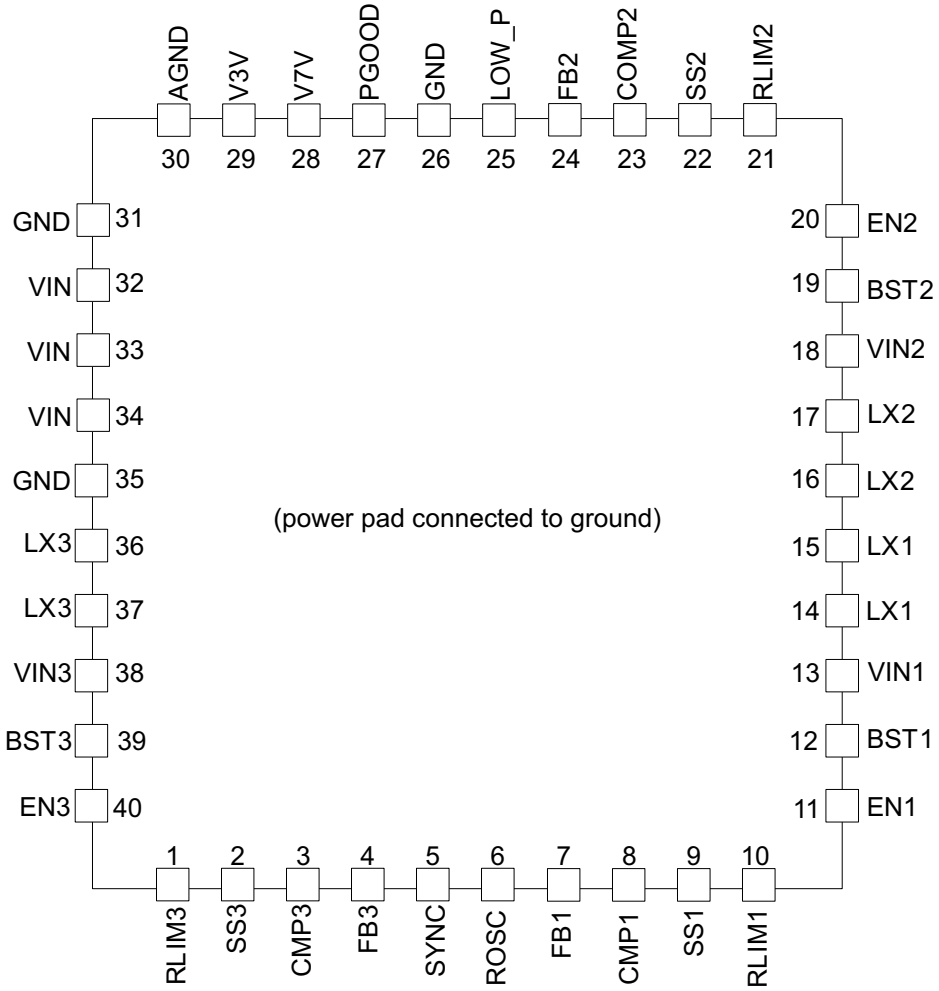
5 Description (continued)

TPS65251 features a supervisor circuit that monitors each converter output. The PGOOD pin is asserted once sequencing is done, all PG signals are reported and a selectable end of reset time lapses. The polarity of the PGOOD signal is active high.

TPS65251 also features a light load pulse skipping mode (PSM) by allowing the LOW_P pin tied to V3V. The PSM mode allows for a reduction on the input power supplied to the system when the host processor is in standby (low-activity) mode.

6 Pin Configuration and Functions

RHA Package
40-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
RLIM3	1	I	Current limit setting for Buck 3. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS3	2	I	Soft-start pin for Buck 3. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
COMP3	3	O	Compensation for Buck 3. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB3	4	I	Feedback input for Buck 3. Connect a divider set to 0.8V from the output of the converter to ground.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SYNC	5	I	Synchronous clock input. If there is a sync clock in the system, connect to the pin. When not used connect to GND.
ROSC	6	I	Oscillator set. This resistor sets the frequency of internal autonomous clock. If external synchronization is used resistor should be fitted and set to about 70% of external clock frequency.
FB1	7	I	Feedback pin for Buck 1. Connect a divider set to 0.8 V from the output of the converter to ground.
COMP1	8	O	Compensation pin for Buck 1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
SS1	9	I	Soft-start pin for Buck 1. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
RLIM1	10	I	Current limit setting pin for Buck 1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
EN1	11	I	Enable pin for Buck 1. A low level signal on this pin disables it. If pin is left open a weak internal pullup to V3V will allow for automatic enable. For a delayed start-up add a small ceramic capacitor from this pin to ground.
BST1	12	I	Bootstrap capacitor for Buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
VIN1	13	I	Input supply for Buck 1. Fit a 10-µF ceramic capacitor close to this pin.
LX1	14	O	Switching node for Buck 1
	15		
LX2	16	O	Switching node for Buck 2
	17		
VIN2	18	I	Input supply for Buck 2. Fit a 10-µF ceramic capacitor close to this pin.
BST2	19	I	Bootstrap capacitor for Buck 2. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN2	20	I	Enable pin for Buck 2. A low level signal on this pin disables it. If pin is left open a weak internal pullup to V3V will allow for automatic enable. For a delayed start-up add a small ceramic capacitor from this pin to ground.
RLIM2	21	I	Current limit setting for Buck 2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS2	22	I	Soft-start pin for Buck 2. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
COMP2	23	O	Compensation pin for Buck 2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter
FB2	24	I	Feedback input for Buck 2. Connect a divider set to 0.8 V from the output of the converter to ground.
LOW_P	25	I	Low-power operation mode (active high) input for TPS65251
GND	26		Ground pin
PGOOD	27	O	Powergood. Open-drain output asserted after all converters are sequenced and within regulation. Polarity is factory selectable (active high default).
V7V	28	O	Internal supply. Connect a 10-µF ceramic capacitor from this pin to ground.
V3V	29	O	Internal supply. Connect a 3.3-µF to 10-µF ceramic capacitor from this pin to ground.
AGND	30		Analog ground. Connect all GND pins and the power pad together.
GND	31		Ground pin
VIN	32	I	Input supply
VIN	33	I	Input supply
VIN	34	I	Input supply
GND	35		Ground pin
LX3	36	O	Switching node for Buck 3
	37		
VIN3	38		Input supply for Buck 3. Fit a 10-µF ceramic capacitor close to this pin.
BST3	39	I	Bootstrap capacitor for Buck 3. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN3	40	I	Enable pin for Buck 3. A low level signal on this pin disables it. If pin is left open a weak internal pullup to V3V will allow for automatic enable. For a delayed start-up add a small ceramic capacitor from this pin to ground.
PAD	—	—	Power pad. Connect to ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Voltage at VIN1,VIN2, VIN3, LX1, LX2, LX3	–0.3	20	V
	Voltage at LX1, LX2, LX3 (maximum withstand voltage transient < 10 ns)	–3	23	V
	Voltage at BST1, BST2, BST3, referenced to Lx pin	–0.3	7	V
	Voltage at V7V, COMP1, COMP2, COMP3	–0.3	7	V
	Voltage at V3V, RLIM1, RLIM2, RLIM3, EN1,EN2,EN3, SS1, SS2,SS3, FB1, FB2, FB3, PGOOD, SYNC, ROSC, LOW_P	–0.3	3.6	V
	Voltage at AGND, GND	–0.3	0.3	V
T_J	Operating virtual junction temperature	–40	125	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VIN	Input operating voltage	4.5	18	V
T_J	Junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS65251 RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to 125°C, VIN = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE						
V_{IN}	Input Voltage range		4.5		18	V
IDD_{SDN}	Shutdown	EN pin = low for all converters		1.3		mA
IDD_Q	Quiescent, low-power disabled (Lo)	Converters enabled, no load Buck 1 = 3.3 V, Buck 2 = 2.5 V, Buck 3 = 7.5 V, L = 4.7 µH , f_{SW} = 800 kHz		20		mA
$IDD_{Q\_LOW\_P}$	Quiescent, low-power enabled (Hi)	Converters enabled, no load Buck 1 = 3.3 V, Buck 2 = 2.5 V, Buck 3 = 7.5 V, L = 4.7 µH , f_{SW} = 800 kHz		1.5		mA
$UVLO_{VIN}$	V_{IN} under voltage lockout	Rising V_{IN}		4.22		V
		Falling V_{IN}		4.1		
$UVLO_{DEGLITCH}$		Both edges		110		µs
V_{3V}	Internal biasing supply	I_{LOAD} = 0 mA	3.2	3.3	3.4	V
I_{3V}	Biasing supply output current	V_{IN} = 12 V			10	mA
V_{7V}	Internal biasing supply	I_{LOAD} = 0 mA	5.63	6.25	6.88	V
I_{7V}	Biasing supply output current	V_{IN} = 12 V			10	mA
$V7V_{UVLO}$	UVLO for internal V7V rail	Rising V7V		3.8		V
		Falling V7V		3.6		
$V7V_{UVLO\_DEGLITCH}$		Falling edge		110		µs
BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT-START, SWITCHING FREQUENCY AND SYNC CIRCUIT, LOW-POWER MODE)						
V_{IH}	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENX} rising	1.55		1.82	V
	Enable high level	External GPIO, V_{ENX} rising	0.66 x V_{3V}			
V_{IL}	Enable threshold low	V3p3 = 3.2 V - 3.4 V, V_{ENX} falling	0.98		1.24	V
	Enable low level	External GPIO, V_{ENX} falling			0.33 x V_{3V}	
R_{EN_DIS}	Enable discharge resistor		–10%	2.1	10%	kΩ
ICH_{EN}	Pullup current enable pin			1.1		µA
t_D	Discharge time enable pins	Power-up		10		ms
I_{SS}	Soft-start pin current source			5		µA
F_{SW_BK}	Converter switching frequency range	Set externally with resistor	0.3		2.2	MHz
R_{FSW}	Frequency setting resistor	Depending on set frequency	50		600	kΩ
f_{SW_TOL}	Internal oscillator accuracy	f_{SW} = 800 kHz	–10%		10%	
V_{SYNCH}	External clock threshold high	V3p3 = 3.3 V	1.55			V
V_{SYNCL}	External clock threshold Low	V3p3 = 3.3 V			1.24	V
$SYNC_{RANGE}$	Synchronization range		0.2		2.2	MHz
$SYNC_{CLK\_MIN}$	Sync signal minimum duty cycle		40%			
$SYNC_{CLK\_MAX}$	Sync signal maximum duty cycle				60%	
VIH_{LOW_P}	Low-power mode threshold high	V3p3 = 3.3 V, V_{ENX} rising	1.55			V
VIL_{LOW_P}	Low-power mode threshold Low	V3p3 = 3.3 V, V_{ENX} falling	0.98		1.24	V
FEEDBACK, REGULATION, OUTPUT STAGE						
V_{FB}	Feedback voltage	V_{IN} = 12V T_J = 25°C	–1%	0.8	1%	V
		V_{IN} = 4.5 to 18 V	–2%	0.8	2%	
I_{FB}	Feedback leakage current				50	nA
t_{ON_MIN}	Minimum on-time (current sense blanking)			80	120	ns
$V_{LINEREG}$	Line regulation - DC $\Delta V_{OUT}/\Delta V_{INB}$	V_{INB} = 4.5 to 18 V, I_{OUT} = 1000 mA		0.5		% V_{OUT}
$V_{LOADREG}$	Load regulation - DC $\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 % - 90% $I_{OUT,MAX}$		0.5		% V_{OUT}/A
MOSFET (BUCK 1)						
H.S. Switch	Turn-On resistance high-side FET on CH1	V_{IN} = 12 V, T_J = 25°C		95		mΩ
L.S. Switch	Turn-On resistance low-side FET on CH1	V_{IN} = 12 V, T_J = 25°C		50		mΩ

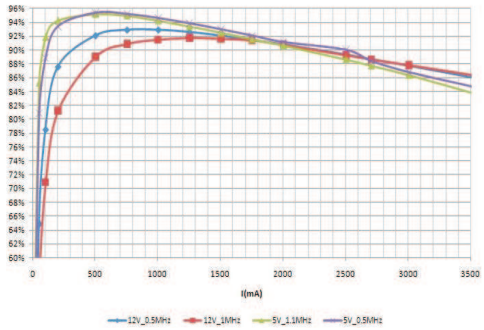
Electrical Characteristics (continued)

T_J = –40°C to 125°C, VIN = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET (BUCK 2)						
H.S. Switch	Turn-On resistance high-side FET on CH2	V_{IN} = 12 V, T_J = 25°C		120		mΩ
L.S. Switch	Turn-On resistance low-side FET on CH2	V_{IN} = 12 V, T_J = 25°C		80		mΩ
MOSFET (BUCK 3)						
H.S. Switch	Turn-On resistance high-side FET on CH3	V_{IN} = 12 V, T_J = 25°C		120		mΩ
L.S. Switch	Turn-On resistance low-side FET on CH3	V_{IN} = 12 V, T_J = 25°C		80		mΩ
ERROR AMPLIFIER						
g_M	Error amplifier transconductance	–2 µA < I_{COMP} < 2 µA		130		µS
gm_{PS}	COMP to ILX g_M	ILX = 0.5 A		10		A/V
POWERGOOD RESET GENERATOR						
VUV_{BUCKX}	Threshold voltage for buck under voltage	Output falling (device will be disabled after t_{ON_HICCUP})		85%		
		Output rising (PG will be asserted)		90%		
$t_{UV\_deglitch}$	Deglitch time (both edges)	Each buck		11		ms
t_{ON_HICCUP}	Hiccup mode ON time	VUV_{BUCKX} asserted		12		ms
t_{OFF_HICCUP}	Hiccup mode OFF time before restart is attempted	All converters disabled. Once t_{OFF_HICCUP} elapses, all converters will go through sequencing again.		15		ms
VOV_{BUCKX}	Threshold voltage for buck overvoltage	Output rising (high-side FET will be forced off)		109%		
		Output falling (high-side FET will be allowed to switch)		107%		
t_{RP}	Minimum reset period	Measured after minimum reset period of all bucks power-up successfully		1		s
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shutdown trip point	Rising temperature		160		°C
T_{HYST}	Thermal shutdown hysteresis	Device restarts		20		°C
$T_{TRIP\_DEGLITCH}$	Thermal shutdown deglitch			110		µs
CURRENT LIMIT PROTECTION						
$RLIM_1$	Limit resistance range Buck 1		75		300	kΩ
$RLIM_{2\&3}$	Limit resistance range Bucks 2 and 3		100		300	kΩ
$ILIM_1$	Buck 1 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 17	1.2		5.5	A
$ILIM_2$	Buck 2 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 18	1		4.1	A
$ILIM_3$	Buck 3 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 19	1.3		4.4	A

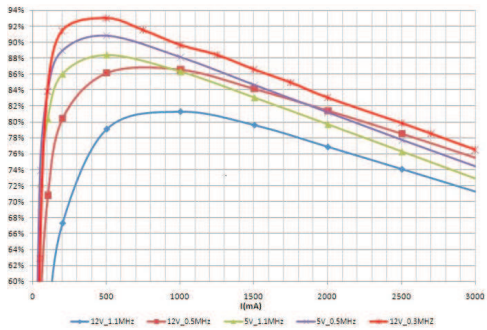
7.6 Typical Characteristics

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)



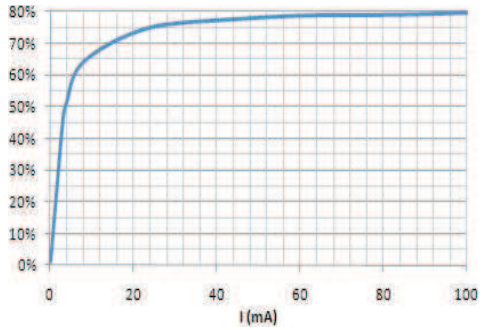
f_{SW} = 500 kHz, V_{OUT} = 3.3 V, L= 4.7 µH, DCR = 28 mΩ

Figure 1. BUCK1 Efficiency



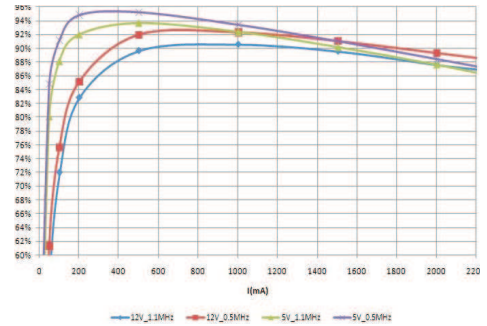
f_{SW} = 500 kHz, V_{OUT} = 1.2 V, L = 4.7 µH, DCR = 28 mΩ

Figure 2. BUCK1 Efficiency



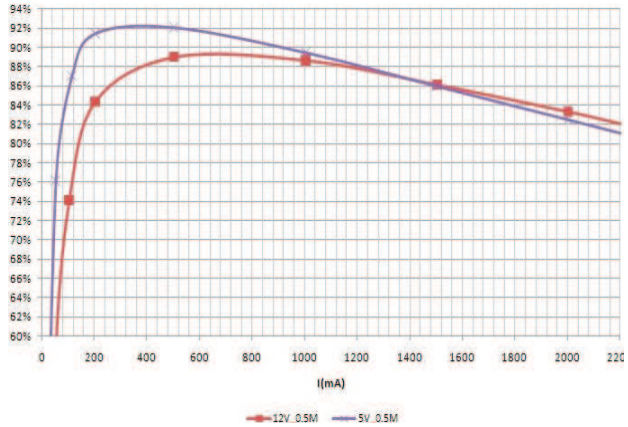
C_O = 22 µF, V_{OUT} = 3.3 V, L = 4.7 µH

Figure 3. BUCK1 Efficiency Low-Power Enabled



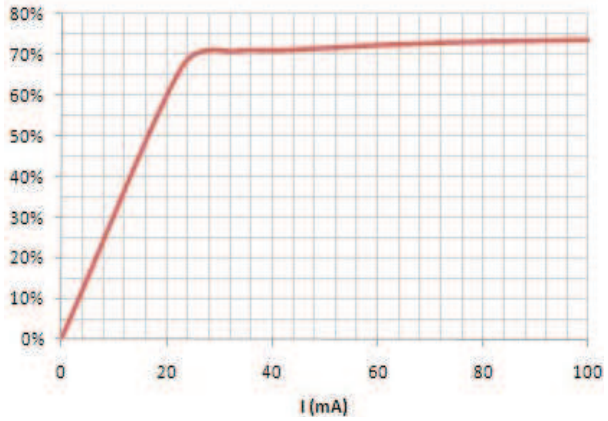
f_{SW} = 500 kHz, V_{OUT} = 3.3 V, L = 4.7 µH, DCR = 28 mΩ
(Also Applies to Buck 3)

Figure 4. BUCK2 Efficiency



f_{SW} = 500 kHz, V_{OUT} = 1.8 V, L = 4.7 µH, DCR = 28 mΩ
(Also Applies to Buck 3)

Figure 5. BUCK2 Efficiency

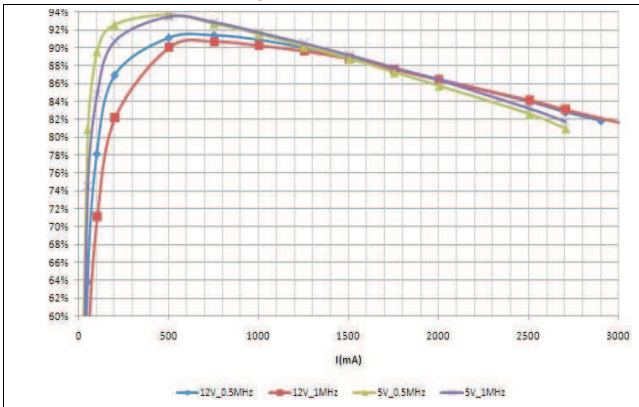


V_{OUT} = 2.5 V, L = 4.7 µF

Figure 6. BUCK2 Efficiency Low-Power Enabled

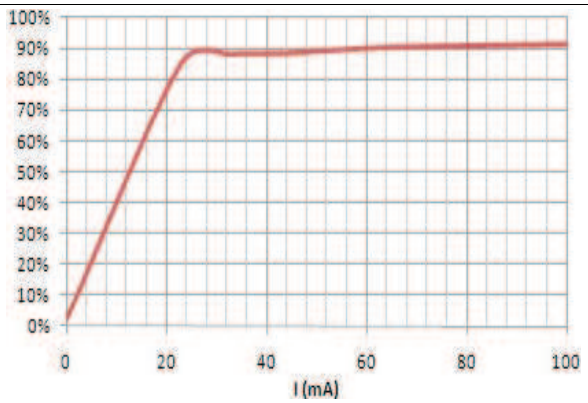
Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)



V_{OUT} = 2.5 V, L = 4.7 µH, DCR = 28 mΩ
(Also Applies to Buck 2)

Figure 7. BUCK3 Efficiency



V_{OUT} = 2.5 V, L = 4.7 µF

Figure 8. BUCK3 Efficiency Low-Power Enabled

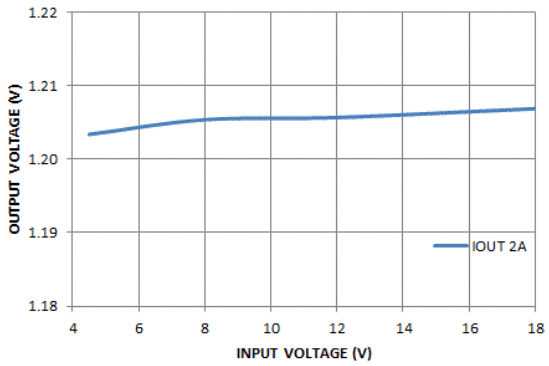


Figure 9. BUCK1 Line Regulation

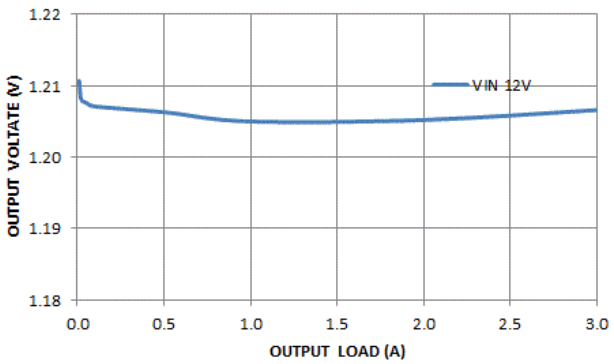


Figure 10. BUCK1 Load Regulation

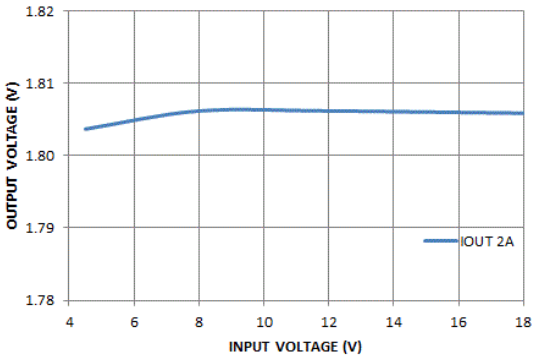


Figure 11. BUCK2 Line Regulation

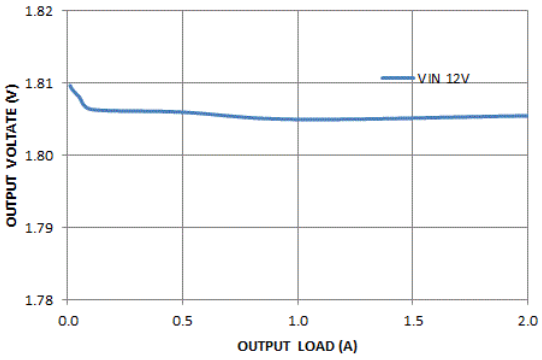


Figure 12. BUCK2 Load Regulation

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

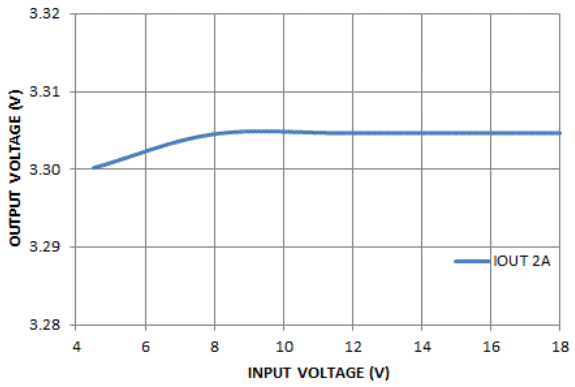


Figure 13. BUCK3 Line Regulation

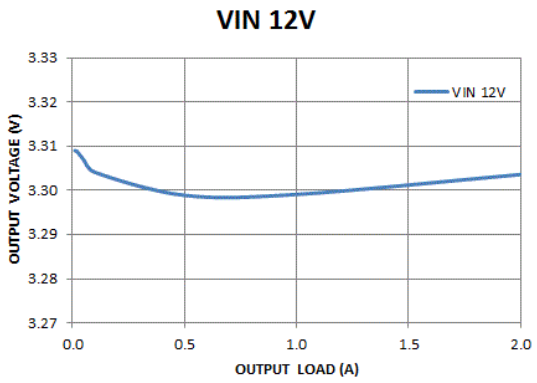


Figure 14. BUCK3 Load Regulation

8 Detailed Description

8.1 Overview

TPS65251 is a power management IC with three step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. TPS65251 can support 4.5-V to 18-V input supply, high load current, 300-kHz to 2.2-MHz clocking. The buck converters have an optional PSM mode, which can improve power dissipation during light loads. Alternatively, the device implements a constant frequency mode by connecting the LOW_P pin to ground. The wide switching frequency of 300 kHz to 2.2 MHz allows for efficiency and size optimization. The switching frequency is adjustable by selecting a resistor to ground on the ROSC pin. The SYNC pin also provides a means to synchronize the power converter to an external signal. Input ripple is reduced by 180 degree out-of-phase operation between Buck 1 and Buck 2. Buck 3 operates in phase with Buck 2.

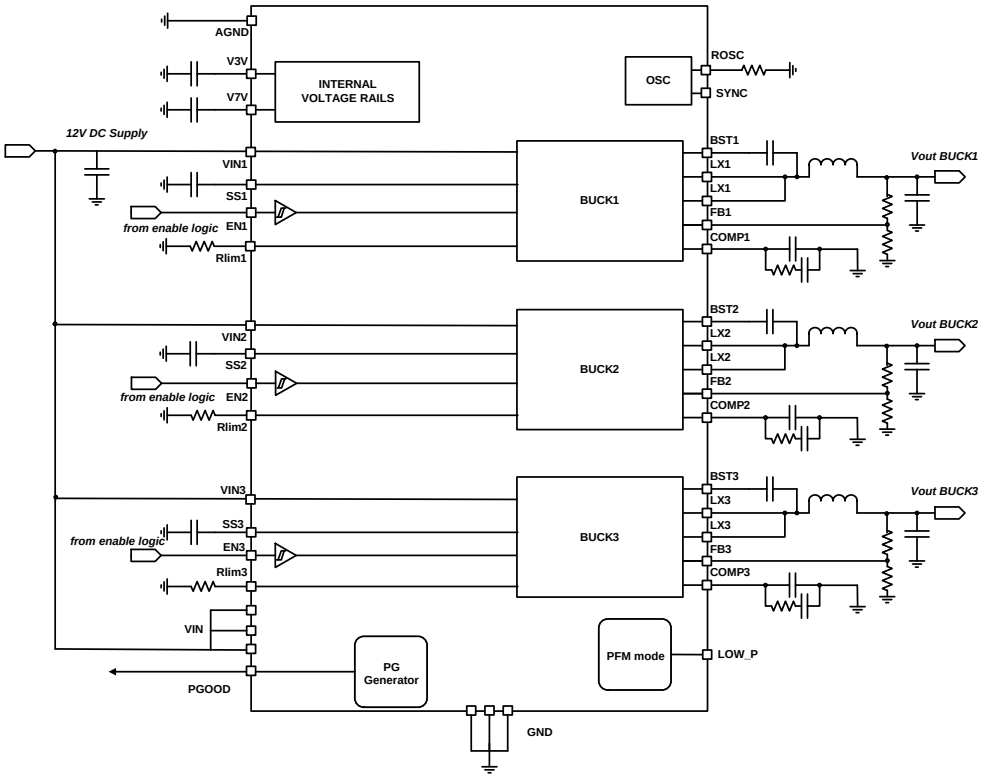
All three buck converters have peak current mode control which simplifies external frequency compensation. A traditional type II compensation network can stabilize the system and achieve fast transient response. Moreover, an optional capacitor in parallel with the upper resistor of the feedback divider provides one more zero and makes the crossover frequency over 100 kHz.

Each buck converter has an individual current limit, which can be set up by a resistor to ground from the RLIM pin. The adjustable current limiting enables high efficiency design with smaller and less expensive inductors.

The device has two built-in LDO regulators. During a standby mode, the 3.3-V LDO and the 6.5-V LDO can be used to drive MCU and other active loads. By this, the system is able to turn off the three buck converters and improve the standby efficiency.

The device has a powergood comparator monitoring the output voltage. Each converter has its own soft-start and enable pins, which provide independent control and programmable soft-start.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjustable Switching Frequency

To select the internal switching frequency connect a resistor from ROSC to ground. Figure 15 shows the required resistance for a given switching frequency.

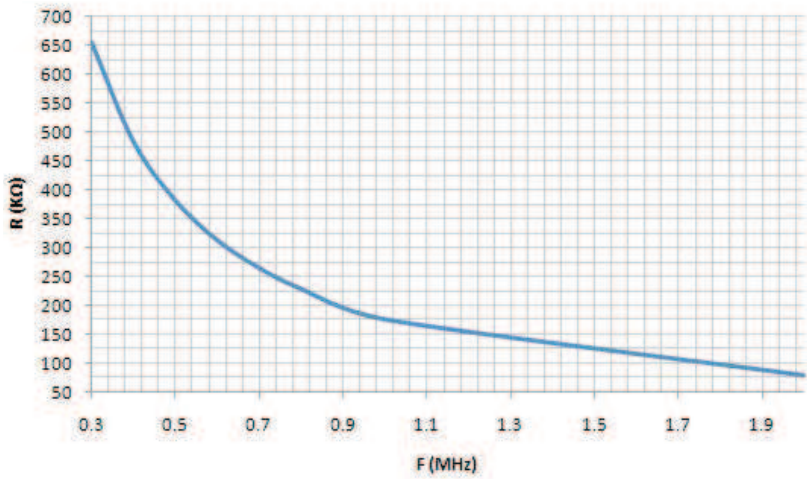


Figure 15. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 174 \times f(MHz)^{-1.122} \quad (1)$$

For operation at 800 kHz a 230-kΩ resistor is required.

8.3.2 Synchronization

The status of the SYNC pin will be ignored during start-up and the TPS65251's control will only synchronize to an external signal after the PGOOD signal is asserted. The status of the SYNC pin will be ignored during start-up and the TPS65251 will only synchronize to an external clock if the PGOOD signal is asserted. When synchronization is applied, the PWM oscillator frequency must be lower than the sync pulse frequency to allow the external signal trumping the oscillator pulse reliably. When synchronization is not applied, the SYNC pin should be connected to ground.

8.3.3 Out-of-Phase Operation

Buck 1 has a low conduction resistance compared to Buck 2 and 3. Normally Buck 1 is used to drive higher system loads. Buck 2 and 3 are used to drive some peripheral loads like I/O and line drivers . The combination of loads from Buck 2 and 3 may be on par with the load of Buck 1. To reduce input ripple current, Buck 2 operates in phase with Buck 3; Buck 1 and Buck 2 operate 180° out-of-phase. This enables the system, having less input ripple, to lower component cost, save board space and reduce EMI.

8.3.4 Delayed Start-Up

If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is about 1.67 ms per nF connected to the pin. Note that the EN pins have a weak 1-µA pullup to the 3V3 rail.

8.3.5 Soft-Start Time

The device has an internal pullup current source of 5 µA that charges an external slow start capacitor to implement a slow start time. Equation 2 shows how to select a slow start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8 V and the slow start charge current (I_{SS}) is 5 µA. The soft-start circuit requires 1 nF per 200 µS to be connected at the SS pin. A 1-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant pins.

Feature Description (continued)

$$t_{SS}\ (ms) = V_{REF}\ (V) \times \left(\frac{C_{SS}\ (nF)}{I_{SS}\ (\mu A)} \right) \quad (2)$$

8.3.6 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with 40.2 kΩ for the R1 resistor and use the Equation 3 to calculate R2.

$$R2 = R1 \times \left(\frac{0.8\ V}{V_O - 0.8\ V} \right) \quad (3)$$

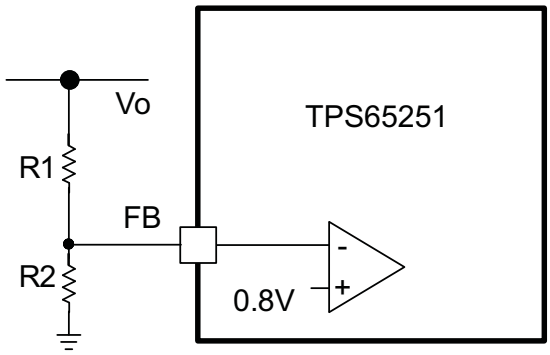


Figure 16. Voltage Divider Circuit

8.3.7 Input Capacitor

Use 10-µF X7R/X5R ceramic capacitors at the input of the converter inputs. These capacitors should be connected as close as physically possible to the input pins of the converters.

8.3.8 Bootstrap Capacitor

The device has three integrated boot regulators and requires a small ceramic capacitor between the BST and LX pin to provide the gate drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.047 µF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

8.3.9 Error Amplifier

The device has a transconductance error amplifier. The frequency compensation network is connected between the COMP pin and ground.

8.3.10 Loop Compensation

TPS65251 is a current mode control DC - DC converter. The error amplifier is a transconductance amplifier with a of 130 µA/V.

8.3.11 Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent subharmonic oscillations in peak current mode control.

8.3.12 Powergood

The PGOOD pin is an open-drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when all three buck converters' outputs are more than 90% of its nominal output voltage and reset time of 1 second elapses. The polarity of the PGOOD is active high.

Feature Description (continued)

8.3.13 Current Limit Protection

Figure 17 shows the (peak) inductor current limit for Buck 1. The typical limit can be approximated with the following graph.

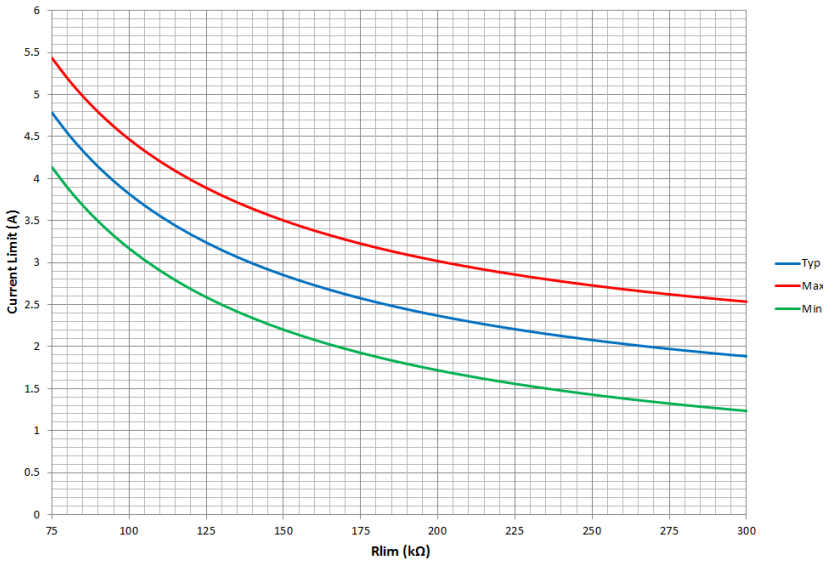


Figure 17. Buck 1

Figure 18 shows the (peak) inductor current limit for Buck 2. The typical limit can be approximated with the following graph.

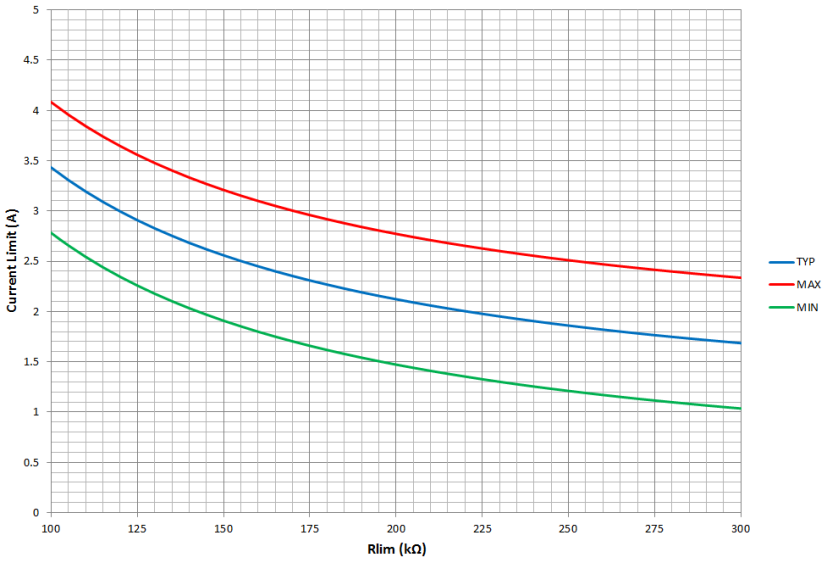


Figure 18. Buck 2

Figure 19 shows the (peak) inductor current limit for Buck 3. The typical limit can be approximated with the following graph.

Feature Description (continued)

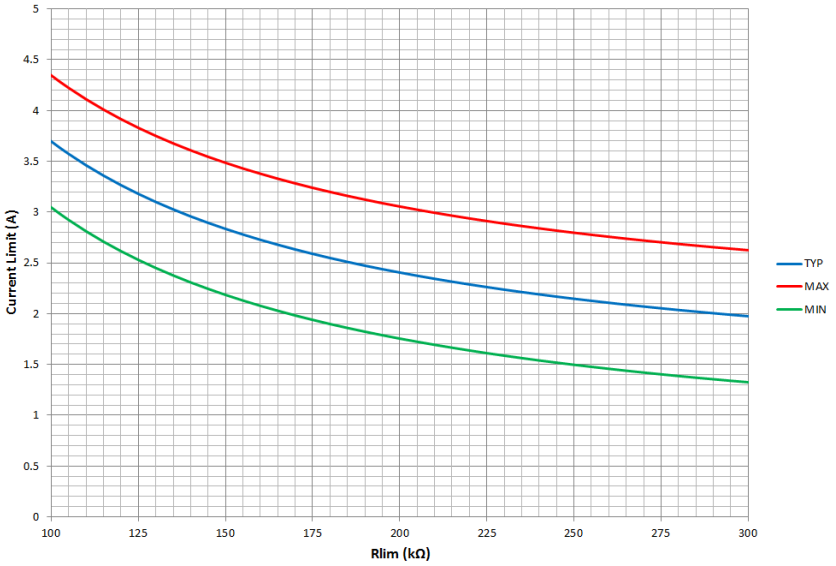


Figure 19. Buck 3

All converters operate in hiccup mode: Once an over-current lasting more than 10 ms is sensed in any of the converters, all the converters will shut down for 10 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

If an overload condition lasts for less than 10 ms, only the relevant converter affected will go into and out of under-voltage and no global hiccup mode will occur. The converter will be protected by the cycle-by-cycle current limit during that time.

8.3.14 Overvoltage Transient Protection

The device incorporates an overvoltage transient protection (OVP) circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVP threshold, the high-side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops below the lower OVP threshold which is 107%, the high-side MOSFET is allowed to turn on the next clock cycle.

8.3.15 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power-up sequence. The thermal shutdown hysteresis is 20°C.

8.4 Device Functional Modes

8.4.1 Low-Power Mode Operation

By pulling the LOW_P pin high all converters will operate in pulse-skipping mode, greatly reducing the overall power consumption at light and no load conditions. Although each buck converter has a skip comparator that makes sure regulation is not lost when a heavy load is applied and low-power mode is enabled, system design needs to make sure that the LP pin is pulled low for continuous loading in excess of 100 mA.

When low-power is implemented, the peak inductor current used to charge the output capacitor is:

Device Functional Modes (continued)

$$I_{LIMIT} = 0.25 \bullet T_{SLEEP\_CLK} \bullet \frac{V_{IN} - V_{OUT}}{L} \quad (4)$$

Where T_{SLEEP_CLK} is half of the converter switching period, $2/f_{SW}$.

The size of the additional ripple added to the output is:

$$\Delta V_{OUT} = \frac{1}{C} \bullet \left(\frac{L \bullet I_{LIMIT}^{2}}{2} \bullet \frac{V_{IN}}{V_{OUT} \bullet (V_{IN} - V_{OUT})} - \frac{I_{LOAD}}{f_{SLEEP\_CLK}} \right) \quad (5)$$

And the peak output voltage during low-power operation is:

$$V_{OUT\_PK} = V_{OUT} + \frac{\Delta V_{OUT}}{2} \quad (6)$$

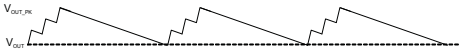


Figure 20. Peak Output Voltage During Low-Power Operation

9 Application and Implementation

NOTE

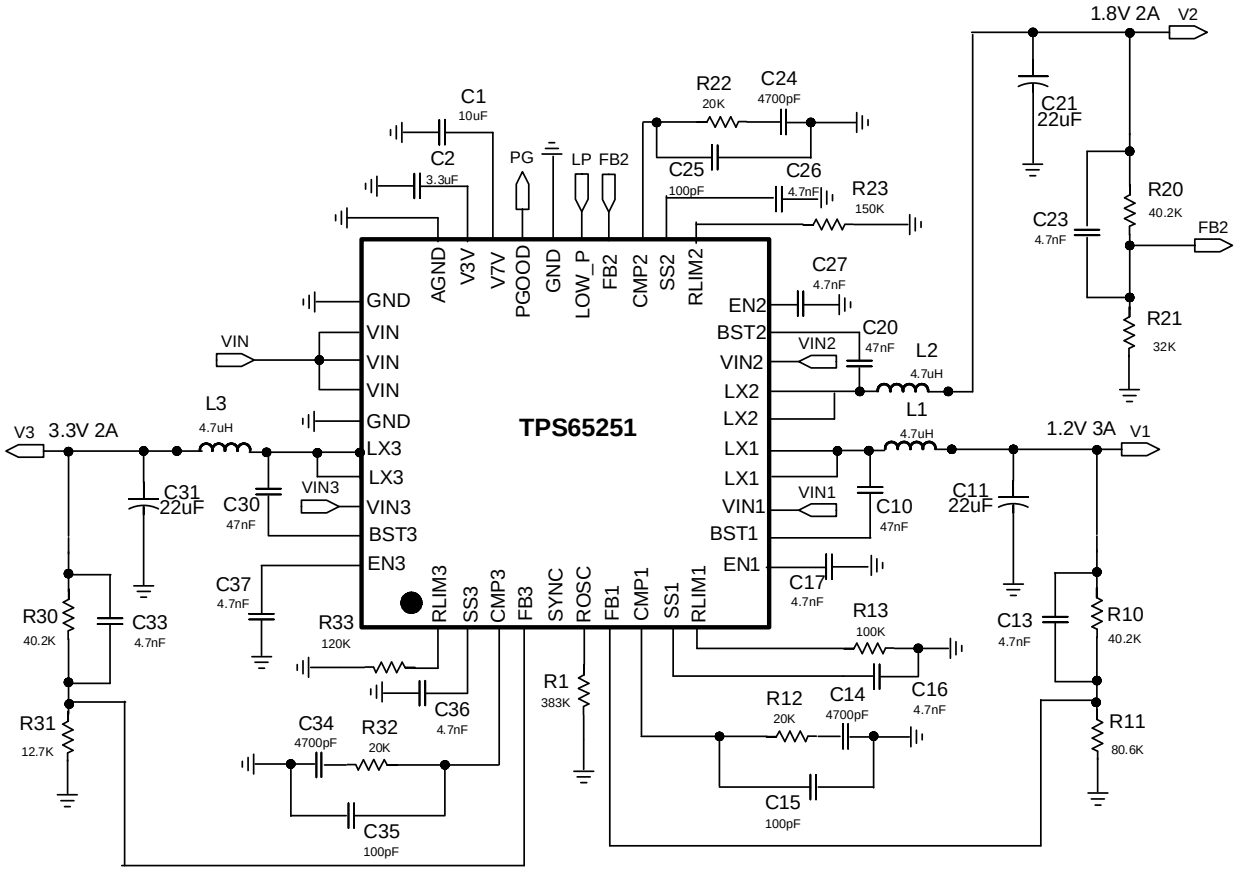
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is triple synchronous step down dc/dc converter. It is typically used to convert a higher dc voltage to lower dc voltages with continuous available output current of 3A/2A/2A.

9.2 Typical Application

The following design procedure can be used to select component values for the TPS65251.



A. VIN pins require local decoupling capacitors.

Figure 21. Typical Application Circuit

9.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Output voltage	1.2 V
Transient response 0.5-A to 2-A load step	120 mV
Maximum output current	3 A

DESIGN PARAMETERS	VALUE
Input voltage	12 V nom, 9.6 V to 14.4 V
Output voltage ripple	< 30 mV p-p
Switching frequency	500 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Loop Compensation Circuit

A typical compensation circuit could be type II (R_c and C_c) to have a phase margin between 60 and 90 degrees, or type III (R_c, C_c and C_{ff}) to improve the converter transient response. C_{Roll} adds a high frequency pole to attenuate high-frequency noise when needed. It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

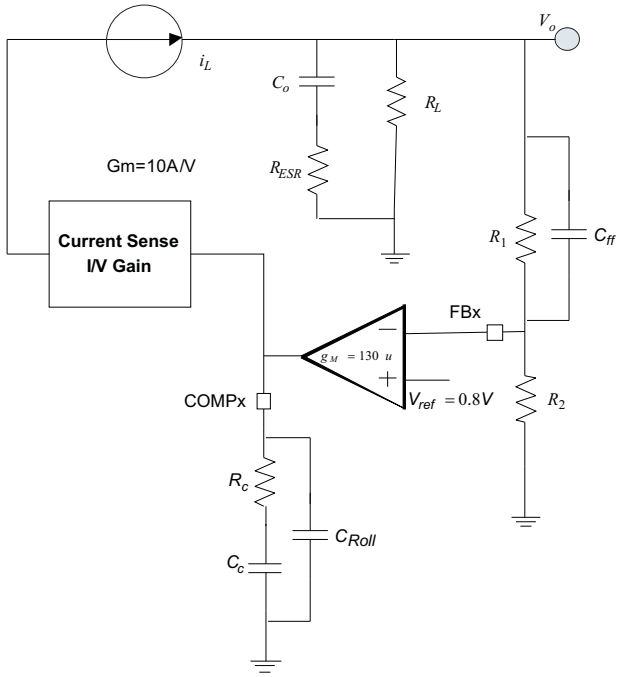


Figure 22. Loop Compensation

To calculate the external compensation components use Table 1:

Table 1. Design Guideline for the Loop Compensation

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies between 500 kHz and 1 MHz give best trade off between performance and cost. When using smaller L and Cs, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Type III circuit recommended for switching frequencies higher than 500 kHz.
Select cross over frequency (fc) to be less than 1/5 to 1/10 of switching frequency.	Suggested fc = fs/10	Suggested fc = fs/10
Set and calculate R_c.	$R_C = \frac{2\pi \times f_c \times V_O \times C_O}{g_M \times Vref \times gm_{ps}}$ (7)	$R_C = \frac{2\pi \times f_c \times C_O}{g_M \times gm_{ps}}$ (8)

Table 1. Design Guideline for the Loop Compensation (continued)

	TYPE II CIRCUIT	TYPE III CIRCUIT
Calculate C_c by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_O \times R_L \times 2\pi}$ (9)	$C_c = \frac{R_L \times Co}{R_c}$ (10)	$C_c = \frac{R_L \times Co}{R_c}$ (11)
Add C_{Roll} if needed to remove large signal coupling to high impedance COMP node. Make sure that $fp_{Roll} = \frac{1}{2 \times \pi \times R_C \times C_{Roll}}$ (12) is at least twice the cross over frequency.	$C_{Roll} = \frac{Re_{sr} \times C_O}{R_C}$ (13)	$C_{Roll} = \frac{Re_{sr} \times C_O}{R_C}$ (14)
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff} is smaller than soft-start equivalent frequency ($1/T_{ss}$).	NA	$C_{ff} = \frac{1}{2 \times \pi \times fz_{ff} \times R_1}$ (15)

9.2.2.2 Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, you will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the converter's performance. The converter is capable of running from 300 kHz to 2.2 MHz. Unless a small solution size is an ultimate goal, a moderate switching frequency of 500 kHz is selected to achieve both a small solution size and a high efficiency operation. Using Figure 15, R1 is determined to be 383 kΩ

9.2.2.3 Output Inductor Selection

To calculate the value of the output inductor, use Equation 16. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, KIND is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use KIND = 0.2 and the inductor value is calculated to be 3.6 µH. For this design, a nearest standard value was chosen: 4.7 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 17 and Equation 18.

$$Lo = \frac{Vin - Vout}{Io \times K_{ind}} \times \frac{Vout}{Vin \times fsw} \quad (16)$$

$$Iripple = \frac{Vin - Vout}{Lo} \times \frac{Vout}{Vin \times fsw} \quad (17)$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times Lo \times fsw} \right)^2} \quad (18)$$

$$ILpeak = Iout + \frac{Iripple}{2} \quad (19)$$

9.2.2.4 Output Capacitor

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements.

Equation 20 gives the minimum output capacitance to meet the transient specification. For this example, L_O = 4.7 µH, ΔI_{OUT} = 1.5 A – 0.75 A = 0.75 A and ΔV_{OUT} = 120 mV. Using these numbers gives a minimum capacitance of 18 µF. A standard 22-µF ceramic capacitor is chose in the design.

$$Co > \frac{\Delta I_{OUT}^2 \times L_o}{V_{out} \times \Delta Vout} \quad (20)$$

Equation 21 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. In this case, the maximum output voltage ripple is 30 mV. From Equation 17, the output current ripple is 0.46 A. From Equation 21, the minimum output capacitance meeting the output voltage ripple requirement is 1.74 µF.

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Vripple}{Iripple}} \tag{21}$$

Additional capacitance de-rating for aging, temperature and DC bias should influence this minimum value. For this example, one 22-µF, 6.3-V X7R ceramic capacitor with 3 mΩ of ESR will be used.

9.2.2.5 Input Capacitor

A minimum 10-µF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND. These capacitors should be connected as close as physically possible to the input pins of the converters as they handle the RMS ripple current shown in Equation 22. For this example, I_{OUT} = 3 A, V_{OUT} = 1.2 V, V_{INmin} = 9.6 V, from Equation 22, the input capacitors must support a ripple current of 0.99 A RMS.

$$Icirms = Iout \times \sqrt{\frac{Vout}{Vinmin} \times \frac{(Vinmin - Vout)}{Vinmin}} \tag{22}$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 23. Using the design example values, I_{OUTmax} = 3 A, C_{IN} = 10 µF, f_{SW} = 500 kHz, yields an input voltage ripple of 150 mV.

$$\Delta Vin = \frac{Ioutmax \times 0.25}{Cin \times fsw} \tag{23}$$

9.2.2.6 Soft-Start Capacitor

The soft-start capacitor determines the minimum amount of time it will take for the output voltage to reach its nominal programmed value during power-up. This is useful if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level.

The soft-start capacitor value can be calculated using Equation 24. In this example, the converter's soft-start time is 0.8 ms. In TPS65251, Iss is 5 µA and Vref is 0.8 V. From Equation 24, the soft-start capacitance is 5 nF. A standard 4.7-nF ceramic capacitor is chosen in this design. In this example, C16 is 4.7nF

$$Css(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)} \tag{24}$$

9.2.2.7 Bootstrap Capacitor Selection

A 0.047-µF ceramic capacitor must be connected between the BST to LX pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10-V or higher voltage rating.

9.2.2.8 Adjustable Current Limiting Resistor Selection

The converter uses the voltage drop on the high-side MOSFET to measure the inductor current. The over current protection threshold can be optimized by changing the trip resistor. Figure 17 governs the threshold of over current protection for Buck 1. When selecting a resistor, do not exceed the graph limits. In this example, the over current threshold is 3.2 A. In order to prevent a premature limit trip, the minimum line is used and the resistor is 100 kΩ.

When setting high-side current limit to large current values, ensure that the additional load immediately prior to an overcurrent condition will not cause the switching node voltage to exceed 20 V. Additionally, ensure during worst case operation, with all bucks loaded immediately prior to current limit, the maximum virtual junction temperature of the device does not exceed 125°C.

9.2.2.9 Output Voltage and Feedback Resistors Selection

For the example design, 40.2 kΩ was selected for R10. Vout is 1.2 V, Vref = 0.8 V. Using Equation 25, R11 is calculated as 80.4 kΩ. A standard 80.6-kΩ resistor is chose in this design.

$$R11 = \frac{Vout - Vref}{Vref} \times R10 \tag{25}$$

9.2.2.10 Compensation

A type-II compensation circuit is adequate for the converter to have a phase margin between 60 and 90 degrees. The following equations show the procedure of designing a peak current mode control dc/dc converter.

The compensation design takes the following steps:

1. Set up the anticipated cross-over frequency. In this example, the anticipated cross-over frequency (fc) is 65 kHz. The power stage gain (gm_{PS}) is 10 A/V and the GM amplifier gain (g_M) is 130 µA/V.

$$R12 = \frac{2\pi \times fc \times Vo \times Co}{g_M \times Vref \times gm_{ps}} \tag{26}$$

2. Place compensation zero at low frequency to boost the phase margin at the crossover frequency. From the procedures above, the compensation network includes a 20-kΩ resistor (R12) and a 4700-pF capacitor (C1).
3. An additional pole can be added to attenuate high frequency noise.

From the procedures above, the compensation network includes a 20-kΩ resistor (R12) and a 4700-pF capacitor (C14).

9.2.2.11 3.3-V and 6.5-V LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 10 µF for V7V pin 28
- 3.3 µF to 10 µF for V3V pin 29

9.2.3 Application Curves

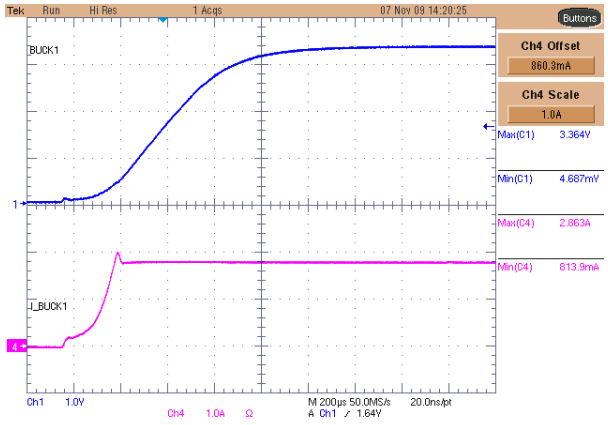


Figure 23. BUCK1 Start-Up
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 3.3 V, 2 A

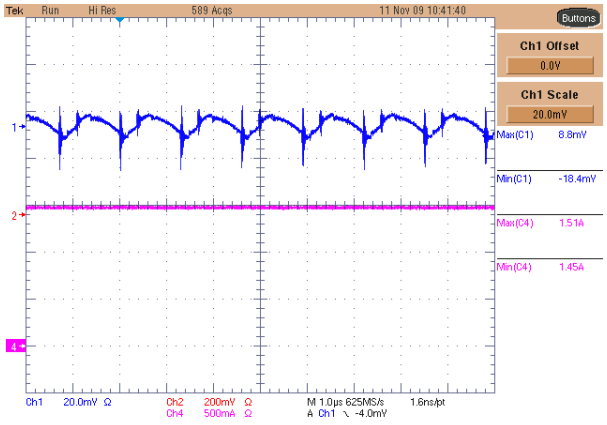


Figure 24. BUCK1 Ripple
V_{OUT} = 3.3 V, 1.5 A, f_{SW} = 800 kHz, 20 mV/div

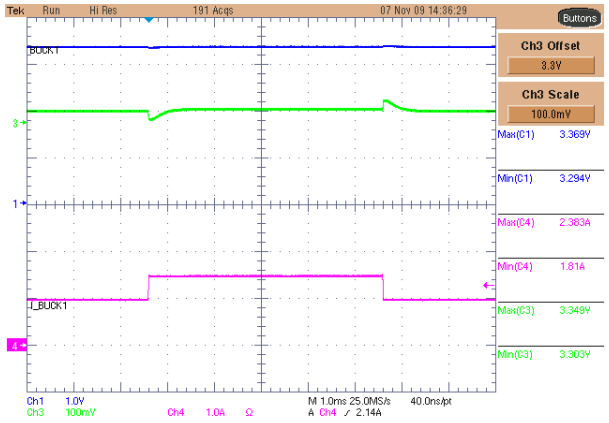


Figure 25. BUCK1 Transient Load Response
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 3.3 V, ΔI = 1 A to 1.5 A, 100 mV/div

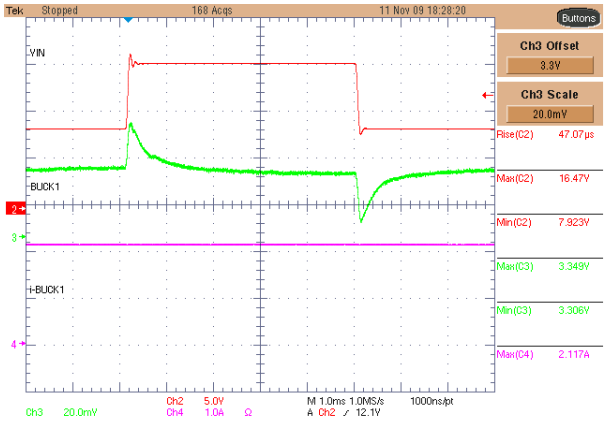


Figure 26. BUCK1 Transient Supply Response
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 3.3 V, ΔV_{IN} = 8 V to 16.5 V, 20 mV/div

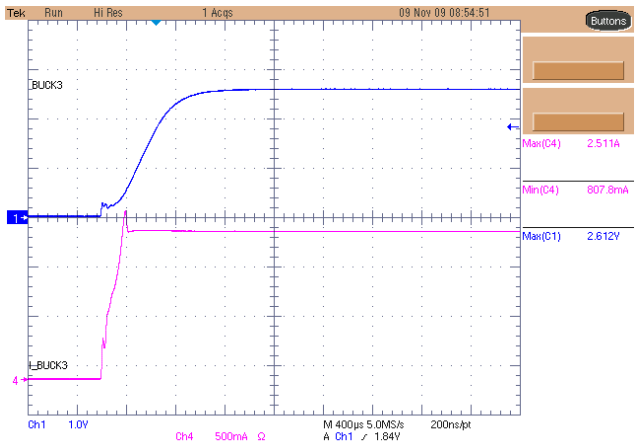


Figure 27. BUCK2 Start-Up
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 2.5 V, 1.5 A

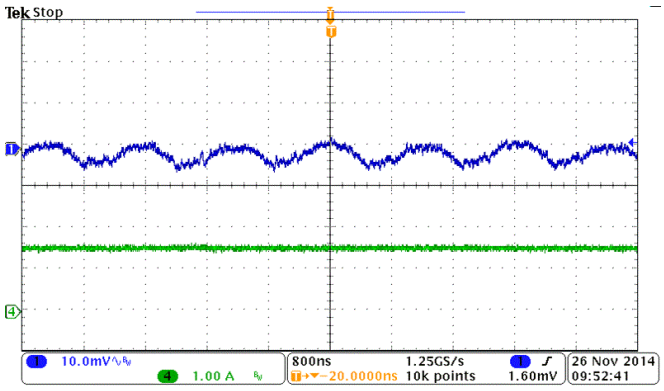


Figure 28. BUCK2 Ripple
V_{OUT} = 2.5 V, 1.5 A, f_{SW} = 800 kHz, 10 mV/div

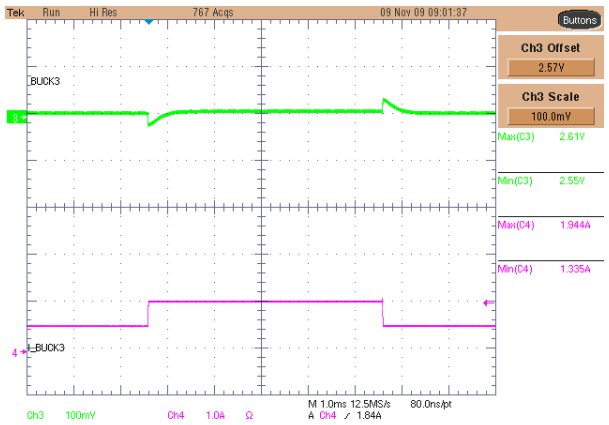


Figure 29. BUCK2 Transient Load Response
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 2.5 V, ΔI = 1 A to 1.5 A

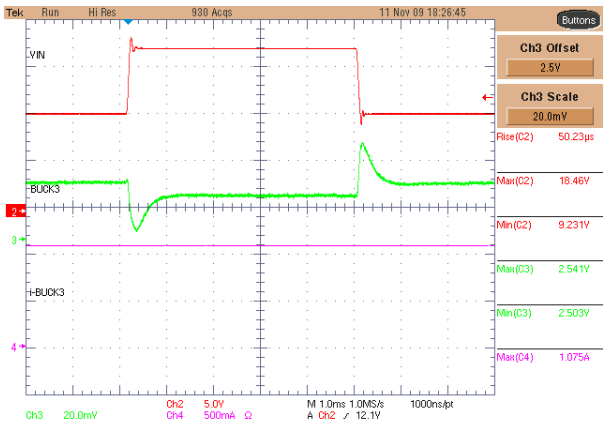


Figure 30. BUCK2 Transient Supply Response
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 2.5 V, ΔV_{IN} = 9 V to 8 V

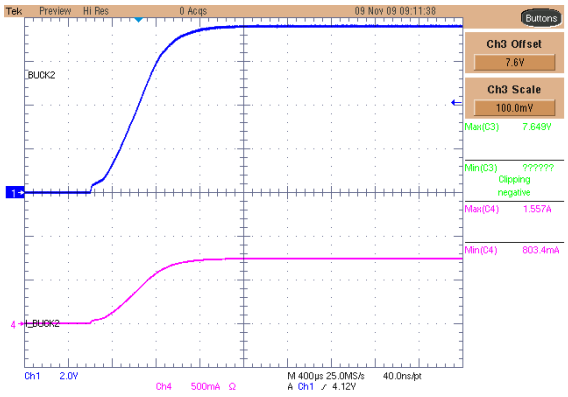


Figure 31. BUCK3 Start-Up
V_{OUT} = 7.5 V, 0.7 A

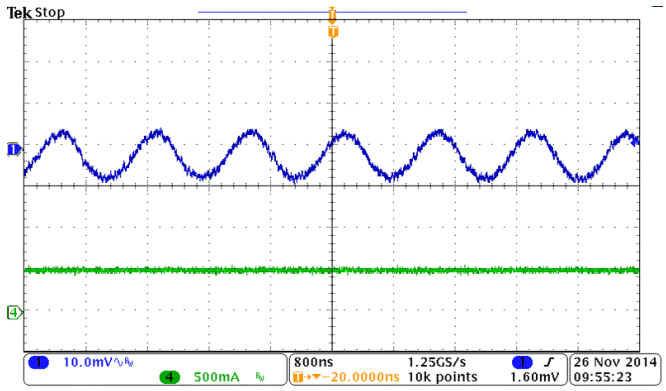


Figure 32. BUCK3 Ripple
V_{OUT} = 7.5 V, 0.5 A, f_{SW} = 800 kHz 10 mV/div

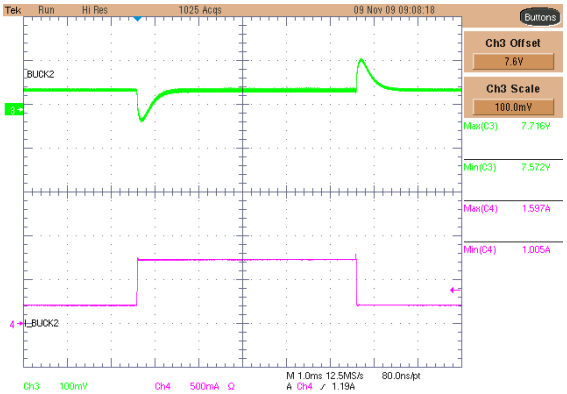


Figure 33. BUCK3 Transient Load Response
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 7.5 V, ΔI = 1 A to 1.5 A

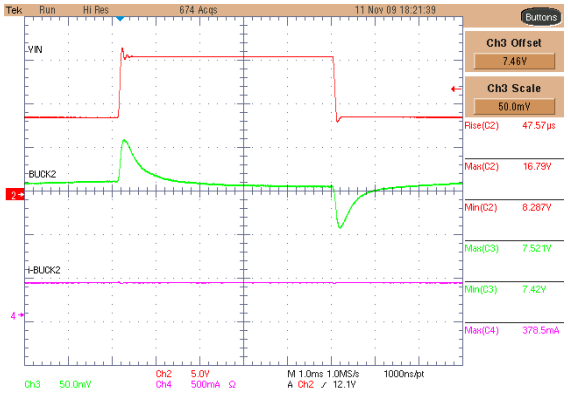


Figure 34. BUCK3 Transient Supply Response
V_{OUT} = 2.5 V, ΔV_{IN} = 9 V to 8 V

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4.5 V and 18 V. This input power supply should be well regulated. If the input supply is located more than a few inches from the TPS65251 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 μF is a typical choice.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of PMIC designs.

- Place VOUT, and LX on the top layer and an inner power plane for VIN.
- Fit also on the top layer connections for the remaining pins of the PMIC and a large top side area filled with ground.
- The top layer ground area sould be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter cpacitor and directly under the TPS65251 device to provide a thermal path from the Powerpad land to ground.
- The AGND pin should be tied directly to the power pad under the IC and the power pad.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the COMP pins. The COMP and OSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.

11.2 Layout Example

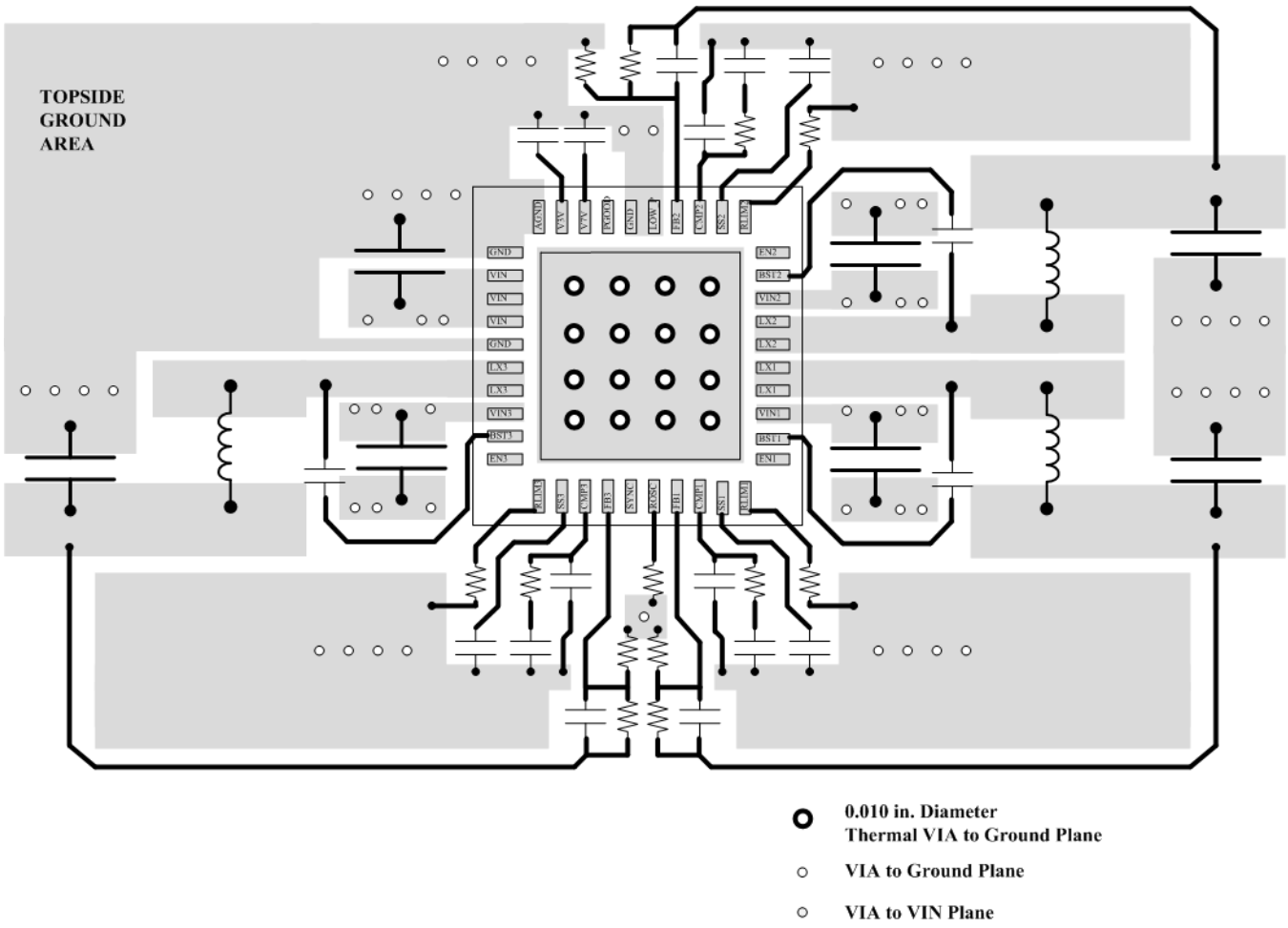


Figure 35. Layout Schematic

11.3 Power Dissipation

The total power dissipation inside TPS65251 should not to exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package (R_{JA}) and ambient temperature.

To calculate the temperature inside the device under continuous loading use the following procedure.

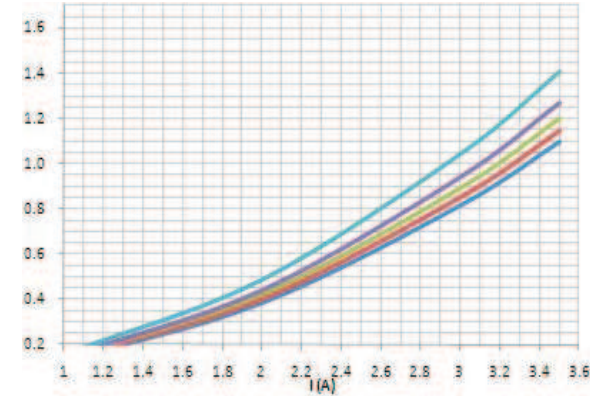
1. Define the set voltage for each converter.
2. Define the continuous loading on each converter. Make sure do not exceed the converter maximum loading.
3. Determine from the graphs below the expected losses (Y axis) in watts per converter inside the device. The losses depend on the input supply, the selected switching frequency, the output voltage and the converter chosen.
4. To calculate the maximum temperature inside the IC use the following formula:

$$T_{HOT\_SPOT} = T_A + P_{DIS} \times R_{\theta JA}$$

where

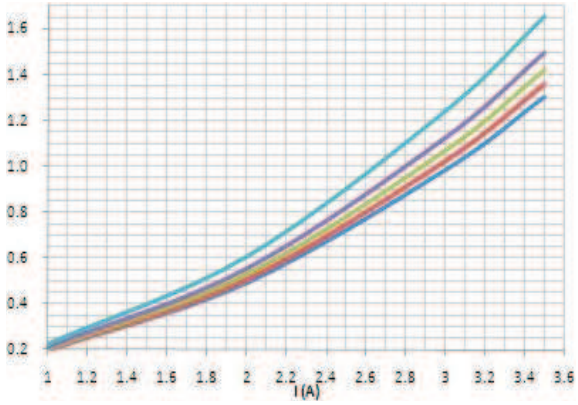
- T_A is the ambient temperature
- P_{DIS} is the sum of losses in all converters
- θ_{JA} is the junction to ambient thermal impedance of the device and it is heavily dependant on board layout (27)

Power Dissipation (continued)



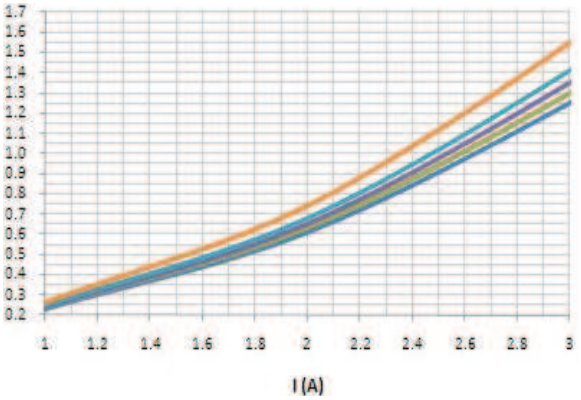
V_O (from top to bottom) = 5 V , 3.3 V, 2.5 V, 1.8 V, 1.2 V

Figure 36. Buck 1 Losses (W) vs Output Current
V_{IN} = 12 V, f_{SW} = 500 kHz



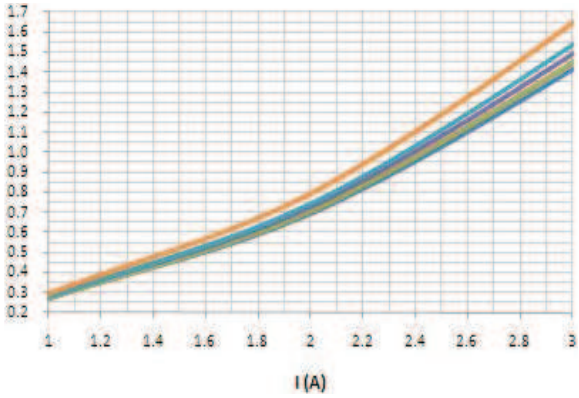
V_O (from top to bottom) = 5 V , 3.3 V, 2.5 V, 1.8 V, 1.2 V

Figure 37. Buck 1 Losses (W) vs Output Current
V_{IN} = 12 V, f_{SW} = 1.1 MHz



V_O (from top to bottom) = 5 V , 3.3 V, 2.5 V, 1.8 V, 1.2 V

Figure 38. Buck 2 and 3 Losses (W) vs Output Current
V_{IN} = 12 V, f_{SW} = 500 kHz



V_O (from top to bottom) = 5 V , 3.3 V, 2.5 V, 1.8 V, 1.2 V

Figure 39. Buck 2 and 3 Losses (W) vs Output Current
V_{IN} = 12 V, f_{SW} = 1.1 MHz

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
905-6525100	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251	Samples
TPS65251RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251	Samples
TPS65251RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

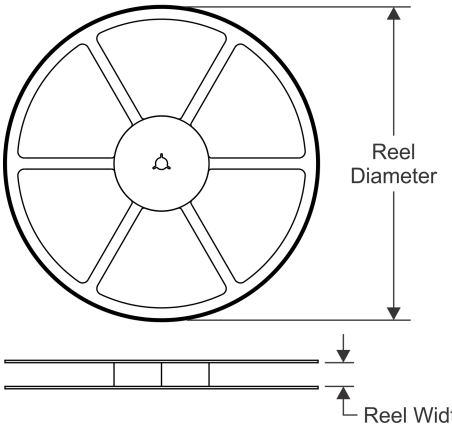
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

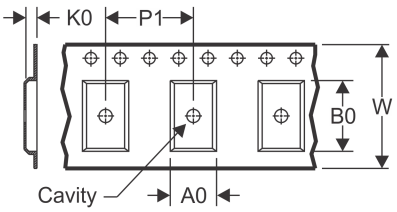
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

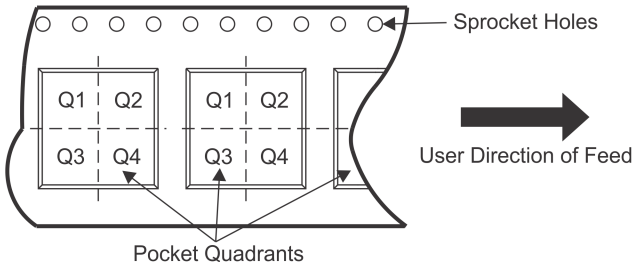


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

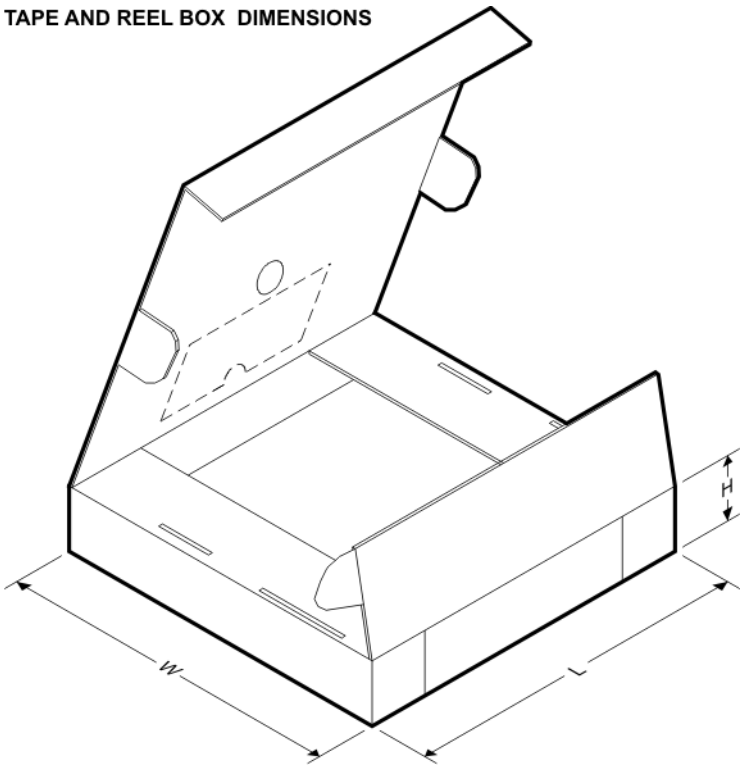
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65251RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65251RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

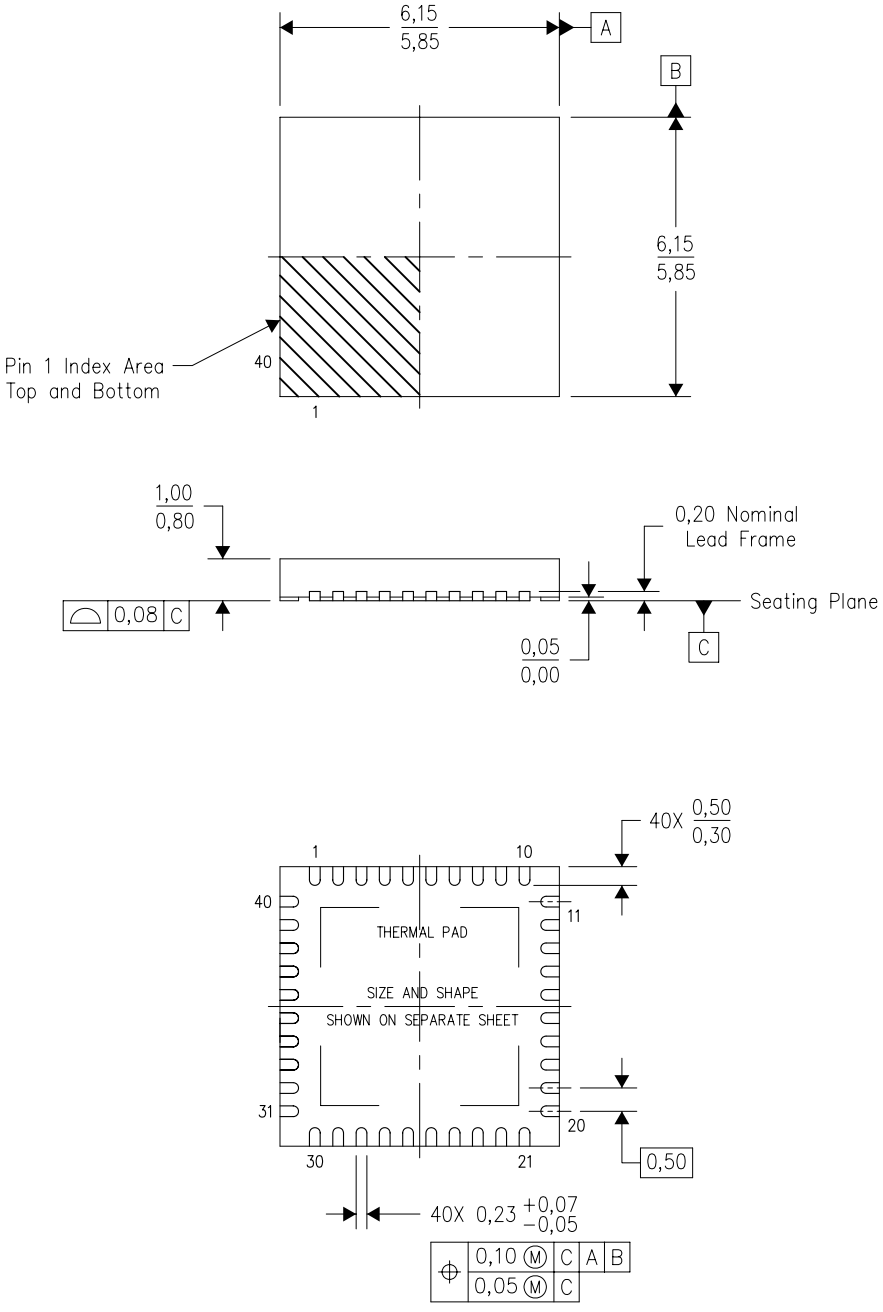
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65251RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS65251RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

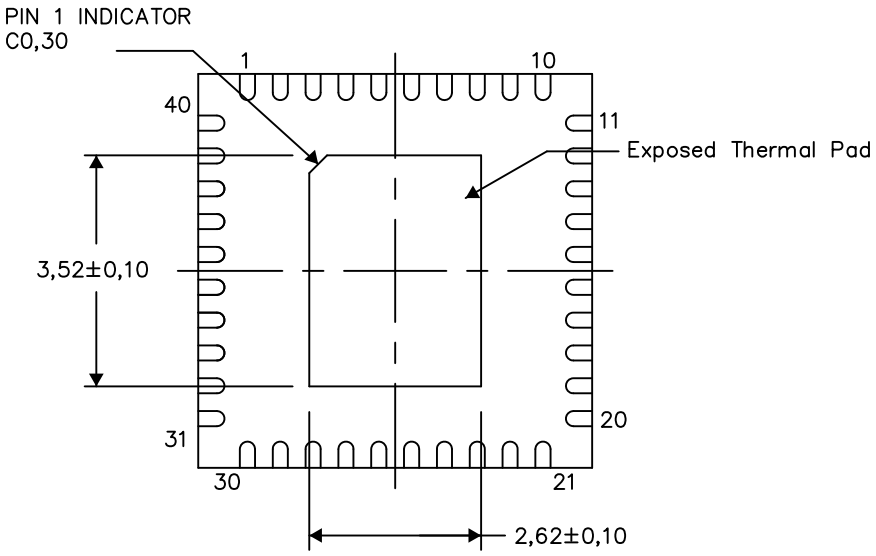
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



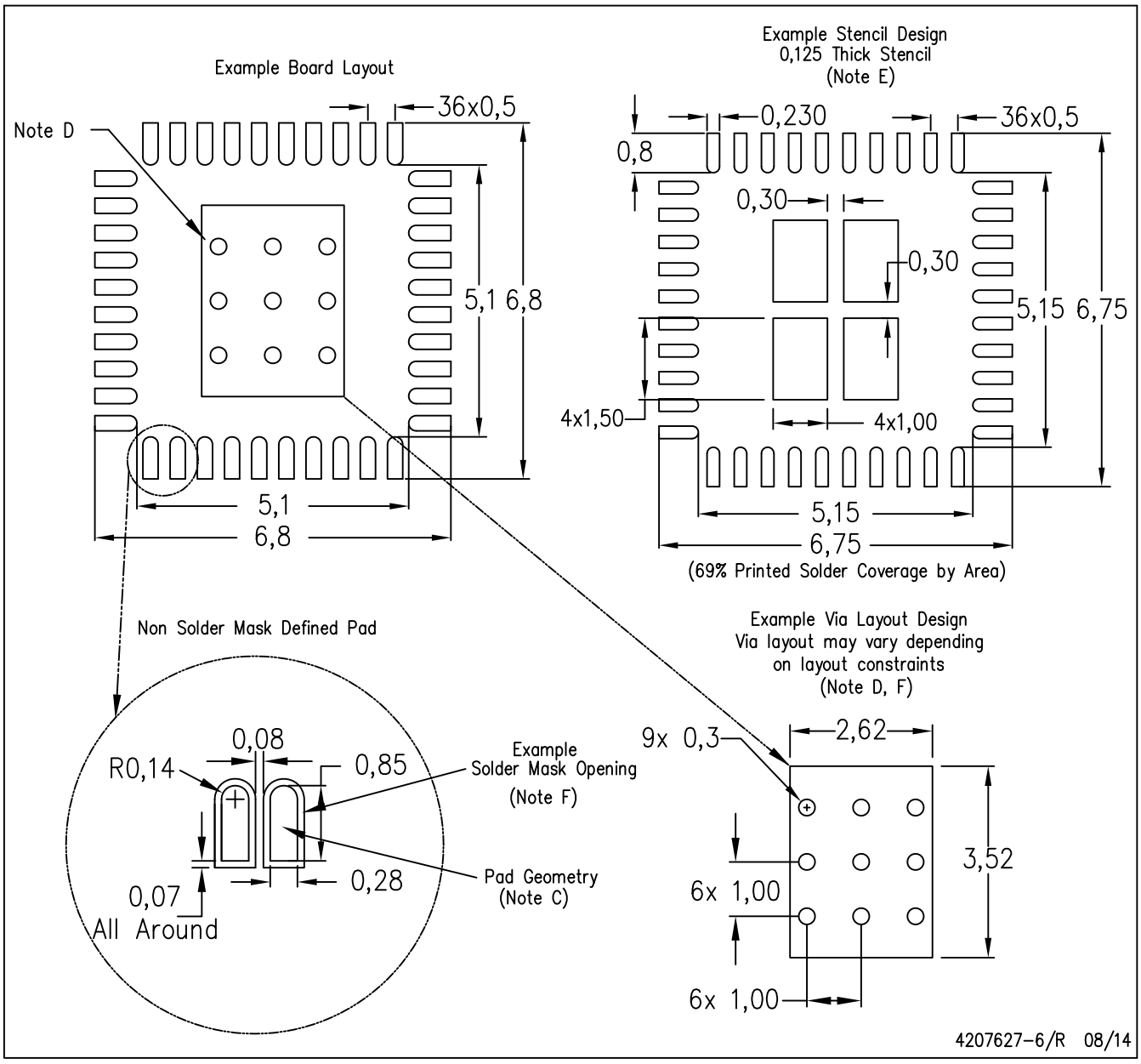
Bottom View

Exposed Thermal Pad Dimensions

4206355–9/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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