LCD Bias Supply

Check for Samples :TPS65170

FEATURES

- **8.6V to 14.7V Input Voltage Range**
- **2.8A Boost Converter Switch Current Limit**
- **Boost Converter Output Voltages up to 18.5V**
- **Boost and Buck Converter Short-Circuit Protection**
- **1.5A Buck Converter Switch Current Limit**
- **Fixed 750kHz Switching Frequency for Buck and Boost Converters**
- **Fixed Buck Converter Soft-Start**
- **Programmable Boost Converter Soft-Start**
- **Two Charge Pump Controllers to Regulate V_{GH} and V_{GL}**
- **Control Signal for External High-Side MOSFET Isolation Switch**
- **Reset Signal With Programmable Reset Pulse Duration**
- **Thermal Shutdown**
- **28-Pin 5×5 mm QFN Package**

APPLICATIONS

- **LCD TVs and Monitors**

DESCRIPTION

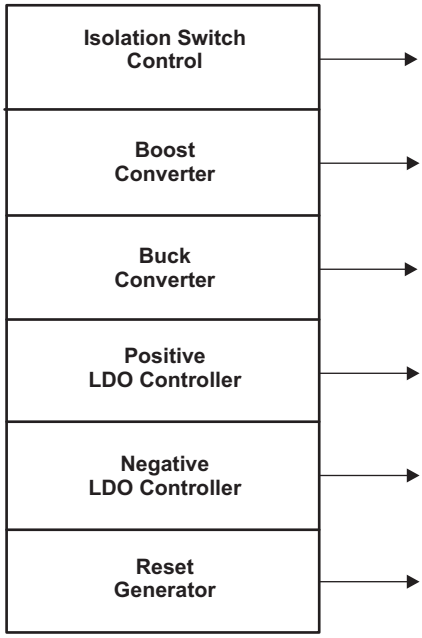
The TPS65170 provides a simple and economic power supply solution for a wide variety of LCD bias applications.

In typical display panel applications, the boost converter generates the display panel's source voltage V_S, the buck converter generates the system's logic supply V_{LOGIC}, and the two charge pump controllers regulate the external charge pumps generating the display transistors' on and off supplies V_{GH} and V_{GL}.

By using external transistors to regulate the charge pump output voltage, power dissipation in the IC is significantly reduced, simplifying PCB thermal design and improving reliability.

The TPS65170 also provides a reset circuit that monitors the buck converter output (V_{LOGIC}) and generates a reset signal for the timing controller during power-up.

A control signal can also be generated to control an external MOSFET isolation switch located between the output of the boost converter and the display panel.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	ORDERING	PACKAGE
–40°C to 85°C	TPS65170RHDR	28-Pin 5x5 QFN

(1) The device is supplied taped and reeled, with 3000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Input voltage(2)	VIN	-0.3 to 20	V
Input voltage(2)	FBN, FBP, FBB, FB, DLY, CRST, SS, COMP, VL	-0.3 to 7	V
Output voltage(2)	$\overline{RST}$	-0.3 to 7	V
	SWB, CTRLP, GD, SW, CTRLN	-0.3 to 20	V
Output current	GD	1	mA
ESD rating	Human Body Model	2000	V
	Machine Model	200	V
	Charged Device Model	700	V
	Continuous Power Dissipation	See Dissipation Table	W
Operating ambient temperature range		–40 to 85	°C
Operating junction temperature range		–40 to 150	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With respect to the GND and AGND pins.

DISSIPATION RATINGS

PACKAGE	θ_{JA}	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
28-Pin QFN	34 °C/W	2.94 W	1.62 W	1.32 W

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	8.6	12	14.7	V
V_S	Boost converter output voltage range	V_{IN}+1	15	18.5	V
L_{BOOST}	Boost converter inductance	6.8	10	15	µH
C_{BOOST}	Boost converter output capacitance	50	60	100	µF
L_{BUCK}	Buck converter inductance	6.8	10	15	µH
C_{BUCK}	Buck converter output capacitance	20	44	100	µF
T_A	Operating ambient temperature	–40	25	85	°C
T_J	Operating junction temperature	–40	85	125	°C

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V; V_S = 17V; V_{LOGIC} = 3.3V; T_A = –40°C to 85°C; typical values are at 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{IN}	Supply current	V_{FB}, V_{FBB}, V_{FBP} = 1.3V, V_{FBN} = –50mV		1	10	mA
UVLO	UVLO threshold	V_{IN} rising	7.8	8.2	8.5	V
INTERNAL OSCILLATOR						
f_{SW}	Switching frequency		600	750	900	kHz
BOOST CONVERTER						
V_S	Output voltage	Measured after isolation switch	13		18.5	V
V_{FB}	Feedback regulation voltage		–1%	1.24	1%	V
I_{FB}	Feedback input bias current	V_{FB} = 1.24V		±0.01	±1	µA
I_{LIM}	Switch current limit		2.8	3.5	4.2	A
I_{lkg}	Switch leakage current	V_{SW} = 12V			10	µA
$r_{DS(on)}$	Switch ON resistance	I_{SW} = I_{LIM}		0.12	0.22	Ω
t_{SW}	Switching time	Turn-on and turn-off		10		ns
	Line regulation	9.6V < V_{IN} < 14.4V, I_S = 750mA		0.02		%/V
	Load regulation	V_S = 17V, I_S = 100mA to 1.5A		0.1		%/A
V_{OVP}	Overvoltage threshold	V_{FB} rising		V_{FB} +3%	V_{FB} +5%	V
I_{SS}	Soft start current	V_{SS} = 1.24V		10		µA
$V_{FB(SC)}$	Short circuit threshold	V_{FB} rising		200		mV
BUCK CONVERTER						
V_{LOGIC}	Output voltage		–3%	3.3	3%	V
I_{FBB}	Feedback input bias current	V_{FBB} = 3.3V			±125	µA
I_{LIM}	Switch current limit		1.5	2.1	2.8	A
I_{lkg}	Switch leakage current	V_{SWB} = GND			10	µA
$r_{DS(on)}$	Switch ON resistance			0.21	0.35	Ω
t_{SW}	Switching time	Turn-on and turn-off		10		ns
	Line regulation	V_{IN} = 9.6V to 14.4V, I_{LOGIC} = 0.5A		0.01		%/V
	Load regulation	I_{LOGIC} = 150mA to 1.5A		0.2		%/A
V_{PG}	Power good threshold	V_{LOGIC} rising		3.2		V
$V_{FBB(SC)}$	Short circuit threshold	V_{FBB} rising		1.065		V
t_{SS}	Soft start time			0.66		ms
POSITIVE CHARGE PUMP CONTROLLER						
V_{FBP}	Feedback regulation voltage	I_{CTRLP} = 1mA (sinking)	-3%	1.24	+3%	V
I_{FBP}	Feedback input bias current	V_{FBP} = 1.24V		±1	±100	nA
I_{CTRLP}	Base drive current for external transistor	Normal operation (sinking)	5			mA
		Short-circuit operation (sinking)	40	55	75	µA
	Line regulation	V_{IN} = 9.6V to 14.4V, V_{GH} = 27V, I_{GH} = 50mA, including external components		±0.1		%/V
	Load regulation	V_{GH} = 27V, I_{GH} = 10mA to 50mA, including external components		±1		%/A
NEGATIVE CHARGE PUMP CONTROLLER						
V_{FBN}	Feedback regulation voltage	I_{CTRLN} = 1mA (sourcing)	–36	0	36	mV
I_{FBN}	Feedback input bias current	V_{FBN} = 0V		±1	±100	nA
I_{CTRLN}	Base drive current for external transistor	Normal operation (sourcing)	2.5			mA
		Short-circuit operation (sourcing)	200	300	480	µA
	Line regulation	V_{IN} = 9.6V to 14.4V, V_{GL} = -7V, I_{GL} = 50mA, including external components		±0.1		%/V

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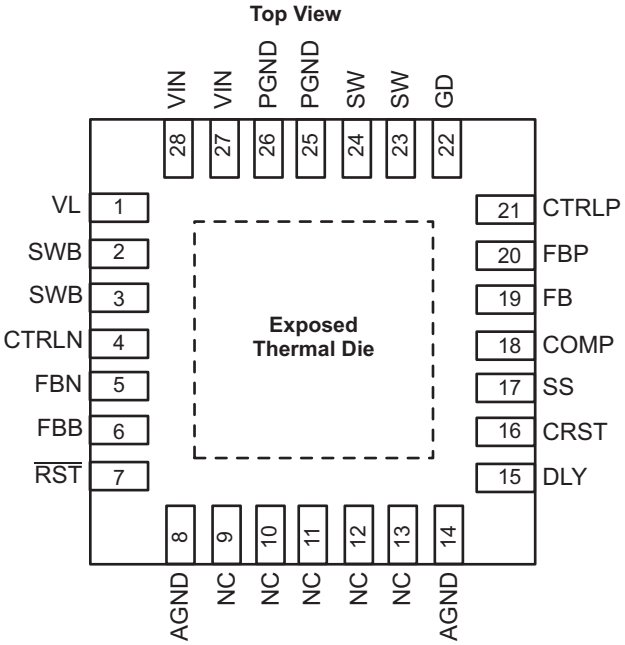
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 12V; V_S = 17V; V_{LOGIC} = 3.3V; T_A = –40°C to 85°C; typical values are at 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Load regulation	V_{GL} = –7V, I_{GH} = 10mA to 50mA, including external components		±1		%/A
RESET GENERATOR						
V_{RST}	Output voltage low	I_{RST} 1mA (sinking)			0.5	V
I_{RST}	Output current high	V_{RST} = 3.3V (sinking)			1	µA
I_{CRST}	Reset delay capacitor charge current	V_{CRST} = 1.24V		10		µA
V_{CRST}	Reset delay threshold voltage	V_{CRST} rising		1.24		V
ISOLATION SWITCH CONTROL						
V_{GD}	Output voltage low	I_{GD} = 500µA (sinking)			0.5	V
I_{LKG}	Leakage Current	V_{GD} = 20V		0.05	1	µA
DELAY DLY						
I_{DLY}	Delay capacitor charge current	V_{DLY} = 1.24V		10		µA
V_{DLY}	Delay threshold voltage	V_{DLY} rising		1.24		V
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			150		°C
T_{HYS}	Thermal shutdown hysteresis			10		°C

DEVICE INFORMATION

PIN ASSIGNMENT



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PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
VL	1	O	Connection for decoupling capacitor for internal bias supply.
SWB	2, 3	O	Buck converter switch node
CTRLN	4	O	Base drive signal for the positive charge pump external regulating transistor.
FBN	5	I	Feedback pin for the negative charge pump. Connect this pin to the center of a resistor divider connected between the negative charge pump output and buck converter output.
FBB	6	I	Buck converter feedback. Connect this pin to the output of the buck converter.
/RST	7	O	Reset generator open drain output
AGND	8	P	Analog ground
NC	9, 10, 11, 12, 13	N/A	Not used, connect to AGND.
AGND	14	P	Analog ground.
DLY	15	I	Positive charge pump and boost converter delay capacitor connection.
CRST	16	I	Reset generator timing capacitor connection.
SS	17	I	Soft-start timing capacitor connection.
COMP	18	I	Boost converter compensation network connection.
FB	19	I	Boost regulator feedback. Connect this pin to the center of a resistor divider connected between the boost converter output and AGND.
FBP	20	I	Feedback pin for the positive charge pump. Connect this pin to the center of a resistor divider connected between the positive charge pump output and AGND.
CTRLP	21	O	Base drive signal for the positive charge pump external regulating transistor
GD	22	O	Gate drive signal for the external MOSFET isolation switch.
SW	23, 24	O	Boost converter switching node
PGND	25, 26	P	Power ground
VIN	27, 28	P	Supply voltage connection
Exposed Thermal Die		P	Connect to the system GND

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TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE NO.
BOOST CONVERTER		
Efficiency	V_{IN} = 12 V, V_S = 15.5V	Figure 1
Load Transient Response	V_{IN} = 12 V, V_S = 15.5V, I_S = 250 mA to 750 mA	Figure 2
Line Transient Response	V_{IN} = 11.5 V to 12.5 V, V_S = 15.5 V, I_S = 750 mA, V_{GH} = 26V, I_{GH} = 50 mA	Figure 3
Output Voltage Ripple	V_{IN} = 12 V, V_S = 15.5 V, I_S = 500 mA, V_{GH} = 26V, I_{GH} = 50 mA	Figure 4
Switch Node (SW) Waveform	CCM Operation, V_{IN} = 12 V, I_S = 250 mA	Figure 5
	DCM Operation, V_{IN} = 12 V, I_S = 50 mA	Figure 6
BUCK CONVERTER		
Efficiency	V_{IN} = 12 V, V_{LOGIC} = 3.3V	Figure 7
Load Transient Response	V_{IN} = 12 V, V_{GL} = -7V, I_{GL} = 50mA, I_{LOGIC} = 250 mA to 500 mA	Figure 8
Line Transient Response	V_{IN} = 11.5 V to 12.5 V, V_{GL} = -7V, I_{GL} = 50mA, I_{LOGIC} = 500 mA	Figure 9
Output Voltage Ripple	V_{IN} = 12 V, V_{GL} = -7V, I_{GL} = 50mA, I_{LOGIC} = 500 mA	Figure 10
Switch Node (SW) Waveform	CCM Operation, V_{IN} = 12 V, I_{LOGIC} = 250 mA	Figure 11
	DCM Operation, V_{IN} = 12 V, I_{LOGIC} = 50 mA	Figure 12
	Skip Mode, V_{IN} = 12 V, I_{LOGIC} = 0 mA	Figure 13
POSITIVE CHARGE PUMP		
Load Transient Response	V_{IN} = 12 V, V_{GH} = 26 V, V_S = 15.5V, I_S = 250 mA, I_{GH} = 10 mA to 50 mA	Figure 14
Line Transient Response	V_{IN} = 11.5 V to 12.5 V, V_{GH} = 26 V, I_{GH} = 50 mA, V_S = 15.5V, I_S = 750 mA,	Figure 15
Output Voltage Ripple	V_{IN} = 12 V, V_{GH} = 26 V, I_{GH} = 50 mA, V_S = 15.5V, I_S = 750 mA,	Figure 16
NEGATIVE CHARGE PUMP		
Load Transient Response	V_{IN} = 12 V, V_{GL} = -7 V, I_{LOGIC} = 250 mA, I_{GL} = 10 mA to 50 mA	Figure 17
Line Transient Response	V_{IN} = 11.5 V to 12.5 V, V_{GL} = -7 V, I_{GL} = 50 mA, I_{LOGIC} = 250 mA	Figure 18
Output Voltage Ripple	V_{IN} = 12 V, V_{GL} = -7 V, I_{LOGIC} = 250 mA, I_{GL} = 50 mA	Figure 19
START-UP SEQUENCING		
Power-Up Sequencing		Figure 20
Reset Operation		Figure 21

BOOST CONVERTER EFFICIENCY vs OUTPUT CURRENT

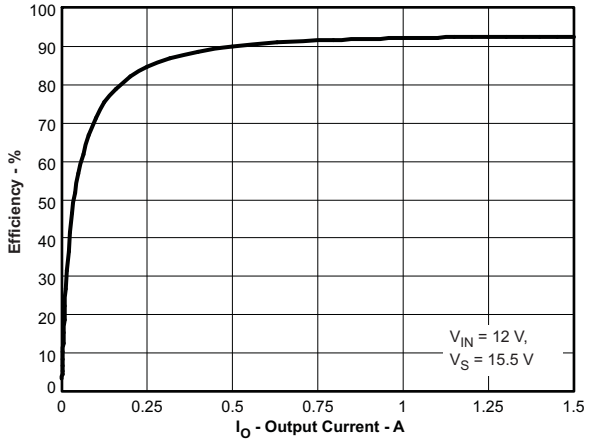


Figure 1.

BOOST CONVERTER LOAD TRANSIENT RESPONSE I_S = 250 mA to 750 mA

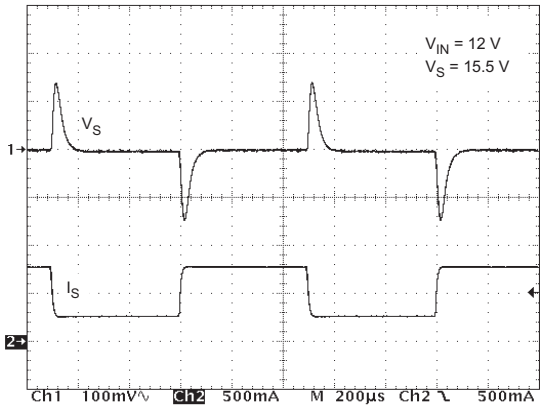


Figure 2.

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BOOST CONVERTER LINE TRANSIENT RESPONSE
V_{IN} = 11.5 V to 12.5 V

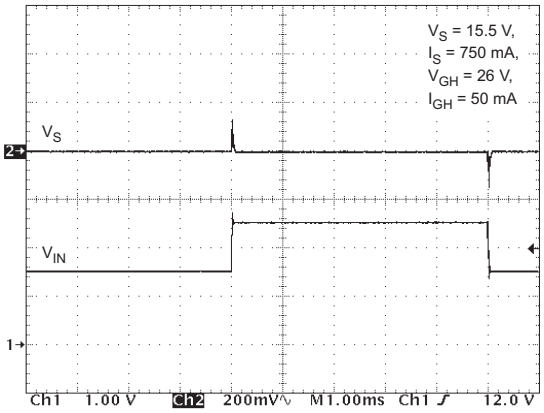


Figure 3.

BOOST CONVERTER OUTPUT VOLTAGE RIPPLE
I_S = 500 mA

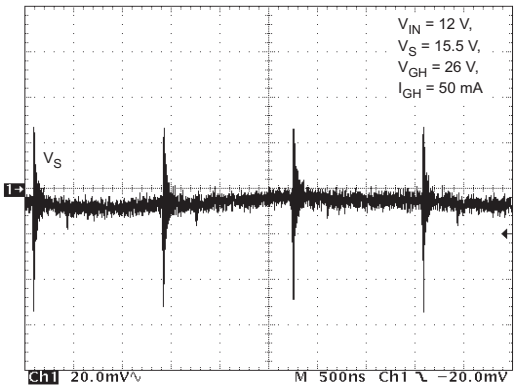


Figure 4.

BOOST CONVERTER SWITCH NODE WAVEFORM
CONTINUOUS CONDUCTION MODE

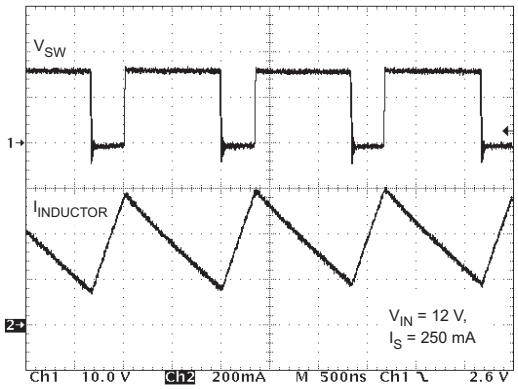


Figure 5.

BOOST CONVERTER SWITCH NODE WAVEFORM
DISCONTINUOUS CONDUCTION MODE

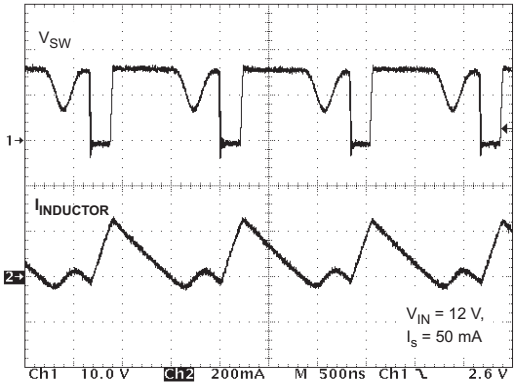


Figure 6.

BUCK CONVERTER EFFICIENCY
vs OUTPUT CURRENT

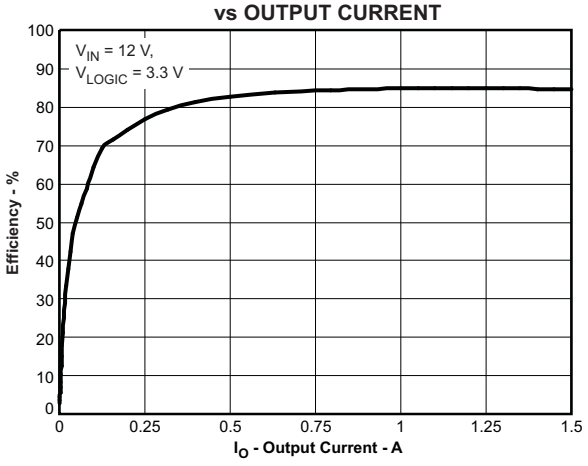


Figure 7.

BUCK CONVERTER LOAD TRANSIENT RESPONSE
I_{LOGIC} = 250 mA to 500 mA

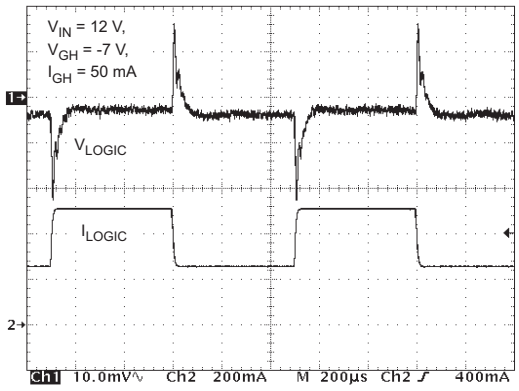


Figure 8.

BUCK CONVERTER LINE TRANSIENT RESPONSE
V_{IN} = 11.5 V to 12.5 V

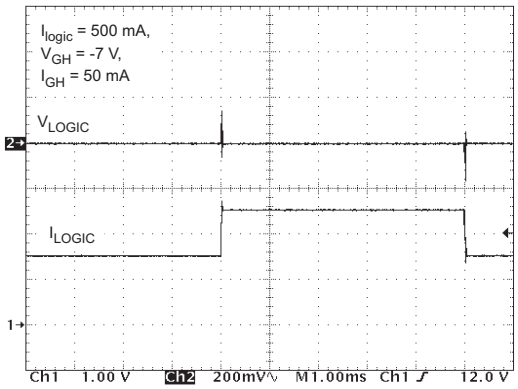


Figure 9.

BUCK CONVERTER OUTPUT VOLTAGE RIPPLE
I_{LOGIC} = 500 mA

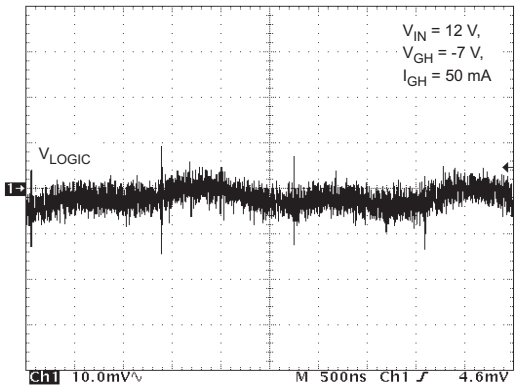


Figure 10.

BUCK CONVERTER SWITCH NODE WAVEFORM
CONTINUOUS CONDUCTION MODE

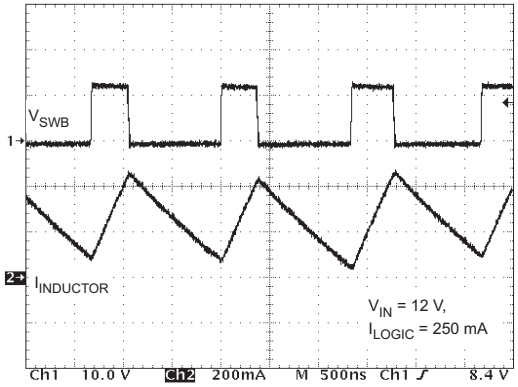


Figure 11.

BUCK CONVERTER SWITCH NODE WAVEFORM
DISCONTINUOUS CONDUCTION MODE

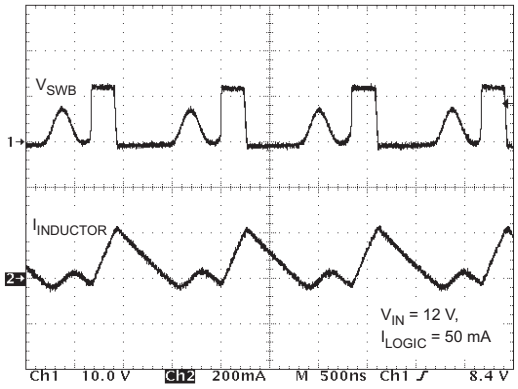


Figure 12.

BUCK CONVERTER SWITCH WAVEFORM
SKIP MODE

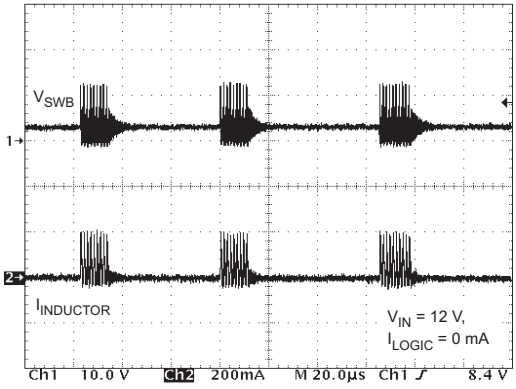


Figure 13.

POSITIVE CHARGE PUMP LOAD TRANSIENT RESPONSE
I_{GH} = 10 mA to 50 mA

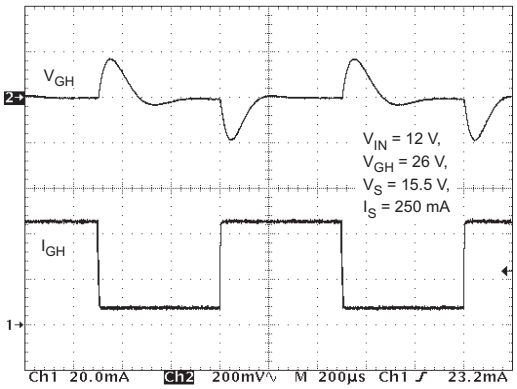


Figure 14.

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POSITIVE CHARGE PUMP LINE TRANSIENT RESPONSE
V_{IN} = 11.5 V to 12.5 V

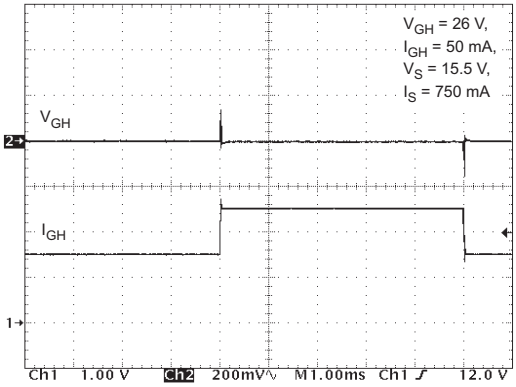


Figure 15.

POSITIVE CHARGE PUMP OUTPUT VOLTAGE RIPPLE
I_{GH} = 50 mA

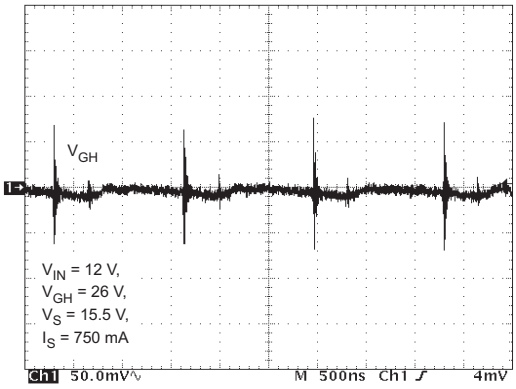


Figure 16.

NEGATIVE CHARGE PUMP LOAD TRANSIENT RESPONSE
I_{GL} = 10 mA to 50 mA

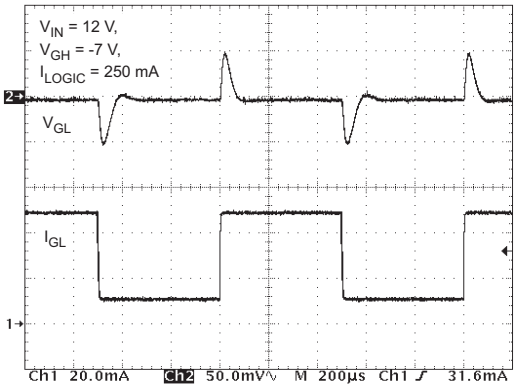


Figure 17.

NEGATIVE CHARGE PUMP LINE TRANSIENT RESPONSE
V_{IN} = 11.5 V to 12.5 V

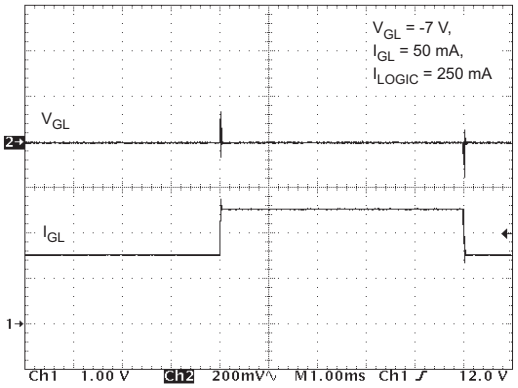


Figure 18.

NEGATIVE CHARGE PUMP OUTPUT VOLTAGE RIPPLE
I_{GL} = 50mA

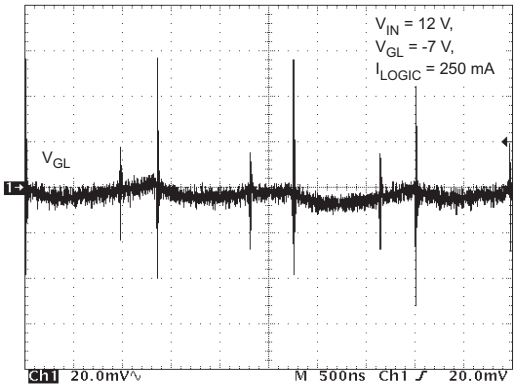


Figure 19.

POWER-UP SEQUENCING

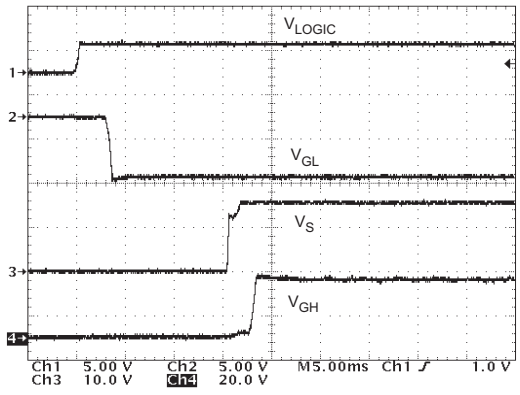


Figure 20.

RESET SEQUENCING

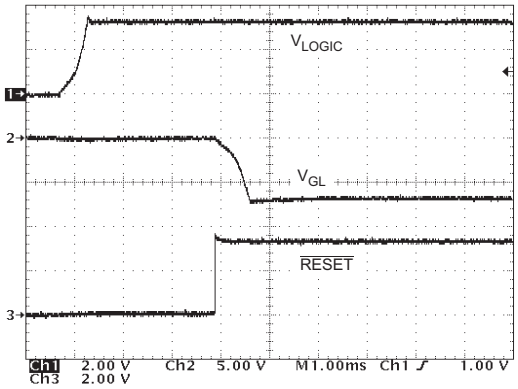


Figure 21.

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DETAILED DESCRIPTION

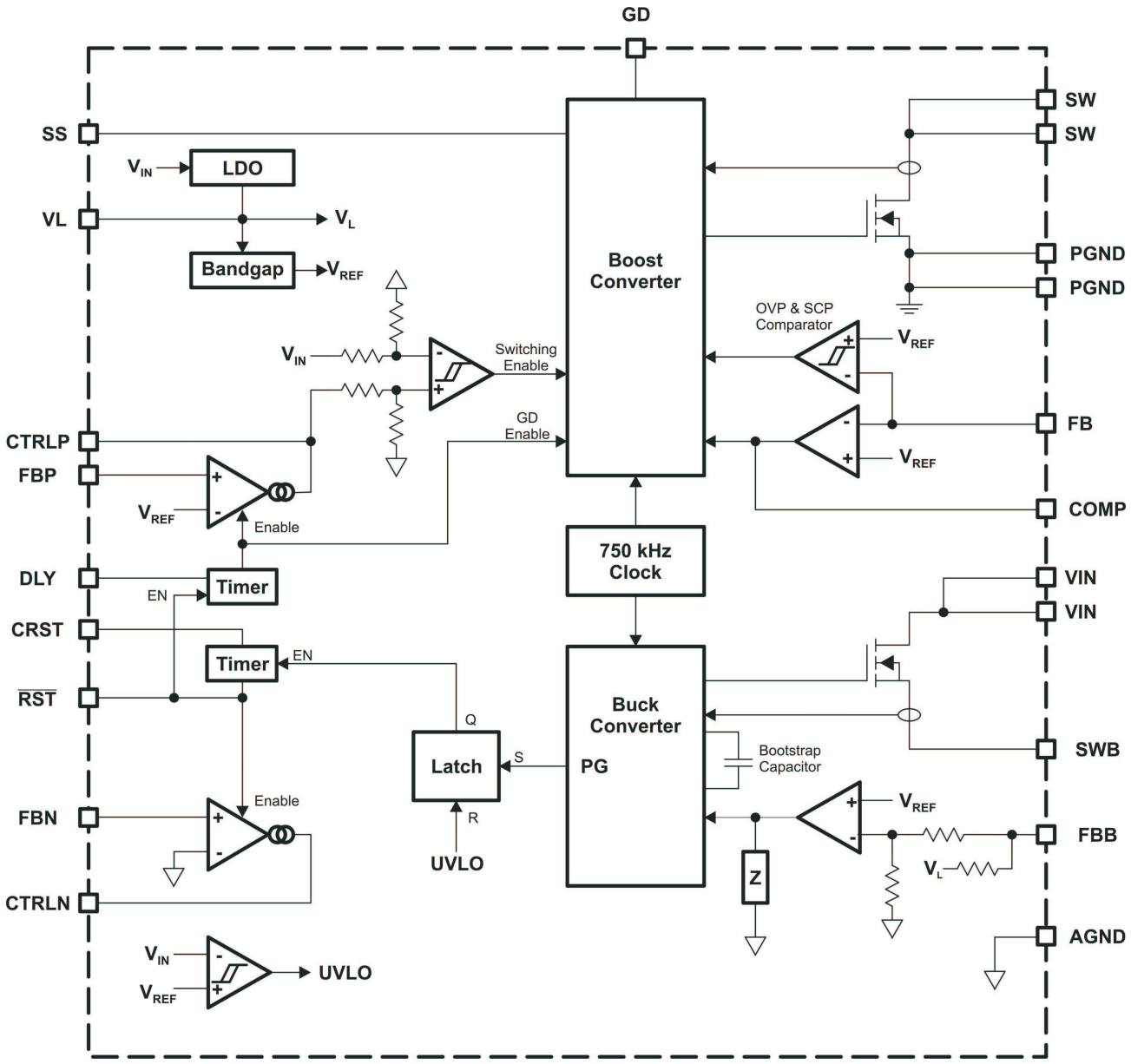


Figure 22. Internal Block Diagram

BOOST CONVERTER

The non-synchronous boost converter uses a current mode topology and operates at a fixed frequency of 750kHz. The internal block diagram of the boost converter is shown in Figure 23 and a typical application circuit in Figure 24. External compensation allows designers to optimize performance for individual applications, and is easily implemented by connecting a suitable capacitor/resistor network between the COMP pin and AGND (see the BOOST CONVERTER DESIGN PROCEDURE section for more details). The boost converter also controls a GD pin that can be used to drive an external isolation MOSFET.

The boost converter can operate in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the load current. At medium and high load currents, the inductor current is always greater

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than zero and the converter operates in CCM; at low load currents, the inductor current is zero during part of each switching cycle, and the converter operates in DCM. The switch node waveforms for CCM and DCM operation are shown in Figure 5 and Figure 6. Note that the ringing seen during DCM operation occurs because of parasitic capacitance in the PCB layout and is quite normal for DCM operation. There is little energy contained in the ringing waveform and it does not significantly affect EMI performance.

Equation 1 can be used to calculate the load current below which the boost converter operates in DCM .

$$I_{DCM} = \frac{(V_S - V_{IN})}{2 \times L \times f_{SW}} \times \frac{V_{IN}}{V_{OUT}} \quad (1)$$

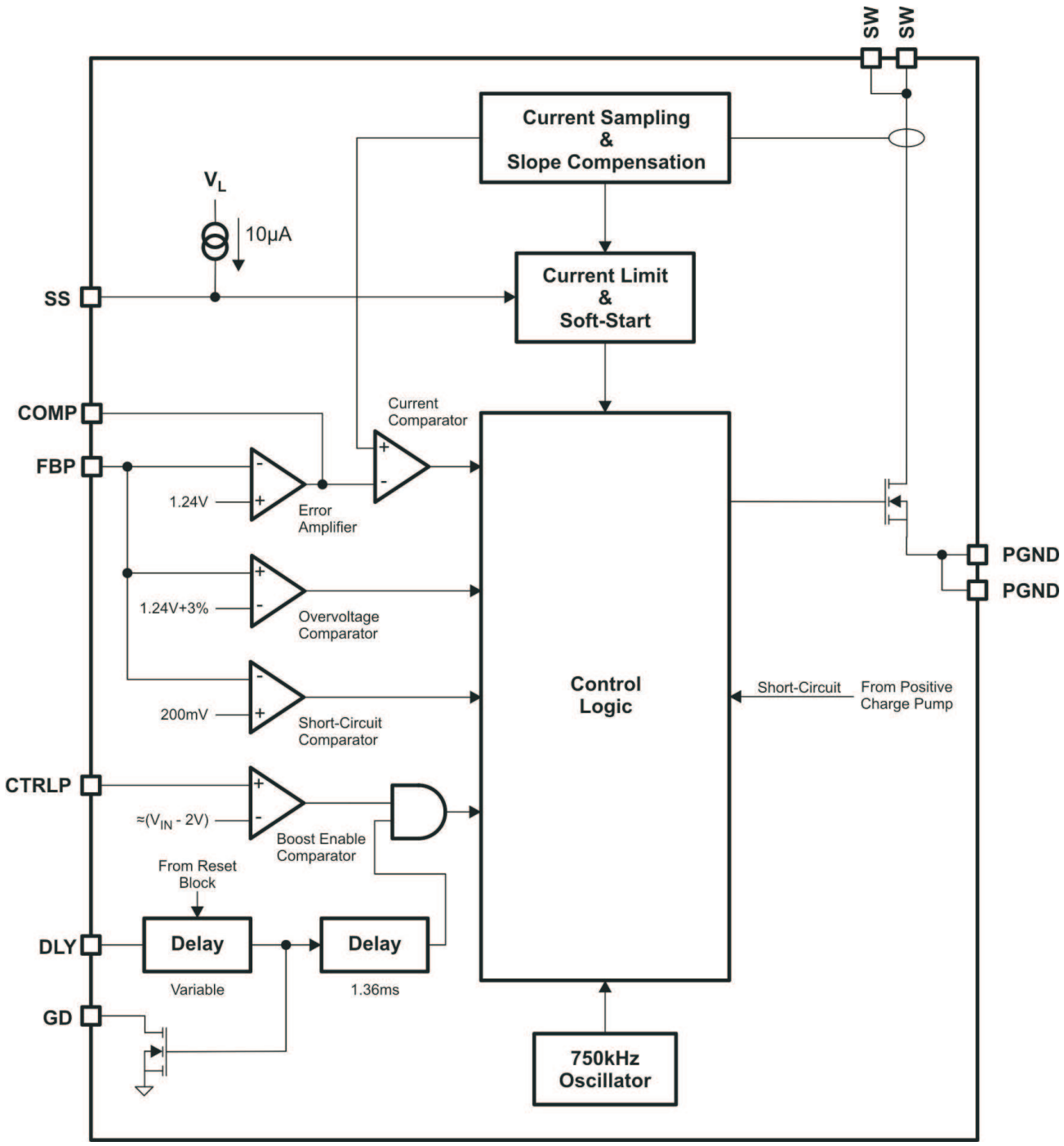


Figure 23. Boost Converter Internal Block Diagram

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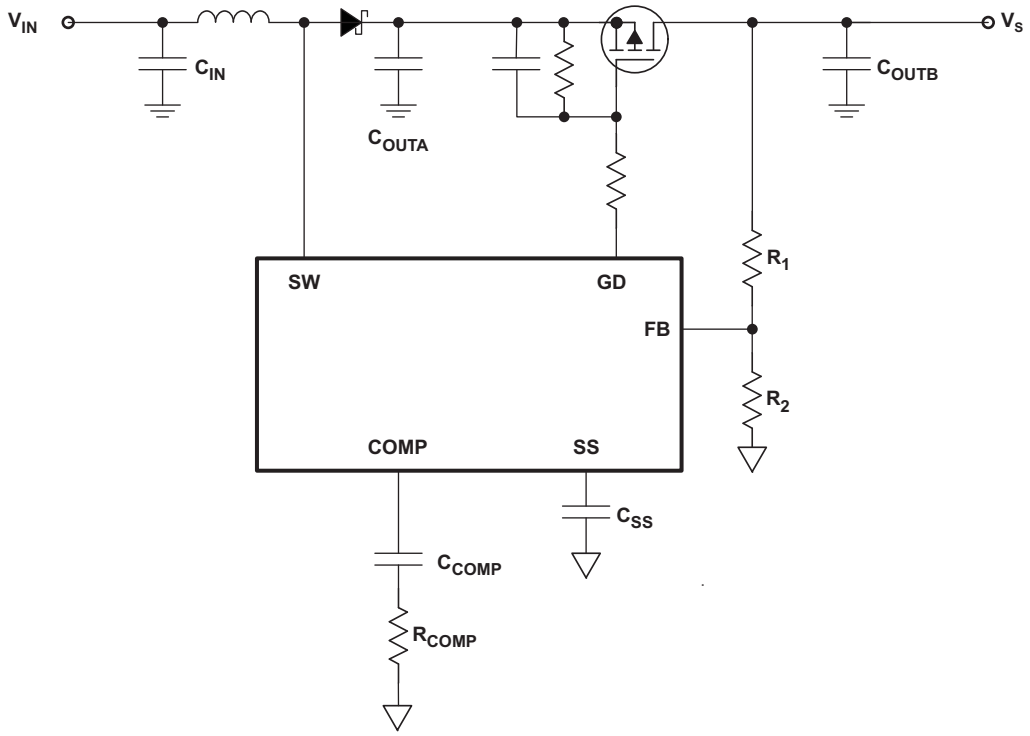


Figure 24. Boost Converter Typical Application Circuit

PROTECTION (BOOST CONVERTER)

The boost converter is protected against potentially damaging conditions such as overvoltage and short circuits. An error condition is detected if the voltage on the converter's FB pin remains below 200mV for longer than 1.36ms, in which case, the converter stops switching and is latched in the OFF condition. To resume normal operation, the TPS65170 must be turned off and then turned on again.

Note: since the positive charge pump is driven from its switch node, an error condition on the boost converter's output will also cause the loss of V_{GH} until the circuit recovers.

The boost converter also stops switching while the positive charge pump is in a short circuit condition. This condition is not latched, however, and the boost converter automatically resumes normal operation once the short circuit condition has been removed from the positive charge pump.

BOOST CONVERTER DESIGN PROCEDURE

Calculate Converter Duty Cycle (Boost Converter)

The simplest way to calculate the boost converter's duty cycle is to use the efficiency curve in Figure 1 to determine the converter's efficiency under the anticipated load conditions and insert this value into Equation 2 (1). Alternatively, a worst-case value (e.g., 90%) can be used for efficiency.

$$D = 1 - \frac{V_{IN} \times \eta}{V_S} \quad (2)$$

A. Valid only when boost converter operates in CCM.

Where V_S is the output voltage of the boost converter.

Calculate Maximum Output Current (Boost Converter)

The maximum output current I_S that the boost converter can supply can be calculated using Equation 3. The minimum specified output current occurs at the maximum duty cycle (which occurs at minimum V_{IN}) and minimum frequency (600kHz).

$$I_S = \left(I_{LIM} - \frac{V_{IN} \times D}{2 \times f_{SW} \times L} \right) \times (1 - D) \quad (3)$$

Where I_{LIM} is the minimum specified switch current limit (2.8A) and f_{SW} is the converter switching frequency.

Calculate Peak Switch Current (Boost Converter)

Equation 4 can be used to calculate the peak switch current occurring in a given application. The worst-case (maximum) peak current occurs at the minimum input voltage and maximum duty cycle.

$$I_{SW(PK)} = \frac{I_S}{1 - D} + \frac{V_{IN} \times D}{2 \times f_{SW} \times L} \quad (4)$$

Inductor Selection (Boost Converter)

The boost converter is designed for use with inductors in the range 6.8µH to 15µH. A 10µH inductor is typical. Inductors should be capable of supporting at least 125% of the peak current calculated by Equation 4 without saturating. This ensures sufficient margin to tolerate heavy load transients. Alternatively, a more conservative approach can be used in which an inductor is selected whose saturation current is greater than the maximum switch current limit (4.2A).

Another important parameter is DC resistance, which can significantly affect the overall converter efficiency. Physically larger inductors tend to have lower DC resistance (DCR) because they can use thicker wire. The type and core material of the inductor can also affect efficiency, sometimes by as much as 10%. Table 1 shows some suitable inductors.

Table 1. Boost Converter Inductor Selection

PART NUMBER	INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (L×W×H mm)	I_{SAT} / DCR
CDRH8D43	10 µH	Sumida	8.3 × 8.3 × 4.5	4A / 29 mΩ
CDRH8D38	10 µH	Sumida	8.3 × 8.3 × 4	3A / 38 mΩ
MSS 1048-103	10 µH	Coilcraft	10.5 × 10.5 × 5.1	4.8A / 26 mΩ
744066100	10 µH	Wuerth	10 × 10 × 3.8	4A / 28 mΩ

Rectifier Diode Selection (Boost Converter)

For highest efficiency, the rectifier diode should be a Schottky type. Its reverse voltage rating should be higher than the maximum output voltage V_S. The average rectified forward current through the diode is the same as the output current.

$$I_{D(AVG)} = I_S \quad (5)$$

A Shottky diode with 2A average rectified current rating is adequate for most applications. Smaller diodes can be used in applications with lower output current, however, the diode must be able to handle the power dissipated in it, which can be calculated using Equation 6. Table 2 lists some diodes suitable for use in typical applications.

$$P_D = I_{D(AVG)} \times V_F \quad (6)$$

Table 2. Boost Converter Rectifier Diode Selection

PART NUMBER	V_R / I_{AVG}	V_F	$R_{\theta JA}$	SIZE	COMPONENT SUPPLIER
MBRS320	20V / 3A	0.44V at 3A	46°C/W	SMC	International Rectifier
SL22	20V / 2A	0.44V at 2A	75°C/W	SMB	Vishay Semiconductor
SS22	20V / 2A	0.50V at 2A	75°C/W	SMB	Fairchild Semiconductor

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Output Capacitance Selection (Boost Converter)

For best performance, a total output capacitance (C_{OUTA}+C_{OUTB} in Figure 24) in the range 50µF to 100µF is recommended. At least 20µF of the total output capacitance should be connected directly to the cathode of the boost converter's rectifier diode, i.e., in front of the isolation switch.

Operating the boost converter with little or no capacitance in front of the isolation switch may cause overvoltage conditions that reduce reliability of the TPS65170.

Table 3 suggests some output capacitors suitable for use with the boost converter.

Table 3. Boost Converter Output Capacitor Selection

PART NUMBER	VALUE / VOLTAGE RATING	COMPONENT SUPPLIER
GRM32ER61E226KE15	22 µF / 25V	Murata
GRM31CR61E106KA12	10 µF / 25V	Murata
UMK325BJ106MM	10 µF / 50V	Taiyo Yuden

Setting the Output Voltage (Boost Converter)

The boost converter's output voltage is programmed by a resistor divider according to Equation 7.

$$V_S = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (7)$$

Where V_{REF} is the IC's internal 1.24V reference.

A current of the order of 100µA through the resistor network ensures good accuracy and improves noise immunity. A good approach is to assume a value of about 12k for the lower resistor (R2) and then select the upper resistor (R1) to set the desired output voltage.

Compensation (Boost Converter)

The boost converter's external compensation can be fine-tuned for each individual application. Recommended starting values are 33kΩ and 1nF, which introduce a pole at the origin for high DC gain and a zero for good transient response. The frequency of the zero set by the compensation components can be calculated using Equation 8.

$$f_z = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} \quad (8)$$

Selecting the Soft-Start Capacitor (Boost Converter)

The boost converter features a programmable soft-start function that ramps up the output voltage to limit the inrush current drawn from the supply voltage. The soft-start duration is set by the capacitor connected between the SS pin and AGND according to Equation 9.

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (9)$$

Where C_{SS} is the capacitor connected between the SS pin and GND, V_{REF} is the IC's internal 1.24V reference, and I_{SS} is the internally generated 10µA soft-start current.

Selecting the Isolation Switch Gate Drive Components

The isolation switch is controlled by an active-low signal generated by the GD pin. Because this signal is open-drain, an external pull-up resistor is required to turn the MOSFET switch off. If the MOSFET's maximum gate-source voltage rating is less than the maximum V_{IN}, two resistors in series can be used to reduce the maximum V_{GS} applied to the device. The exact value of the gate drive resistors is not critical: 100k for both is a good value to start with.

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A capacitor can also be connected in parallel with the top resistor, as illustrated in Figure 24. The effect of this capacitor is to slow down the speed with which the transistor turns on, thereby limiting inrush current. (Note that the capacitor also slows down the speed with which the transistor turns off, and therefore the speed with which it can respond to error conditions.)

Even when trying to limit inrush current, the capacitor must not be too large or the output voltage will rise so slowly the condition will be interpreted as an error (see *Power Supply Sequencing in Detail* later in this data sheet). Typical values are 10nF to 100nF, depending on the transistor used for the isolation switch and the value of the gate-drive resistors.

Note that even in applications that do not use an isolation switch, an external pull-up resistor (typically 100kΩ) connected between the GD and V_{IN} is required.

BUCK CONVERTER

The buck converter is a non-synchronous type that runs at a fixed frequency of 750kHz. The converter features integrated soft-start (0.66ms), bootstrap, and compensation circuits to minimize external component count. The buck converter's internal block diagram is shown in Figure 25 and a typical application circuit in Figure 26.

The output voltage of the buck converter is internally programmed to 3.3V and is enabled as soon as V_{IN} exceeds the UVLO threshold. For best performance, the buck converter's FB pin should be connected directly to the positive terminal of the output capacitor(s).

The buck converter can operate in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the load current. At medium and high load currents, the inductor current is always greater than zero and the converter operates in CCM; at low load currents, the inductor current is zero during part of each switching cycle, and the converter operates in DCM. The switch node waveforms for CCM and DCM operation are shown in Figure 11 and Figure 12. Note that the ringing seen during DCM operation occurs because of parasitic capacitance in the PCB layout and is quite normal for DCM operation. However, there is very little energy contained in the ringing waveform and it does not significantly affect EMI performance. Equation 10 can be used to calculate the load current below which the buck converter operates in DCM

$$I_{DCM} = \frac{(V_{IN} - V_{LOGIC})}{2 \times L \times f_{SW}} \times \frac{V_{LOGIC}}{V_{IN}} \quad (10)$$

The buck converter uses a skip mode to regulate V_{LOGIC} at very low load currents. This mode allows the converter to maintain its output at the required voltage while still meeting the requirement of a *minimum on time*. The buck converter enters skip mode when its feedback voltage exceeds the skip mode threshold (1% above the normal regulation voltage). During skip mode, the buck converter switches for a few cycles, then stops switching for a few cycles, and then starts switching again and so on, for as long as the feedback voltage is above the skip mode threshold. Output voltage ripple can be a little higher during skip mode (see Figure 13).

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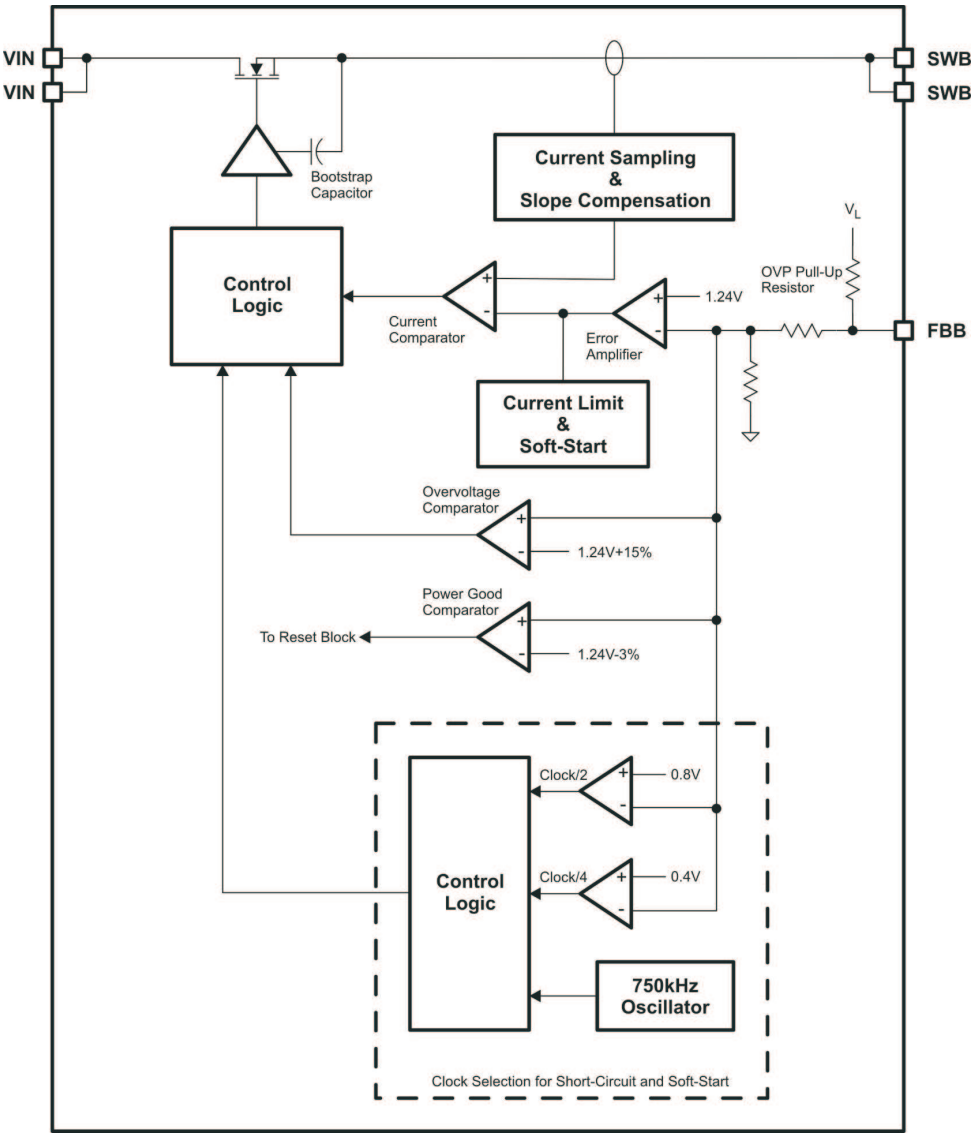


Figure 25. Buck Converter Internal Block Diagram

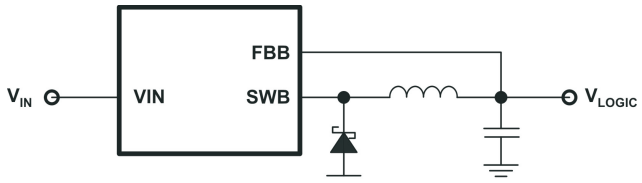


Figure 26. Buck Converter Application Circuit

PROTECTION (BUCK CONVERTER)

To protect against short circuit conditions, the buck converter automatically limits its output current when the voltage applied to its FBB pin is less than 400mV. Normal operation is resumed as soon as the feedback voltage exceeds 400mV.

Note: since the negative charge pump is driven from its switch node, a short circuit condition on the buck converter's output will also cause the loss of V_{GL} until the short circuit is removed.

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An internal pull-up prevents the buck converter from generating excessive output voltages if its FBB pin is left floating.

Buck Converter Design Procedure

Because the negative charge pump is driven from the buck converter's switch node, the effective output current for design purposes is greater than I_{LOGIC} alone. For best performance, the effective current calculated using Equation 11 should be used during the design.

$$I_{LOGIC(EFFECTIVE)} = I_{LOGIC} + \frac{|V_{GL}| \times I_{GL}}{V_{LOGIC}} \quad (11)$$

Calculate Converter Duty Cycle (Buck Converter)

The best way to calculate the converter's duty cycle is to use the efficiency curve in Figure 7 to determine the converter's efficiency under the anticipated load conditions and insert this value into Equation 12 (1). Alternatively, a worst-case value (e.g., 80%) can be used for efficiency.

$$D = \frac{V_{LOGIC}}{V_{IN} \times \eta} \quad (12)$$

(1) Valid only when buck converter perates in CCM.

Calculate Maximum Output Current (Buck Converter)

The maximum output current that the buck converter can supply can be calculated using Equation 13. The minimum specified output current occurs at the minimum duty cycle (which occurs at maximum V_{IN}) and maximum frequency (900kHz).

$$I_{LOGIC(EFFECTIVE)} = I_{SW(LIM)} - \frac{V_{IN} \times (1 - D)}{2 \times f_{SW} \times L} \times D \quad (13)$$

Where $I_{SW(LIM)}$ is the minimum specified switch current limit (1.5A) and f_{SW} is the converter switching frequency.

Calculate Peak Switch Current (Buck Converter)

Equation 14 can be used to calculate the peak switch current occurring in a given application. The worst-case (maximum) peak current occurs at maximum V_{IN}.

$$I_{SW(PK)} = I_{LOGIC(EFFECTIVE)} + \frac{V_{IN} \times (1 - D)}{2 \times f_{SW} \times L} \times D \quad (14)$$

Inductor Selection (Buck Converter)

The buck converter is designed for use with inductors in the range 6.8µH to 15µH, and is optimized for 10µH. The inductor must be capable of supporting the peak current calculated by Equation 14 without saturating. Alternatively, a more conservative approach can be used in which an inductor is selected whose saturation current is greater than the maximum switch current limit (2.25A).

Another important parameter is DC resistance, which can significantly affect the overall converter efficiency. Physically larger inductors tend to have lower DC resistance (DCR) because they can use thicker wire. The type and core material of the inductor can also affect efficiency, sometimes by as much as 10%. Table 4 shows some suitable inductors.

Table 4. Buck Converter Inductor Selection

PART NUMBER	INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (L×W×H mm)	I_{SAT} / DCR
CDRH8D43	10 µH	Sumida	8.3 × 8.3 × 4.5	4A / 29 mΩ
CDRH8D38	10 µH	Sumida	8.3 × 8.3 × 4	3A / 38 mΩ
MSS 1048-103	10 µH	Coilcraft	10.5 × 10.5 × 5.1	4.8A / 26 mΩ
744066100	10 µH	Wuerth	10 × 10 × 3.8	4A / 28 mΩ

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Rectifier Diode Selection (Buck Converter)

To achieve good efficiency, the rectifier diode should be a Schottky type. Its reverse voltage rating should be higher than the maximum V_{IN}. The average rectified forward current through the diode can be calculated using Equation 15.

$$I_{RECT(AVG)} = I_{LOGIC(EFFECTIVE)} \times (1 - D) \quad (15)$$

A Schottky diode with 2A average rectified current rating is adequate for most applications. Smaller diodes can be used in applications with lower output current, however, the diode must be able to handle the power dissipated in it, which can be calculated using Equation 16.

$$P_{RECT} = I_{RECT(AVG)} \times V_F \quad (16)$$

Table 5. Buck Converter Rectifier Diode Selection

PART NUMBER	V_R / I_{AVG}	V_F	$R_{\theta JA}$	SIZE	COMPONENT SUPPLIER
MBRS320	20V / 3A	0.44V at 3A	46°C/W	SMC	International Rectifier
SL22	20V / 2A	0.44V at 2A	75°C/W	SMB	Vishay Semiconductor
SS22	20V / 2A	0.50V at 2A	75°C/W	SMB	Fairchild Semiconductor

Output Capacitance Selection (Buck Converter)

To minimize output voltage ripple, the output capacitors should be good quality ceramic types with low ESR. The buck converter is stable over a range of output capacitance values, but an output capacitance of 44µF is a good starting point for typical applications.

POSITIVE CHARGE PUMP CONTROLLER

The positive charge pump is driven directly from the boost converter's switch node and regulated by controlling the current through an external PNP transistor. An internal block diagram of the positive charge pump is shown in Figure 27 and a typical application circuit in Figure 28.

During normal operation, the TPS65170 is able to provide up to 5mA of base current and is designed to work best with transistors whose DC gain (h_{FE}) is between 100 and 300. The charge pump is protected against short-circuits on its output, which are detected when the voltage on the charge pump's feedback pin (V_{FBP}) is below 100mV. During short-circuit mode, the base current available from the CTRLP pin is limited to 55µA (typical). Note that if a short-circuit is detected during normal operation, boost converter switching is also halted until V_{FBP} > 100mV.

NOTE

The emitter of the external PNP transistor should always be connected to V_S, the output of the boost converter at the output side of the isolation switch. The TPS65170 uses the CTRLP pin to sense the voltage across the isolation switch and control boost converter start-up. Connecting the emitter of the external PNP transistor to any other voltage (e.g., V_{IN}) will prevent proper start-up of the boost converter and positive charge pump.

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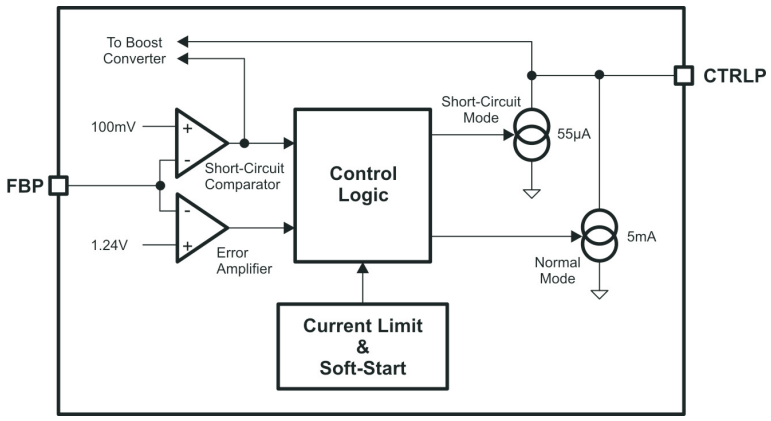


Figure 27. Positive Charge Pump Internal Block Diagram

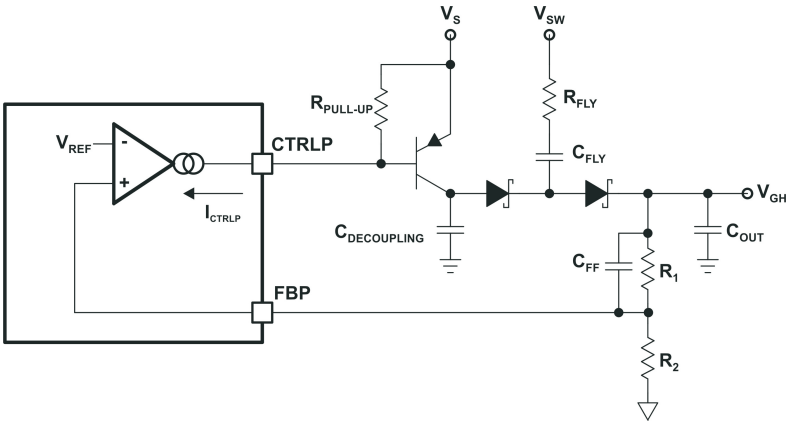


Figure 28. Positive Charge Pump Application Circuit

POSITIVE CHARGE PUMP DESIGN PROCEDURE

Setting the Output Voltage (Positive Charge Pump)

The positive charge pump's output voltage is programmed by a resistor divider according to Equation 17.

$$V_{GH} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \tag{17}$$

Where V_{REF} is the TPS65170's internal 1.24V reference.

Rearranging Equation 17, the values of R1 and R2 can be easily calculated:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \tag{18}$$

A current of the order of 1mA through the resistor network ensures good accuracy and increases the circuit's immunity to noise. It also ensures a minimum load on the charge pump, which reduces output voltage ripple under no-load conditions. A good approach is to assume a value of about 1.2kΩ for the lower resistor (R2) and then select the upper resistor (R1) to set the desired output voltage.

Note that the maximum voltage in an application is determined by the boost converter's output voltage and the voltage drop across the diodes and PNP transistor. For a typical application in which the positive charge pump is configured as a voltage doubler, the maximum output voltage is given by Equation 19.

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$$V_{GH(MAX)} = (2 \times V_S) - (2 \times V_F) - V_{CE} \quad (19)$$

Where V_S is the output voltage of the boost converter, V_F is the forward voltage of each diode and V_{CE} is the collector-emitter voltage of the PNP transistor (recommended to be at least 1V, to avoid transistor saturation).

Selecting the Feed-Forward Capacitor (Positive Charge Pump)

To improve transient performance, a feed-forward capacitor connected across the upper feedback resistor (R1) is recommended. The feed-forward capacitor modifies the frequency response of the feedback network by adding the zero, which improves high frequency gain. For typical applications, a zero at 5kHz is a good place to start, in which case C_{FF} can be calculated using Equation 20.

$$C_{FF} = \frac{1}{2 \times \pi \times 5\,kHz \times R_1} \quad (20)$$

Selecting the PNP Transistor (Positive Charge Pump)

The PNP transistor used to regulate V_{GH} should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able to withstand voltages up to $2 \times V_S$ across its collector-emitter (V_{CE}).

The power dissipated in the transistor is given by Equation 21. The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design.

$$P_Q = \left[(2 \times V_S) - (2 \times V_F) - V_{GH}\right] \times I_{GH} \quad (21)$$

Where I_{GH} is the mean (not RMS) output current drawn from the charge pump.

A pull-up resistor is also required between the transistor's base and emitter. The value of this resistor is not critical, but it should be large enough not to divert significant current away from the base of the transistor. A value of 100kΩ is suitable for most applications.

Selecting the Diodes (Positive Charge Pump)

Small-signal diodes can be used for most low current applications (<50mA) and higher rated diodes for higher power applications. The average current through the diode is equal to the output current, so that the power dissipated in the diode is given by Equation 22.

$$P_D = I_{GH} \times V_F \quad (22)$$

The peak current through the diode occurs during start-up and for a few cycles may be as high as a few amps. However, this condition typically lasts for <1ms and can be tolerated by many diodes whose repetitive current rating is much lower. The diodes' reverse voltage rating should be equal to $2 \times V_S$.

Table 6. Positive Charge Pump Diode Selection

PART NUMBER	I_{AVG}	I_{PK}	V_R	V_F	COMPONENT SUPPLIER
BAV99W	150mA	1A for 1ms	75V	1V at 50mA	NXP
BAT54S	200mA	600mA for 1s	30V	0.8V at 100mA	Fairchild Semiconductor
MBR0540	500mA	5.5A for 8ms	40V	0.51 at 500mA	Fairchild Semiconductor

Selecting the Capacitors (Positive Charge Pump)

For lowest output voltage ripple, low-ESR ceramic capacitors are recommended. The actual value is not critical and 1µF to 10µF is suitable for most applications. Larger capacitors provide better performance in applications where large load transient currents are present.

A flying capacitor in the range 100nF to 1µF is suitable for most applications. Larger values experience a smaller voltage drop by the end of each switching cycle, and allow higher output voltages and/or currents to be achieved. Smaller values tend to be physically smaller and cheaper. For best performance, it is recommended to include a resistor of a few ohms (2Ω is a good value to start with) in series with the flying capacitor to limited peak currents occurring at the instant of switching.

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A collector capacitor in the range 100nF to 1µF is suitable for most applications. Larger values are more suitable for high current applications, but can affect stability.

A combination of C_{OUT} = 10µF, C_{FLY} = 1µF, and $C_{COLLECTOR}$ = 100nF is a good starting point for most applications (the final values can be optimized on a case-by-case basis if necessary).

NEGATIVE CHARGE PUMP

The negative charge pump controller uses an external NPN transistor to regulate an external charge pump circuit. The IC is optimized for use with transistors having a DC gain (h_{FE}) in the range 100 to 300; however, it is possible to use transistors outside this range, depending on the application requirements. Regulation of the charge pump is achieved by using the external transistor as a controlled current source whose output depends on the voltage applied to the FBN pin: the higher the transistor current the greater the charge transferred to the output during each switching cycle and therefore the higher (i.e., the more negative) the output voltage. The internal block diagram of the negative charge pump is shown in Figure 29 and a typical application circuit in Figure 30.

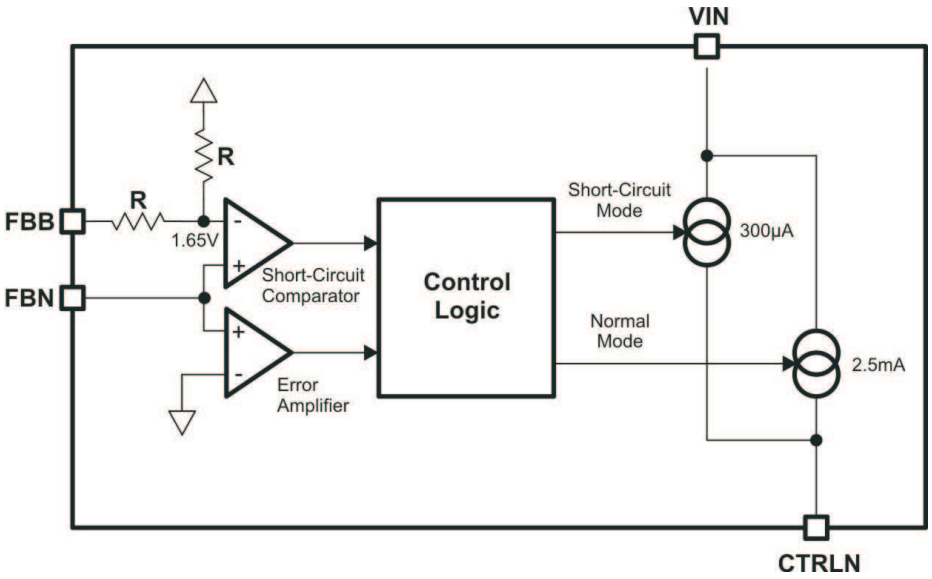


Figure 29. Negative Charge Pump Internal Block Diagram

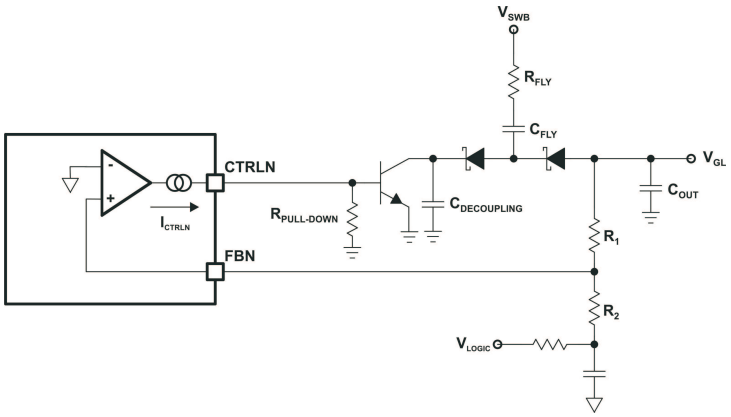


Figure 30. Negative Charge Pump Application Circuit

The TPS65170 contains a circuit to protect the negative charge pump against short circuits on its output. A short circuit condition is detected as long as the FBN pin remains above 1.65V, during which time the charge pump's output current is limited.

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To ensure proper start-up under normal conditions, circuit designers should ensure that the full load current is not drawn by the load until the feedback voltage V_{FBN} is below the short circuit threshold voltage. The value of V_{GL} beyond which the negative charge pump no longer works in short-circuit mode is given by Equation 23.

$$V_{GL(SC)} = -1.65\ V \times \left(1 - \frac{R_1}{R_2}\right) \quad (23)$$

NEGATIVE CHARGE PUMP DESIGN PROCEDURE

Setting the Output Voltage (Negative Charge Pump)

The negative charge pump's output voltage is programmed by a resistor divider according to Equation 24.

$$V_{GL} = -V_{LOGIC} \times \frac{R_1}{R_2} \quad (24)$$

Rearranging Equation 25, the values of R1 and R2 can be easily calculated.

$$R_1 = R_2 \times \frac{|V_{GL}|}{V_{LOGIC}} \quad (25)$$

A current of the order of 1mA through the resistor network ensures good accuracy and increases the circuit's immunity to noise. It also ensures a minimum load on the charge pump, which reduces output voltage ripple under no-load conditions. A good approach is to assume a value of about 3.3k for the lower resistor (R2) and then select the upper resistor (R1) to set the desired output voltage.

Note that the maximum voltage in an application is determined by the boost converter's output voltage and the voltage drop across the diodes and NPN transistor. For a typical application in which the negative charge pump is configured as a voltage inverter, the maximum (i.e., most negative) output voltage is given by Equation 26.

$$V_{GL(MAX)} = -V_{IN} + (2 \times V_F) + V_{CE} \quad (26)$$

Where V_F is the forward voltage of each diode and V_{CE} is the collector-emitter voltage of the NPN transistor (recommended to be at least 1V, to avoid transistor saturation).

Selecting the NPN Transistor (Negative Charge Pump)

The NPN transistor used to regulate V_{GL} should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able to withstand voltages up to V_{IN} across its collector-emitter (V_{CE}).

The power dissipated in the transistor is given by Equation 27. The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends on adequate PCB thermal design.

$$P_Q = \left[V_{IN} - (2 \times V_F) - |V_{GL}|\right] \times I_{GL} \quad (27)$$

Where I_{GL} is the *mean* (not RMS) output current drawn from the charge pump.

Selecting the Diodes (Negative Charge Pump)

Small-signal diodes can be used for most low current applications (<50mA) and higher rated diodes for higher power applications. The average current through the diode is equal to the output current, so that the power dissipated in the diode is given by Equation 28.

$$IP_D = I_{GL} \times V_F \quad (28)$$

The peak current through the diode occurs during start-up and for a few cycles may be as high as a few amps. However, this condition typically lasts for <1ms and can be tolerated by many diodes whose repetitive current rating is much lower. The diodes' reverse voltage rating should be equal to at least $2 \times V_{IN}$.

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Table 7. Negative Charge Pump Diode Selection

PART NUMBER	I_{AVG}	I_{PK}	V_R	V_F	COMPONENT SUPPLIER
BAV99W	150mA	1A for 1ms	75V	1V at 50mA	NXP
BAT54S	200mA	600mA for 1s	30V	0.8V at 100mA	Fairchild Semiconductor
MBR0540	500mA	5.5A for 8ms	40V	0.51 at 500mA	Fairchild Semiconductor

Selecting the Capacitors (Negative Charge Pump)

For lowest output voltage ripple, low-ESR ceramic capacitors are recommended. The actual value is not critical and 1µF to 10µF is suitable for most applications. Larger capacitors provide better performance in applications where large load transient currents are present.

A flying capacitor in the range 100nF to 1µF is suitable for most applications. Larger values experience a smaller voltage drop by the end of each switching cycle, and allow higher output voltages and/or currents to be achieved. Smaller values tend to be physically smaller and cheaper.

A collector capacitor in the range 100nF to 1µF is suitable for most applications. Larger values are more suitable for high current applications but can affect stability.

A combination of C_{OUT} = 10 µF, C_{FLY} = 1µF, and $C_{COLLECTOR}$ = 100nF is a good starting point for most applications (the final values can be optimized on a case-by-case basis if necessary).

POWER SUPPLY SEQUENCING

Figure 31 shows the power supply sequencing block diagram. The four supply rails generated by the TPS65170 turn on the following sequence: first V_{LOGIC}, then V_{GL}, then V_{GH} and V_S, as shown in Figure 31.

The buck converter turns on when the supply voltage exceeds the undervoltage threshold.

When the buck converter's internal power good signal has been asserted, the reset timer starts; after the reset time is over, $\overline{RESET}$ goes high and the negative charge pump is enabled. This sequence ensures that the negative charge pump, which is driven by the switch node of the buck converter, does not attempt to draw current until the T-CON is out of reset and drawing current from V_{LOGIC}.

At the same time as the negative charge pump is enabled, an internal delay timer is started. This timer generates a delay, after which the boost converter and positive charge pump are enabled. The delay time t_{DLY} is determined by the capacitor C_{DLY} connected between the DLY pin and AGND according to Equation 29.

$$t_{DLY} = \frac{C_{DLY} \times V_{REF}}{I_{DLY}} \quad (29)$$

No special sequencing is implemented during power-down, and all power supplies are disabled if V_{IN} falls below V_{UVLO}.

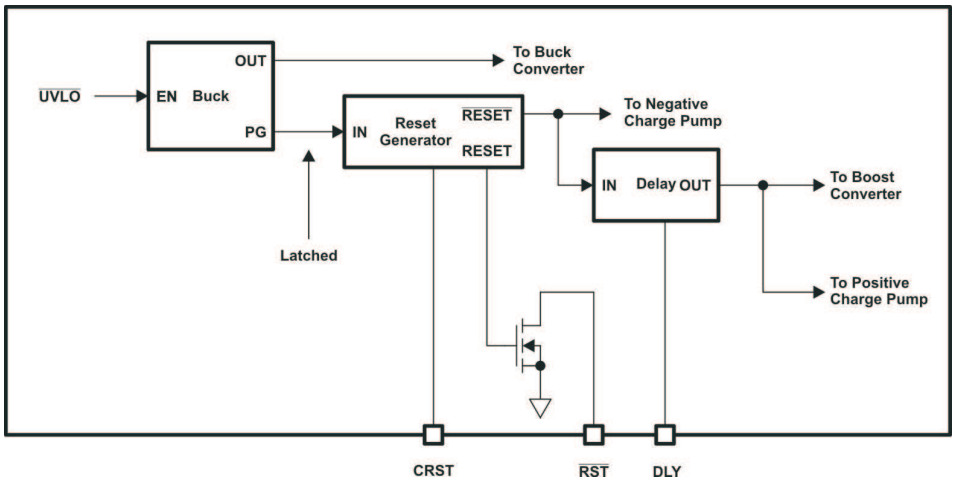


Figure 31. Power Supply Sequencing Block Diagram

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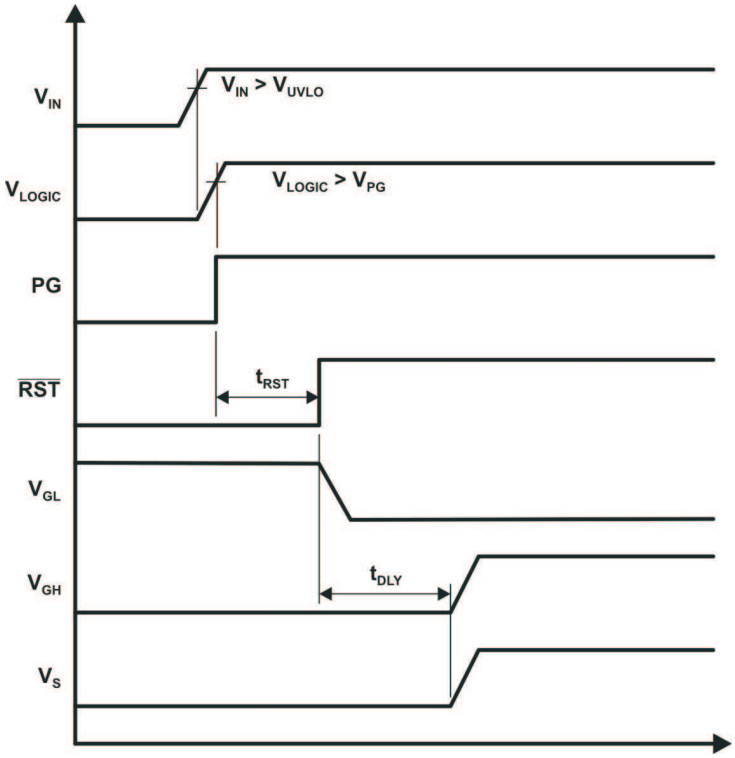


Figure 32. Power Supply Sequencing

POWER SUPPLY SEQUENCING IN DETAIL

The detailed start-up behavior of the boost converter and positive charge pump is illustrated in Figure 33.

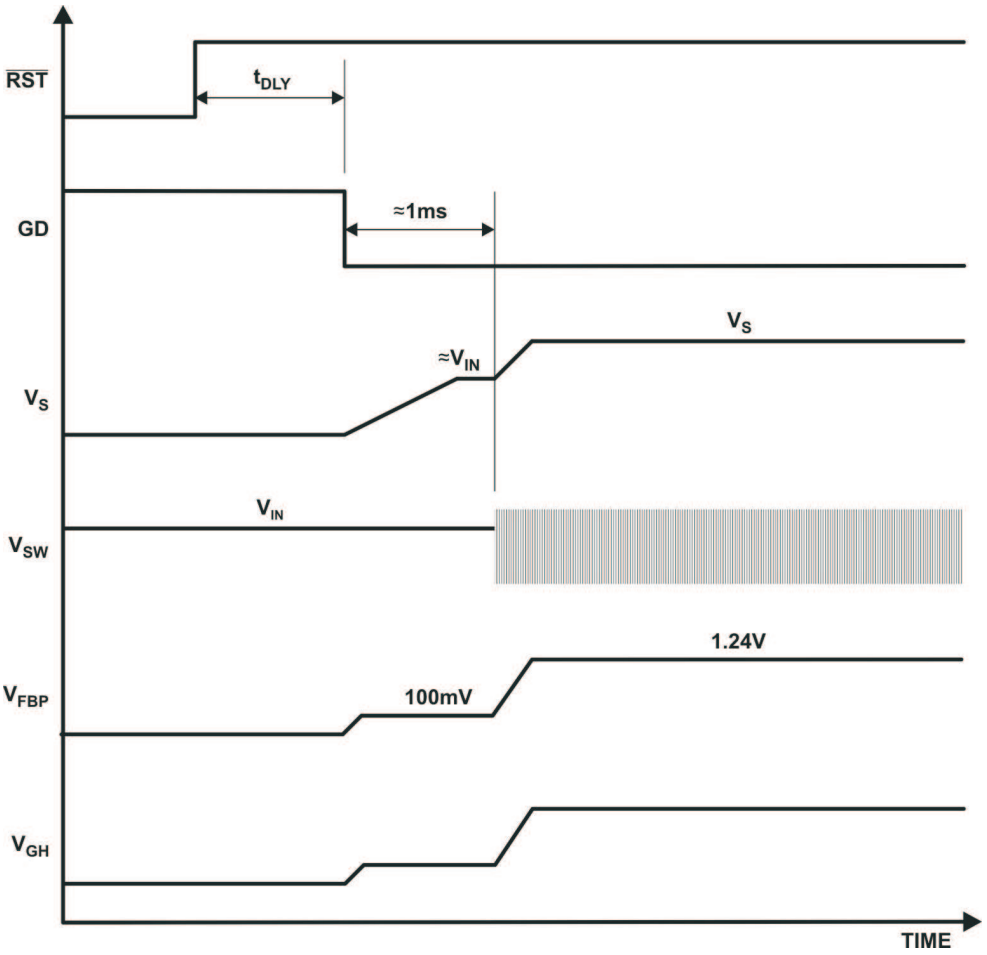


Figure 33. Boost Converter and Positive Charge Pump Detailed Start-Up Behavior

The isolation switch is enabled when the GD pin goes low, t_{DLY} seconds after $\overline{RST}$ goes high. When the isolation switch turns on, V_S rises at a rate determined by the RC network controlling the switch's gate and the amount of capacitance on the output. The TPS65170 senses the rising V_S via the CTRLP pin and 1ms after GD goes low checks that $V_S \approx V_{IN}$. If it is, then the boost converter is enabled. This scheme prevents the boost converter from switching before the isolation switch is fully enabled, which could otherwise cause overvoltage conditions to damage the switch node. If V_S does not reach $\approx V_{IN}$ within 1ms of the GD pin going low, the TPS65170 detects an error condition and the boost converter is not enabled.

The positive charge pump's short-circuit mode is enabled when the GD pin goes low. Although the boost converter is not switching at this point, there is a DC path from V_S to V_{GH} and the output ramps up as current flows into the collector capacitor and output capacitors. When V_{FBP} reaches 100mV the IC determines that no short-circuit exists and the output current from the CTRLP pin is disabled temporarily. (If there is no significant load connected to V_{GH}, the output voltage will remain almost constant, held-up by the output capacitance; if there is a load, the output voltage will decay.) When the boost converter starts switching, the positive charge pump's normal operation is enabled and V_{GH} ramps up to its programmed value. (Note that the positive charge pump implements a soft-start characteristic that ramps the current available from the CTRLP pin over time. This causes the collector voltage of the regulating PNP to temporarily go negative.)

RESET GENERATOR

The reset generator generates an active low signal that can used to reset the timing controller used in LCD applications. The $\overline{RST}$ output is an open-drain type and requires an external pull-up resistor. This signal is typically pulled up to the 3.3V supply generated by the buck converter, which also supplies the timing controller's I/O functions.

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Reset pulse timing starts when the buck converter's internal power good signal is asserted and its duration is set by the size of the capacitor connected between the CRST pin and AGND, as described by Equation 30.

$$t_{RST} = \frac{C_{RST} \times V_{REF}}{I_{RST}} \quad (30)$$

The duration of the reset pulse also affects power supply sequencing, as the boost converter and positive charge pump are not enabled until the reset pulse is finished. In applications that do not require a reset signal the $\overline{RST}$pin can be left floating or tied to AGND. This will not prevent boost converter or positive charge pump from starting.

If the CRST pin is left open circuit, the duration of the reset pulse will be close to zero (determined only by the parasitic capacitance present), and the boost converter and positive charge pump will start up instantaneously.

Alternatively, the CRST pin can also be used to enable the boost converter and charge pumps by connecting an 3.3V logic level ENABLE signal via a 10kΩ resistor, as shown in Figure 34. Using this scheme, the buck converter starts as soon as V_{IN} exceeds the UVLO threshold, but the negative charge pump is not enabled until ENABLE goes high. RST also remains low until ENABLE goes high. The boost regulator and positive charge pump enabled t_{DLY} seconds after ENABLE goes high, where t_{DLY} is defined by the capacitor connected to the DLY pin. The resulting power supply sequencing is shown in Figure 35.

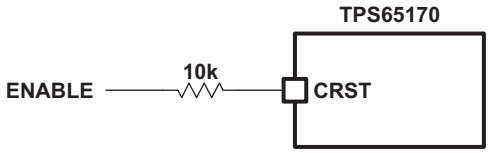


Figure 34. Using an ENABLE Signal to Control Boost Converter and Charge Pumps

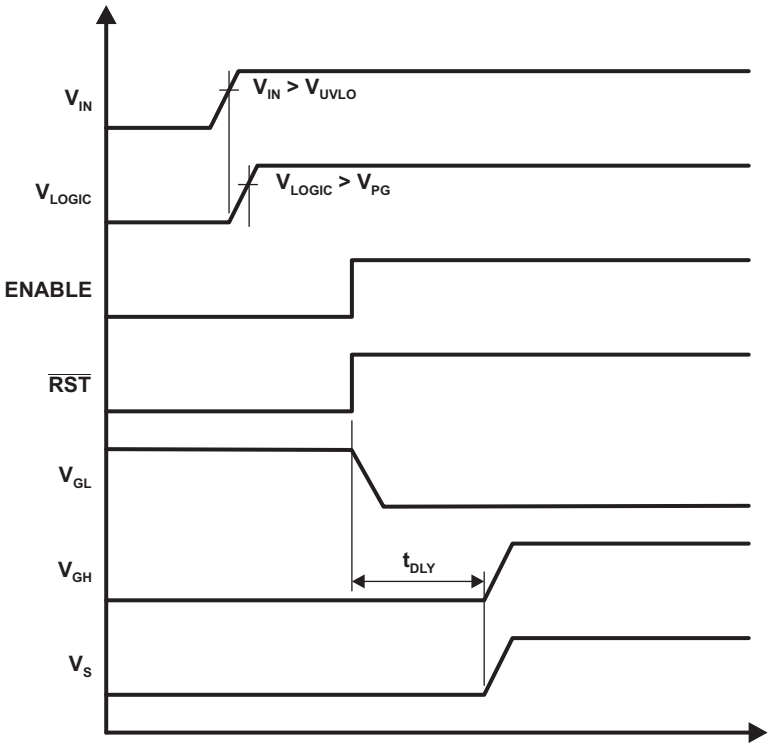


Figure 35. Power Supply Sequencing Using an Enable Signal

Undervoltage Lockout

An undervoltage lockout function inhibits the device if the supply voltage V_{IN} is below the minimum needed for proper operation.

Thermal Shutdown

A thermal shutdown function automatically disables all functions if the device's junction temperature exceeds ≈150°C. The device automatically starts operating again once it has cooled down to ≈140°C.

APPLICATION INFORMATION

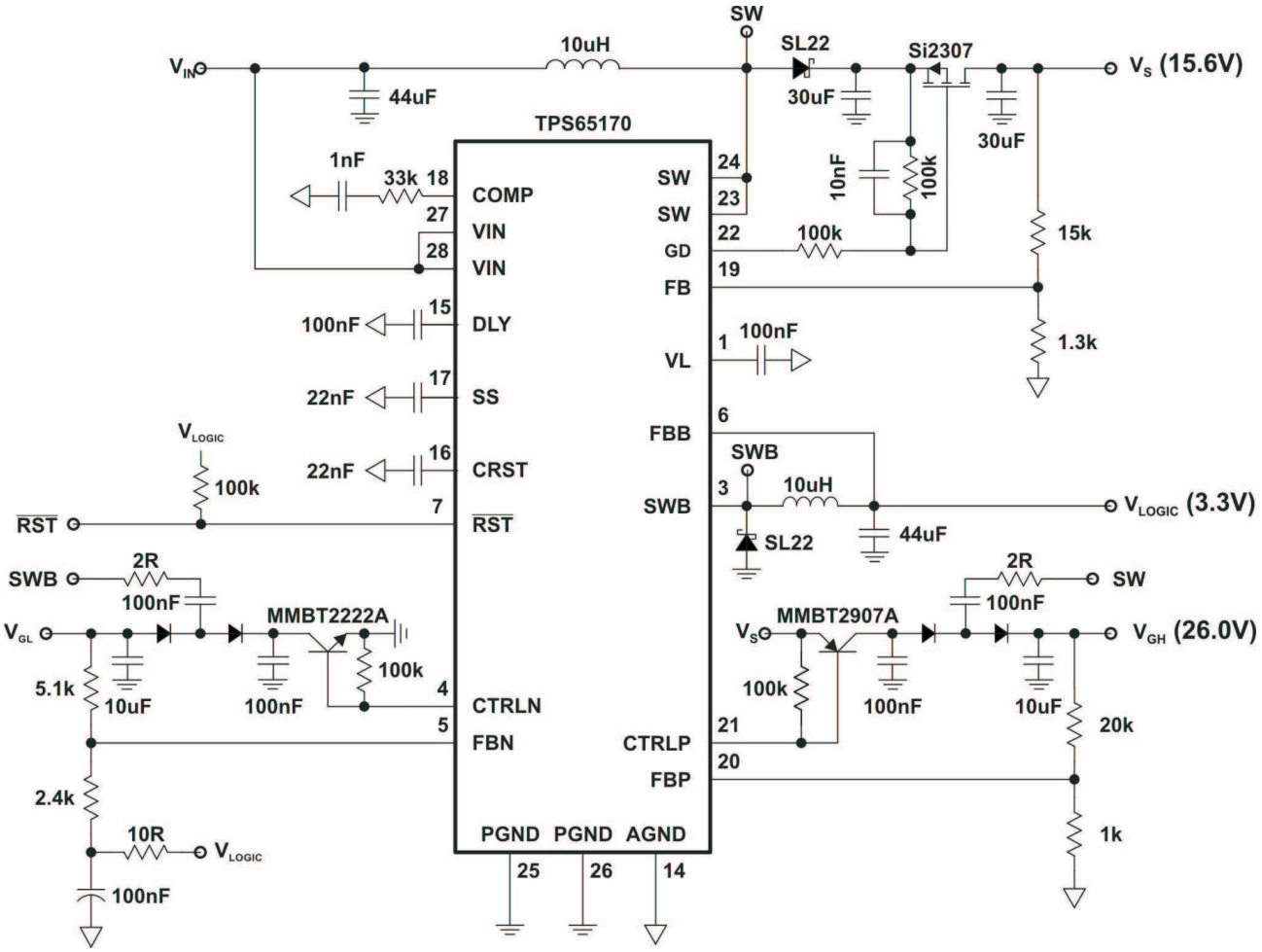


Figure 36. Typical LCD Bias Application Circuit

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65170RHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65170	Samples
TPS65170RHDT	ACTIVE	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65170	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

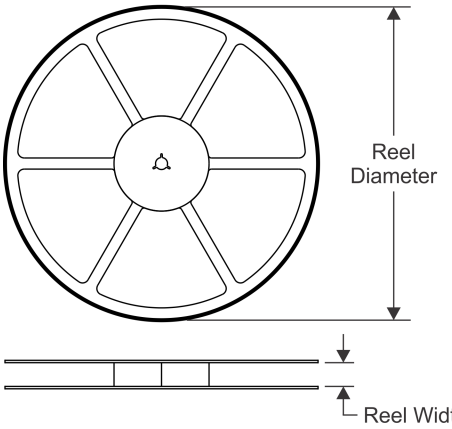
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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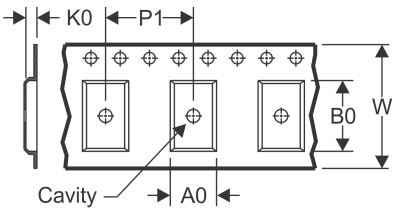
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

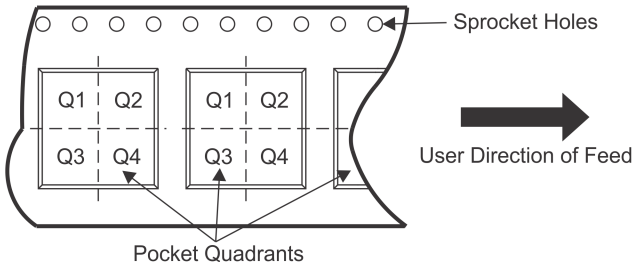


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

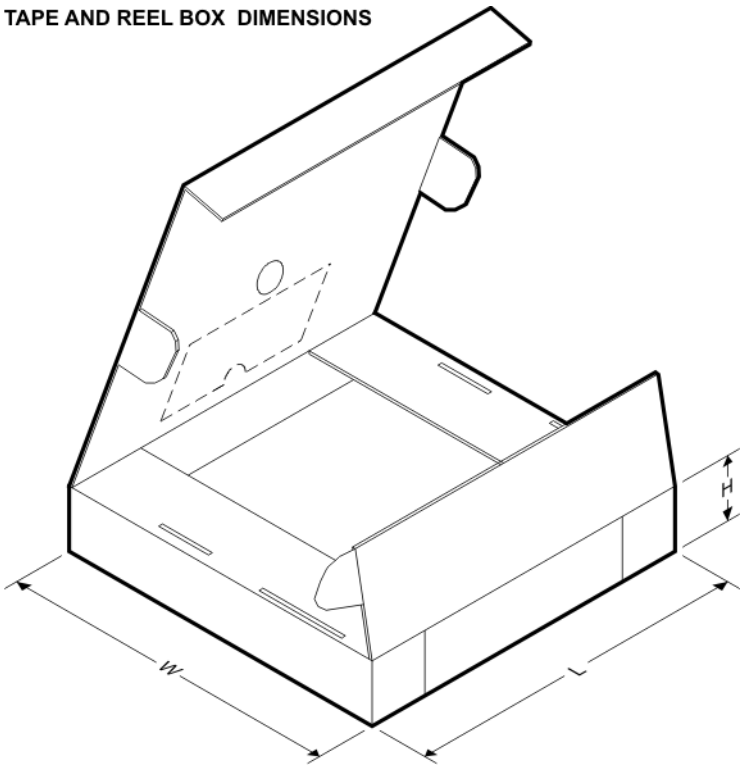
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65170RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65170RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS65170RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65170RHDR	VQFN	RHD	28	3000	367.0	367.0	35.0
TPS65170RHDR	VQFN	RHD	28	3000	367.0	367.0	35.0
TPS65170RHDT	VQFN	RHD	28	250	210.0	185.0	35.0

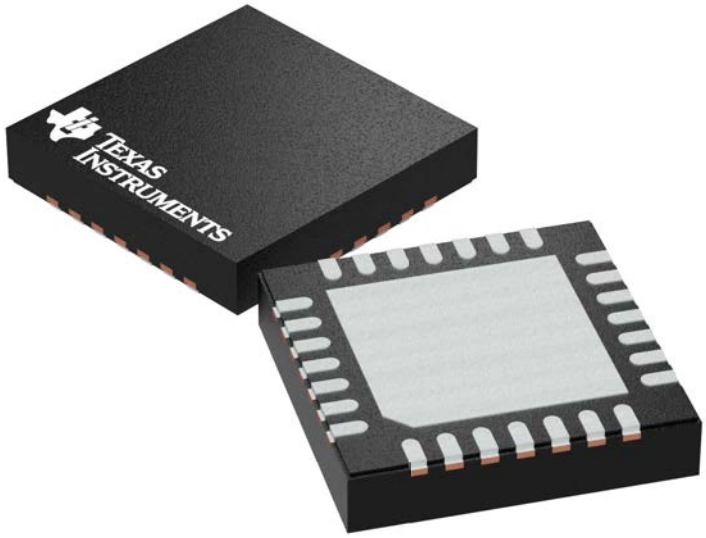
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

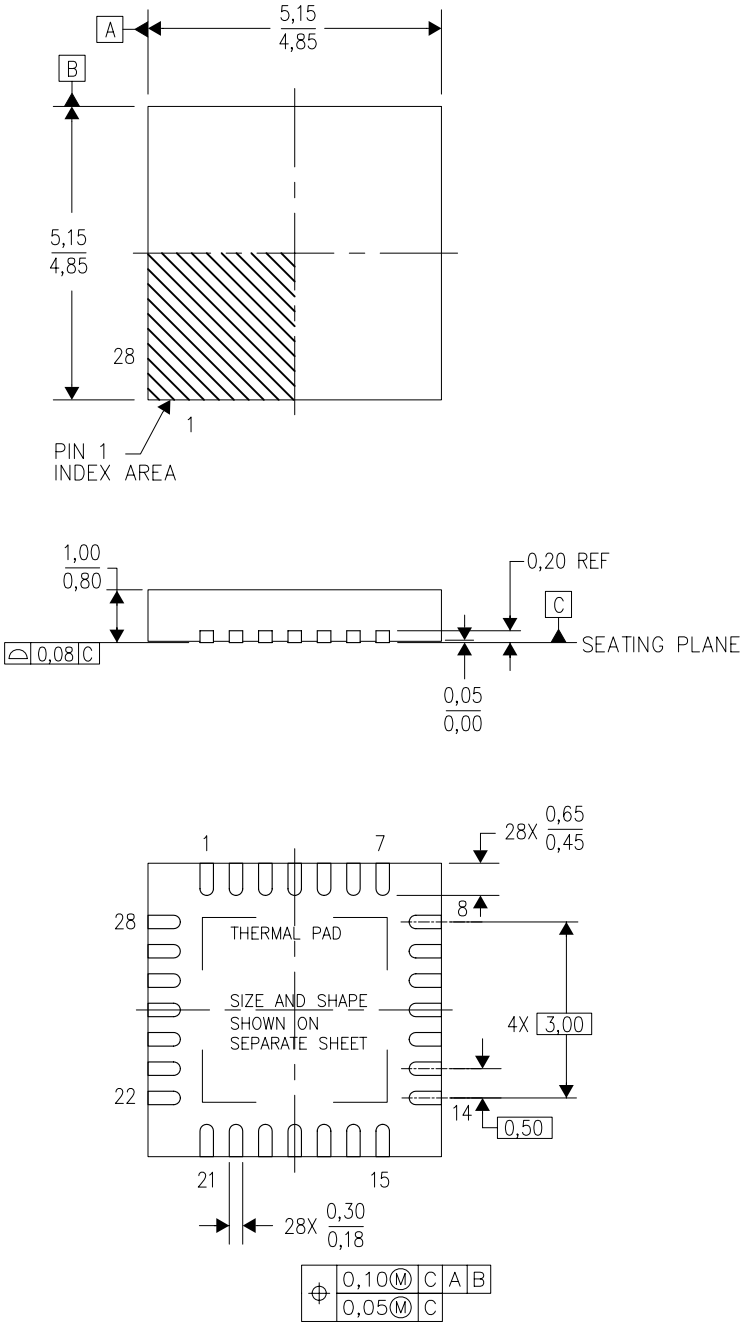
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204400/G

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



4204400/F 09/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

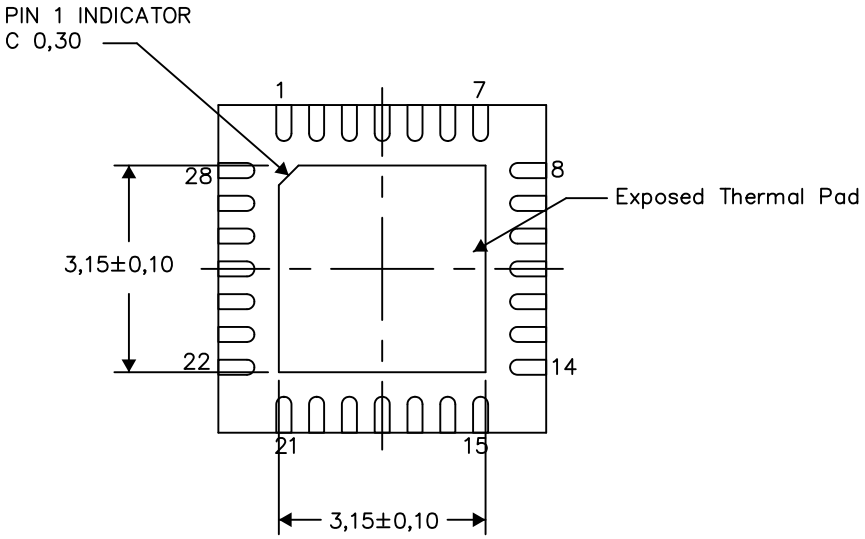
RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



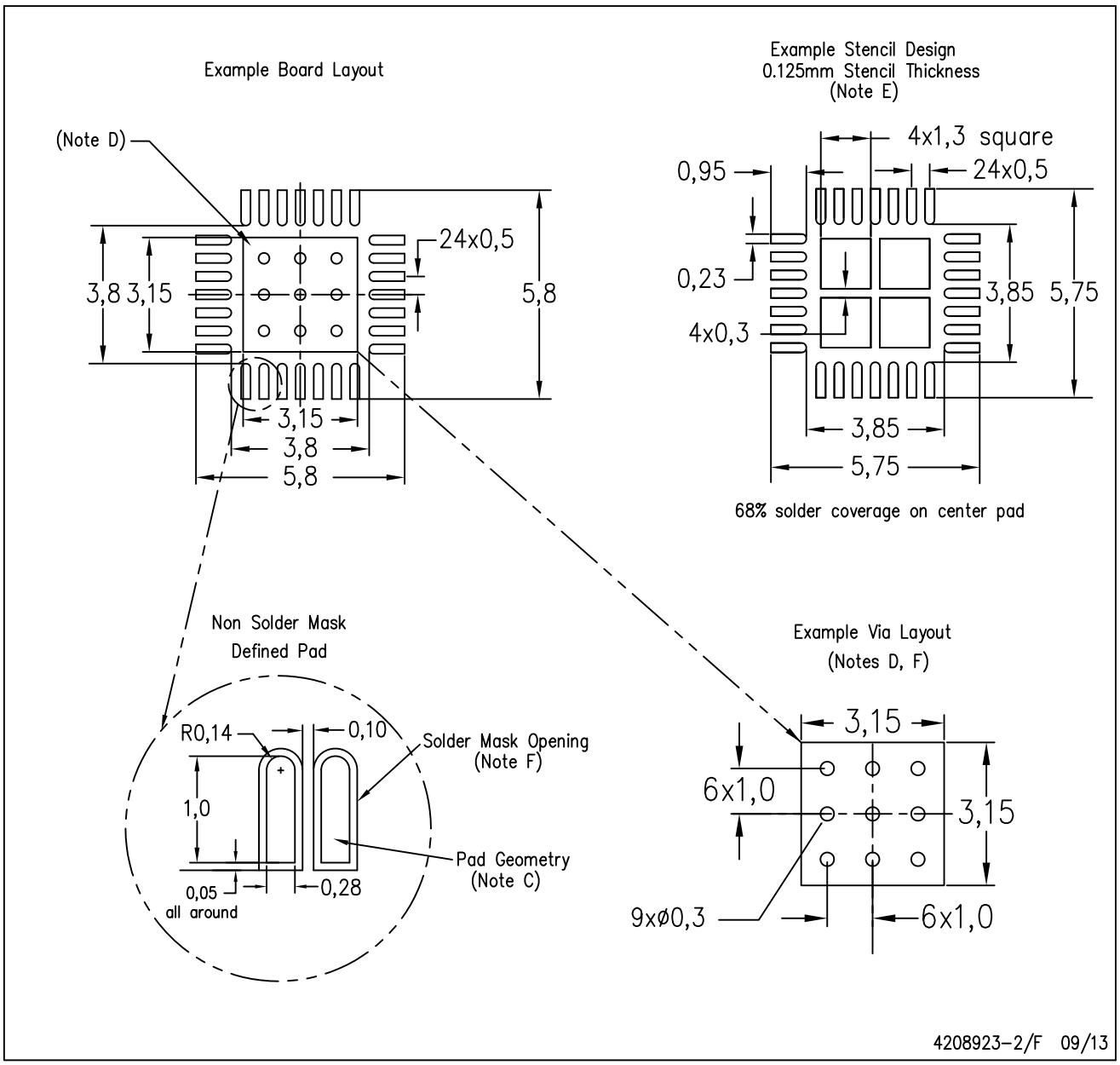
Bottom View

Exposed Thermal Pad Dimensions

4206358–2/L 05/15

NOTE: All linear dimensions are in millimeters

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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