Compact LCD Bias IC With High Speed Amplifiers for TV and Monitor TFT-LCD Panels

FEATURES

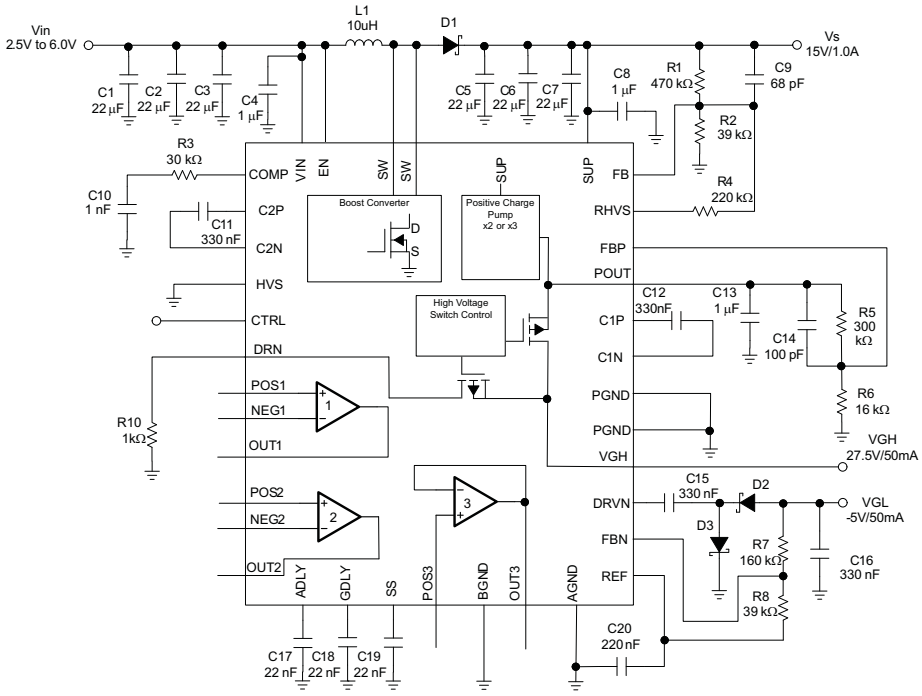
- 2.5 V to 6.0 V Input Voltage Range
- Vs Output Voltage up to 18 V
  - 1%-Accurate Boost Converter With 4.5 A Switch Current
  - 600 kHz Fixed Frequency PWM Operation
  - Overvoltage Protection
  - Adjustable Softstart
- Regulated Positive Charge Pump Converter VGH
- Integrated Gate Voltage Shaping of VGH
- Regulated Negative Charge-Pump Driver VGL
- Adjustable Sequencing for Vs and VGH
- 3 Integrated High-Speed Operational Amplifiers
  - 50 MHz 3 db Bandwidth
  - Slew Rate 45 V/μs
  - 215 mA Short Circuit Current
- High Voltage Test Mode (HVS)
- Thermal Shutdown
- 40-Pin 5×5-mm QFN Package

APPLICATIONS

- LCD Monitor
- LCD TV Panel

DESCRIPTION

The TPS65165 is a Compact LCD Bias IC with 3 high-speed operational amplifiers for gamma correction and/or VCOM supply. The device generates all 3 voltage rails for TFT-LCD displays (Vs, VGL and VGH). The device incorporates a high-voltage switch that can be controlled by a logic signal from the timing controller (TCON) to provide the gate-voltage modulation for VGH. If this function is not required, the CTRL pin can be tied high.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2006–2007, Texas Instruments Incorporated

The device also features a high-voltage stress test, where the output voltage of VGH is typically set to 30 V, and the output voltage of Vs is programmable to any higher voltage. The high-voltage stress test is enabled by pulling the HVS pin high. Adjustable sequencing is implemented, and can be programmed by selecting the capacitor values connected to ADLY and GDLY. The device consists of a boost converter to provide the source voltage Vs operating at a fixed switching frequency of 600 kHz. A fully integrated positive charge pump, switching automatically between doubler and tripler mode provides an adjustable regulated TFT gate on voltage VGH. A negative charge pump driver provides adjustable regulated output voltage VGL. To minimize external components the charge pumps for VGH and VGL operate at a fixed switching frequency of 1.2 MHz. The device includes safety features like overvoltage protection of the boost converter, short circuit protection of VGH and VGL as well as thermal shutdown.

ORDERING INFORMATION(1)

T_A	ORDERING	QFN PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65165RSBR	RSB	TPS65165

(1) The TPS65165RSBR is available taped and reeled and shipped in quantities of 3000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
	Input voltage range V_{IN}(2)		–0.3 V to 7.0	V
	Voltage range at EN, CTRL, HVS		–0.3 V to 7.0	V
	Voltage on	SUP	22	V
		SW	25	
		POUT, VGH, DRN	32	
	Peak switch current		Internally limited	V
	ESD rating	HBM	2	kV
		MM	200	V
		CDM	750	V
	Continuous total power dissipation		See Dissipation Rating Table	
T_J	Operating junction temperature range		–40 to 150	°C
T_A	Operating ambient temperature range		–40 to 85	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$	T_A < 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
40-pin QFN	30°C/W	3.3 W	1.8 W	1.3 W

(1) Exposed thermal die is soldered to the PCB using thermal vias. Refer to Texas Instruments Application report (SLUA271) QFN/SON PCB Attachment.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.5		6.0	V
T_A	Operation ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_{IN}=5.0V, Vs=15V, HVS=low, EN=CTRL=high, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.5		6.0	V
I_{QVIN}	No load quiescent current into VIN	Device not switching		1	1.5	mA
I_{QSUP}	No load quiescent current into SUP	Device not switching		20	25	mA
I_{SD}	Shutdown current into VIN	Vin=6V			1	µA
	Shutdown current into SUP	Vin=6V, SUP = Vin-0.5V			8	
V_{UVLO}	Under-voltage lockout threshold	Vin rising		2.3	2.5	V
		Vin falling		2.2	2.3	V
	Thermal shutdown	Temperature rising		155		°C
	Thermal shutdown hysteresis			5		°C
LOGIC SIGNALS EN, CTRL, HVS						
V_{th}	Threshold voltage	Vin = 2.5 V to 6.0 V	0.4		1.4	V
I_I	Input leakage current			±0.01	±0.1	µA
HIGH VOLTAGE STRESS TEST (HVS)						
V_{POUT}	Positive charge pump output voltage	HVS = high	28.5	30	31.5	V
RHVS	RHVS pull down resistance	HVS = high, Vin = 2.5 V to 6.0 V, I_{HVS} = 100 µA	0.5	1	1.5	kΩ
I_{RHVS}	RHVS leackage current	HVS = low, V_{RHVS} = 1.5 V			100	nA
MAIN BOOST CONVERTER Vs						
Vs	Output voltage range		7		18	V
V_{FB}	Feedback regulation voltage		1.136	1.146	1.154	V
I_{FB}	Feedback input bias current	V_{FB} = 1.146			100	nA
$R_{DS(ON)}$	N-MOSFET on-resistance (Q1)	Vs = 15 V, I_{SW} = 500 mA, Vs = 7 V, I_{SW} = 500 mA		75	140	mΩ
	P-MOSFET on-resistance (Q2)	Vs = 15 V; I_{SW} = 100 mA, Vs = 7 V; I_{SW} = 100 mA		10	16	Ω
I_{MAX}	Maximum P-MOSFET peak switch current (Q2)				1	A
I_{LIM}	N-MOSFET switch current limit (Q1)		4.4	5.5	6.6	A
I_{leak}	Switch leakage current	V_{SW} = 15 V			10	µA
V_{ovp}	Output overvoltage protection	FB = GND, Vout rising	19.5	20	21	V
f_{OSC}	Oscilator frequency		480	600	720	kHz
	Line regulation	Vin=3.0V to 6.0V, Iout=100mA		0.045		%/V
	Load regulation	Iout=100mA to 700mA, Vin=5.0V		0.23		%/A
NEGATIVE CHARGE PUMP VGL						
VGL	Output voltage range				–2	V
V_{FB}	Feedback regulation voltage		–48	0	48	mV
I_{FB}	Feedback input bias current	V_{FB} = 0 V			100	nA
V_{ref}	Reference voltage	V_{IN} = 2.5 V to 6 V, I_{REF} = 10µ A	1.205	1.213	1.219	V
R_{DSon}	Q7 P-Channel switch RDSon	I_{DRVN} = 40 mA		4.4		Ω
V_{DropN}	Current sink voltage drop(1)	I_{DRN} = 40 mA, V_{FBN} = $V_{FBNnominal}$– 5%		130	300	mV
		I_{DRN} = 100 mA, V_{FBN} = $V_{FBNnominal}$– 5%		280	450	mV
POSITIVE CHARGE PUMP (POUT)						
V_{POUT}	Output voltage range				30	V
V_{FB}	Feedback regulation voltage	CTRL = GND, VGH = open	1.187	1.214	1.238	V
I_{FB}	Feedback input bias current	FBO = 1.214 V			100	nA

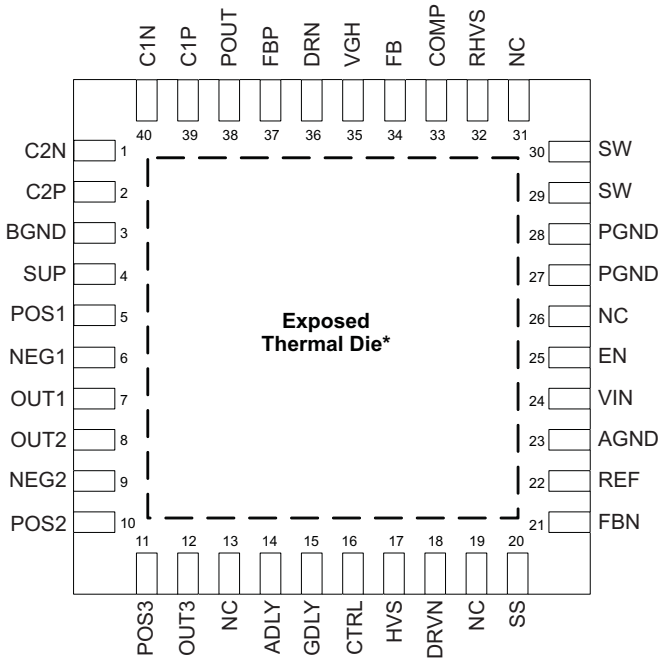
(1) The maximum charge pump output current is half the drive current $I_{DRN}$of the internal current source or sink

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=5.0V, Vs=15V, HVS=low, EN=CTRL=high, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vd	D1–D4 Schottky diode forward voltage	I_{D1-D4} = 40 mA		610	800	mV
Reff	Effective output resistance	Doubler Mode (x2); I_{POUT} = 20 mA		94		Ω
		Doubler Mode (x2); I_{POUT} = 50 mA		63		Ω
		Tripler Mode (x3); I_{POUT} = 20 mA		141		Ω
		Tripler Mode (x3); I_{POUT} = 50 mA		94		Ω
HIGH VOLTAGE SWITCH VGH						
R_{DSon}	POUT to VGH RDSon	CTRL = high, P_{OUT} = 27 V, I = 20 mA		8.5	16	Ω
	DRN to VGH RDSon	CTRL = low, V_{DRN} = 5 V, I = 20 mA		38	62	Ω
I_{DRN}	DRN input current	CTRL = low, V_{VGH} = V_{DRN}		10		µA
t_{dly}	CTRL to VGH propagation delay	CTRL = high to low, P_{OUT} = 27 V, VDRN = GND		125		ns
R_{VGH}	VGH pull down resistance	EN = low, I = 20 mA		1		kΩ
CONTROL AND SOFTSTART ADLY, GDLY, SS						
I_{ADLY}	Drive current into delay capacitor ADLY	V_{ADLY} = 1.213 V	3.5	4.8	6.2	µA
I_{GDLY}	Drive current into delay capacitor GDLY	V_{ADLY} = 1.213 V	3.5	4.8	6.2	µA
I_{SS}	SS charge current	V_{SS} = 0 V	2.8	4.5	6.2	µA
OPERATIONAL AMPLIFIERS 1, 2, 3						
Vos	Input offset voltage	V_{CM} = Vs/2	–15	3	18	mV
I_B	Input bias current	V_{CM} = Vs/2		0	3	µA
V_{CM}	Common mode input voltage range		0		Vs	V
CMRR	Common mode rejection ratio	V_{CM} = 7.5 V	55	75		dB
A_{VOL}	Open loop gain	0.5 V ≤ Vout ≤ 14.5 V, No load	50			dB
V_{OL}	Output voltage swing low	I_{OUT} = 10 mA		100	200	mV
V_{OH}	Output voltage swing high	I_{OUT} = 10 mA		100	Vs–200	mV
I_{sc}	Short circuit current		120	215		mA
I_O	Output current	V_{OUT} = 7.5V , Input offset voltage 10 mV	90	170		mA
PSRR	Power supply rejection ratio			80		dB
SR	Slew rate	A_V = 1, V_{IN} = 2 Vpp		45		V/µs
BW	– 3dB Bandwidth	A_V = 1, V_{OUT} = 50 mVpp, Output High Impedance		50		MHz
GBWP	Gain bandwidth product			26		MHz
Roff	Pull down resistor			10		kΩ

PIN ASSIGNMENT



NOTE: The exposed thermal die is connected to AGNG. NC pin is internally not connected.

TERMINAL FUNCTIONS

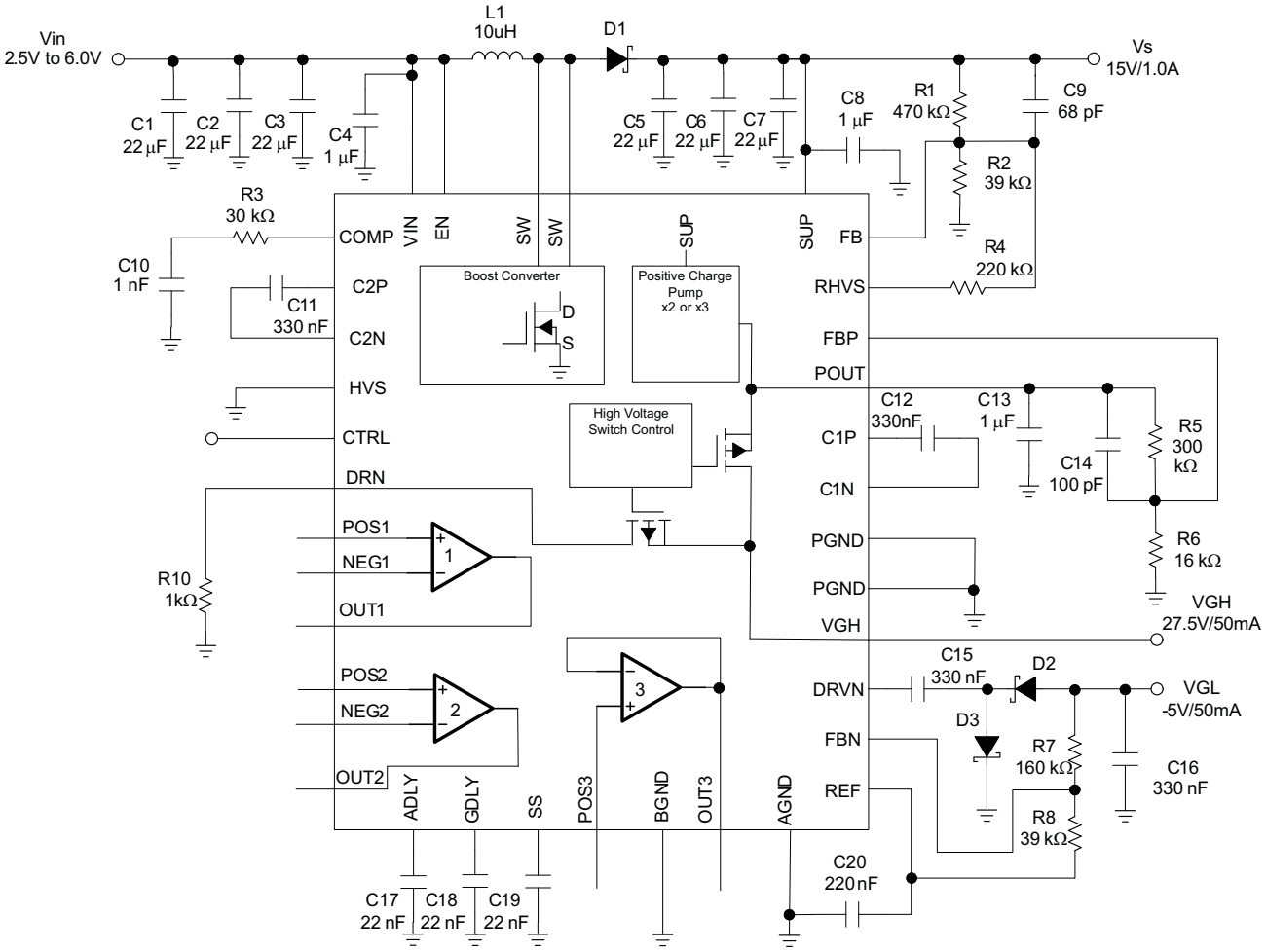
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
C2N	1	I/O	Negative terminal of the flying capacitor for the positive charge pump. Typically a 330nF flying capacitor is required.
C2P	2	I/O	Positive terminal of the flying capacitor for the positive charge pump. Typically a 330nF flying capacitor is required.
BGND	3		Low noise ground for the operational amplifier.
SUP	4	I	Supply input for the operational amplifier and charge pump stages. Connect to the main output Vs, with a 1-µF bypass capacitor.
POS1	5	I	Non-inverting input of Operational Amplifier 1.
NEG1	6	I	Inverting input of the Operational Amplifier 1.
OUT1	7	O	Output of Operational Amplifier 1. When the device is disabled, the output is pulled to GND via a 1-kΩ resistor.
OUT2	8	O	Output of Operational Amplifier 2. When the device is disabled, the output is pulled to GND via a 1-kΩ resistor.
NEG2	9	I	Inverting input of Operational Amplifier 2.
POS2	10	I	Non-inverting input of Operational Amplifier 2.
POS3	11	I	Non-inverting input of Operational Amplifier 3.
OUT3	12	O	Output of Operational Amplifier 3. When the device is disabled, the output is pulled to GND via a 1-kΩ resistor.
NC	13, 19, 26, 31		Not connected. These pin can be connected to GND to improve the thermal resistance of the package.
ADLY	14	O	Adjustable EN high-to-start-up delay of the main boost converter, negative and positive charge pump. Connect a capacitor from this pin to GND to set the desired delay time. (See *SETTING THE DELAY TIMES ADLY, GDLY*)
GDLY	15	O	Adjustable EN high-to-enable delay of the high-voltage switch Q8 (gate voltage shaping). Connect a capacitor from this pin to GND to set the desired delay time. (See *SETTING THE DELAY TIMES ADLY, GDLY*)
CTRL	16	I	Logic control input for the internal high voltage switch (gate voltage shaping).

PIN ASSIGNMENT (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
HVS	17	I	Logic control input to enable High Voltage Stress Test. With HVS=low the high voltage stress test is disabled. With HVS=high the high voltage stress test is enabled.
DRVN	18	I/O	Drive pin for the negative charge pump converter generating VGL. Using a single stage charge pump inverts the voltage present at the main boost converter Vs and regulates it down to the desired voltage programmed by the feedback divider.
SS	20	O	Softstart for the main boost converter generating Vs. Connect a capacitor to this pin to set the softstart time.
FBN	21	I	Feedback of the negative charge pump converter.
REF	22	O	Reference output. Connect a 220-nF capacitor directly from REF pin to AGND to minimize possible noise coupling into the reference of the IC.
AGND	23	I	Analog Ground , positive and negative charge pump ground.
VIN	24	I	Supply pin for the IC. Bypass this pin with a 1-µF capacitor directly to GND.
EN	25	I	Enable pin of the IC. EN=high enables the IC. EN= low disables the IC. This pin must be terminated.
PGND	27, 28		Power Ground for the boost converter.
SW	29, 30	I/O	Switch pin of the boost regulator generating Vs
RHVS	32	I	This resistor sets the voltage of the boost converter Vs when the High Voltage Stress test is enabled. (HVS=high). With HVS=high the RHVS pin is pulled to GND which sets the output voltage for the boost converter. When HVS is disabled (HVS=low) the RHVS pin is high impedance.
COMP	33	O	Compensation for the regulation loop of the boost converter generating Vs.
FB	34	I	Feedback of the boost converter generating Vs.
VGH	35	O	This is the output voltage of the internal high voltage switch, controlled by the CTRL signal.
DRN	36	I/O	Connect the discharge resistor for the Gate voltage shaping to this pin.
FBP	37	I	This is the feedback for the positive charge pump converter generating VGH
POUT	38	O	Output of the positive charge pump which is internally connected to the high voltage switch Q2. Connect a 1-µF output capacitor to this pin as well as the feedback divider to set the output voltage for the positive charge pump respectively for VGH.
C1P	39	I/O	Positive terminal of the flying capacitor for the positive charge pump. Typically a 330-nF flying capacitor is required.
C1N	40	I/O	Negative terminal of the flying capacitor for the positive charge pump. Typically a 330-nF flying capacitor is required.

BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
MAIN BOOST CONVERTER (Vs)			
η	Efficiency, main boost converter Vs	vs Load current	Figure 1
	PWM operation at nominal load current		Figure 2
	PWM operation at light load current		Figure 3
	Load transient response		Figure 4
	Softstart boost converter V_S		Figure 5
	Overvoltage protection		Figure 6
SYSTEM FUCTIONALITY			
	Power-on sequencing		Figure 7
	Gate voltage shaping VGH		Figure 8
NEGATIVE CHARGE PUMP DRIVER			
	VGL	vs load current	Figure 9
POSITIVE CHARGE PUMP			
	VGH	vs load current (doubler mode)	Figure 10
VCOM BUFFERS			
	Input to output offset voltage	vs Opamp 1 load current	Figure 11
	Input to output offset voltage	vs Opamp 2 load current	Figure 12
	Input to output offset voltage	vs Opamp 3 load current	Figure 13

EFFICIENCY, MAIN BOOST CONVERTER vs LOAD CURRENT

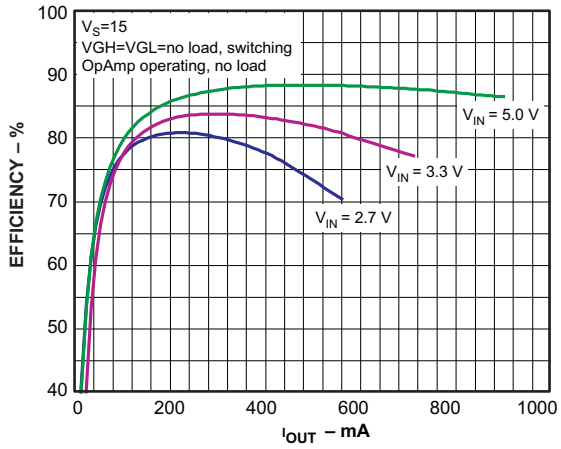


Figure 1.

PWM OPERATION NOMINAL LOAD CURRENT

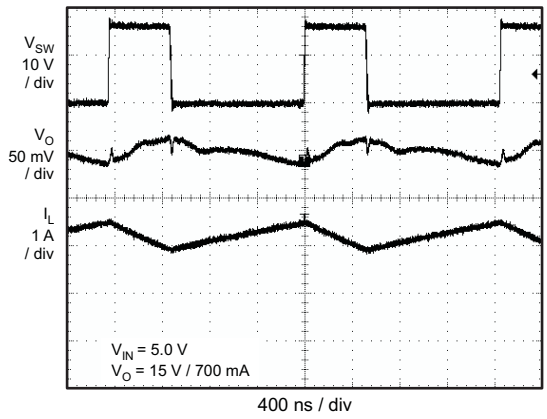


Figure 2.

PWM OPERATION AT LIGHT LOAD CURRENT

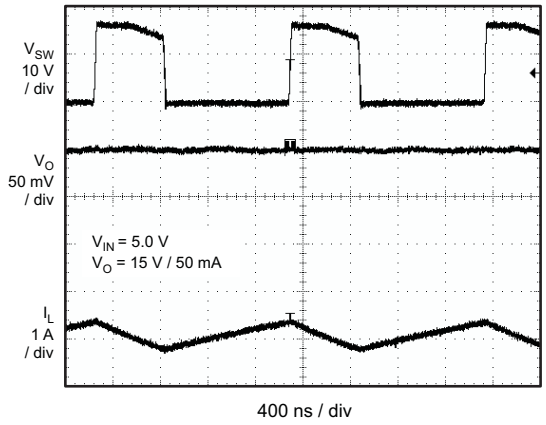


Figure 3.

LOAD TRANSIENT RESPONSE

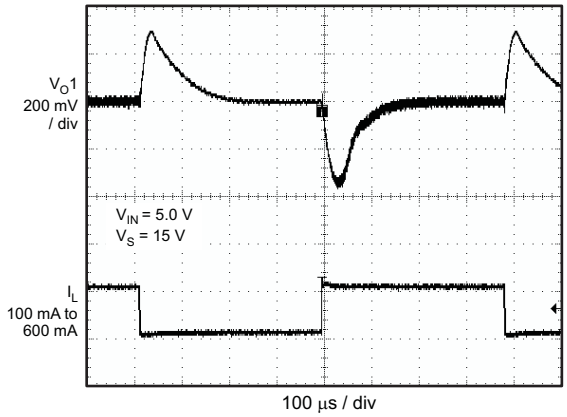


Figure 4.

SOFTSTART BOOST CONVERTER - V_S

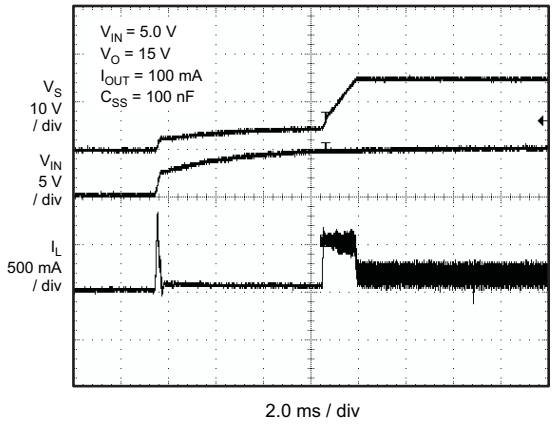


Figure 5.

OVERVOLTAGE PROTECTION

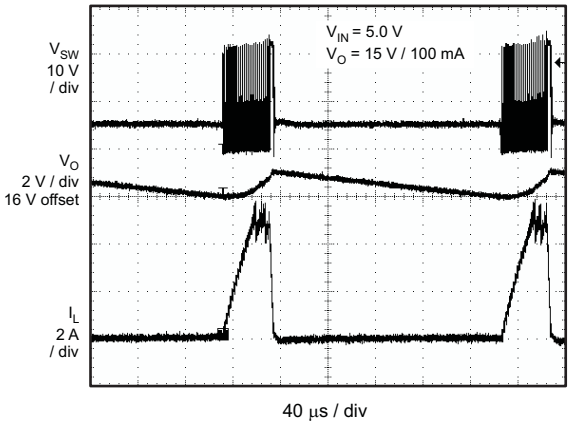


Figure 6.

POWER-ON SEQUENCING

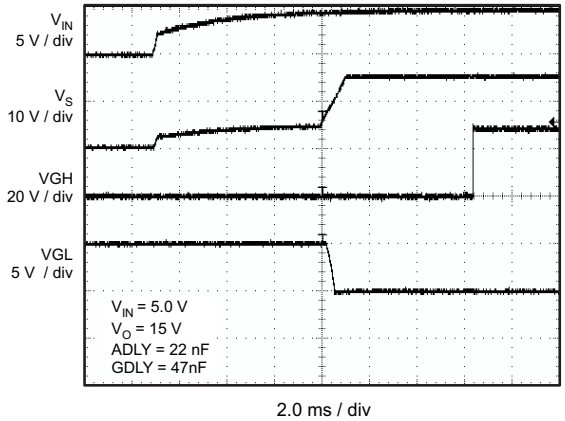


Figure 7.

GATE VOLTAGE SHAPING - VGH

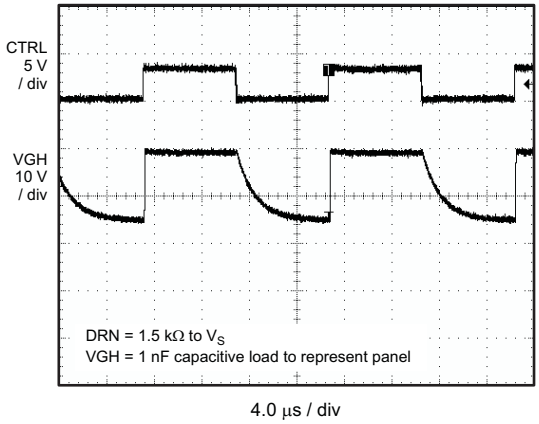


Figure 8.

VGL vs LOAD CURRENT

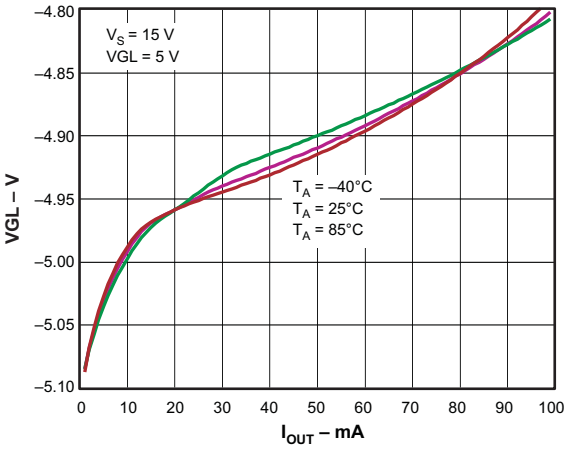


Figure 9.

VGH vs LOAD CURRENT - DOUBLER STAGE

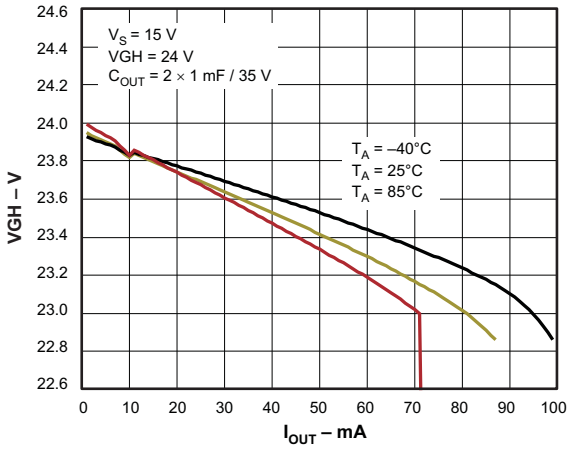


Figure 10.

INPUT TO OUTPUT OFFSET VOLTAGE vs OPAMP 1 LOAD CURRENT

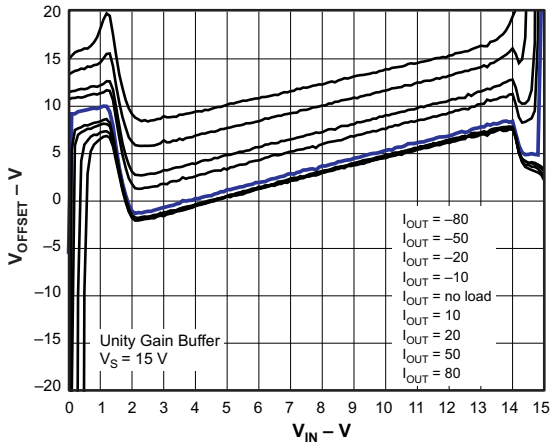


Figure 11.

INPUT TO OUTPUT OFFSET VOLTAGE vs OPAMP 2 LOAD CURRENT

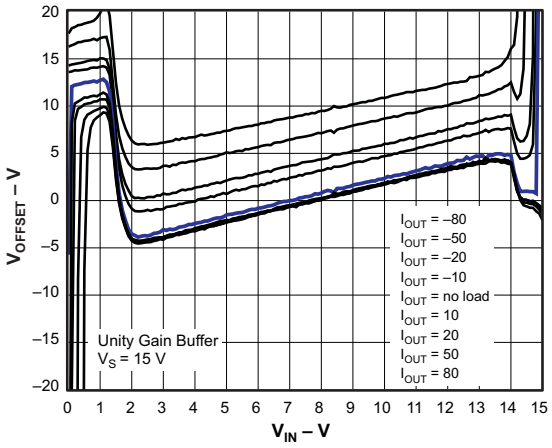


Figure 12.

INPUT TO OUTPUT OFFSET VOLTAGE vs OPAMP 3 LOAD CURRENT

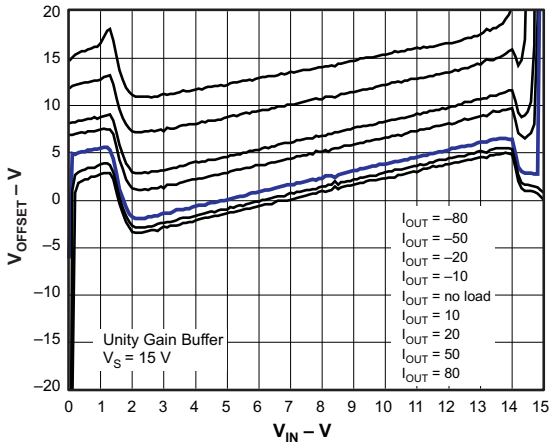


Figure 13.

APPLICATION INFORMATION

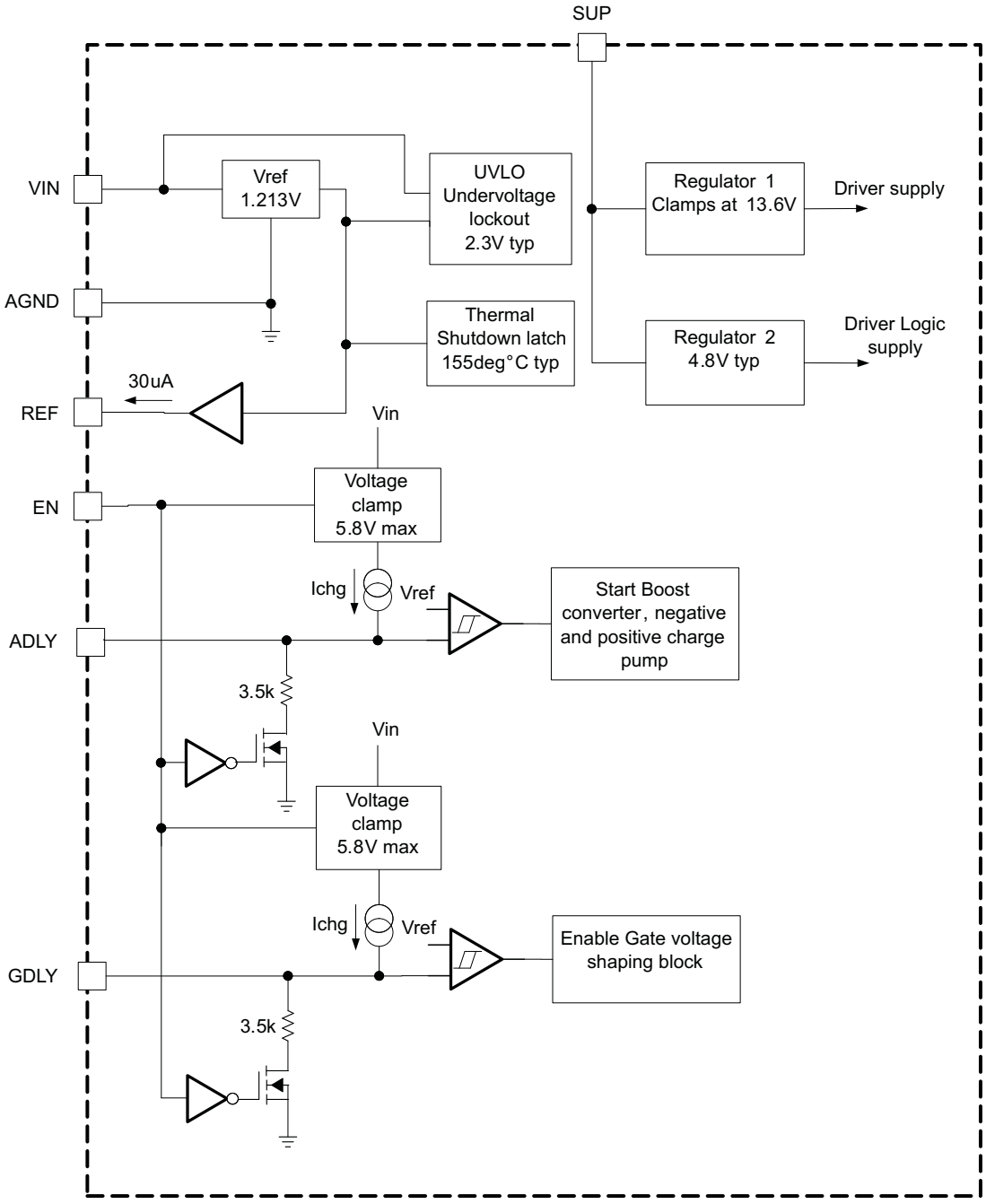


Figure 14. Control Block TPS65165

THERMAL SHUTDOWN

The thermal-shutdown feature prevents damage from excessive heat and power dissipation. Typically the thermal-shutdown threshold is 155°C. When the device enters thermal-shutdown then the device does not restart automatically. The device can only be restarted by cycling the input voltage below its undervoltage-lockout threshold or by cycling the enable EN to ground.

APPLICATION INFORMATION (continued)

UNDERVOLTAGE LOCKOUT

To avoid device malfunction at low input voltages, an undervoltage lockout is included which enables the device only when the input voltage exceeds 2.3 V.

REFERENCE OUTPUT, REF

The device provides a reference output that is used to regulate the negative charge pump. In order to have a stable reference voltage, a 220-nF bypass capacitor is required, connected directly from REF to AGND. The reference output has a current capability of 30 μA which should not be exceeded. Because of this, the feedback resistor value from FBN to REF should not be smaller than 40 kΩ.

START-UP SEQUENCING

Start-up sequencing can be controlled by adjusting the delay times ADLY and GDLY. After the delay time set by ADLY passed by, the boost converter, negative and positive charge pumps start at the same time. VGH will only go high once the delay time, set by GDLY passed by and the signal applied to CTRL is high.

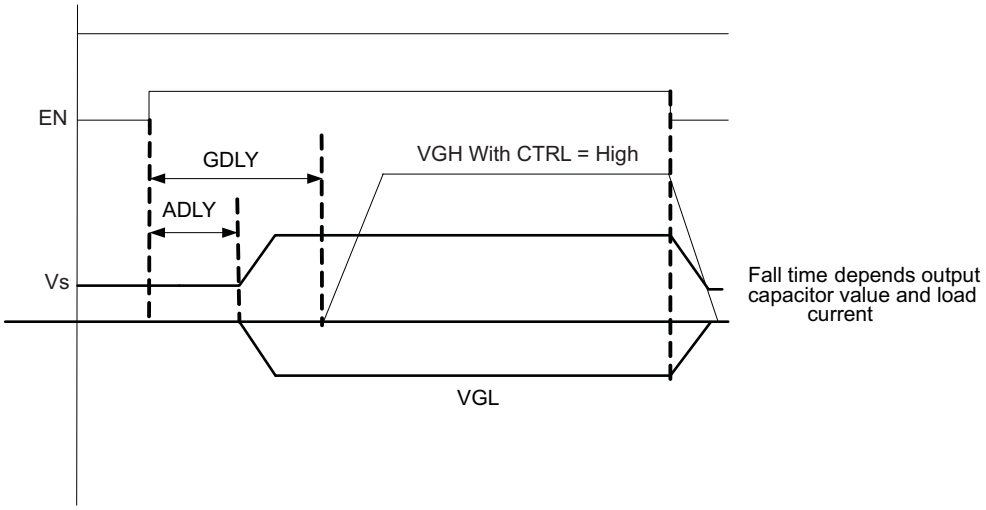


Figure 15. Power-On Sequencing

SETTING THE DELAY TIMES ADLY, GDLY

Connecting an external capacitor to the ADLY and GDLY pin sets the delay time. If no delay time is required these pins can be left open. To set the delay time, the external capacitor connected to ADLY and GDLY is charged with a constant current source (typically 5 μA). The delay time is terminated when the capacitor voltage has reached the internal reference voltage of Vref = 1.213 V. The external delay capacitor is calculated by:

$$C_{dly} = \frac{5\ \mu A \times td}{Vref} = \frac{5\ \mu A \times td}{1.213V} \quad (1)$$

with td = Desired delay time

APPLICATION INFORMATION (continued)

BOOST CONVERTER

The TPS65165 boost converter block is shown in Figure 16. The boost converter operates with PWM (Pulse Width Modulation) and a fixed switching frequency of 600 kHz. The converter uses a unique fast-response, voltage-mode controller scheme with input voltage feedforward. This achieves excellent line and load regulation (0.2%/A load regulation typical) and allows the use of small external components. To increase the flexibility in the selection of external component values, the device uses external loop compensation. Although the boost converter looks like a non-synchronous boost converter topology operating in discontinuous conduction mode, at light loads, the TPS65165 maintains continuous conduction even at minimal load currents. This is achieved with a novel architecture using an external Schottky diode with an integrated MOSFET in parallel connected between SW pin and the SUP pin. The purpose of this MOSFET is to allow the current to go below ground, which is the case at light load conditions. For this purpose, a small integrated P-Channel MOSFET (Q2) with a typical R_{DSON} of 10 Ω is sufficient. When the inductor current is positive, the external Schottky diode with the lower forward voltage carries the current. This causes the converter to operate with a fixed frequency in continuous-conduction mode over the entire load-current range. This avoids ringing on the switch pin as seen with a typical non-synchronous boost converter, and allows a simpler compensation network.

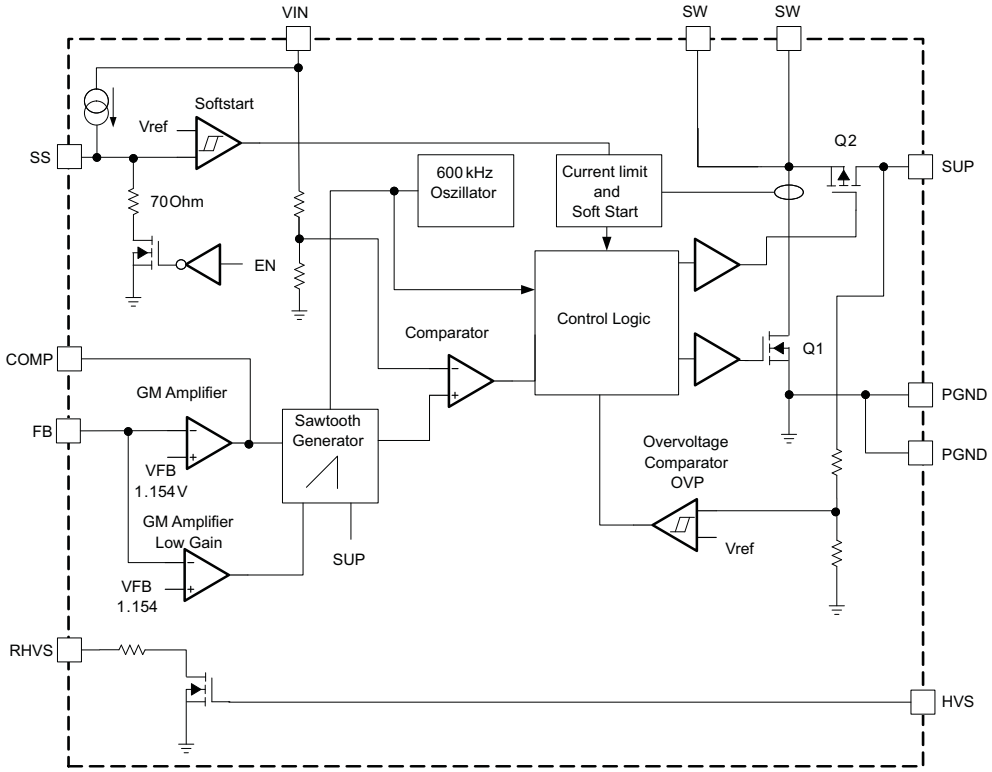


Figure 16. Boost Converter Block TPS65165

SOFTSTART BOOST CONVERTER

To minimize inrush current during start-up, an external capacitor connected to the softstart pin (SS) is used to slowly ramp up the internal current limit of the boost converter. The larger the capacitor, the slower the ramp-up of the current limit, and the longer the softstart time. A 22-nF capacitor is usually sufficient for typical applications.

APPLICATION INFORMATION (continued)

HIGH VOLTAGE STRESS TEST BOOST CONVERTER AND POSITIVE CHARGE PUMP

The TPS65165 incorporates a high voltage stress test where the output voltage of the boost converter Vs and the positive charge pump POUT are set to a higher output voltage compared to the nominal programmed output voltage. The High Voltage Stress test is enabled by pulling the HVS pin to high. With HVS=high the voltage on POUT, respectively VGH is regulated to a fixed output voltage of 30 V. The boost converter Vs is programmed to a higher voltage determined by the resistor connected to RHVS. With HVS=high the RHVS pin is pulled to GND which sets the voltage for the boost converter during the High Voltage Stress Test. The output voltage for the boost converter during high voltage stress test is calculated as:

$$Vs_{HVS} = V_{FB}\frac{R1 + R2 \parallel R4}{R2 \parallel R4} = 1.146V\frac{R1 + R2 \parallel R4}{R2 \parallel R4}$$

$$R4 = \frac{R1 \times R2}{\left(\frac{Vs_{HVS}}{V_{FB}} - 1\right) \times R2 - R1} \quad (2)$$

With:

Vs_{HVS} = Boost converter output voltage with HVS=high

V_{FB} = 1.146V

R4 = Resistor connected to pin RHVS

OVERVOLTAGE PROTECTION BOOST CONVERTER

The boost converter has an integrated overvoltage-protection circuit to prevent the switch voltage from exceeding the absolute maximum switch voltage rating in the event of a system fault. The device protects itself if the feedback pin is shorted to ground by clamping the boost-converter output voltage to 20 V. To implement the overvoltage protection, the overvoltage comparator shown in Figure 16 monitors the output voltage via the SUP pin. When the output voltage exceeds the overvoltage threshold of typically 20 V, the device stops switching until the output voltage drops below the comparator threshold again. The typical waveform is shown in Figure 6.

INPUT CAPACITOR SELECTION VIN, SUP

Low-ESR ceramic capacitors are recommended for good input-voltage filtering. The TPS65165 has an analog input (VIN) and a power supply input (SUP) powering all the internal rails, including the operational amplifiers. 1-µF bypass capacitors are required as close as possible from VIN to GND, and from SUP to GND. Depending on the overall load current, two or three 22-µF input capacitors are required. For better input-voltage filtering, the input capacitor values can be increased. Refer to Table 1 and typical applications for input capacitor recommendations.

Table 1. Input Capacitor Selection

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMMENTS
22µF/1210	6.3 V	Taiyo Yuden	Cin
1µF/1206	6.3 V	Taiyo Yuden	Bypass AVIN, SUP

BOOST CONVERTER DESIGN PROCEDURE

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. To simplify the calculation the fastest approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g., 80%. With the efficiency number it is possible to calculate the steady state values of the application.

1. Converter Duty Cycle:

$$D = 1 - \frac{Vin \times \eta}{Vout} \quad (3)$$

2. Maximum output current:

$$Iout = \left(Isw - \frac{Vin \times D}{2 \times fs \times L} \right) \times (1 - D) \quad (4)$$

3. Peak switch current:

$$I_{swpeak} = \frac{Vin \times D}{2 \times fs \times L} + \frac{I_{out}}{I - D} \quad (5)$$

With:

Isw = converter switch current (minimum switch current limit=4.4 A)

fs = converter switching frequency (typical 600kHz)

L = Selected inductor value

η = Estimated converter efficiency (use the number from the efficiency curves or 0.8 as an estimation)

The peak switch current is the steady state peak switch current the integrated switch, inductor and external Schottky diode has to be rated for. The calculation must be done for the minimum input voltage where the peak switch current is highest.

INDUCTOR SELECTION

The TPS65165 typically operates with a 10-µH inductor. The main parameter for inductor selection is the inductor saturation current. This should be higher than the peak switch current as calculated in Equation 5, with additional margin for heavy load transients. An alternative, more conservative approach is to choose the inductor with saturation current at least as high as the typical switch current limit of 5.5 A.

The second important parameter is the inductor DC resistance. Usually the lower the DC resistance the higher the efficiency of the converter. The choice of an inductor can affect converter efficiency by as much as 10%. Possible inductors are shown in Table 2.

Table 2. Inductor Selection Boost Converter

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS IN mm	Isat/DCR
10 µH	Sumida CDRH8D38-100	8.3×8.3×4.0	3.0 A / 38 mΩ
10 µH	Wuerth 744066100	10×10×3.8	4.0 A / 25 mΩ
10 µH	Coilcraft DO3316P-103	12.95×9.4×5.51	3.8 A / 3838 mΩ

OUTPUT CAPACITOR SELECTION

For best output voltage filtering, a low-ESR output capacitor is recommended. Ceramic capacitors have a low ESR value and work best with the TPS65165. Three 22µF or six 10uF ceramic output capacitors in parallel are sufficient for most applications. More capacitors can be added to improve the load transient regulation. Refer to Table 3 for details on selecting output capacitors.

Table 3. Output Capacitor Selection

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER
22 µF / 1812	16 V	Taiyo Yuden EMK432BJ226MM

Rectifier diode selection

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the converter. The current rating for the Schottky diode is calculated as the off time of the converter times the typical switch current of the TPS65165:

$$I_{avg} = (1 - D) \times Isw = \frac{Vin}{Vout} \times 5.5A \quad (6)$$

where Isw = the typical switch current of the TPS65165 (5.5 A)

A Schottky diode with 2-A maximum average rectified forward current rating is sufficient for most applications.

The Schottky rectifier must have adequate power dissipation. The dissipated power is the average rectified forward current times the diode forward voltage.

$$P_D = I_{avg} \times V_F = Isw \times (1 - D) \times V_{sw} \times \frac{Vin}{Vout} \times V_F \quad (7)$$

where Isw = typical switch current of the TPS65165 (5.5 A)

Table 4. Rectifier Diode Selection (Boost Converter)

CURRENT RATING I_{avg}	Vr	$V_{forward}$	$R_{\theta JA}$	SIZE	COMPONENT SUPPLIER
3 A	20 V	0.36 V at 3 A	46°C/W	SMC	MBRS320, International Rectifier
2 A	20 V	0.44 V at 2 A	75°C/W	SMB	SL22, Vishay Semiconductor
2 A	20 V	0.5 V at 2 A	75°C/W	SMB	SS22, Fairchild Semiconductor

SETTING THE OUTPUT VOLTAGE AND SELECTING THE FEEDFORWARD CAPACITOR

The output voltage is set by the external resistor-divider value, and is calculated as:

$$V_{out} = 1.146V \times \left(1 + \frac{R1}{R2}\right) \quad (8)$$

Across the upper resistor, a bypass capacitor is required to speed up the circuit during load transients. The capacitor value is caluculated as:

$$Cff = \frac{1}{2 \times \pi \times fz \times R1} = \frac{1}{2 \times \pi \times 5000 \times R1} \quad (9)$$

A standard value nearest to the calculated value should be used.

COMPENSATION (COMP)

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. A single capacitor connected to this pin sets the low-frequency gain. A 1.0-nF capacitor is sufficient for most of the applications. Adding a series resistor sets an additional zero and increases the high-frequency gain. Equation 10 calculates the frequency where the resistor increases the high frequency gain.

$$f_z = \frac{1}{2 \times \pi \times Cc \times Rc} \quad (10)$$

Lower input voltages require a higher gain, and therefore a lower compensation-capacitor value. Refer to the typical applications for the appropriate component selection.

POSITIVE CHARGE PUMP

The fully-integrated positive charge pump automatically switches its gain between doubler and tripler mode. As shown in Figure 17, the input voltage of the positive charge pump is the SUP pin, that is connected to the output of the main boost converter (Vs).

The charge pump requires two 330-nF flying capacitors and a 1-µF output capacitance for stable operation. The positive charge pump also supports the high-voltage stress test by pulling the HVS pin high. This programs the output voltage to a fixed output voltage of 30 V by using the internal voltage divider as shown in Figure 17. During normal operation the HVS pin is pulled low, and the output voltage is programmed with the external voltage divider.

$$V_{out} = 1.213V \times \left(1 + \frac{R5}{R6}\right)$$

$$R5 = R6 \times \left(\frac{V_{out}}{V_{FB}} - 1\right) = R6 \times \left(\frac{V_{out}}{1.213} - 1\right) \quad (11)$$

To minimize noise and leakage-current sensitivity, we recommend a value of approximately 20 kΩ for the lower feedback divider resistor R6. A 100-pF feedforward capacitor across the upper feedback resistor R5 is typically required.

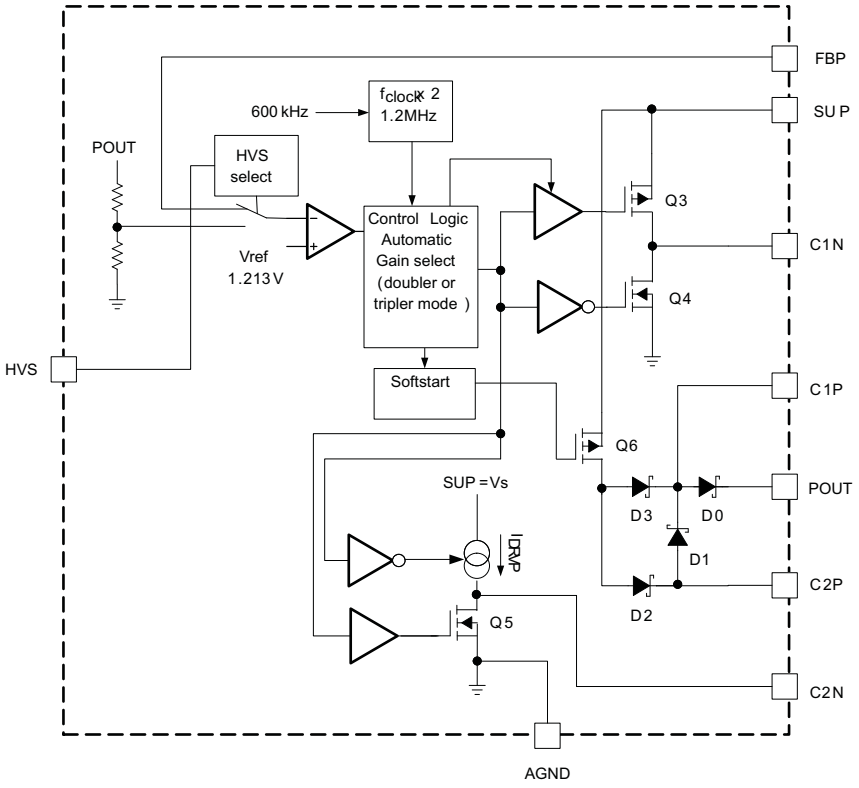


Figure 17. Positive Charge Pump Block TPS65165

NEGATIVE CHARGE PUMP DRIVER

The negative charge pump provides a regulated output voltage set by the external resistor divider. It inverts the voltage applied to the SUP pin (the boost-converter output voltage), and regulates it to the programmed voltage.

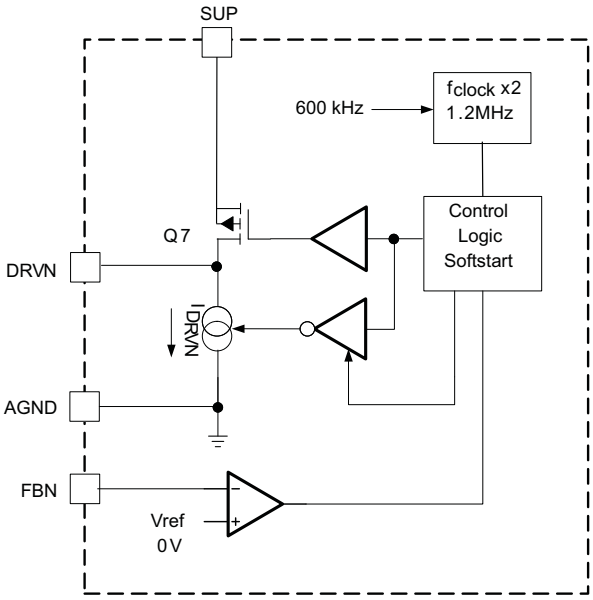


Figure 18. Negative Charge Pump Block TPS65165

The output voltage is VGL = (–Vs) + V_{DROP}. V_{DROP} is the voltage drop across the external diodes and internal charge pump MOSFETs.

Setting the output voltage:

$$V_{out} = -V_{REF} \times \frac{R7}{R8} = -1.213V \times \frac{R7}{R8} \quad (12)$$

$$R7 = R8 \times \frac{|V_{out}|}{V_{REF}} = R8 \times \frac{|V_{out}|}{1.213} \quad (13)$$

Since the reference-output driver current should typically not exceed 30 µA, the lower feedback-resistor value R8 should be in a range of 40 kΩ to 120 kΩ. The negative charge pump requires two external Schottky diodes. The peak current rating of the Schottky diode must be twice the load current of the output. For a 20-mA output current, the dual Schottky diode BAT54 is a good choice.

HIGH VOLTAGE SWITCH CONTROL (Gate Voltage Shaping)

For correct operation of this block it is not recommended to connect an output capacitor to VGH. If the output shows higher output ripple voltage than expected then the output capacitor value on POUT needs to be increased instead. The device has an integrated high-voltage switch to provide gate-voltage modulation of VGH. If this feature is not required, then CTRL pin must be pulled high or connected to VIN. When the device is disabled or the input voltage is below the undervoltage lockout (UVLO), both switches (Q4 and Q5) are off, and VGH is discharge by a 1-kΩ resistor over Q8, as shown in Figure 19.

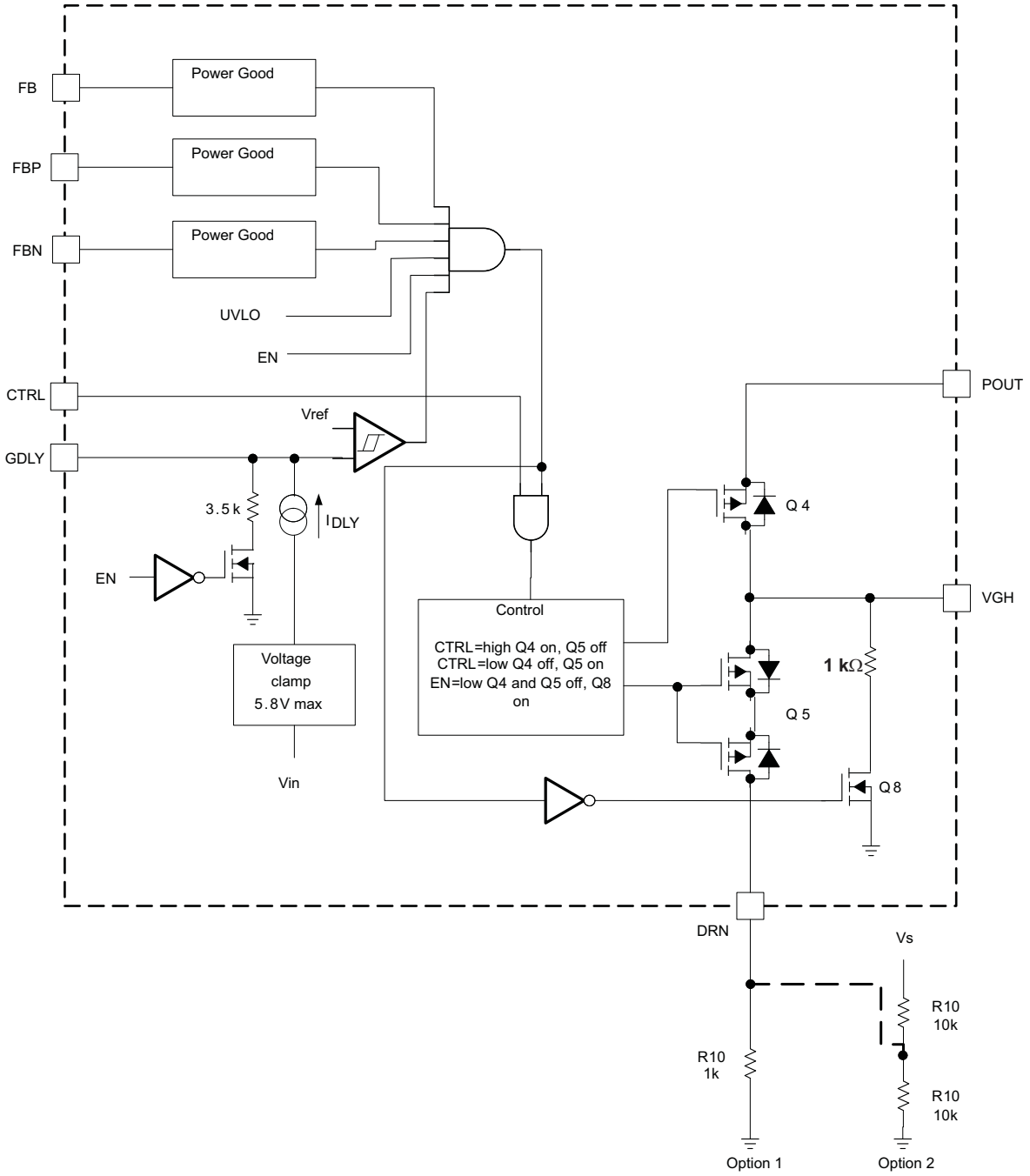


Figure 19. High Voltage Switch (Gate Voltage Shaping) Block TPS65165

To implement gate-voltage shaping, the control signal from the LCD timing controller (TCON) is connected to the CTRL pin. CTRL is activated when the device is enabled, the input voltage is above the undervoltage lockout, all the output voltages (Vs, VGL, VGH) are in regulation, and the delay time is set by the GDLY pin passed by. As soon as one of the outputs is pulled below its Power Good level, Q4 and Q5 are turned off and VGH is discharged via a 1-kΩ resistor over Q8.

With CTRL = high, Q4 is turned on and the charge pump output voltage is present at VGH. When the CTRL pin is pulled low, Q4 is turned off and Q5 is turned on, discharging VGH. The slope and time for discharging VGH is determined by the LCD capacitance and the termination on DRN. An additional output capacitor is not recommended on VGH. There are basically two options available to terminate the DRN pin, depending on the LCD capacitance and required overall converter efficiency.

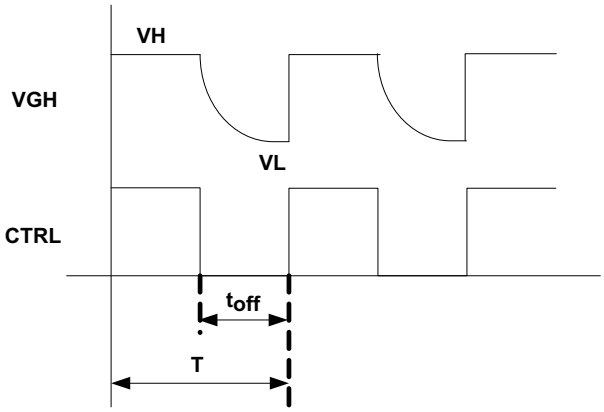


Figure 20. High Voltage Switch (Gate Voltage Shaping) Timing Diagram

Option 1 in Figure 19 draws no current from Vs, and is therefore better in terms of converter efficiency. The voltage level VL (the discharge level of VGH) is determined by the LCD capacitance, the resistor connected to DRN and the off time, t_{off}. The lower the resistor value connected to DRN, the lower the discharge voltage level VL.

Option 2 in Figure 19 constantly draws current from Vs due to the voltage divider connected to Vs. The advantage of this solution is that the low-level voltage VL is given by the voltage divider, assuming the feedback resistor values are small, allowing the LCD capacitance to discharge during t_{off}. This solution is not recommended for very large display panels because the feedback divider resistor values must be too low, drawing too much current from Vs.

Operational Amplifier 1, 2 and 3

The TPS65165 has three integrated operational amplifiers. OpAmp 3 is already configured as a standard buffer as shown in Figure 21. The operational amplifiers can be used as a gamma correction buffer or as a VCOM buffer.

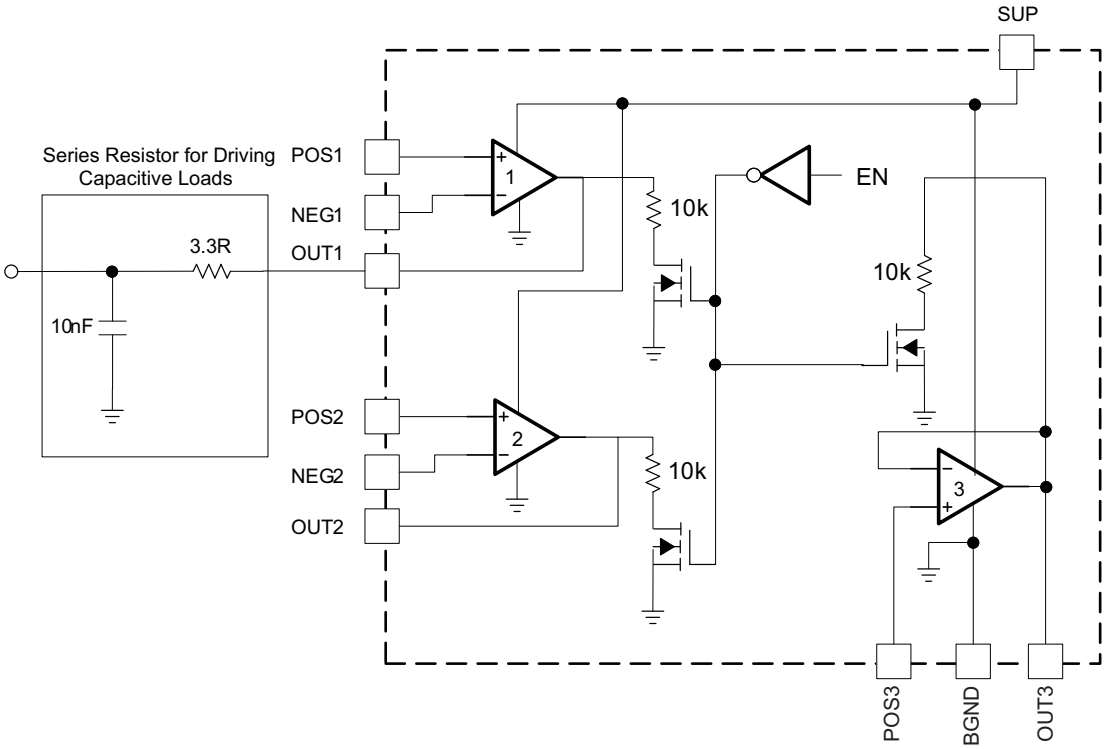


Figure 21. Operational Amplifier Block

The OpAmp power supply pin is the SUP pin connected to the boost converter Vs. To achieve good performance and minimize the output noise, a 1-µF bypass capacitor is required directly from the SUP pin to ground. When the device is disabled, the OpAmp outputs are pulled low via a 10kΩ resistor. The OpAmps are not designed to drive capacitive loads; therefore it is not recommended to connect a capacitor directly to the OpAmp outputs. If capacitive loads are driven we recommend using a series resistor at the output to provide stable operation. With a 3.3-Ω series resistor, a capacitive load of 10 nF can be driven, which is usually sufficient for typical LCD applications.

Operational Amplifier Termination

The TPS65165 has three integrated operational amplifiers. For some applications, not all of the amplifiers are used. To minimize device quiescent current the terminals need to be terminated. For the unity gain buffer, OpAmp 3 the positive terminal is connected to GND and the output is left open. For OpAmp 2 and 3 the negative terminal is connected to the OpAmp output and the positive terminal is connected to GND. Using such a termination minimizes device quiescent current and correct functionality of the device.

PCB Layout Design Guidelines:

1. Place the power components outlined in bold first on the PCB.
2. Rout the traces outlined in bold with wide PCB traces
3. Place a 1-µF bypass capacitor directly from the Vin pin to GND since this is the supply pin for internal circuits.
4. Place a 1-µF bypass capacitor directly from the SUP pin to GND since this is the supply pin for internal circuits.
5. Use a short and wide trace to connect the SUP pin to the output of the boost converter Vs.
6. Place the 220-nF reference capacitor directly from REF to AGND close to the IC pins.
7. The feedback resistor for the negative charge pump between FBN and REF needs to be >40kΩ.
8. Use short traces for the charge pump drive pin (DRVN) of VGL because the traces carry switching waveforms.
9. Place the flying capacitors as close as possible to the C1P, C1N and C2P, C2N pin.
10. Solder the Power Pad of the QFN package to GND and use thermal vias to lower the thermal resistance

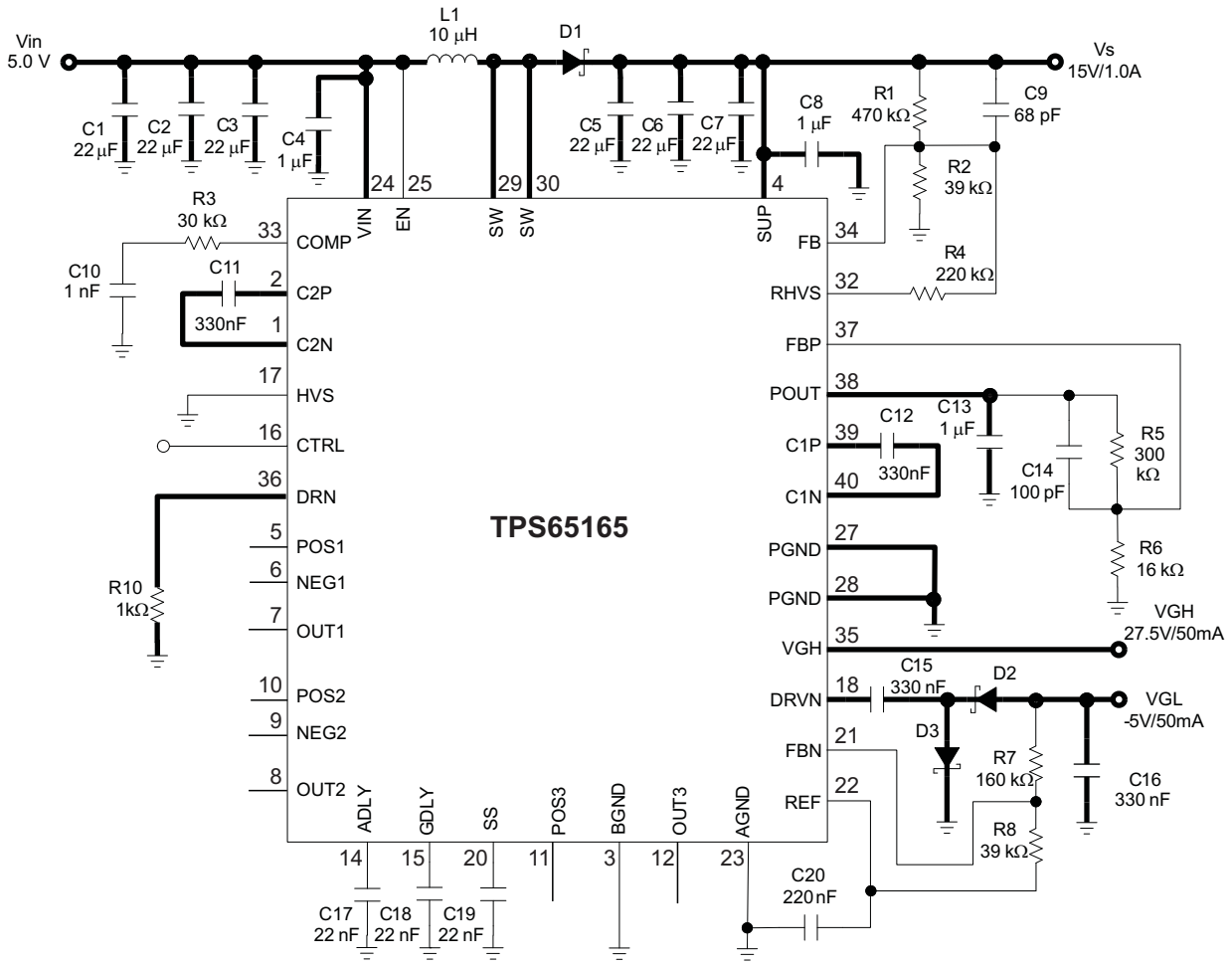


Figure 22. Layout Recommendation

TYPICAL APPLICATION

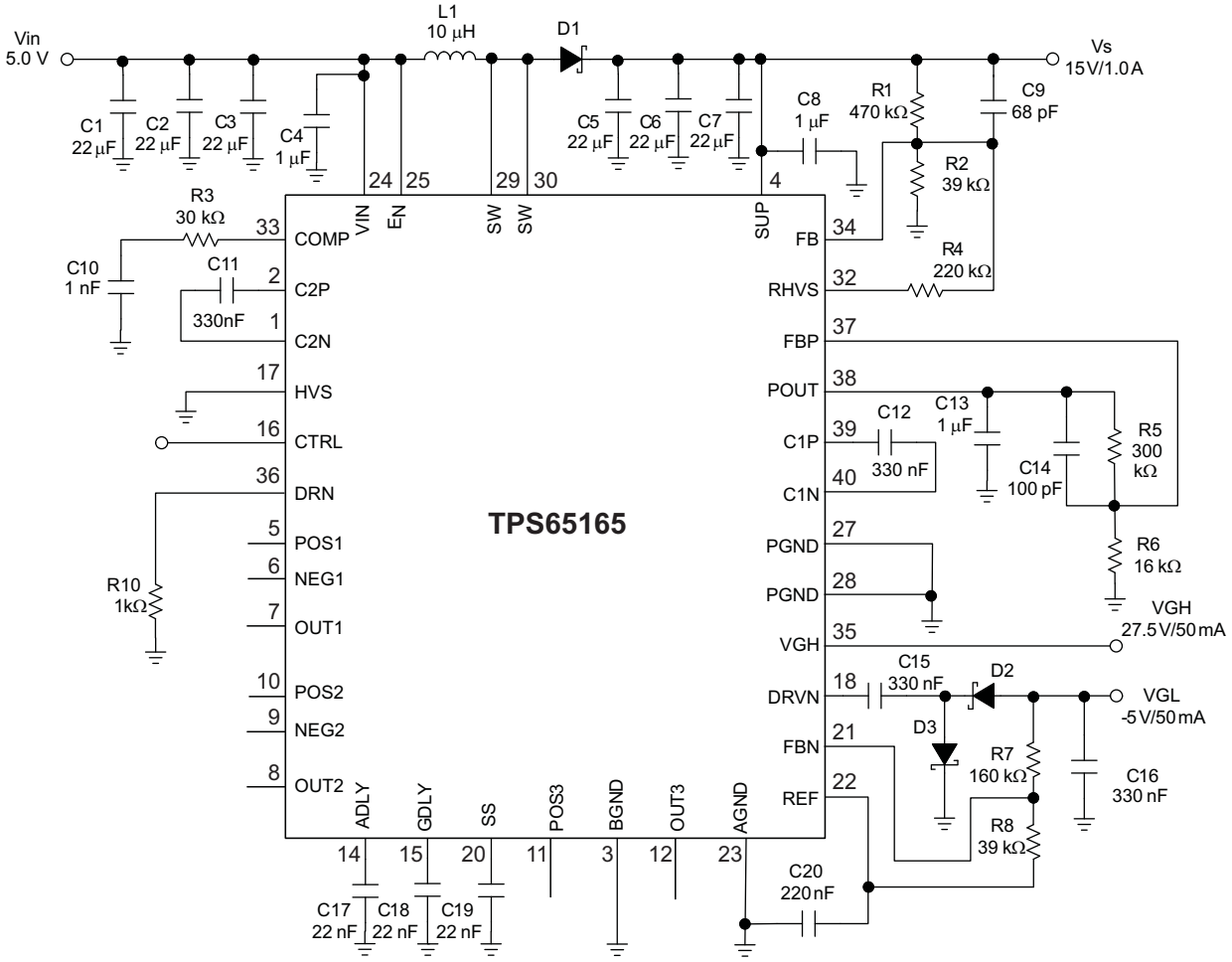


Figure 23. Typical application running from a 5V supply rail

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65165RSBR	ACTIVE	WQFN	RSB	40	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65165	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

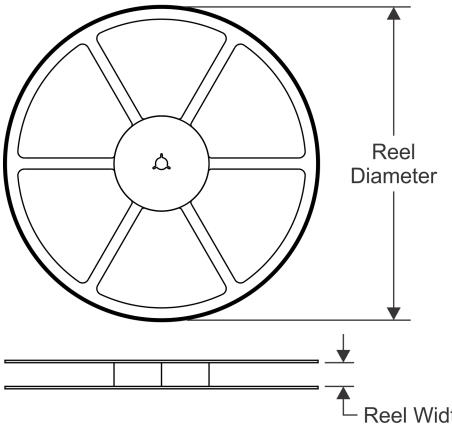
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

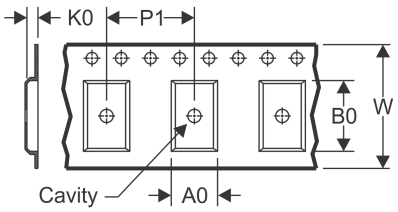
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

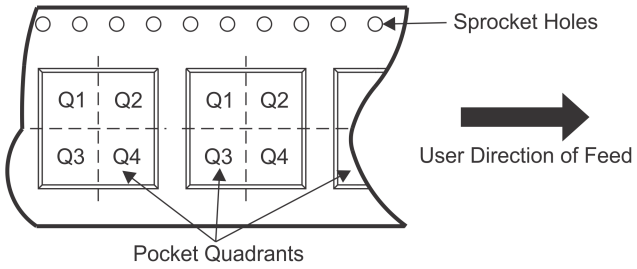


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

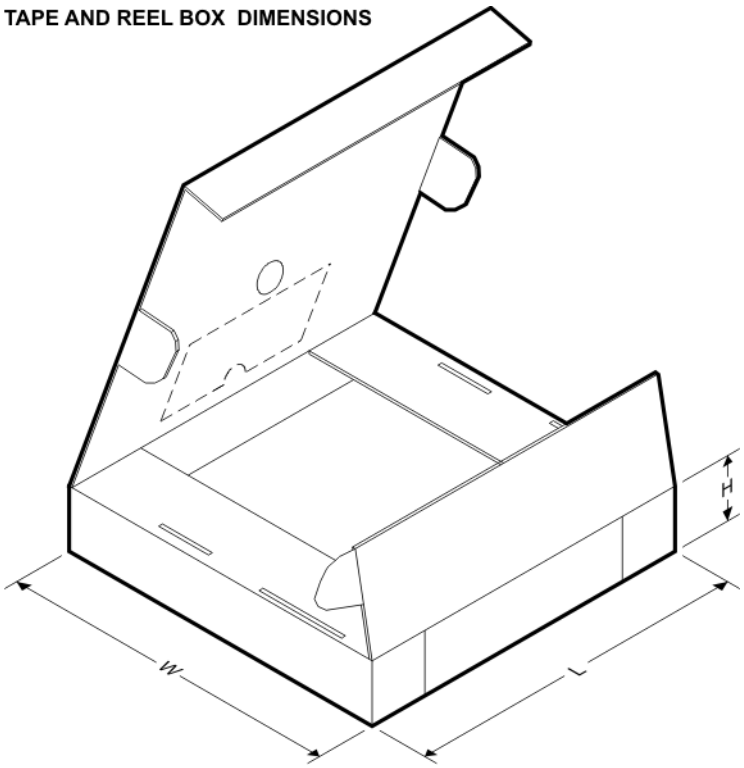
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65165RSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65165RSBR	WQFN	RSB	40	3000	367.0	367.0	35.0

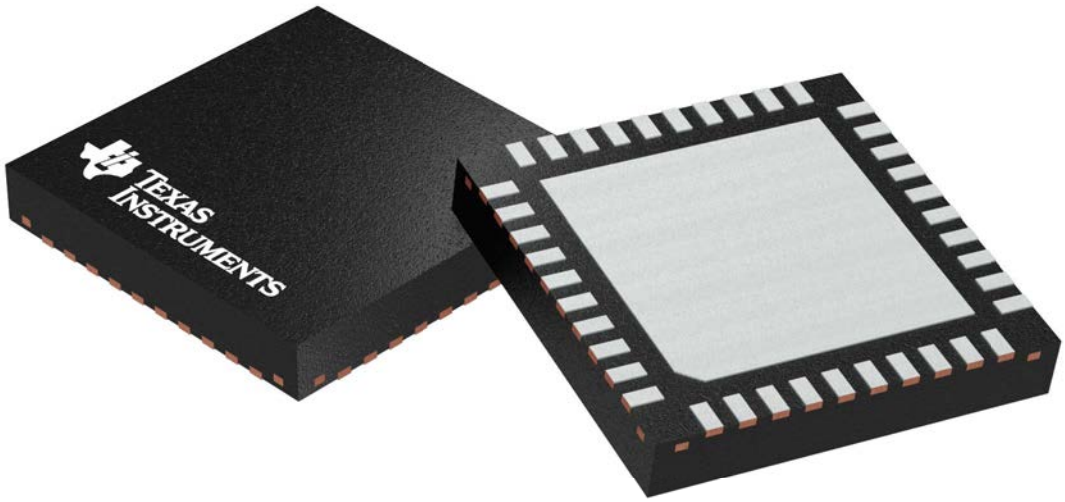
GENERIC PACKAGE VIEW

RSB 40

WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



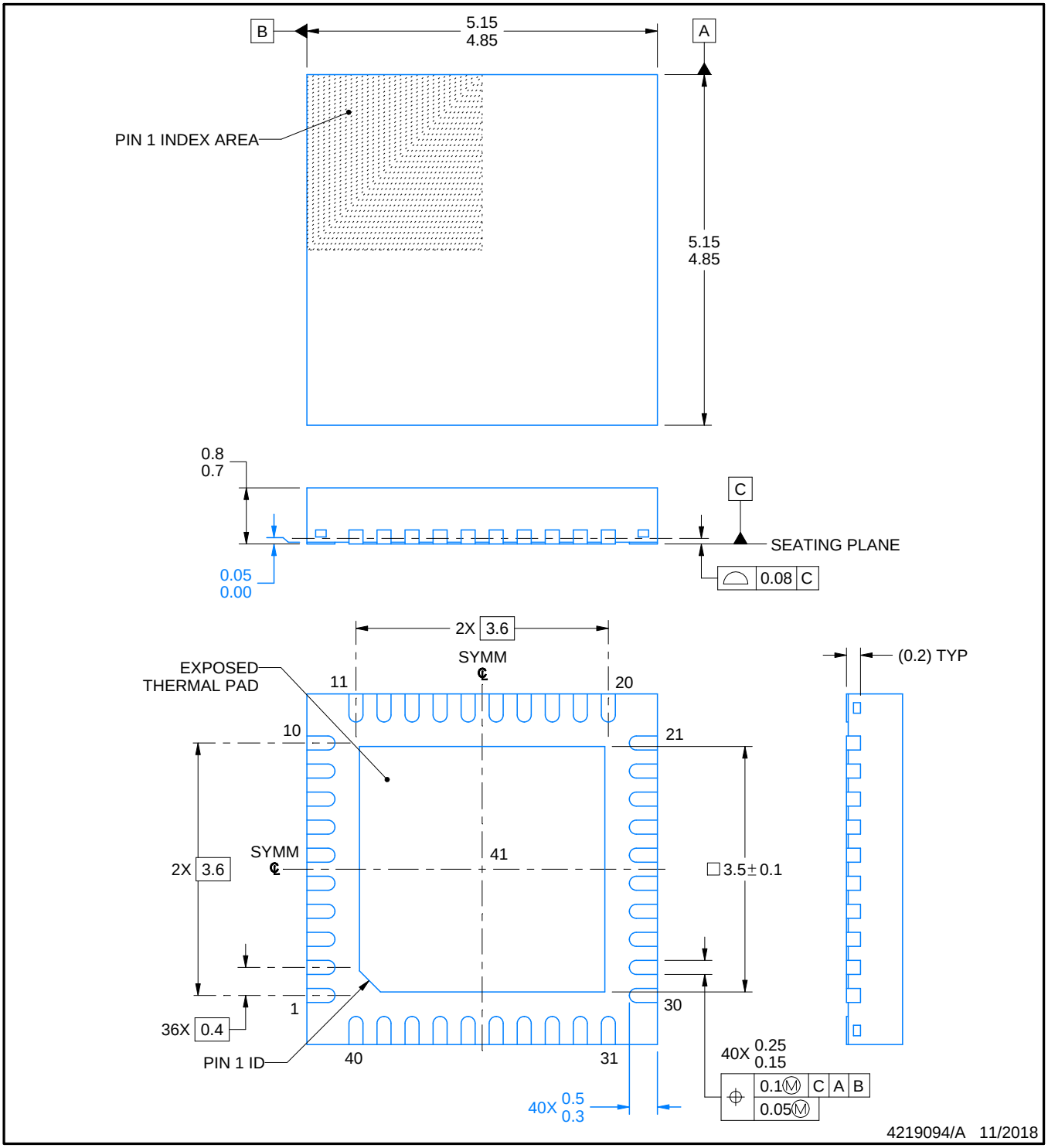
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RSB0040B

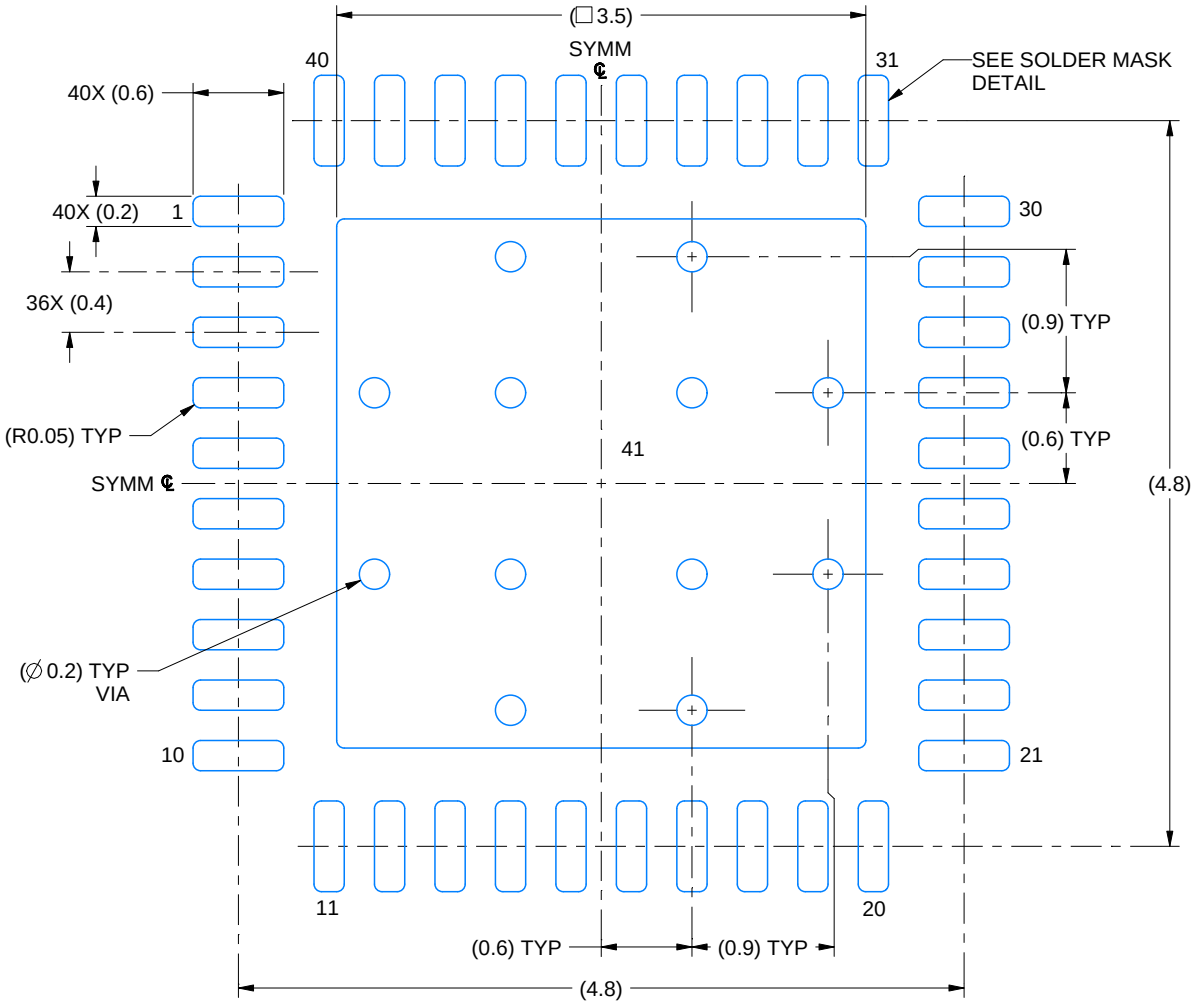
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

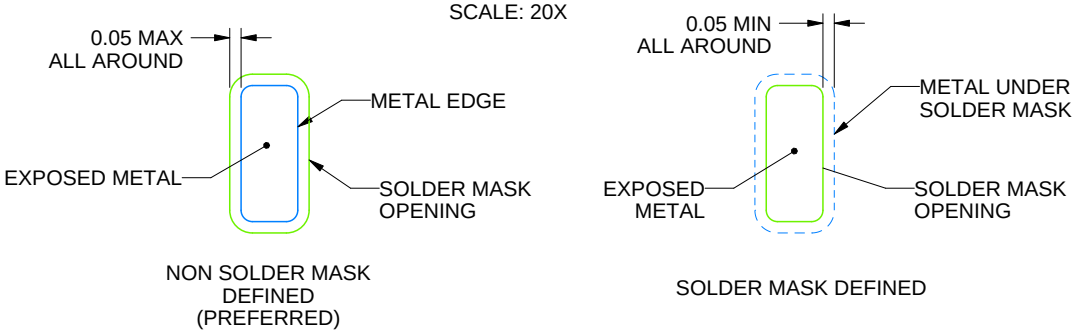


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4219094/A 11/2018

NOTES: (continued)

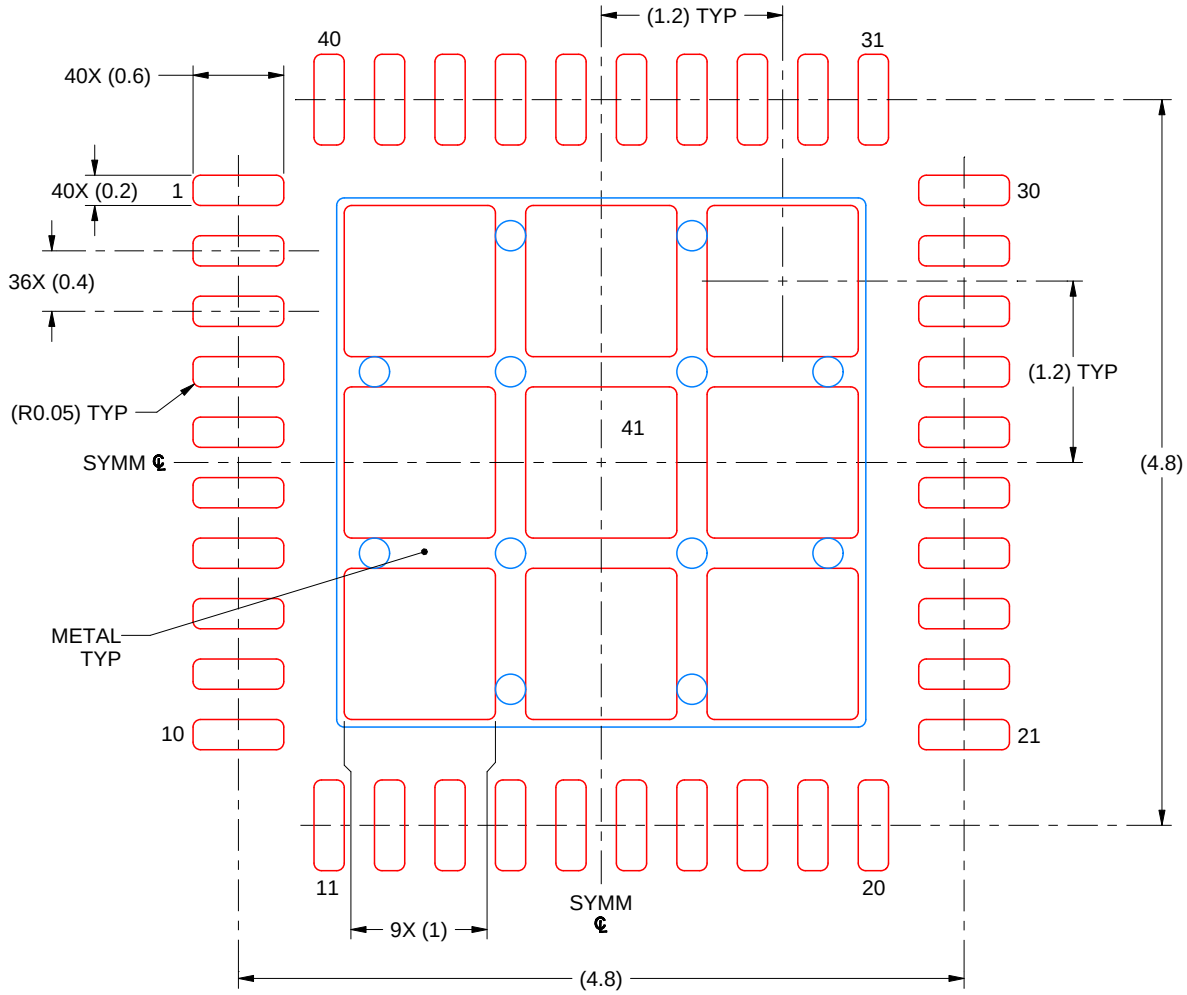
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSB0040B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

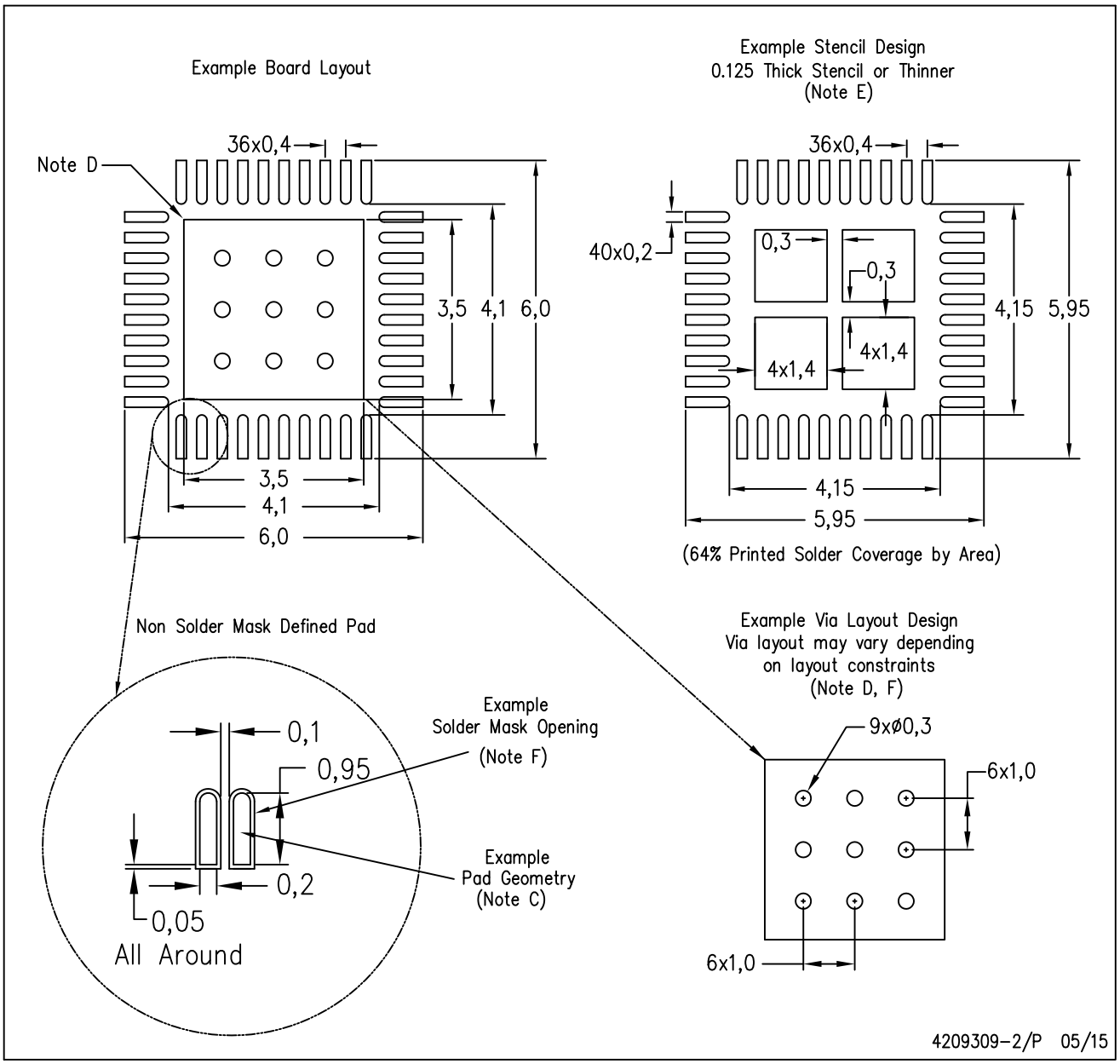
EXPOSED PAD 41
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219094/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated