TPS65055EVM

This User's Guide describes the characteristics, operation, and use of the TPS65055EVM-258 evaluation module (EVM). This EVM is designed to help the user evaluate and test the various operating modes of the TPS65055. This User's Guide includes setup instructions for the hardware and software, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation.module.

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1 Introduction

The Texas Instruments TPS65055 is an integrated Power Management IC for applications that are powered with one Li-Ion or Li-Polymer cell and require multiple power rails. The TPS65055 contains two highly efficient switching step-down converters, four LDOs, and additional status and I/O pins. The device is controlled via an I2C interface (HPA172).

1.1 Requirements

In order for this EVM to operate properly, the following components must be connected and properly configured.

1.1.1 Personal Computer (PC)

A computer with a USB port is required to operate this EVM. The TPS65055 interface software, which is run on the PC, communicates with the EVM via the PC USB port. The user sends commands to the EVM as well as reads the contents of the TPS65055 internal registers through the USB port.

1.1.2 Printed Circuit Board Assembly

The TPS65055EVM-258 PCB contains the TPS65055 IC and its required external components. This board contains several jumpers and connectors that allow the user to customize the board for specific operating conditions.

1.1.3 USB to I2C Adapter

The HPA172 is the link that allows the PC and the EVM to communicate. The adapter connects to the PC with the supplied USB cable on one side and to the EVM though the supplied ribbon cable on the other. When the user writes a command to the EVM, the interface program, which is run from the PC, sends the command to the PC USB port. The adapter receives the USB command and converts the signal to an I2C protocol. It then sends the I2C signal to the TPS65055 board. When the user reads a status register from the EVM, the PC sends a command to read a register on the EVM. When the EVM receives the command, it reports the status of the register via the I2C interface. The adapter receives the information on the I2C interface, converts it to a USB protocol, and sends it to the PC.

1.1.4 Software

Texas Instruments has provided software to assist the user in evaluating this EVM. To install the software, insert the enclosed CD into your computer. The software should start automatically. If it does not, simply go to <Start>, <Run>, and type “D:\setup.exe”, and click <OK> (assuming that D: is your CD drive). Check the TPS65055 product folder on the TI website for the latest revision of the software.

2 Setup

This chapter describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the TPS65055EVM-258.

2.1 Input / Output Connector Descriptions

2.1.1 J1 –VIN

Input voltage from external power supply, recommended max 5.5V. Input current is dependent on load but will typically be below 2A.

2.1.2 J2 –GND

This is the return connection for VIN.

2.1.3 J3 – I2C

This is the I2C serial interface connector.

2.1.4 J4 – Discrete Outputs

Three discrete outputs are available on this connector:

$\overline{\text{RST}}$ – Active low by default. The state can be changed using the REG_CTRL register of the TPS65055 using the I2C interface. This Open-Drain output is pulled up externally on the EVM to VIN.

$\overline{\text{DPD}}$ – Active low by default. The state can be changed using the REG_CTRL register of the TPS65055 using the I2C interface. This Open-Drain output is pulled up externally on the EVM to VIN.

$\overline{\text{DISCHG}}$ – The state of this output is dependent on the voltage level of the THRESHOLD input. This Open-Drain output is pulled up externally on the EVM to VIN.

2.1.5 J5 – VDCDC1

The output from DCDC1 switching regulator which has a max output current of 0.6A.

2.1.6 J6 – GND

Return for VDCDC1.

2.1.7 J7 – VDCDC2

The output from DCDC2 switching regulator which has a max output current of 0.6A.

2.1.8 J8 – GND

Return for VDCDC2.

2.1.9 J9 – VLDO1

The output from low drop out regulator VLDO1 which has a max output current of 400mA.

2.1.10 J10 –GND

Return for VLDO1.

2.1.11 J11 – VLDO2

The output from low drop out regulator VLDO2 which has a max output current of 400mA.

2.1.12 J12 – GND

Return for VLDO2.

2.1.13 J13 –VLDO3

The output from low drop out regulator VLDO3 which has a max output current of 200mA.

2.1.14 J14 –GND

Return for VLDO3.

2.1.15 J15 –VLDO3

The output from low drop out regulator VLDO4 which has a max output current of 200mA.

2.1.16 J16 – GND

Return for VLDO4.

2.1.17 JP1 –ENDCDC1

Enable for DCDC1 converter. The default setting is ON.

2.1.18 JP2 –DEFLDO2

Along with DEFLDO1, this input sets default voltages for LDO1, LDO2 and DCDC1.

2.1.19 JP3 – DEFLDO1

Along with DEFLDO2, this input sets default voltages for LDO1, LDO2 and DCDC1.

2.1.20 JP4 – ENDCDC2

Enable for DCDC2 converter.

2.1.21 JP5 – ENLDO1

Enable for LDO1.

2.1.22 JP6 – ENLDO2

Enable for LDO2.

2.1.23 JP7 – ENLDO3

Enable for LDO3.

2.1.24 JP8 – ENLDO4

Enable for LDO4.

2.1.25 JP9 – VINLDO1

Input voltage for LDO1. Recommended max input voltage is 5.5V

2.1.26 JP10 –VINLDO2

Input voltage for LDO2. Recommended max input voltage is 5.5V.

2.1.27 JP11 –DEFDCDC2

Sets the output voltage for DCDC2 (High = 1.0V and Low = 1.2V)

2.1.28 JP12 –VINLDO3/4

Input voltage for LDO3 and LDO4. Recommended max input voltage is 5.5V.

2.2 Setup

The following steps must be followed before the EVM can be operated.

1. Install the TPS65055EVM Software.
2. Connect input voltages and loads to the EVM.
3. Configure all EVM jumpers to factory setting.

Jumper	Shunt Location
JP1	Between EN_DCDC1 and VIN
JP2	Between DEFLDO2 and HIGH
JP3	Between DEFLDO1 and HIGH
JP4	Between EN_DCDC2 and VIN
JP5	Between ENLDO1 and VINLDO1
JP6	Between ENLDO2 and VINLDO2
JP7	Between ENLDO3 and VINLDO3/4
JP8	Between ENLDO4 and VINLDO3/4
JP9	Between VINLDO1 and VIN
JP10	Between VINLDO2 and VIN
JP11	Between DEFDCDC2 and HIGH
JP12	Between VINLDO3/4 and VIN

4. Connect the ribbon cable between the EVM and the USB-TO-GPIO (HPA172) Adapter
5. Connect the USB cable between the computer and the HPA172 EVM.
6. Turn on all supplies.
7. Run the TPS65055EVM software.

3 Board Layout

This chapter provides the TPS65055EVM-258 board layout and illustrations.

3.1 Layout

Board layout is critical for all switch mode power supplies. The following shows the board layout for the TPS65055EVM-258 PWB. The nodes with high switching frequencies and currents are short and are isolated from the noise sensitive feedback circuitry. Careful attention has been given to the routing of high frequency current loops. Refer to the datasheet for specific layout guidelines.

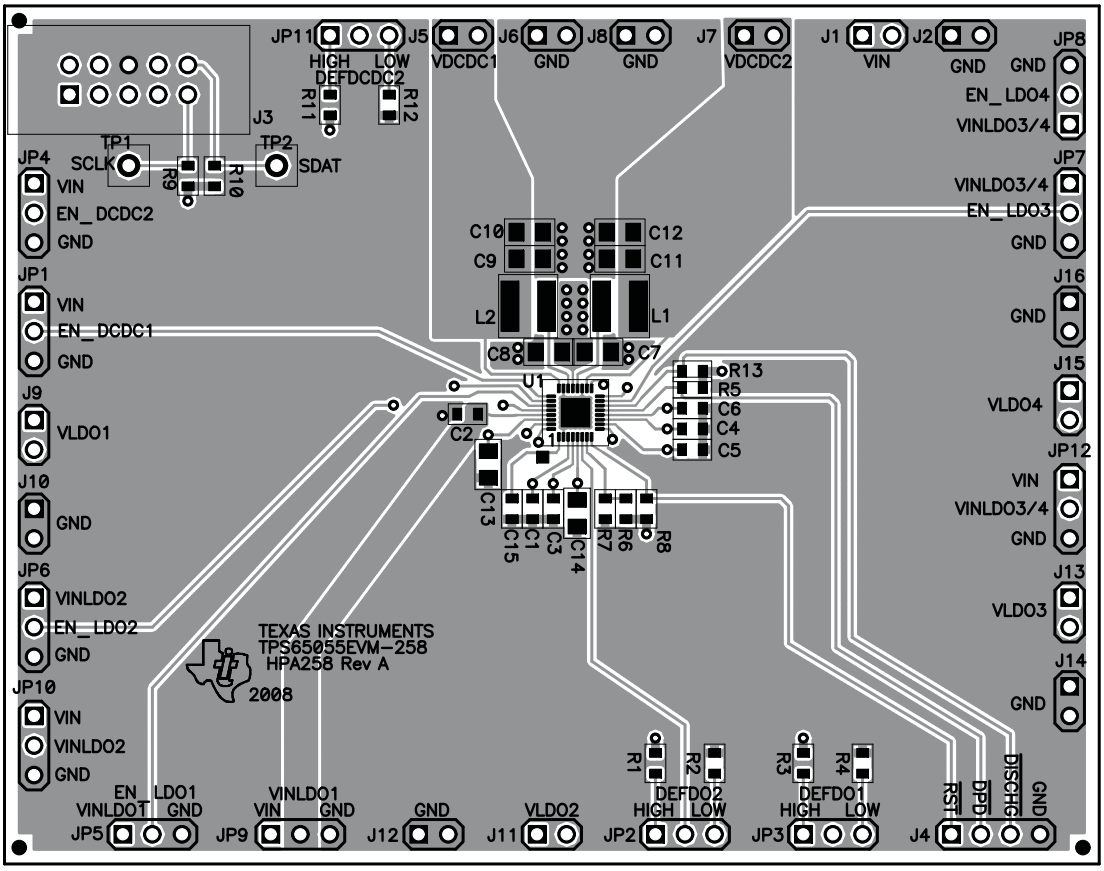
JP11
HIGH LOW
DEFDCDC2
J5
VDCDC1
J6
GND
J8
GND
J7
VDCDC2
J1
VIN
J2
GND
JP8
GND
EN_LDO4
VINLDO3/4
J3
TP1
SCLK
TP2
SDAT
R9
R10
R11
R12
JP4
VIN
EN_DCDC2
GND
JP7
VINLDO3/4
EN_LDO3
GND
C10
C12
C9
C11
L2
L1
C8
C7
JP1
VIN
EN_DCDC1
GND
U1
R13
R5
C6
C4
C5
C2
J16
GND
J15
VLDO4
J9
VLDO1
J10
GND
C13
C15
C1
C3
C14
R7
R6
R8
JP12
VIN
VINLDO3/4
GND
JP6
VINLDO2
EN_LDO2
GND
TEXAS INSTRUMENTS
TPS65055EVM-258
HPA258 Rev A
2008
J13
VLDO3
J14
GND
JP10
VIN
VINLDO2
GND
R1
R2
R3
R4
DISCHG
RST
EN_LDO1
VINLDO1
GND
VINLDO1
VIN
GND
GND
VLDO2
DEFDO2
HIGH LOW
DEFDO1
HIGH LOW
GND
JP5
JP9
J12
J11
JP2
JP3
J4

Figure 1. PCB

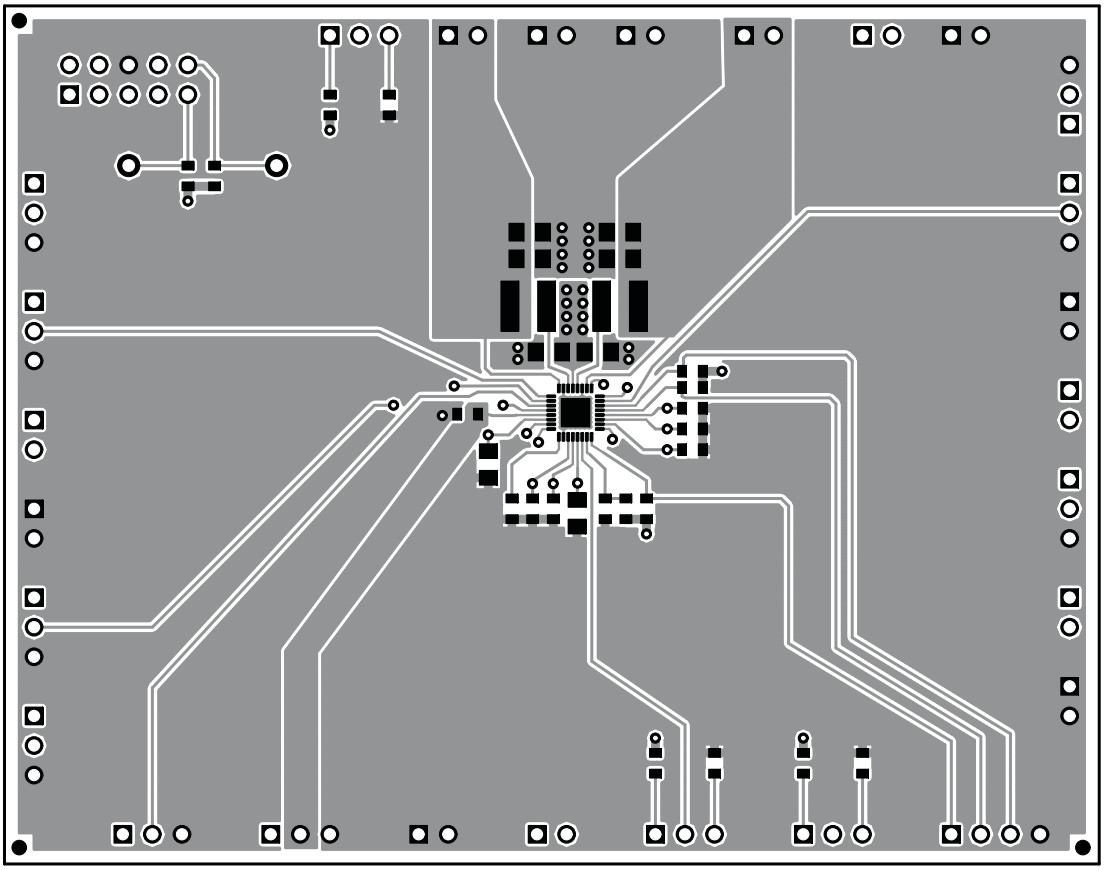

Figure 2. PCB

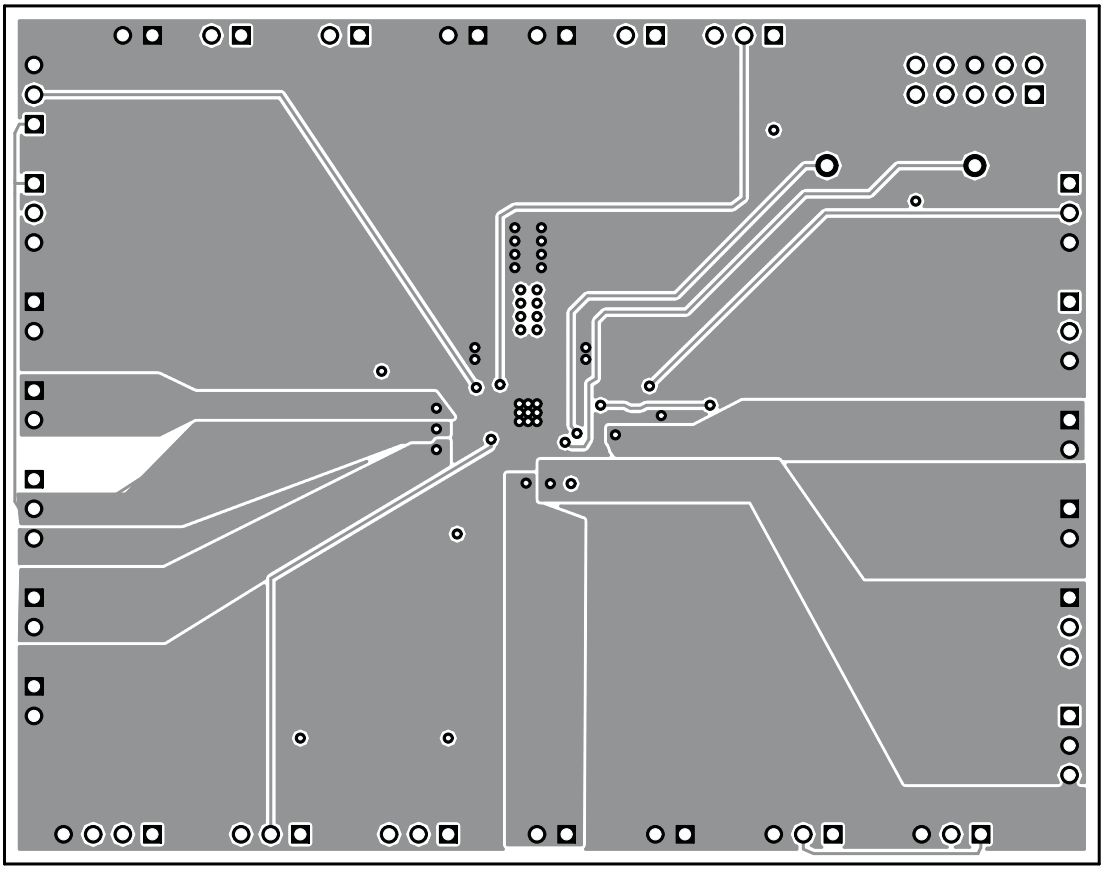

Figure 3. PCB

4 Schematic and Bill of Materials

This chapter provides the TPS65055EVM-258 schematic and bill of materials.

4.1 Schematic

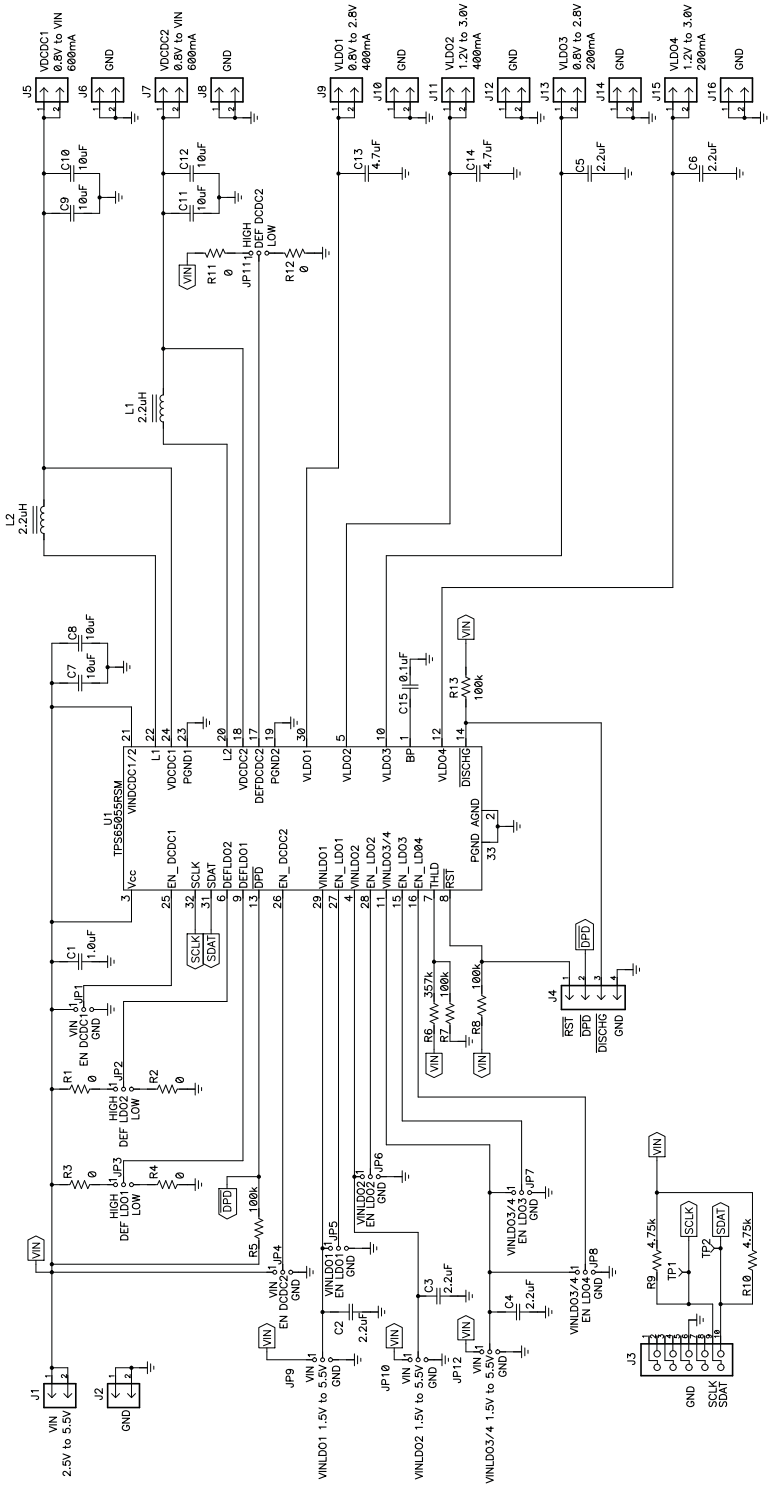

Figure 4. TPS65055EVM-258 Schematic

4.2 Bill of Materials

Table 1. TPS65055EVM-258 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	1.0 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	GRM188R61E105KA12D	Murata
2	C13, C14	4.7 µF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM219R61A475KE19D	Murata
1	C15	0.1 µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H104K	TDK
5	C2–C6	2.2 µF	Capacitor, Ceramic, 10V, X5R, 10%	0603	GRM188R61A225KE34D	Murata
6	C7–C12	10 µF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	Murata
14	J1, J2, J5–J16	PTC36SAAN	Header, Male 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
1	J3	2510-6002UB	Connector, Male Straight 2x5 pin, 100mil spacing, 4 Wall	0.338 × 0.788 inch	2510-6002UB	3M
1	J4	PTC36SAAN	Header, Male 4 pin, 100mil spacing, (36-pin strip)	0.100 inch × 4	PTC36SAAN	Sullins
3	JP1 - JP12	PTC36SAAN	Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 inch × 3	PTC36SAAN	Sullins
2	L1, L2	2.2 µH	Inductor, SMT, 2.5A, 70 milliohm	0.153 × 0.153 inch	LPS4018-222ML	Coilcraft
6	R1–R4, R11, R12	0	Resistor, Chip, 1/16W, 5%	0603	Std	Std
4	R5, R7, R8, R13	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	357k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R9, R10	4.75k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	TP1, TP2	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 inch	5000	Keystone
1	U1	TPS65055RSM	IC, 2.25 MHz, Two Step Down DC to DC Converters		TPS65055RSM	TI
12	—		Shunt, 100-mil, Black	0.100	929950-00	3M
1	—		PCB, 2.9" x 3.7" × 0.062"		HPA258	Any
4	—	SJ-5303	Bumper foot, self adhesive	0.44" × 0.2"	SJ-5303	3M

Notes : 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

4.3 Related Documentation From Texas instruments

TPS65055 data sheet (SLVS844)

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