TPS62840 1.8-V to 6.5-V, 750-mA, 60-nA I_Q Step-Down Converter

1 Features

- 60-nA operating quiescent current
- 100% duty-cycle mode with 150-nA I_Q
- Input voltage range V_{IN} from 1.8 V to 6.5 V
- Output current up to 750 mA
- RF friendly DCS-Control™
- 80% efficiency at 1 µA I_{OUT} (3.6 V_{IN} to 1.8 V_{OUT})
- 16 selectable output voltages via VSET pin
- Auto transition PFM/PWM or forced-PWM mode
- Selectable forced PWM and STOP modes
- Output discharge function
- 20-nA shutdown current
- SON-8, WCSP-6 and HVSSOP-8 packages

2 Applications

- Smart meters, smart thermostats
- Tracking devices
- Wearable electronics
- Medical sensor patches and patient monitors
- Industrial IoT (smart sensors)
- Test and measurement

3 Description

The TPS62840 is a high efficiency step-down converter with ultra-low operating quiescent current of typically 60 nA. The device contains special circuitry to achieve just 150 nA IQ in 100% mode to further extend battery life near the end of discharge.

The device uses DCS-Control™ to cleanly power radios and operates with a typical switching frequency of 1.8 MHz. In Power-Save Mode the device extends the light load efficiency down to a load current range of 1-µA and below.

16 predefined output voltages can be selected by connecting a resistor to pin VSET, making the device flexible for various applications with a minimum amount of external components.

The device's STOP pin immediately eliminates any switching noise in order to take a noise-free measurement in data acquisition systems.

The TPS62840 provides an output current of up to 750 mA. With an input voltage of 1.8 V to 6.5 V, the device supports multiple power sources such a single coin cell, 2S to 4S Alkaline, 1S/2S Li-MnO2 or 1S Li-Ion.

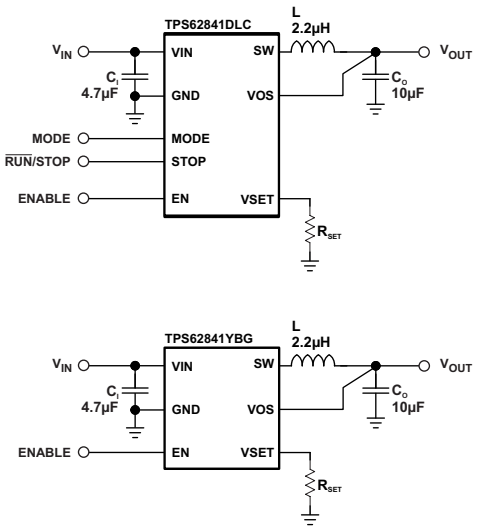
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62840	8 pin DLC (SON)	1.5mm x 2mm
	6 pin YBG (WCSP)	0.97mm x 1.47mm
	8 pin DGR (HVSSOP)	3mm x 5mm

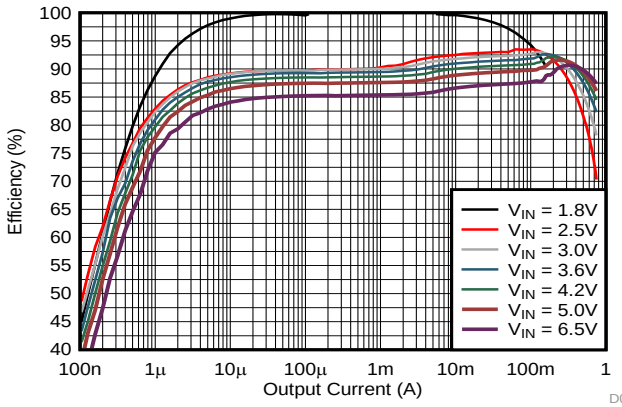
(1) For all available packages, see the orderable addendum at the end of the datasheet.

ADVANCE INFORMATION

Typical Application



Efficiency vs. Load Current (V_{OUT} = 1.8V)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2019	*	Advance Information release

5 Device Comparison Table

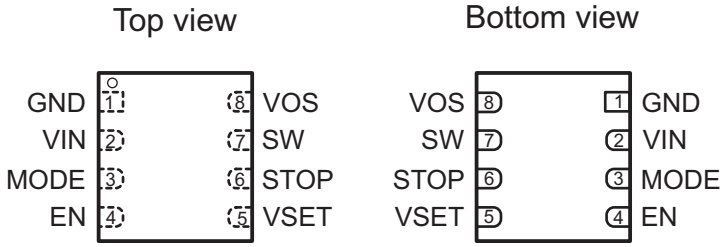
ORDERABLE PART NUMBER	OUTPUT VOLTAGE	OUTPUT CURRENT	OUTPUT DISCHARGE	MODE PIN	STOP PIN	PACKAGE	PACKAGE MARKING
TPS62841DLC	0.8 V to 1.55 V in 50mV steps	750 mA	yes	yes	yes	SON-8 (DLC)	E9
TPS62841YBG			yes	no	no	WCSP-6 (YBG)	1FB
TPS62840DLC	1.8 V to 3.3 V in 100-mV steps	750 mA	yes	yes	yes	SON-8 (DLC)	E5
TPS62840YBG			yes	no	no	WCSP-6 (YBG)	1FA
TPS62842DGR(1)	1.8 V, 2.0 V, 2.2 V, 2.4 V to 3.6 V in 100-mV steps	750 mA	yes	yes	no	HVSSOP-8 (DGR)	62842
TPS62849DLC(1)	3.4-V fixed output voltage				yes	SON-8 (DLC)	FF

(1) Future device options

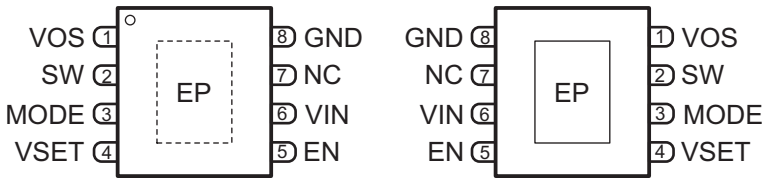
ADVANCE INFORMATION

6 Pin Configuration and Functions

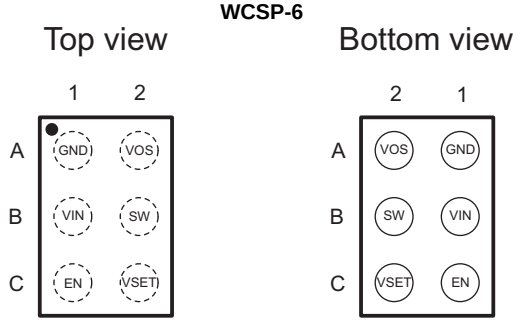
DLC
SON-8



DGR
HVSSOP-8



YBG
WCSP-6



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DLC (SON-8)	DGR (HVSSOP-8)	YBG (WCSP-6)		
VIN	2	6	B1	PWR	V_{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A 4.7-µF ceramic capacitor is required.
SW	7	2	B2	PWR	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
GND	1	8	A1	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitors.
VSET	5	4	C2	IN	Connecting a resistor to GND sets the output voltage when the converter is enabled. For TPS62849, connect this pin to GND.
VOS	8	1	A2	IN	Output voltage sense pin for the internal feedback divider network and regulation loop. When the converter is disabled this pin discharges V_{OUT} by an internal MOSFET. Connect this pin directly to the output capacitor with a short trace.
EN	4	5	C1	IN	Enable pin. A high level enables the device and a low level turns the device off. The pin features an internal pull-down resistor, which is disabled once the device has started up and the output voltage is regulated. The pull-down resistor is activated again, once a low level has been detected.
STOP	6	n/a	n/a	IN	STOP Switching pin. When this pin is logic high, the converter stops switching in order to provide a quiet supply rail. The output is powered from the charge available in the output capacitor. When this pin is logic low, the device immediately resumes operation. The pin features an internal pull-down resistor, which is disabled once a high level is detected at the input. The pull-down resistor is activated again, once a low level has been detected.
MODE	3	3	n/a	IN	MODE pin. A low level enables Power-Save Mode operation with an automatic transition between PFM and PWM modes. A high level forces the converter to operated in PWM mode. This pin must be terminated.
NC	n/a	7	n/a		This pin is not connected internally. Do not connect this pin.
EP	n/a	9	n/a	PWR	Exposed thermal pad. The PowerPAD must be connected to GND.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	–0.3	7	V
	SW (DC)	–0.3	V_{IN} +0.3	V
	SW (AC), less than 10ns	–2.0	8.5	V
	EN, MODE, STOP	–0.3	6.5	V
	VSET		V_{IN} + 0.3 <3.6	V
	VOS	–0.3	3.7	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage V_{IN}	1.8		6.5	V
L	Effective inductance	1.51	2.2	2.9	µH
C_{OUT}	Effective output capacitance	3	10	40	µF
C_{IN}	Effective input capacitance	1	4.7		µF
C_{VSET}	External parasitic capacitance at VSET pin			100	pF
R_{SET}	Nomial resistance range for external voltage selection resistor (E96 resistor series)	0.909		267	kΩ
	External voltage selection resistor tolerance			1%	
	External voltage selection resistor temperature coefficient			±200	ppm/°C
T_J	Operating junction temperature range	-40		125	°C

7.4 Thermal Information

THERMAL METRIC		DLC Package	YBG Package	DGR Package	UNIT
		JEDEC PCB		JEDEC PCB	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.2	133.4	63.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.2	0.4	53.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.4	39.4	37.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.5	0.1	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.1	39.4	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	13.5	°C/W

7.5 Electrical Characteristics

V_{IN} = 3.6 V, T_J = –40°C to 125°C, STOP = GND, MODE = GND, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q\_NO\_LOAD}$	No load operating input current	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.8V MODE = GND, device switching		60		nA
$I_{Q\_NO\_LOAD}$	No load operating input current	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.2V, MODE = GND device switching		80		nA
$I_{Q\_NO\_LOAD}$	No load operating input current (PWM Mode)	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.8V, MODE = V_{IN} device switching		3		mA
I_{Q_VIN}	Operating quiescent current into pin VIN	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.55V or V_{OUT} = 1.8V MODE = GND, device not switching, T_J = 25°C (DLC package option)		44	100	nA
I_{Q_VOS}	Operating quiescent current into pin VOS	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.55V or V_{OUT} = 1.8V MODE = GND, device not switching, T_J = 25°C (DLC package option)		41	120	nA
I_{Q_VIN}	Operating quiescent current into pin VIN	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.55V or V_{OUT} = 1.8V MODE = GND, device not switching, T_J = -40°C to 85°C (DLC and DGR package options)		44	290	nA
		EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.55V or V_{OUT} = 1.8V MODE = GND, device not switching, T_J = -40°C to 85°C (YBG package option)		44	360	nA
I_{Q_VOS}	Operating quiescent current into pin VOS	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.55V or V_{OUT} = 1.8V MODE = GND, device not switching, T_J = -40°C to 85°C		41	150	nA
I_{Q_VOS}	Operating quiescent current into VOS pin	EN = V_{IN}, V_{OUT} = 3.3V, MODE = GND device not switching		50		nA
		EN = V_{IN}, V_{OUT} < 1.5 V, MODE = GND device not switching		5		nA
		EN, STOP = V_{IN}, 3V < V_{OUT} < 3.3V, MODE = GND T_J = -40°C to 85°C		5	100	nA
$I_{Q\_100\%\_MODE}$	Operating quiescent current 100% Mode	V_{IN} = V_{OUT} = 3.3V, T_J = -40°C to 85°C		150		nA
$I_{Q\_VIN\_STOP}$	Operating quiescent current into pin VIN	STOP = High, V_{OUT} = 1.8V, T_J = -40°C to 85°C		90	175	uA

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Electrical Characteristics (continued)

V_{IN} = 3.6 V, T_J = –40°C to 125°C, STOP = GND, MODE = GND, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SD}	Shutdown current	EN = GND, shutdown current into V_{IN} VSET = GND, MODE = GND, T_J = -40°C to 85°C (DLC and DGR package options)		20	250	nA
		EN = GND, shutdown current into V_{IN} VSET = GND, MODE = GND, T_J = -40°C to 85°C (YBG package option)		20	300	nA
V_{TH_UVLO+}	Undervoltage lockout threshold	Rising V_{IN}		1.72	1.8	V
$V_{TH\_UVLO–}$		Falling V_{IN}		1.45	1.75	V
EN, MODE, STOP INPUTS						
V_{IH_TH}	High level input voltage		1.1			V
V_{IL_TH}	Low level input voltage				0.4	V
I_{IN}	Input bias current	T_J = -40°C to 85°C		1	25	nA
R_{PD}	Internal pull-down resistance	EN, STOP inputs	200	450		kΩ
POWER SWITCHES						
$R_{DS(ON)}$	High-side MOSFET on-resistance (SON, WCSP package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		430	600	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		340	465	
	Low-side MOSFET on-resistance (SON, WCSP package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		170	240	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		135	180	
	High-side MOSFET on-resistance (HVSSOP package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		460	630	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		370	495	
	Low-side MOSFET on-resistance (HVSSOP package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		200	270	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		165	210	
I_{LIMF_SS}	Soft-start switch current limit	open-loop	0.15	0.225	0.3	A
I_{LIMF}	High-side MOSFET switch current limit	open-loop	1.0	1.2	1.4	A
	Low-side MOSFET switch current limit	open-loop		1.0		A
I_{LIM_DELAY}	Current limit propagation delay			50		ns
I_{LKG_SW}	Leakage current into SW pin	V_{SW} = 1.8V, T_J = -40°C to 85°C		10		nA
OUTPUT VOLTAGE DISCHARGE						
$I_{DISCHARGE\_VOS}$	Output discharge current	EN = GND, sink current into VOS pin, over VIN range V_{OUT} = 1.8V, T_J = -40°C to 85°C	16	35	44	mA
THERMAL PROTECTION						
T_{SD}	Thermal shutdown temperature	Rising junction temperature		160		°C
	Thermal shutdown hysteresis			5		°C
OUTPUT						
V_{OUT}	Output voltage accuracy	MODE = GND, I_{OUT} = 0 mA, V_{OUT} > 1.8 V		±2		%
V_{OUT}	Output voltage accuracy	MODE = GND, I_{OUT} = 0 mA, V_{OUT} <= 1.55 V		±2.5		%
V_{OUT}	Output voltage accuracy	PWM Mode. I_{OUT} = 0 mA, V_{OUT} > 1.8 V	-1.5	0	1.5	%
		PWM Mode. I_{OUT} = 0 mA, V_{OUT} <= 1.55 V	-2	0	2	%
V_{OUT}	DC output voltage load regulation	PWM Mode		0		%/mA
	DC output voltage line regulation	PWM Mode V_{OUT} = 1.8V, I_{OUT} = 200 mA, over VIN range		0		%/V
f_{SW}	Switching frequency	V_{IN} = 3.6V, V_{OUT} = 1.8V, MODE = V_{IN} I_{OUT} = 0mA		1.8		MHz

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Electrical Characteristics (continued)

V_{IN} = 3.6 V, T_J = –40°C to 125°C, STOP = GND, MODE = GND, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{STARTUP\_DELAY}$	Regulator start up delay time	V_{IN} = 3.6V, from EN = low to high until device starts switching			200	µs
t_{SS}	Soft-start time	I_{OUT} = 0mA		120		µs
t_{SS_ILIMF}	Reduced current limit soft-start timeout			700	1200	µs

ADVANCE INFORMATION

7.6 Typical Characteristics

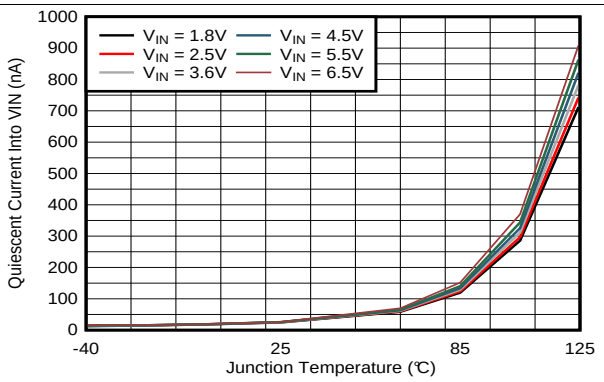


Figure 1. Quiescent Current Into VIN (I_{Q_VIN})

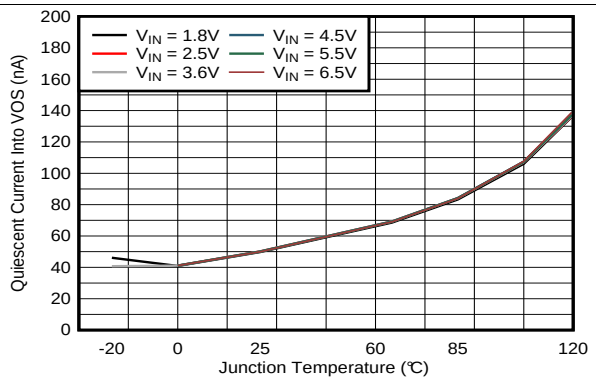


Figure 2. Quiescent Current Into VOS (I_{Q_VOS})

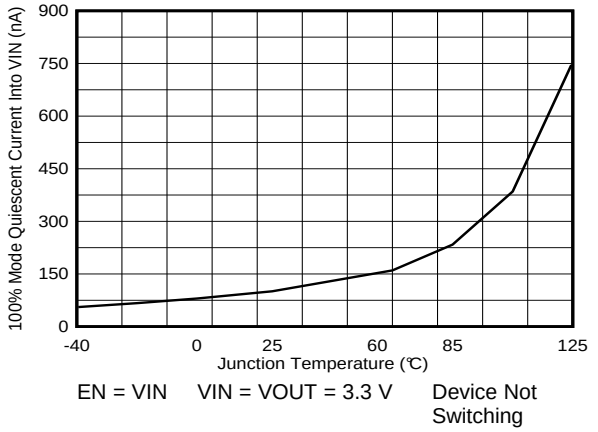


Figure 3. 100% Mode Quiescent Current Into VIN ($I_{Q\_100\%\_MODE\_VIN}$)

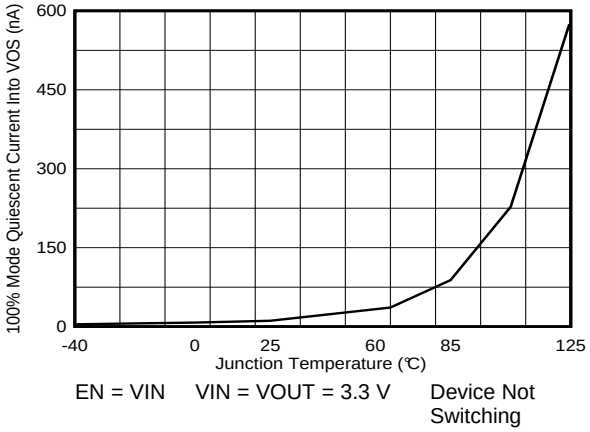


Figure 4. 100% Mode Quiescent Current Into VOS ($I_{Q\_100\%\_MODE\_VOS}$)

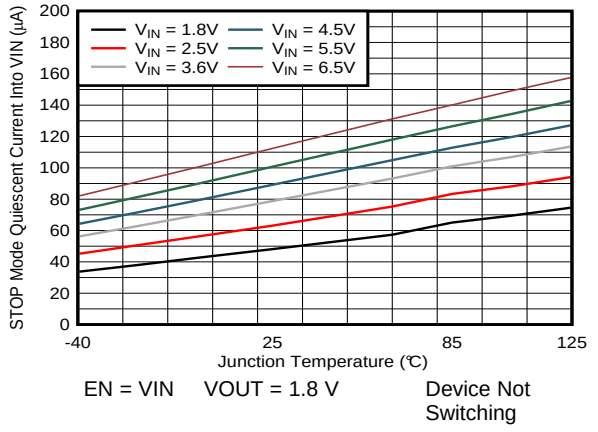


Figure 5. STOP Mode Quiescent Current Into VIN ($I_{Q\_VIN\_STOP}$)

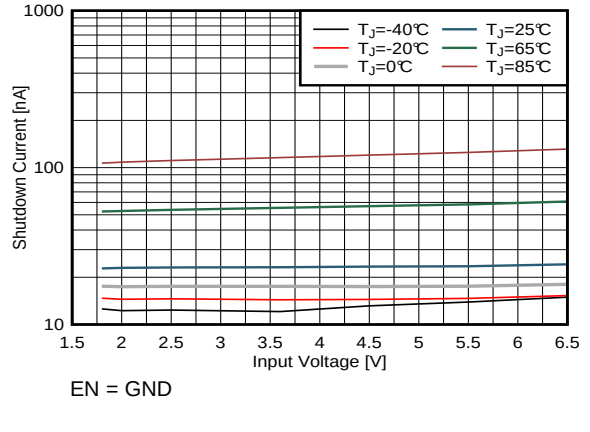


Figure 6. Shutdown Current (I_{SD})

ADVANCE INFORMATION

Typical Characteristics (continued)

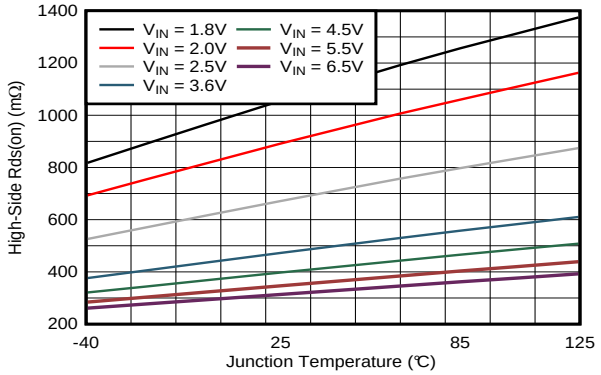


Figure 7. High-Side R_{DSON} vs. Temperature (DLC, YBG packages)

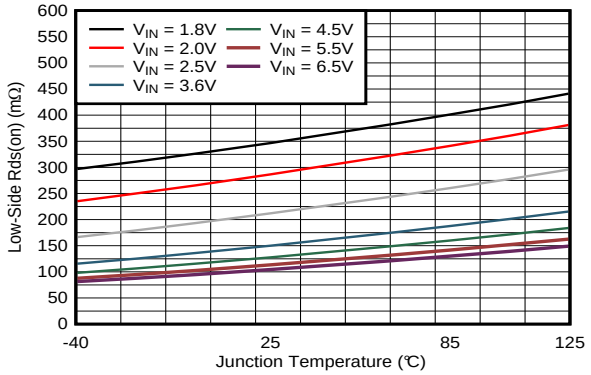


Figure 8. Low-Side R_{DSON} vs. Temperature (DLC, YBG packages)

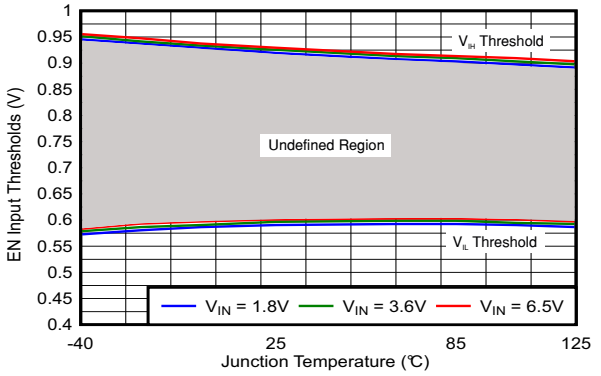


Figure 9. EN Input Thresholds vs. Temperature

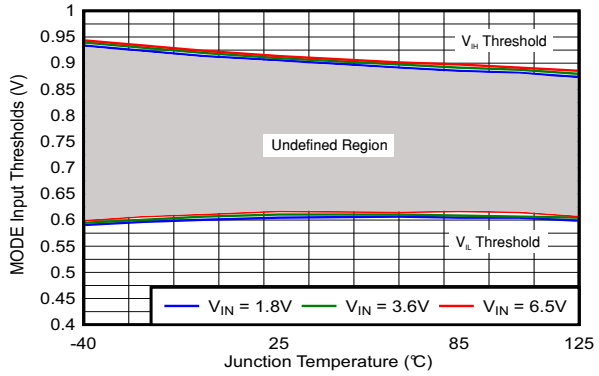


Figure 10. MODE Input Thresholds vs. Temperature

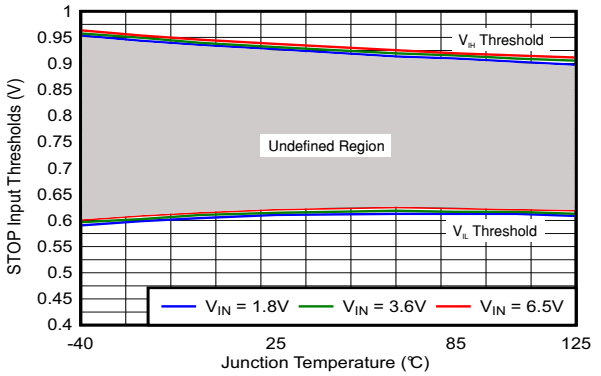
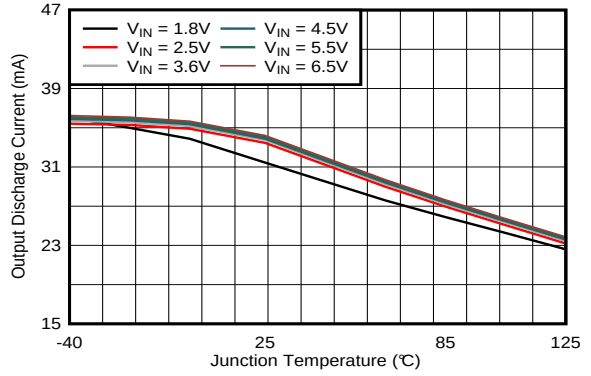


Figure 11. STOP Input Thresholds vs. Temperature



EN = GND VOUT = 1.8 V

Figure 12. Output Discharge Current vs. Temperature

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

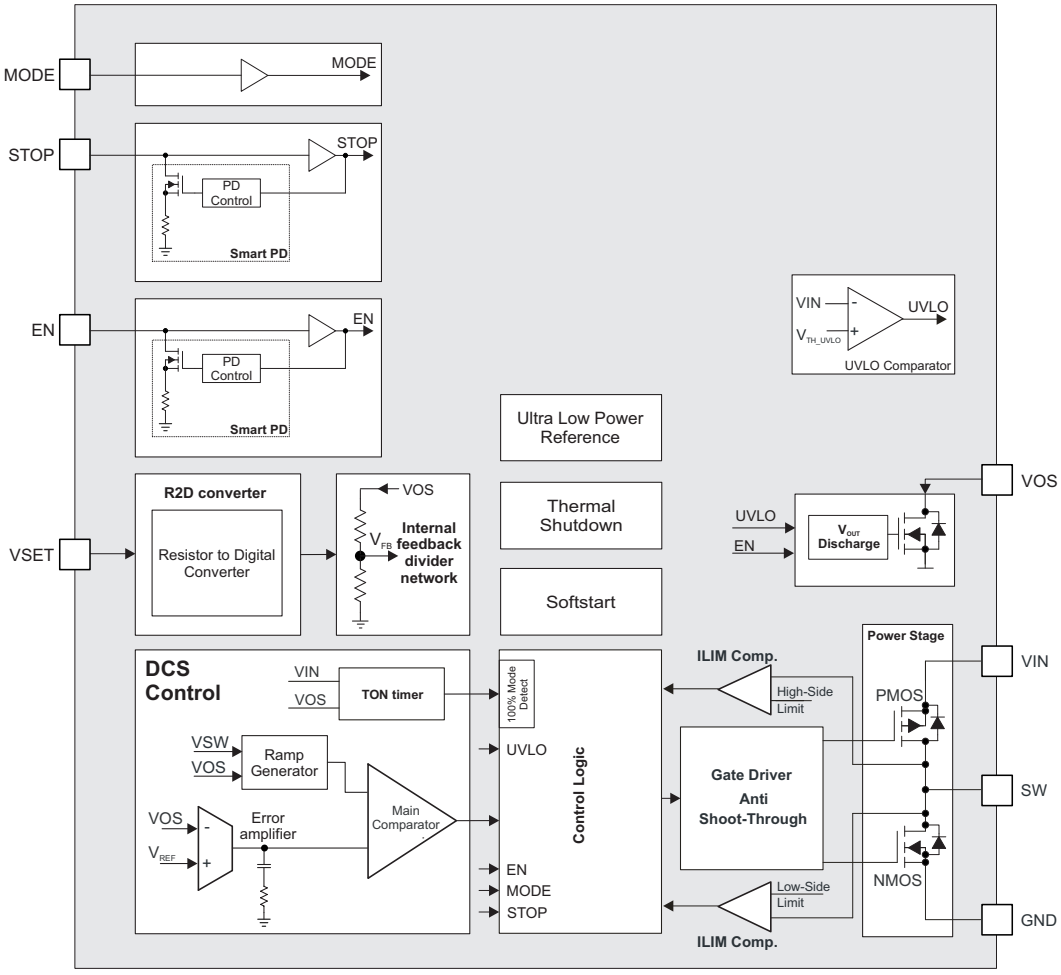
The TPS62840 is a synchronous step-down converter with ultra-low quiescent current consumption. Using TI's DCS-Control™ topology the device extends the high efficiency operation area down to micro amperes of load current during Power-Save Mode Operation.

TI's DCS-Control™ (Direct Control with Seamless Transition into Power-Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode controls. Characteristics of DCS-Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM mode operation. DCS-Control™ includes an AC loop which senses the output voltage (VOS pin) and directly feeds this information into a fast comparator stage.

The device operates with a quasi-fixed frequency of 1.8MHz (typ). A high gain voltage feedback loop is used to achieve accurate DC load regulation. To save extra quiescent current under light load condition (i.e. I_{OUT} in the mA range), the internal error amplifier is powered down with a minimum influence on the DC line and load regulation characteristic. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

In Power-Save Mode, the switching frequency varies linearly with the load current. Since DCS-Control™ supports both operating modes with one single building block, the transition from PWM to PFM is seamless with minimum output voltage ripple. The TPS62840 offers both excellent DC voltage and superior load transient regulation, combined with low output voltage ripple thereby minimizing interferences with RF circuits.

8.2 Functional Block Diagram



ADVANCE INFORMATION

8.3 Feature Description

8.3.1 Smart Enable and Shutdown

To avoid a floating input an internal 450kΩ resistor pulls the EN pin to GND. This prevents an uncontrolled start-up of the device in case the EN pin can not be driven low safely. The device is in shutdown mode when the EN input is logic low.

The device turns on with a logic high EN signal. An internal control circuit disconnects the EN pin pull-down resistor once the reference system and the control logic have been powered up successfully and the output voltage is in regulation. With the EN pin set low, the device enters shutdown mode and the pull-down resistor is activated again.

8.3.2 Softstart

Once the device has been enabled, it initializes and powers up its internal circuits. This occurs during the regulator start-up delay time ($t_{STARTUP\_DELAY}$). Once this delay expires, the device enters soft-start, starts switching and ramps up the output voltage.

The device operates with a reduced switch current limit (I_{LIMF_SS}) throughout the entire soft-start phase (t_{SS}). The switch current limit is increased to its nominal value (I_{LIMF}) once the output voltage has reached its nominal value or the soft-start time (t_{SS}) has expired, which ever occurs first. The soft-start phase (t_{SS}) can last up to approx. 700µs.

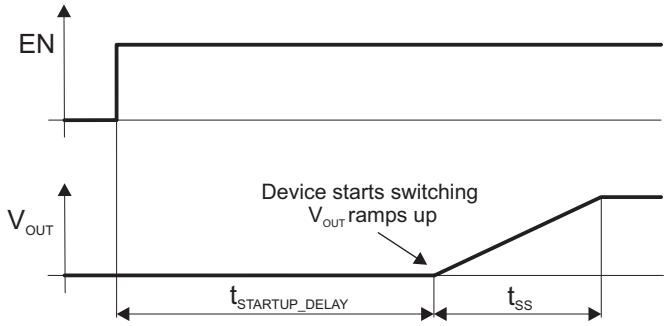


Figure 13. Device Startup

8.3.3 Mode Selection: Power-Save Mode (PFM/PWM) or Forced PWM Operation (FPWM)

Connecting the MODE input to GND enables the automatic PWM and power-save mode operation. The converter operates in quasi-fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter operates with a quasi-fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

8.3.4 Output Voltage Selection (VSET)

The output voltage is set with a single external resistor connected between the VSET and GND pins. Once the device has been enabled and the control logic as well as the reference system are powered-up, an R2D (resistor to digital) conversion is started to detect the value of the external R_{SET} resistor. A pre-defined fixed output voltage is set based on the R_{SET} value. The output voltage is preset once during the device startup delay phase.

Once the output voltage is preset, the R2D converter is turned-off to avoid current flowing permanently through the external set resistor. Care must be taken that no parasitic current and/or capacitance greater than 100pF is present between the VSET and GND pins. This could cause false R_{SET} readings and a faulty output voltage set. The R2D converter is designed to operate with resistor values out of E96 series.

ADVANCE INFORMATION

Feature Description (continued)

Table 1. Output Voltage Setting, RSET Resistor

Output voltage setting V_{OUT} [V]			VSET resistance to GND [kΩ] - E96 values		
TPS62841YBG	TPS62840YBG	TPS62842YBG	MIN	NOM	MAX
TPS62841DLC	TPS62840DLC	TPS62842DLC			
0.8	1.8	1.8	0	GND	0.01
0.85	1.9	2.0	0.87	0.909	0.95
0.9	2.0	2.2	1.67	1.74	1.81
0.95	2.1	2.4	2.76	2.87	2.98
1.0	2.2	2.5	4.15	4.32	4.49
1.05	2.3	2.6	5.80	6.04	6.28
1.1	2.4	2.7	8.11	8.45	8.79
1.15	2.5	2.8	11.04	11.5	11.96
1.2	2.6	2.9	15.17	15.8	16.43
1.25	2.7	3.0	20.64	21.5	22.36
1.3	2.8	3.1	27.55	28.7	29.85
1.35	2.9	3.2	36.77	38.3	39.83
1.4	3.0	3.3	50.21	52.3	54.39
1.45	3.1	3.4	68.64	71.5	74.36
1.5	3.2	3.49	97.92	102	106.08
1.55	3.3	3.59	256.32	267	277.68

8.3.5 Undervoltage Lockout UVLO

To avoid mis-operation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.75V (max.) with falling V_{IN}. The device will start at an input voltage of 1.8V(max.) rising V_{IN}.

When the device resumes operation from an under voltage lockout condition, it behaves like being enabled (i.e. the internal control logic is powered-up and the external R_{SET} resistor is read out).

8.3.6 Switch Current Limit / Short Circuit Protection

The TPS62840 integrates a current limit on the high-side as well as on the low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle-by-cycle. If the high-side MOSFET current limit (I_{LIMF}) trips, the high-side element is turned off and the low-side MOSFET is turned on thereby ramping the inductor current down. Once the inductor current has decreases below the low-side current limit (I_{LIMF}), the low-side device is turns off and the high-side MOSFET turns on again.

8.3.7 Output Voltage Discharge of the Buck Converter

The purpose of the output discharge function is to ensure a defined ramp-down of the output voltage when the device is disabled. The device will maintain the output voltage close to zero in shutdown. For the output discharge function to become active, the device needs to be enabled at least once after applying the supply voltage (i.e. applying the input supply for the first time while the device is disabled will not activate the output discharge function).

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is $V_{IN} > V_{TH\_UVLO-}$.

8.3.8 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. The device enters thermal shutdown when the junction temperature exceeds the thermal shutdown threshold (T_{SD}) of 160°C (typ.). Both the high-side and low-side power FETs are turned-off. The device continues its operation when the junction temperature falls below typically 150°C again. The converter resumes operation by beginning with a soft-start cycle. In Power-Save Mode, the thermal shutdown feature is not active during skip pause longer than 20µs.

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8.3.9 STOP Mode

The TPS62840 includes the STOP input pin, allowing the user to temporarily stop the regulator switching regardless of the mode of operation.

When a logic high level is applied to the STOP pin, the regulator is forced to stop switching after the current cycle. In this case, the application is powered by the charge available in the output capacitor. No switching noise is generated which could beneficial in noise sensitive sampled applications.

An MCU controlling this pin needs to take care to turn the device back on before the output voltage reaches a system critical level. Should this not happen, the output voltage will be clamped to nominal set point - ca. 0.5V (e.g. V_{OUT} clamped to approx. 1.3V for a 1.8V regulated output voltage). In STOP mode, the device consumes approx. 90µA operating quiescent current from the input supply.

When a logic low level is applied to the STOP pin, the regulator resumes switching operation. To avoid a floating input an internal 450kΩ resistor pulls the STOP pin to GND. A control circuit disconnects the pull-down resistor at the STOP pin once a high level has been detected (similarly to the EN pin).

8.4 Device Functional Modes

8.4.1 Power-Save Mode Operation

The DCS-Control™ topology supports Power-Save Mode operation. The device operates at light loads in PFM (Pulse Frequency Modulation) mode that generates a single switching pulse to ramp-up the inductor current and recharges the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typical 60nA. This low quiescent current consumption is achieved by an ultra-low power reference, an integrated high impedance feedback divider network and an optimized Power-Save Mode operation.

In PFM Mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device enters automatically PWM (Pulse Width Modulation) mode and operates in continuous conduction mode with a nominal switch frequency (f_{SW}). The switching frequency in PWM mode is controlled and depends on V_{IN} and V_{OUT}. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to ultra-light loads. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to PFM modes is seamless with minimum output voltage ripple.

8.4.2 Forced PWM Mode Operation

With a high level on the MODE input, the device enters forced PWM Mode and operates with a quasi-constant switching frequency over the entire load range, even at very light loads. This reduces or eliminates interference with RF and noise sensitive circuits, but reduces efficiency at light loads.

8.4.3 100% Mode Operation

In PWM mode, the duty-cycle of a buck converter is given as $D = V_{OUT}/V_{IN}$. The duty-cycle increases as the input voltage comes closer to the output voltage. As the input voltage decreases to the point the on-time reaches 1.6µs, the nominal output set point is offset by +30mV. As the input voltage decreases further, the device enters 100% duty-cycle mode and maintains the high-side switch on continuously. The output (V_{OUT}) is connected to the input (V_{IN}) via the inductor and the internal high-side MOSFET switch. The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_{OUT}max + I_{OUT}max \times (R_{DS(on)}max + R_L)$$

where

- $I_{OUT}max$ = Maximum output current plus inductor ripple current
- $R_{DS(on)}max$ = Maximum P-channel switch $R_{DS(on)}$
- R_L = DC resistance of the inductor
- $V_{OUT}max$ = Nominal output voltage plus maximum output voltage tolerance

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

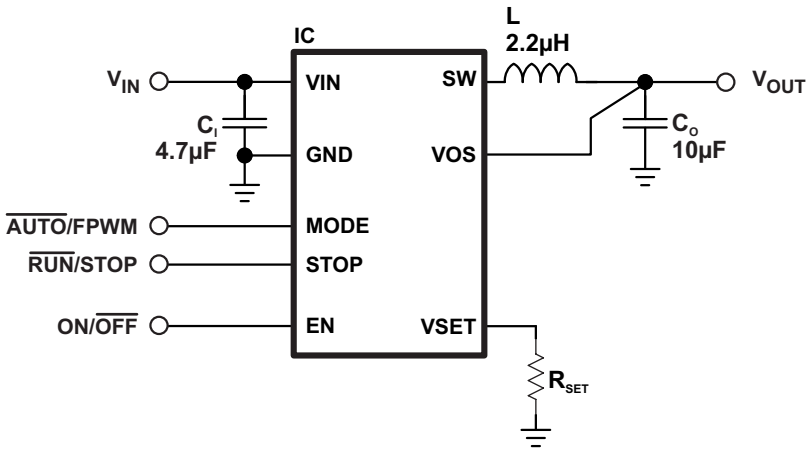

Figure 14. TPS62840 Adjustable V_{OUT} Application Circuit

Additional circuits are shown in the *System Examples* section.

9.2.1 Design Requirements

Table 2 shows the list of components for the application circuit and the characteristic application curves

Table 2. Components for Application Characteristic Curves

Reference	Description	Value	Size [L x W x T]	Manufacturer(1)
IC	TPS62840 step-down converter			TI
C_I	GRM155R61A475MEAAD ceramic capacitor	4.7 µF / 10V / X5R	(0402) [1mm x 0.5mm x 0.65mm max.]	muRata
C_O	GRM155R60G106ME44D ceramic capacitor	10 µF / 4V / X5R	(0402) [1mm x 0.5mm x 0.65mm max.]	muRata
L	DFE201612E-2R2M=P2 inductor	2.2 µH / 100mΩ DCR	[2.0mm x 1.6mm x 1.2mm max.]	muRata
R_{SET}	Resistor E96 series 1%, TC ±200ppm	see Table 1		

(1) See *Third-party Products Disclaimer*

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9.2.2 Detailed Design Procedure

The inductor and output capacitor together provide a low-pass filter. To simplify this process, Table 3 outlines possible inductor and capacitor value combinations.

Table 3. Recommended LC Output Filter Combinations

Inductor Value [µH](1)	Output Capacitor Value [µF](2)	
	10µF	22µF
2.2	√(3)	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -20%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance varies by +20% and –50%.
(3) Typical application configuration. Other check marks indicate alternative filter combinations.

9.2.2.1 Inductor Selection

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according to Equation 1.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, as calculated with Equation 2. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit, I_{LIMF}.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- f = Switching Frequency
- L = Inductor Value
- ΔI_L= Peak to Peak inductor ripple current
- I_{Lmax} = Maximum Inductor current

The table below shows a list of possible inductors.

Table 4. List of Possible Inductors(1)

INDUCTANCE [µH]	INDUCTOR TYPE	SIZE [L x W x T]	SUPPLIER
2.2	DFE201612	[2.0mm x 1.6mm x 1.2mm max.]	muRata

(1) See *Third-party Products Disclaimer*

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9.2.2.2 Output Capacitor Selection

The DCS-Control™ scheme of the TPS62840 allows the use of tiny ceramic capacitors. Ceramic capacitors with low-ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric.

At light load currents, the converter operates in Power-Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple. The leakage current of the output capacitor adds to the overall quiescent current.

Table 5. List of Possible Capacitors(1)

CAPACITOR [µF]	CAPACITOR TYPE	SIZE IMPERIAL (METRIC)	SIZE [L x W x T]	SUPPLIER
10	GRM155R60G106ME44D	0402 (1005)	[1mm x 0.5mm x 0.65mm max.]	muRata

(1) See *Third-party Products Disclaimer*

9.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications a 4.7-µF input capacitor is sufficient.

When operating from a high impedance source, a larger input buffer capacitor is recommended avoiding voltage drops during start-up and load transients.

The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall quiescent current. shows a selection of input and output capacitors.

Table 6. List of Possible Capacitors(1)

CAPACITOR [µF]	CAPACITOR TYPE	SIZE IMPERIAL (METRIC)	SIZE [L x W x T]	SUPPLIER
4.7	GRM155R61A475MEAAD	0402 (1005)	[1mm x 0.5mm x 0.65mm max.]	muRata
4.7	GRM31CR71H475MA12L	1206 (3216)	[3.2mm x 1.6mm x 1.8mm max.]	muRata
4.7	C1608X7S1A475M080AC	0603 (1608)	[1.6mm x 0.8mm x 1.0mm max.]	TDK
10	GRM155R60J106ME15D	0402 (1005)	[1mm x 0.5mm x 0.65mm max.]	muRata

(1) See *Third-party Products Disclaimer*

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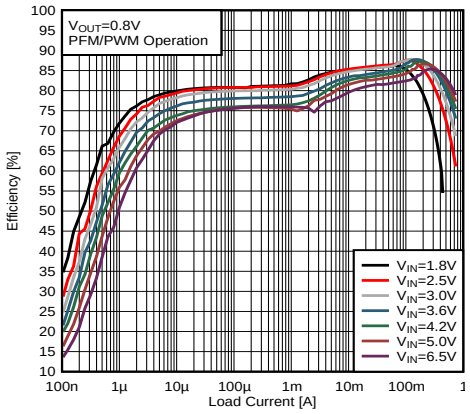
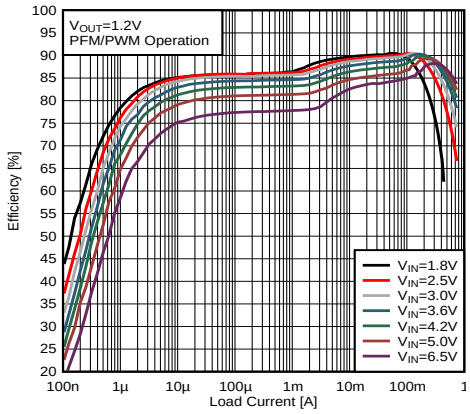
9.2.3 Application Curves

The condition for below application curves are V_{IN} = 3.6V, V_{OUT} = 1.8V, MODE = GND, STOP = GND and the used components listed in Table 2, unless otherwise noted.



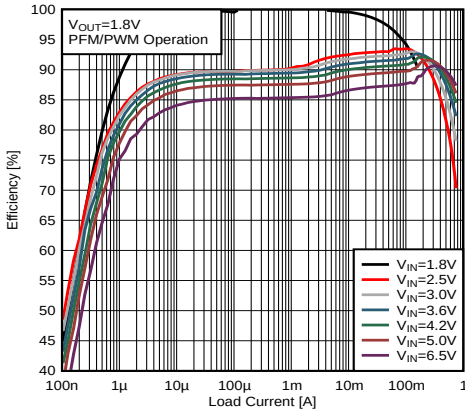
R_{SET} = 0Ω to GND

Figure 15. Efficiency Power Save Mode V_{OUT} = 0.8V



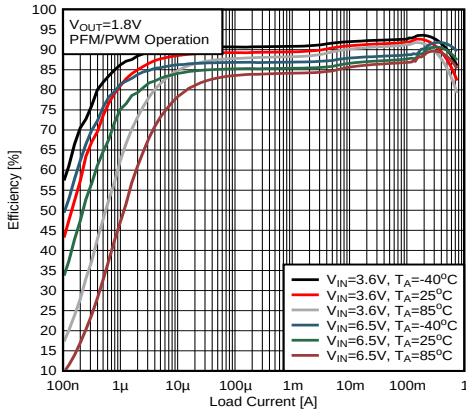
R_{SET} = 15.8kΩ to GND

Figure 16. Efficiency Power Save Mode V_{OUT} = 1.2V



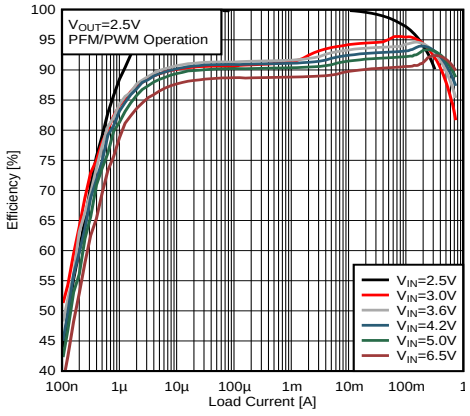
R_{SET} = 0Ω to GND

Figure 17. Efficiency Power Save Mode V_{OUT} = 1.8V



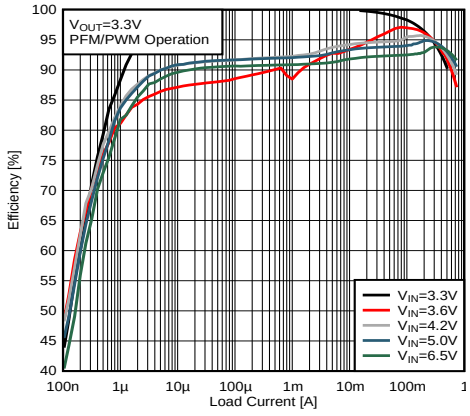
R_{SET} = 0Ω to GND

Figure 18. Efficiency Power Save Mode V_{OUT} = 1.8V



R_{SET} = 11.5kΩ to GND

Figure 19. Efficiency Power Save Mode V_{OUT} = 2.5V



R_{SET} = 267kΩ to GND

Figure 20. Efficiency Power Save Mode V_{OUT} = 3.3V

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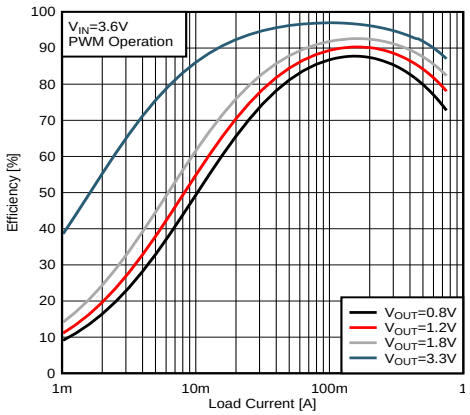
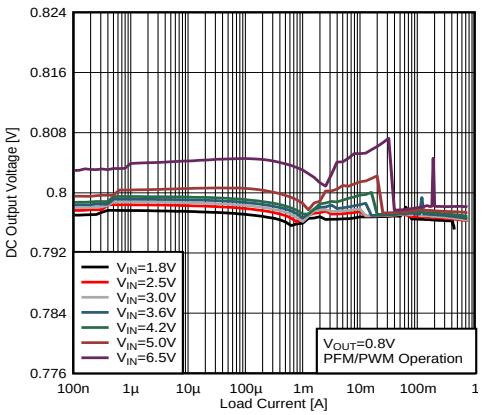
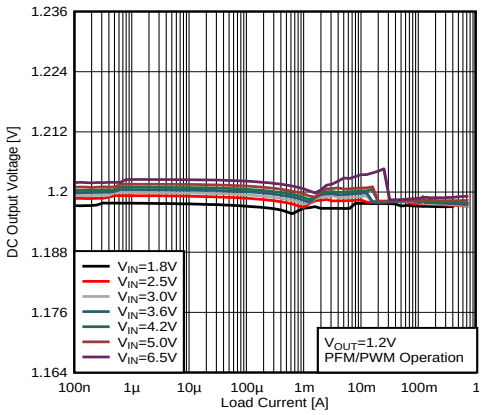


Figure 21. Efficiency Forced PWM Mode
V_{OUT} = 0.8V / 1.2V / 1.55V / 1.8V / 2.5V / 3.3V



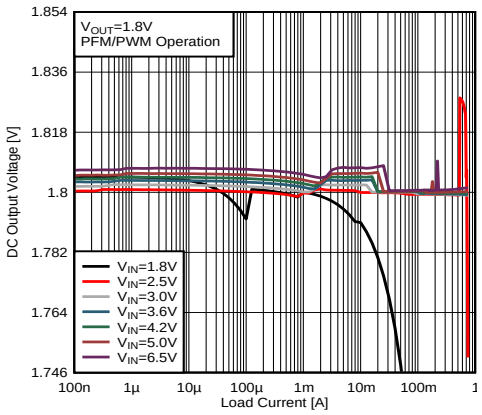
R_{SET} = 0Ω to GND

Figure 22. Output Voltage vs. Load Current
V_{OUT} = 0.8V



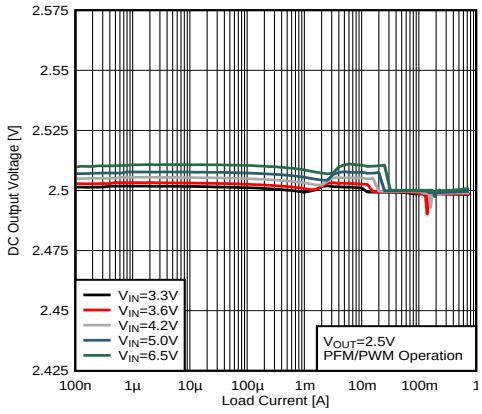
R_{SET} = 15.8kΩ to GND

Figure 23. Output Voltage vs. Load Current
V_{OUT} = 1.2V



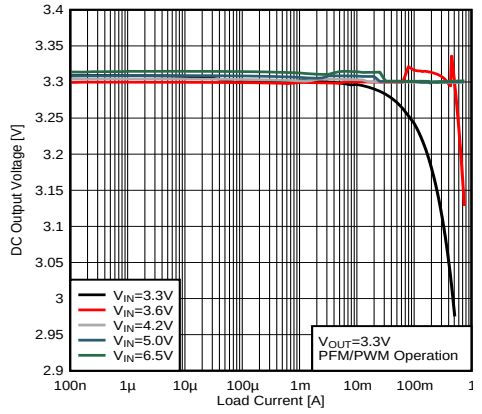
R_{SET} = 0Ω to GND

Figure 24. Output Voltage vs. Load Current
V_{OUT} = 1.8V



R_{SET} = 11.5kΩ to GND

Figure 25. Output Voltage vs. Load Current
V_{OUT} = 2.5V



R_{SET} = 267kΩ to GND

Figure 26. Output Voltage vs. Load Current
V_{OUT} = 3.3V

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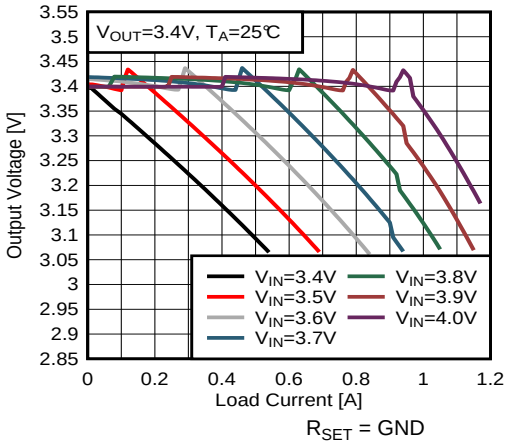


Figure 27. Output Voltage vs. Load Current
V_{OUT} = 3.4V

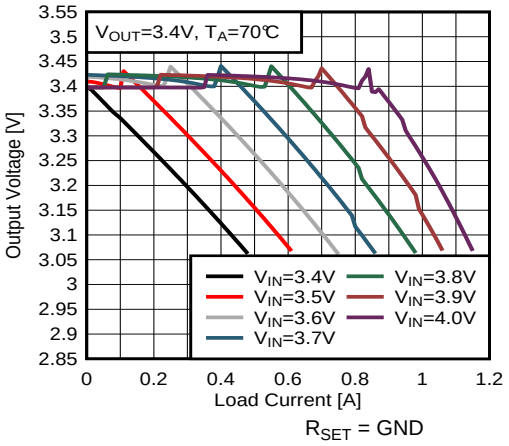


Figure 28. Output Voltage vs. Load Current
V_{OUT} = 3.4V

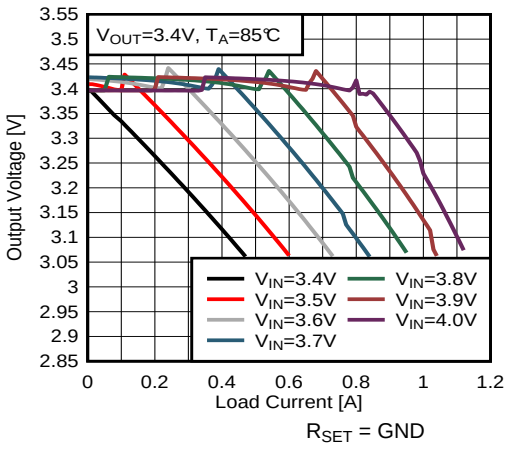


Figure 29. Output Voltage vs. Load Current
V_{OUT} = 3.4V

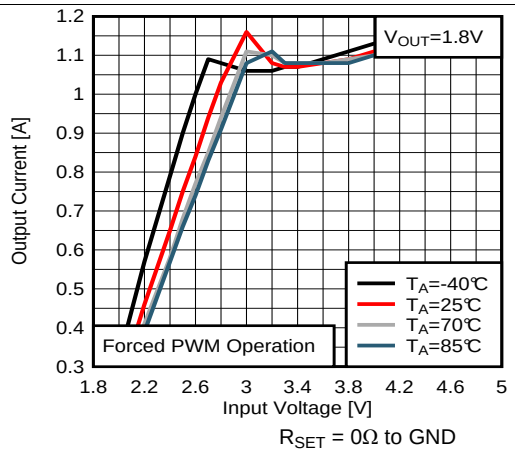


Figure 30. Output Current vs. Input Voltage
V_{OUT} = 1.8V

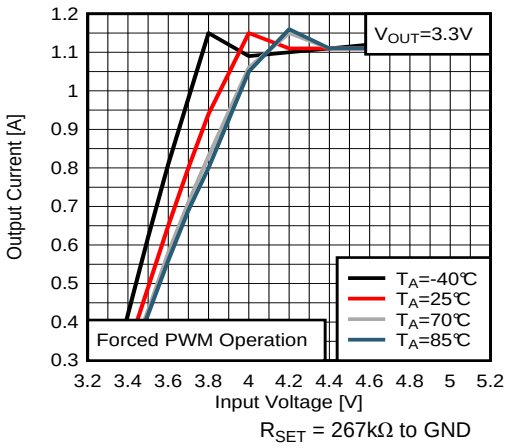


Figure 31. Output Current vs. Input Voltage
V_{OUT} = 3.3V

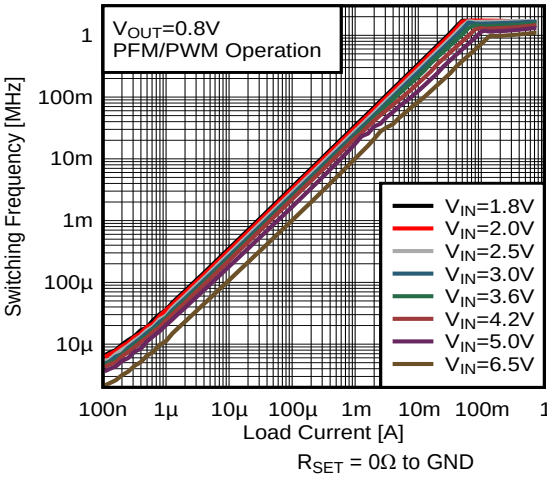


Figure 32. Switching Frequency vs. Load Current
V_{OUT} = 0.8V

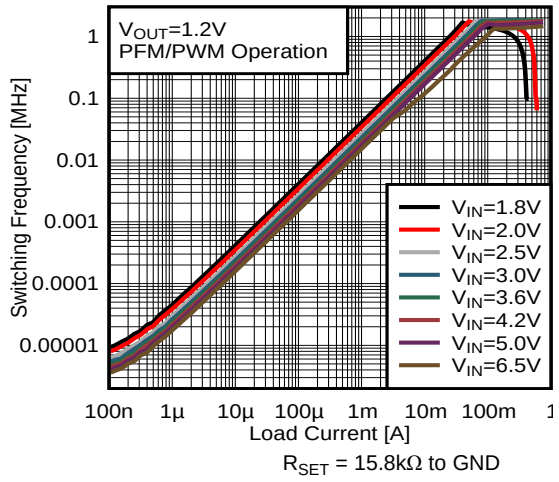


Figure 33. Switching Frequency vs. Load Current
V_{OUT} = 1.2V

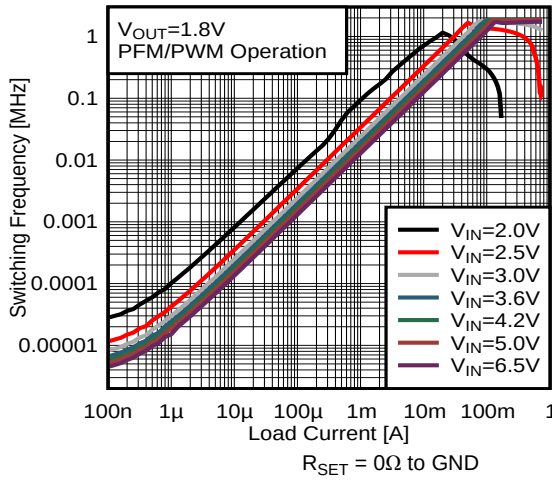


Figure 34. Switching Frequency vs. Load Current
V_{OUT} = 1.8V

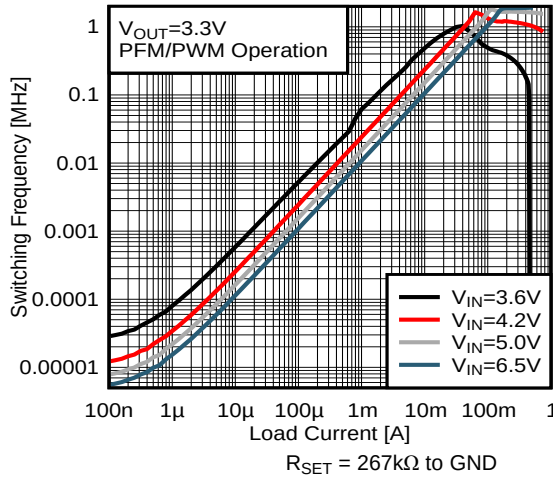


Figure 35. Switching Frequency vs. Load Current
V_{OUT} = 3.3V

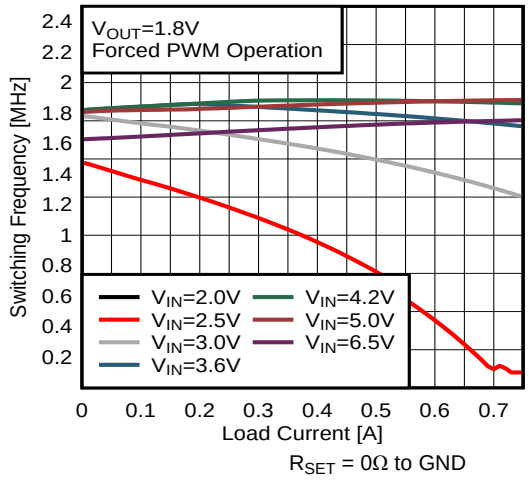


Figure 36. Switching Frequency vs. Load Current
V_{OUT} = 1.8V

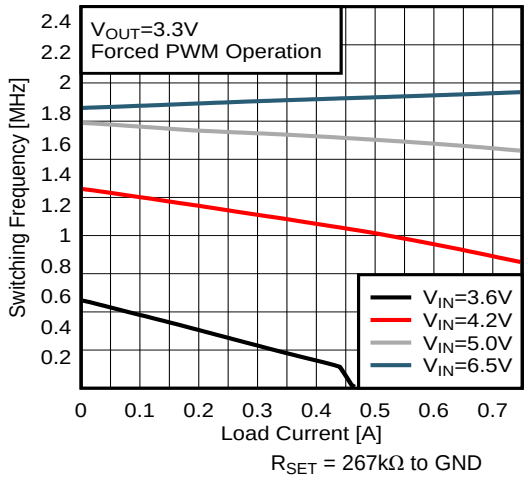


Figure 37. Switching Frequency vs. Load Current
V_{OUT} = 3.3V

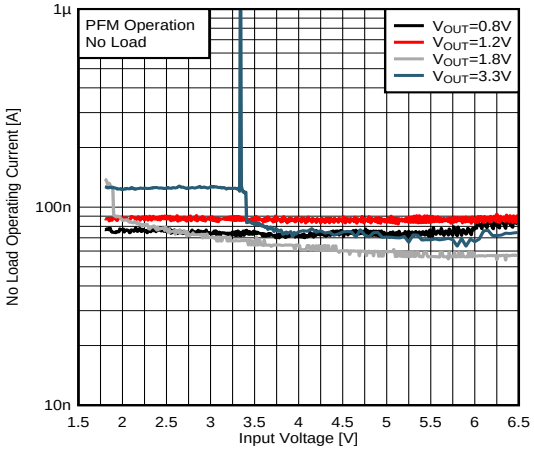


Figure 38. No Load Operating Current vs. Input Voltage

ADVANCE INFORMATION

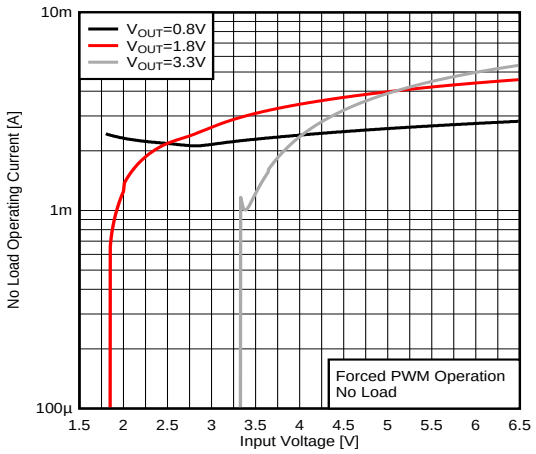
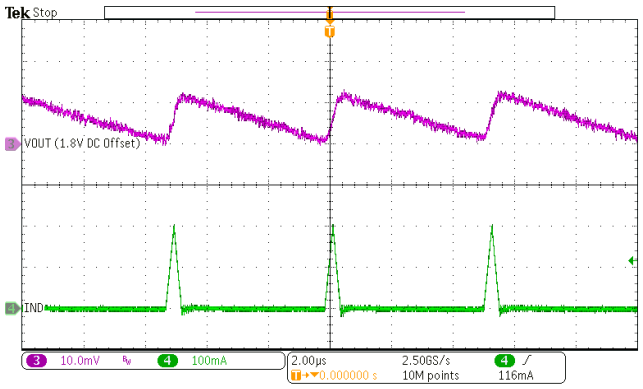
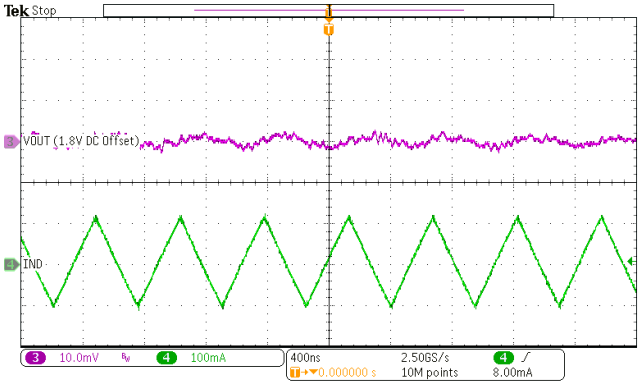


Figure 39. No Load Operating Current vs. Input Voltage



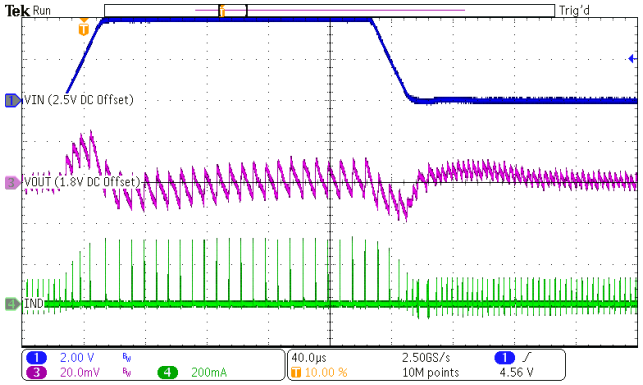
V_{OUT} = 1.8V I_{OUT} = 10mA

Figure 40. PFM Operation



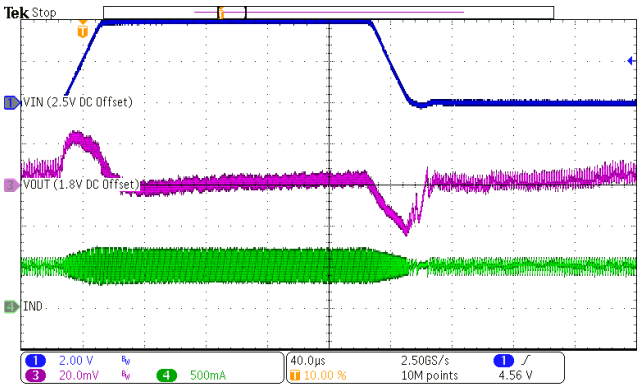
V_{OUT} = 1.8V I_{OUT} = 10mA
MODE = HIGH

Figure 41. PWM Operation



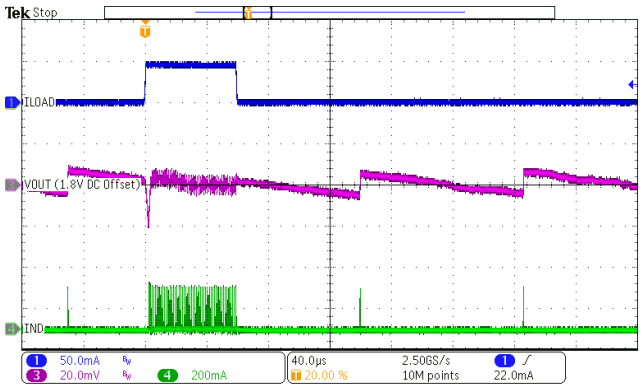
V_{OUT} = 1.8V V_{IN} = 2.5V to 6.5V
rise/fall time = 20µs I_{OUT} = 10mA

Figure 42. Line Transient PFM Mode



V_{OUT} = 1.8V V_{IN} = 2.5V to 6.5V
rise/fall time = 20µs I_{OUT} = 500mA

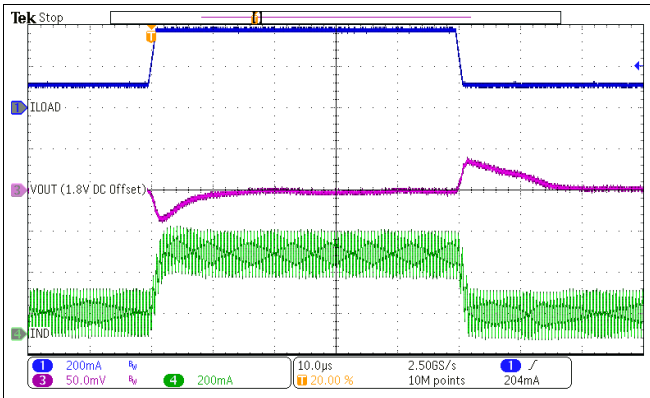
Figure 43. Line Transient PWM Mode



V_{OUT} = 1.8V V_{IN} = 3.6V
rise/fall time < 1µs I_{OUT} = 125µA to 50mA

Figure 44. Load Transient PFM Mode

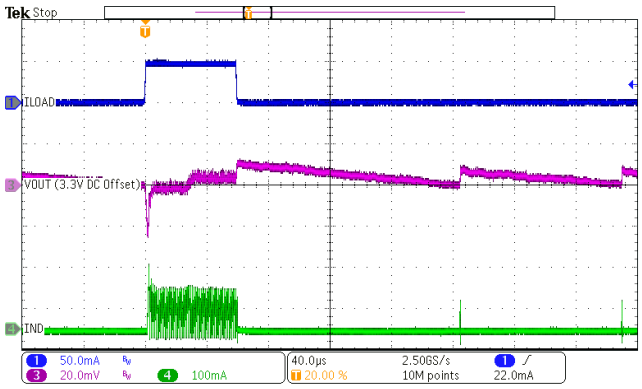
ADVANCE INFORMATION



V_{OUT} = 1.8V
rise/fall time < 1µs

V_{IN} = 3.6V
I_{OUT} = 125mA to 375mA

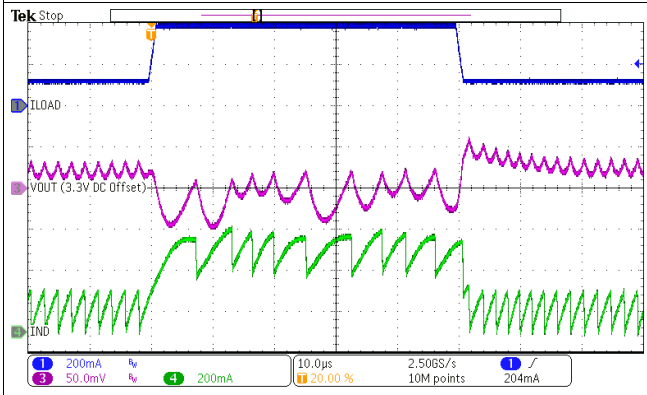
Figure 45. Load Transient PFM/PWM Mode



V_{OUT} = 3.3V
rise/fall time < 1µs

V_{IN} = 3.6V
I_{OUT} = 75µA to 50mA

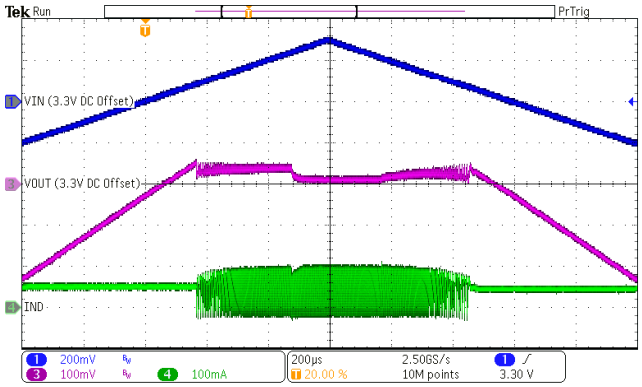
Figure 46. Load Transient PFM Mode



V_{OUT} = 3.3V
rise/fall time < 1µs

V_{IN} = 3.6V
I_{OUT} = 125mA to 375mA

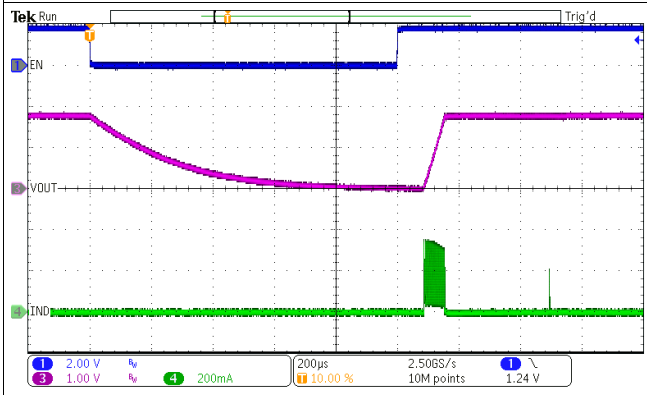
Figure 47. Load Transient PFM/PWM Mode



V_{OUT} = 3.3V

V_{IN} = 3.1V to 3.6V
I_{OUT} = 50mA

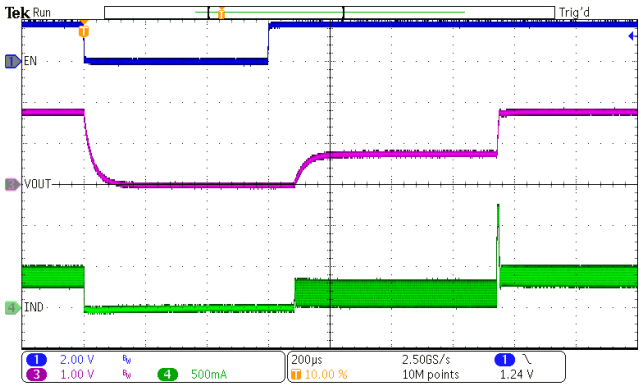
Figure 48. 100% Mode Entry/Exit Operation



V_{OUT} = 1.8V
Turned-on via EN input

V_{IN} = 3.6V
I_{OUT} = 0mA

Figure 49. Startup/Shutdown Into No Load

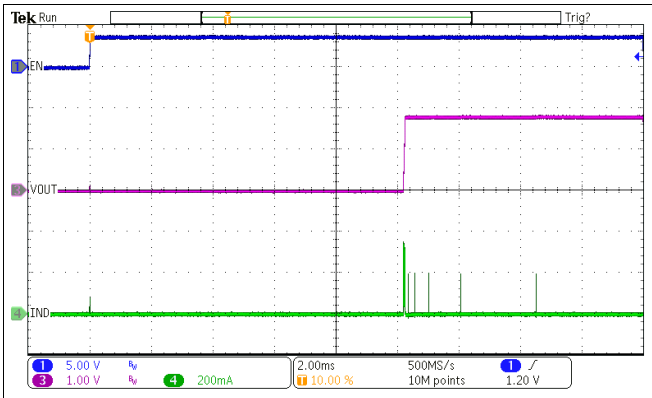


V_{OUT} = 1.8V
Turned-on via EN input

V_{IN} = 3.6V
I_{OUT} = 400mA
R_{LOAD} = 4.5Ω

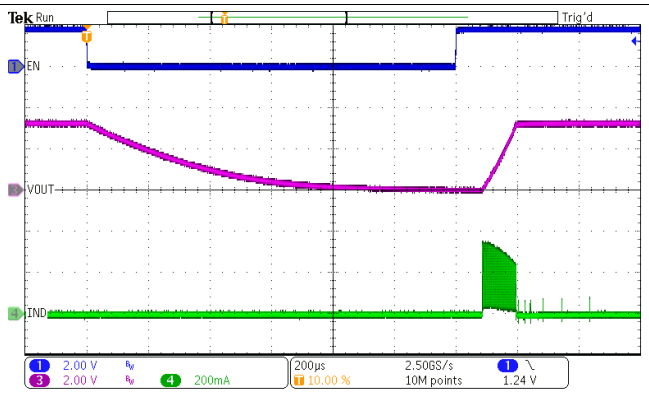
Figure 50. Startup/Shutdown Into No Load

ADVANCE INFORMATION



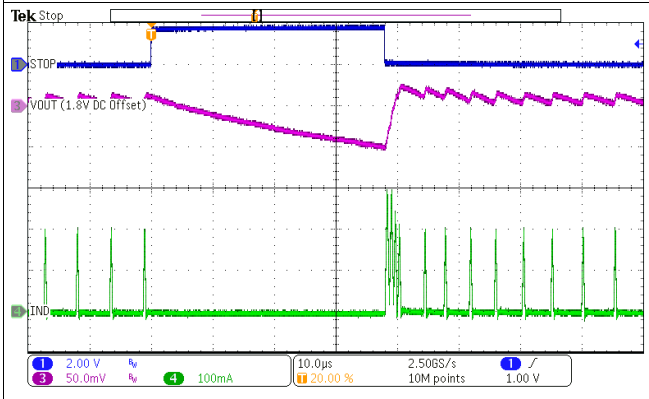
V_{OUT} = 1.8V
V_{IN} rising from 0V to 3.6V
EN = V_{IN}
I_{OUT} = 0mA

Figure 51. Startup/Shutdown Into No Load



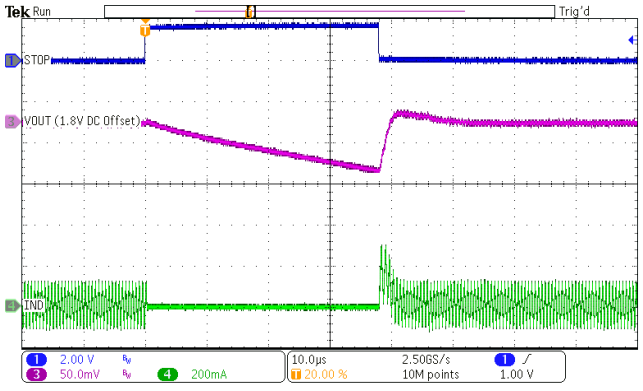
V_{OUT} = 3.3V
Turned-on via EN input
V_{IN} = 3.6V
I_{OUT} = 0mA

Figure 52. Startup/Shutdown Into No Load



V_{OUT} = 1.8V
PFM Operation
V_{IN} = 3.6V
I_{OUT} = 10mA

Figure 53. STOP Mode Operation



V_{OUT} = 1.8V
PWM Operation
V_{IN} = 3.6V
I_{OUT} = 10mA

Figure 54. STOP Mode Operation

ADVANCE INFORMATION

9.3 System Example

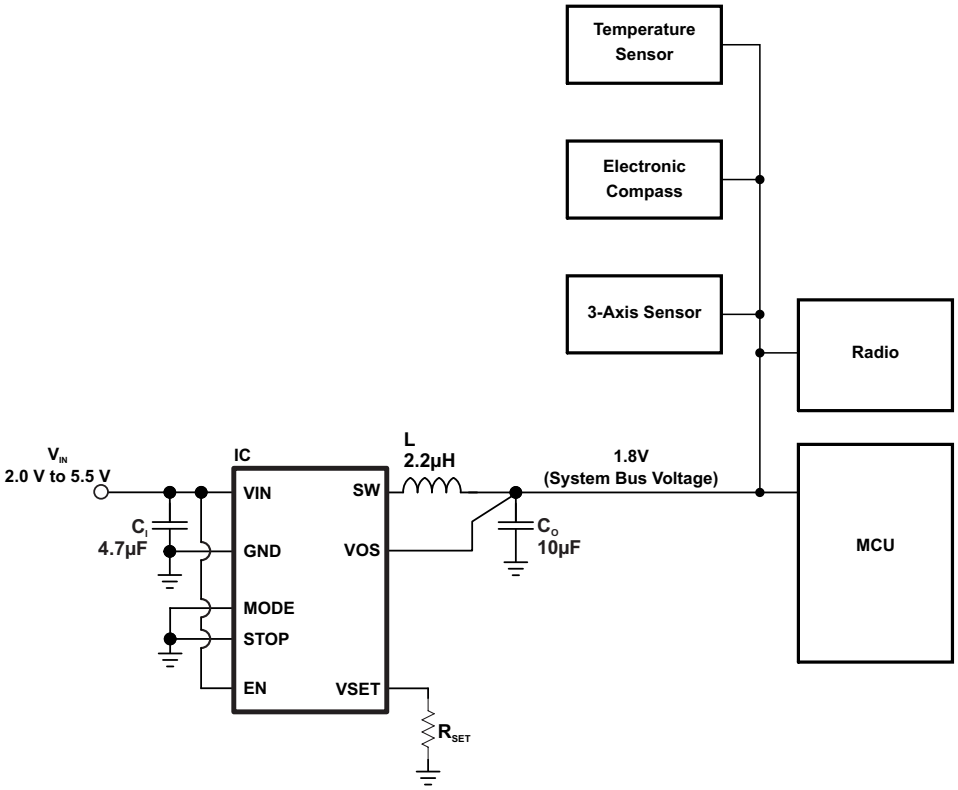


Figure 55. Example Of Implementation In A Master MCU Based System

ADVANCE INFORMATION

10 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage and output current of the TPS62840.

11 Layout

11.1 Layout Guidelines

The TPS62840 pinout has been optimized to enable a single layer PCB routing of the device and its critical passive components such as C_{IN}, C_{OUT} and L.

- As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance.
- It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor should be placed as close as possible to the device's VIN and GND pins. This is the most critical component placement.
- The VOS line is a sensitive, high impedance line and should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line) or other noise sources.

11.2 Layout Example

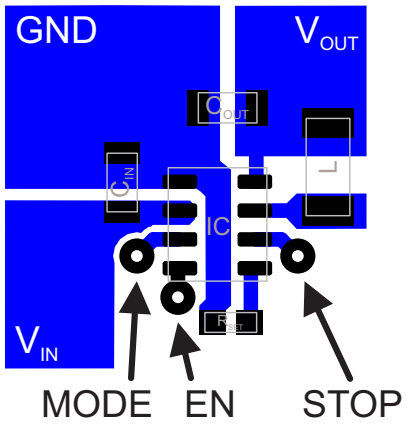


Figure 56. Recommended PCB Layout DLC Package

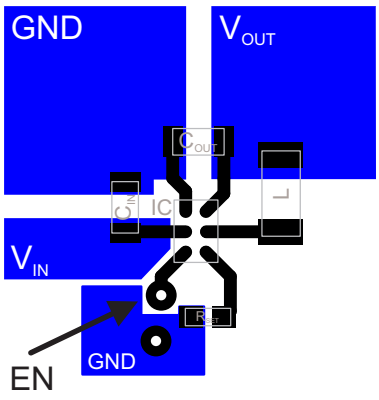


Figure 57. Recommended PCB Layout YBG Package

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

DCS-Control, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62840DLCR	PREVIEW	VSON-HR	DLC	8	3000	TBD	Call TI	Call TI	-40 to 125		
TPS62840YBGR	PREVIEW	DSBGA	YBG	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS62841DLCR	PREVIEW	VSON-HR	DLC	8	3000	TBD	Call TI	Call TI	-40 to 125		
TPS62841YBGR	PREVIEW	DSBGA	YBG	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS62849DLCR	PREVIEW	VSON-HR	DLC	8	3000	TBD	Call TI	Call TI	-40 to 125		
XPS62840DLCR	ACTIVE	VSON-HR	DLC	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XPS62840YBGR	ACTIVE	DSBGA	YBG	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	XPS840	Samples
XPS62841DLCR	ACTIVE	VSON-HR	DLC	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	EB	Samples
XPS62841YBGR	ACTIVE	DSBGA	YBG	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	XPS841	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

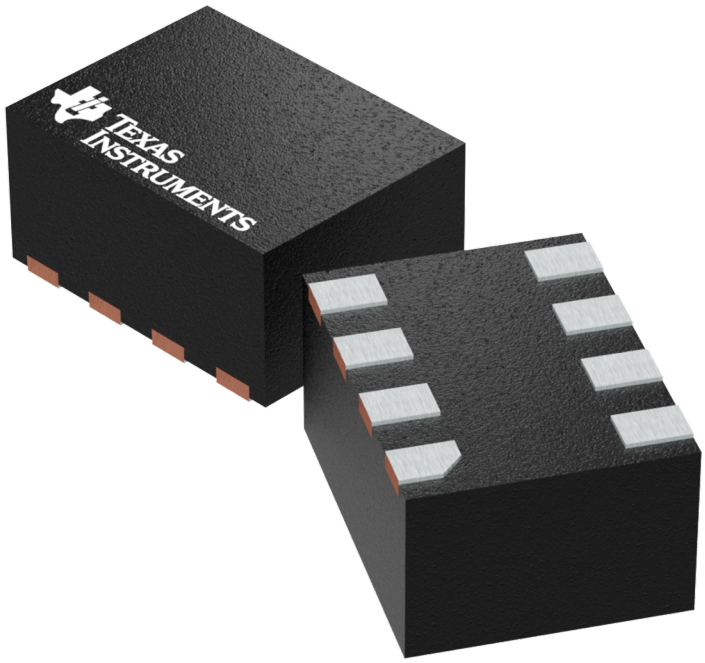
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DLC 8 VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

2.0 x 1.5 mm, 0.5 mm pitch



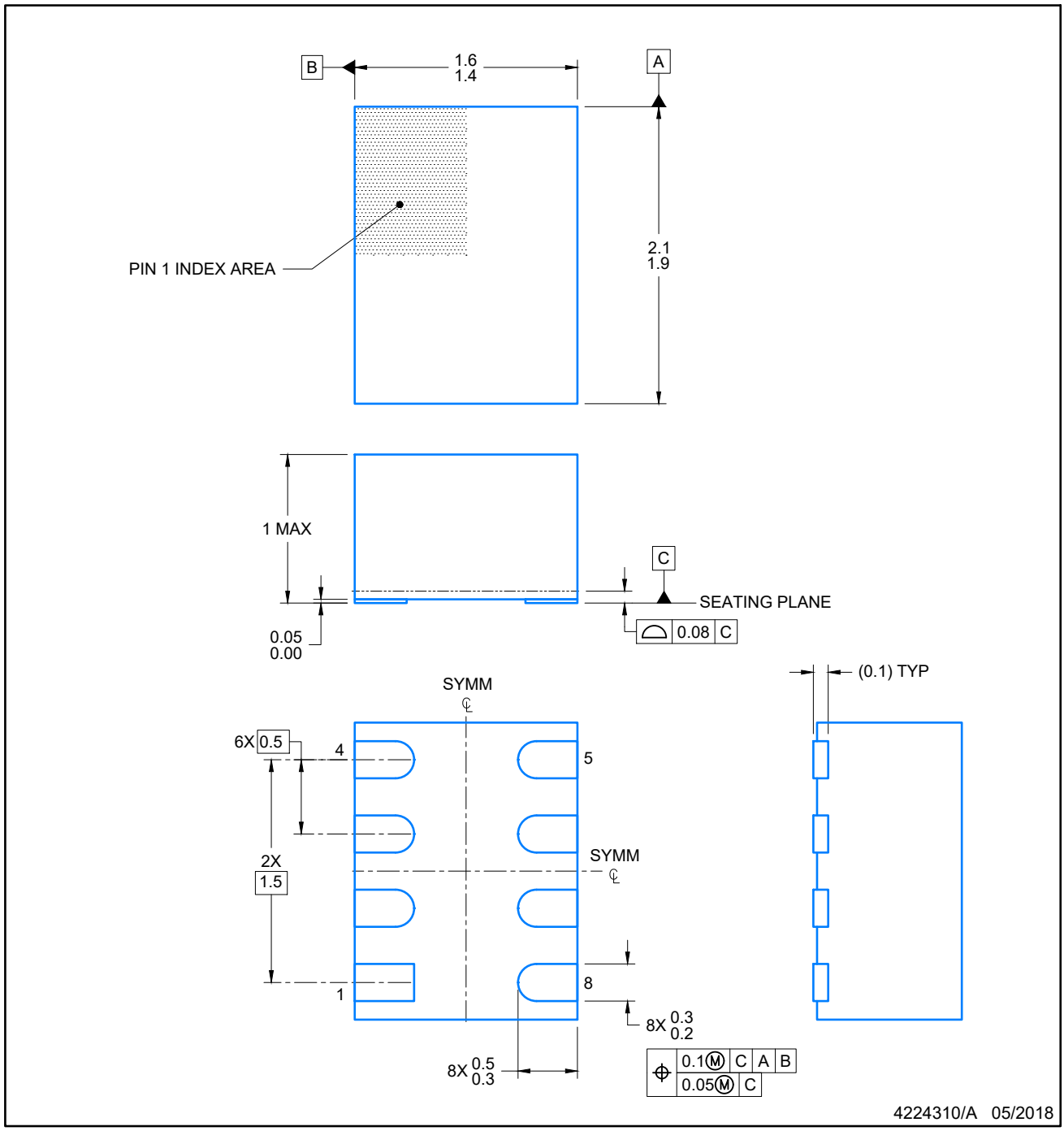
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DLC0008B

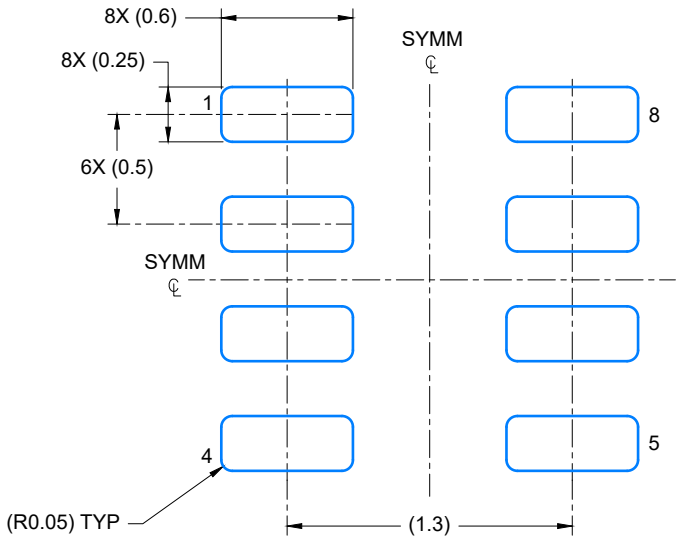
VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE- NO LEAD

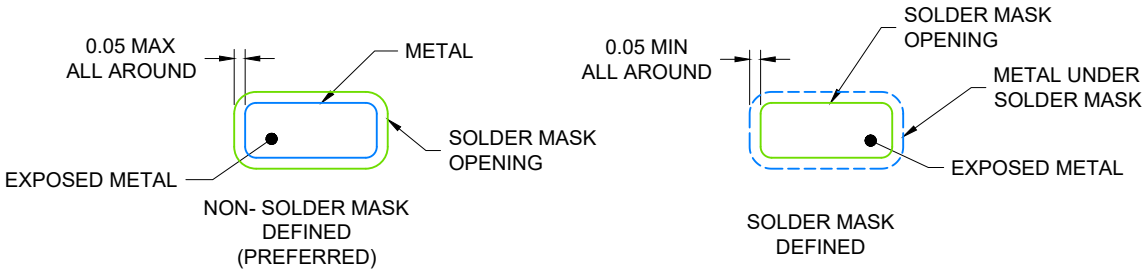


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

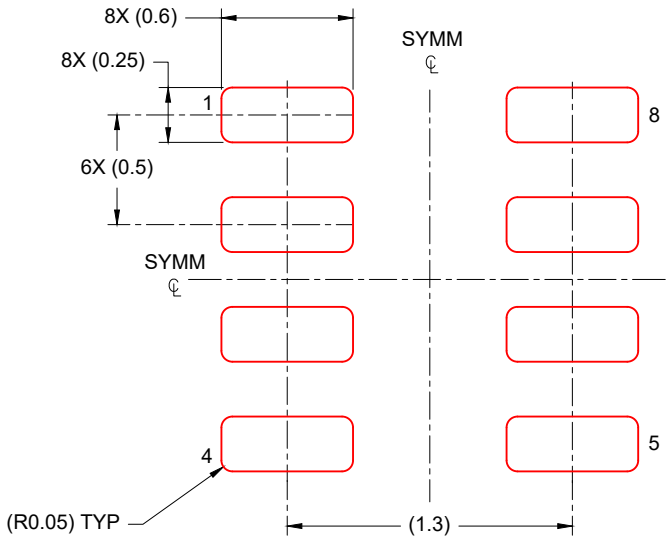


SOLDER MASK DETAILS

4224310/A 05/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224310/A 05/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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