TPS62300EVM-085 User's Guide

This user's guide describes the characteristics, operation, and use of the TPS6230xEVM-085 evaluation module (EVM). This EVM demonstrates four individual configurations of the Texas Instruments TPS6230X 3-MHz, synchronous step-down converter capable of supplying up to 500 mA of output current. This user's guide includes setup instructions, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

Contents

1 Introduction 2
2 Setup 2
3 Board Layout 4
4 Schematic and Bill of Materials 8
5 Related Documentation From Texas Instruments 10

List of Figures

1 **Top Layer Routing 5**
2 **Bottom Layer Routing 6**
3 **Assembly Layer 7**
4 **TPS6230xEVM-085 Schematic 9**

List of Tables

1 **Device and Output Voltage Configurations 2**
2 **Input and Output Connections 3**
4.3 **TPS6230xEVM-085 Bill of Materials 10**

1 Introduction

The Texas Instruments TPS6230xEVM-085 evaluation module helps designers evaluate the operation and performance of the TPS6230x family of devices. These devices are high efficiency, small size, buck converters that switch at 3 MHz.

The EVM contains four independent DC/DC converters. The default output voltages of the converters is listed in Table 1.

Table 1. Device and Output Voltage Configurations

Converter	IC	Package	Output Voltage	Type
1	TPS62300DRC3	QFN-10	1.800	adjustable
2	TPS62300YZD3	CSP-8 chipscale	1.500	adjustable
3	TPS62301YZD	CSP-8 chipscale	1.500	fixed
4	TPS62302YZD3	CSP-8 chipscale	1.500	fixed

If desired, converters 1 and 2 on this EVM can be easily modified to supply higher or lower output voltages. The converter can be adjusted to provide an output voltage between 0.6 V and 5.4 V. Output voltages other than the default values may be evaluated by adjusting the appropriate feedback resistors. Also, other fixed output voltage versions of the devices can be easily evaluated using this EVM. Refer to the data sheet (SLVS528) for the various fixed output voltage options available in the TPS6230x device family as well as for more information on adjusting the output voltage.

2 Setup

This chapter describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the TPS230xEVM-085.

2.1 Input/Output Connector Descriptions

J1 , TP1, TP5, and TP9 – VIN — This is the positive input connection to the corresponding converter. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission.

J2 , TP2, TP6, and TP12 – GND — This is the return connection for the input power supply for the corresponding converter.

J3 – Vadj — This input is used to apply a voltage directly to the FB pin of the controller of converter 1. This allows for external control of the output voltage as outlined in the TPS62300 data sheet (SLVS528).

J4, TP3, TP7, and TP11 – VOUT — This is the positive connection from the output of the corresponding buck power supply.

J5 , TP4, TP8, and TP10 –GND— This is the negative connection from the output of the corresponding buck power supply.

JP1 – EN — This jumper enables or disables converter 1. Connect the shorting jumper from the center (EN) pin to either the ON or OFF pssition. JP1 should never be left floating.

JP2 – Mode — This jumper is used to select the operating mode of converter 1. The converter will operate in a fixed frequency PWM mode when a jumper is used to short the MODE pin to the PWM pin. Shorting the MODE pin and PFM pin together allows the controller to utilize the power saving (PFM) mode at low output currents. An external clock can be applied to the MODE pin for synchronous operation.

2.2 Setup

All four converters are designed to use an input voltage between 2.7 V and 6.0 V. The input voltage must be higher than the output voltage in order to maintain voltage regulation. All four power supplies are designed to provide up to 500 mA of output current at the specified output voltage. Connect the input voltage power supply and output according to Table 2.

Table 2. Input and Output Connections

Converter No.	Output Voltage	Signal	Connection
1	1.80 VDC Adjustable	Positive Input Voltage	J1
		Input Voltage Return	J2
		Positive Output Voltage	J4
		Output Voltage Return	J5
2	1.50 VDC Adjustable	Positive Input Voltage	TP1
		Input Voltage Return	TP2
		Positive Output Voltage	TP3
		Output Voltage Return	TP4
3	1.50 VDC Fixed	Positive Input Voltage	TP5
		Input Voltage Return	TP6
		Positive Output Voltage	TP7
		Output Voltage Return	TP8
4	1.60 VDC Fixed	Positive Input Voltage	TP9
		Input Voltage Return	TP12
		Positive Output Voltage	TP11
		Output Voltage Return	TP10

For converters number 1 and 2, the factory supplied TPS62300 device can be replaced with other fixed voltage converters in the TPS6230x family. R1, R2, R3, and C3 should be removed and left open when using a fixed voltage IC in converter 1. R4 and R5 should be left open in converter 2 when using a fixed voltage IC.

2.3 Operation

JP1 and JP2 must be configured for proper operation of converter number 1. Use a shorting block to set JP1 and JP2 to the desired configurations. For JP2 jump the MODE pin to the PWM pin for fixed frequency PWM mode. Jump the MODE pin to the PFM pin for PWM operation with power saving PFM mode enabled. To synchronize to an external clock source, the jumper can be removed and the external clock supplied directly to the MODE pin of JP2.

For JP1, jump the EN pin to the ON pin to enable and operate the converter. Jumping the EN pin to the OFF pin disables the converter. The EN pin of JP1 must be jumped to one of these positions. Do not leave the EN pin floating.

Converters number 2, 3 and 4 do not require any additional configuration for operation other than input power. These converters are hard wired to always be enabled and use the power saving PFM mode with low output currents.

3 Board Layout

This chapter provides the TPS6230xEVM-085 board layout and illustrations.

Board layout is critical for all high frequency switch mode power supplies. Figure 1, Figure 2, and Figure 3 show the board layout for the TPS6230xEVM-085 PWB. The nodes with high switching frequencies and currents are kept as short as possible to minimize trace inductance. High impedance inputs to the TPS62300, such as the Vout pin, have traces that are shielded by ground traces and planes. Careful attention has been given to the routing of high frequency current loops and a single point grounding scheme is used. Refer to the data sheet for specific layout guidelines.

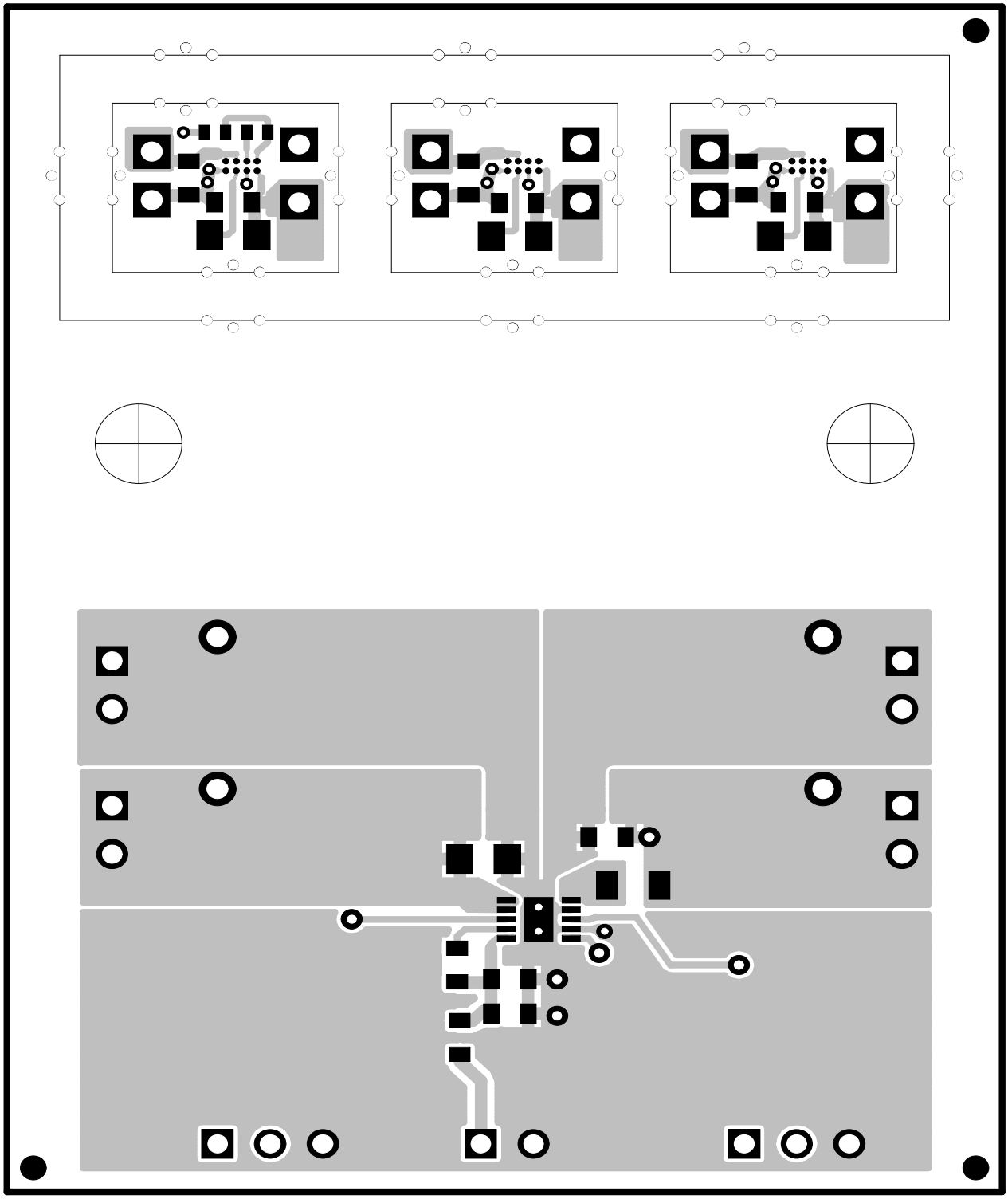


Figure 1. Top Layer Routing

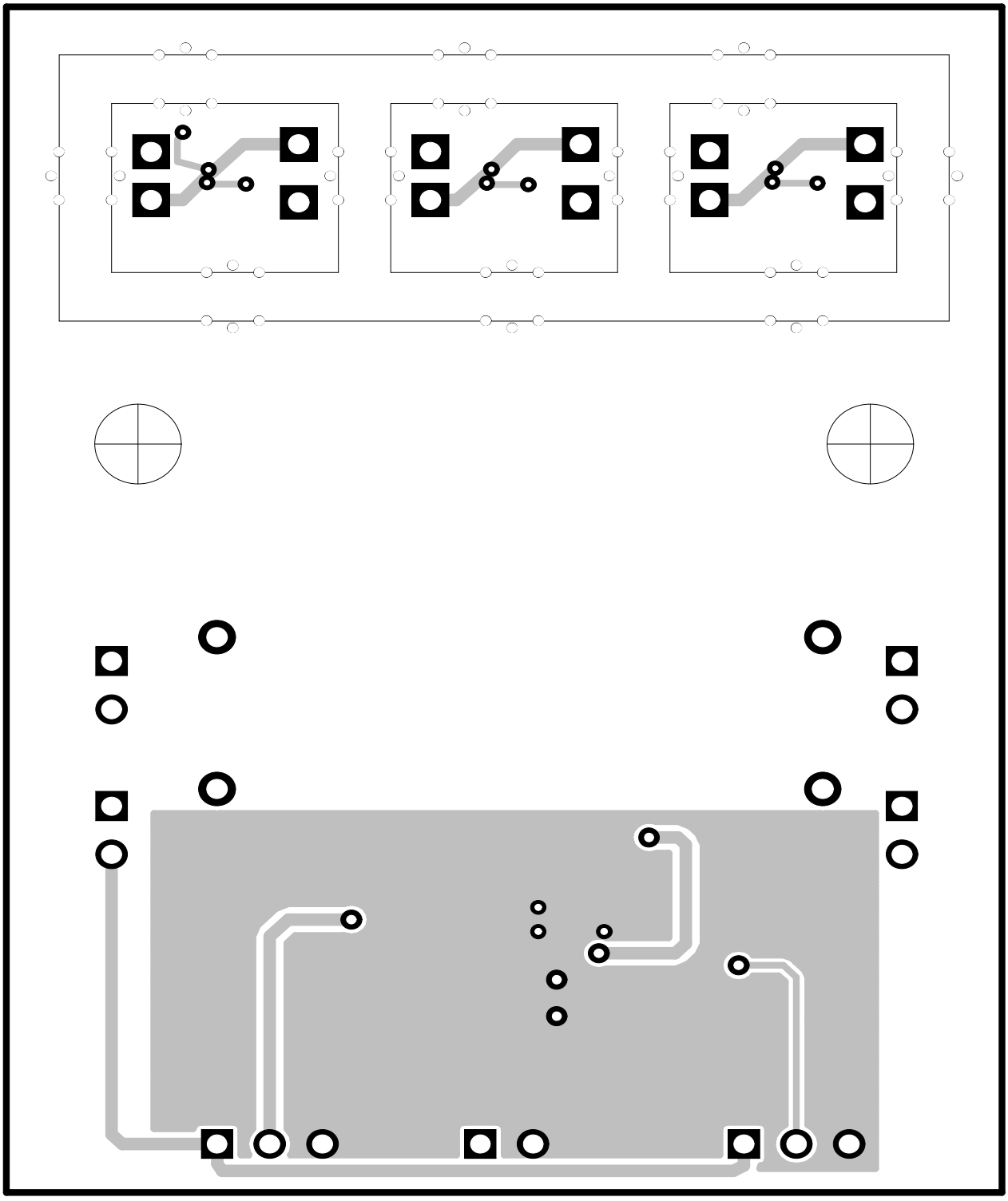


Figure 2. Bottom Layer Routing

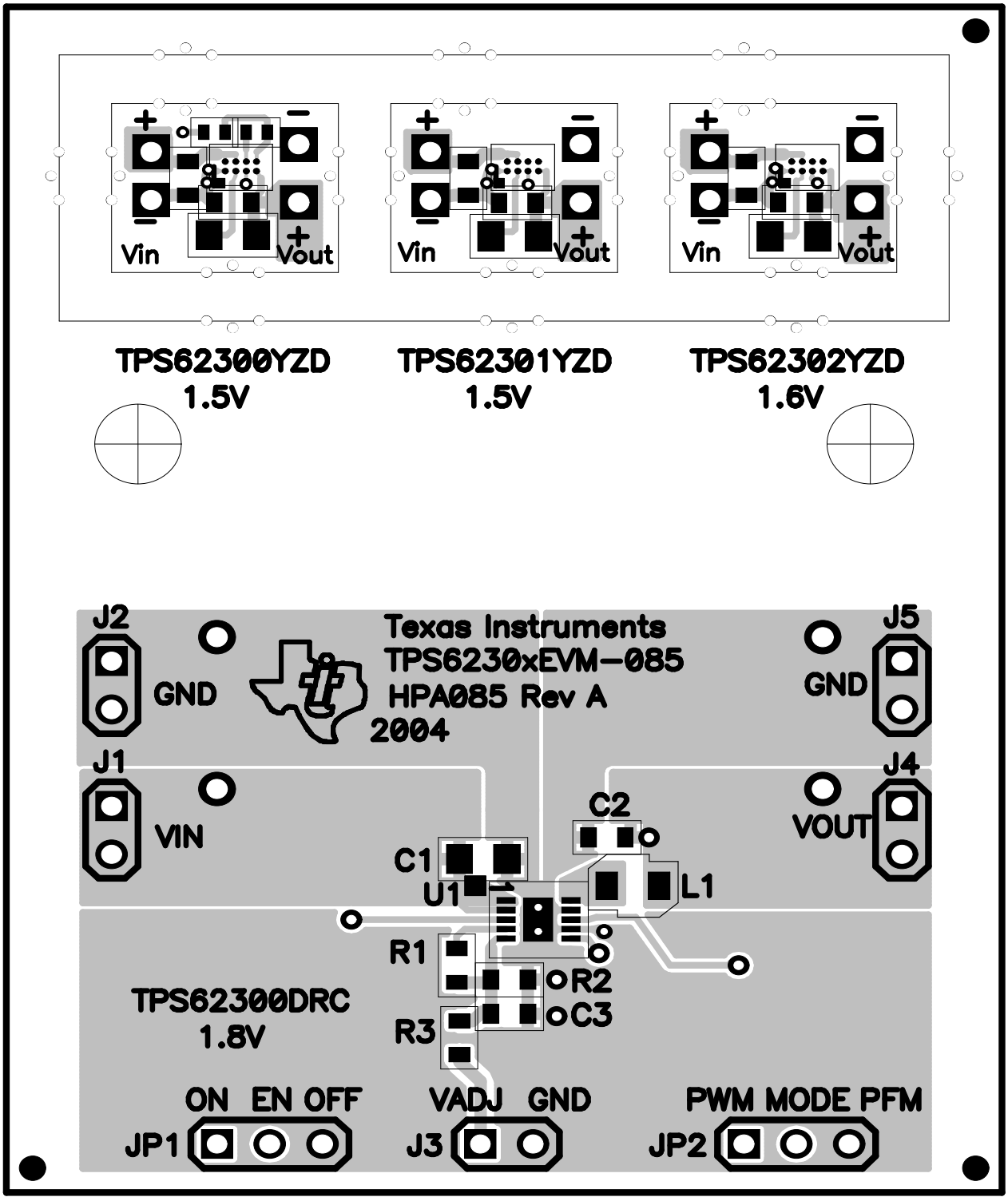


Figure 3. Assembly Layer

4 Schematic and Bill of Materials

This chapter provides the TPS6230xEVM-085 schematic and bill of materials.

4.1 Schematic

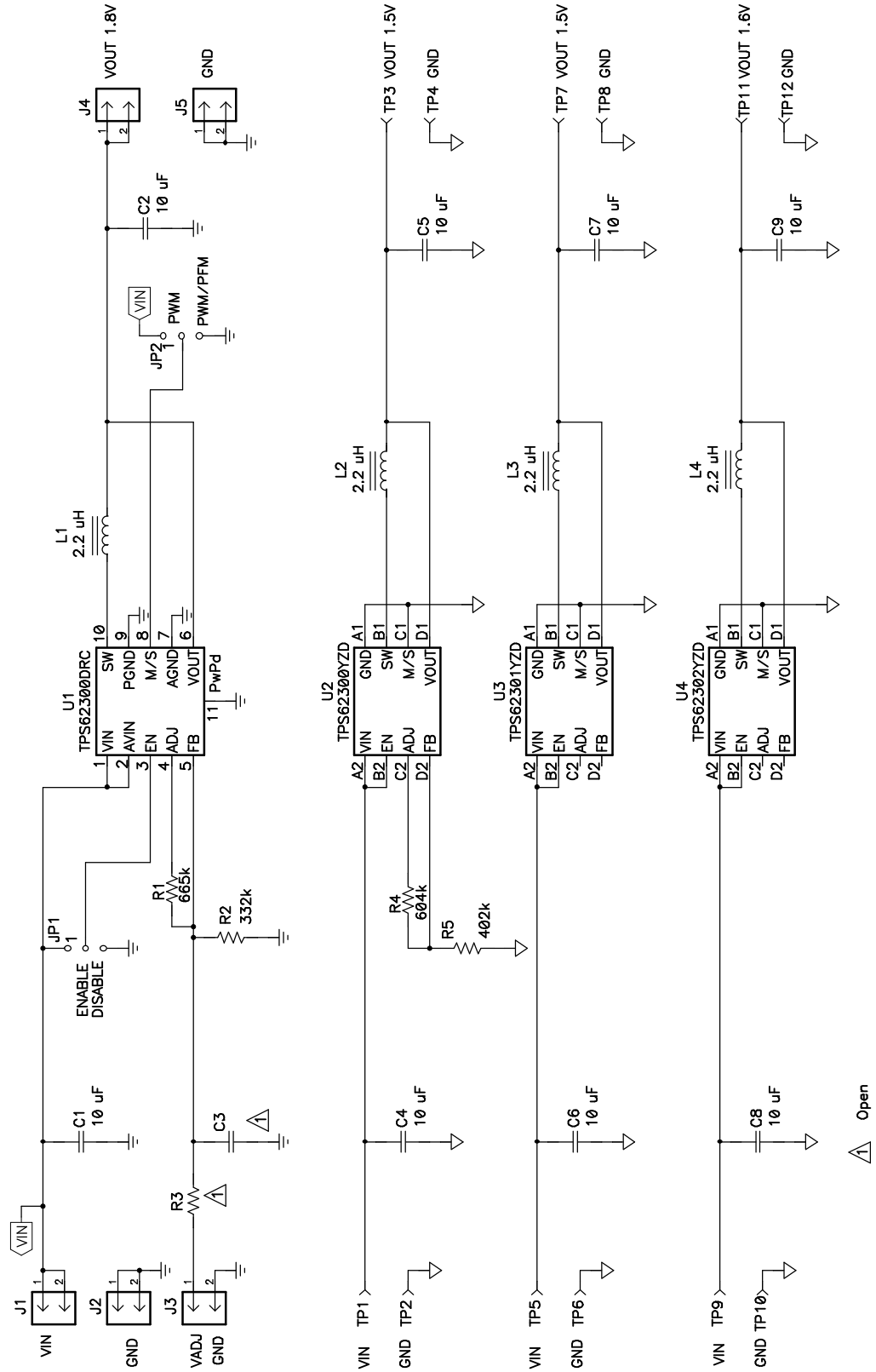


Figure 4. TPS6230xEVM-085 Schematic

4.2 Bill of Materials

Table 4.3. TPS6230xEVM-085 Bill of Materials

COUNT	Ref Des	DESCRIPTION	SIZE	MFR	PART NUMBER
8	C1, C2, C4–C9	Capacitor, ceramic, 10-µF, 4-V, X5R, 10%	603	TDK	C1608X5R0G106MT
1	C3	Capacitor, ceramic, xx-µF, xx-V	603		
5	J1–J5	Header, 2-pin, 100-mil spacing, (36-pin strip)	0.100 In x 2 In	Sullins	PTC36SAAN
2	JP1, JP2	Header, 3-pin, 100-mil spacing, (36-pin strip)	0.100 In x 3 In	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 2.2-µH, 1.0-A, 120-mΩ	0.1.2 In x 0.110 In	TDK	VLF3010AT-2R2M1R0
3	L2–L4	Inductor, SMT, 2.2-µH, 770-mA, 230-mΩ	805	Taiyo Yuden	CB2016T2R2M
1	R1	Resistor, chip, 665-kΩ, 1/16-W, 1%	603	Std	Std
1	R2	Resistor, chip, 332-kΩ, 1/16-W, 1%	603	Std	Std
0	R3	Resistor, chip, xx-Ω, 1/16-W, 1%	603	Std	Std
1	R4	Resistor, chip, 604-kΩ, 1/16-W, 1%	402	Std	Std
1	R5	Resistor, chip, 402-kΩ, 1/16-W, 1%	402	Std	Std
6	TP1, TP3, TP5, TP7, TP9, TP11	Test point, red, 1 mm	0.038	Farnell	240-345
6	TP2, TP4, TP6, TP8, TP10, TP12	Test point, black, 1 mm	0.038	Farnell	240-333
1	U1	IC, 3-MHz synchronous step-down converter, 400 mA, Vout adjustable	QFN10	TI	TPS62300DRC
1	U2	IC, 3-MHz synchronous step-down converter, 400 mA	CSP-8	TI	TPS62300YZD
1	U3	IC, 3-MHz synchronous step-down converter, 400 mA	CSP-8	TI	TPS62301YZD
1	U4	IC, 3-MHz synchronous step-down converter, 400 mA	CSP-8	TI	TPS62302YZD
1	--	PCB, 2.455 In x 1.89 In x 0.032 In		Any	HPA085
2	--	Shunt, 100-mil, black	0.100 In	3M	929950-00

5 Related Documentation From Texas Instruments

TPS62300 data sheet (SLVS528 A)

FCC Warnings

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.7 V to 6.0 V and the output voltage range of 0.6 V to 5.4 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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