TPS6217x 28-V, 0.5-A Step-Down Converter With Sleep Mode

1 Features

- DCS-Control™ Topology
- Input Voltage Range 4.75 V to 28 V
- Quiescent Current Typically 4.8 µA (Sleep Mode)
- 100% Duty Cycle Mode
- Active Output Discharge
- Power Good Output
- Output Current of 500 mA
- Output Voltage Range 1 VDC to 6 V
- Switching Frequency of Typically 1 MHz
- Seamless Power Save Mode Transition
- Undervoltage Lockout
- Short Circuit Protection
- Over Temperature Protection
- Available in 2-mm × 3-mm 10-pin WSON Package

2 Applications

- General 12 V / 24 V Point Of Load Supply
- Ultra Mobile PC, Embedded PC
- Low Power Supply for Microprocessor
- High Efficiency LDO Alternative
- Industrial Sensors

3 Description

The TPS6217x is a high efficiency synchronous step-down DC/DC converter, based on the DCS-Control™ topology.

With a wide operating input voltage range of 4.75 V to 28 V, the device is ideally suited for systems powered from multi cell Li-Ion as well as 12 V and even higher intermediate supply rails, providing up to 500-mA output current.

The TPS6217x automatically enters power save mode at light loads, to maintain high efficiency across the whole load range. As well, it features a sleep mode to supply applications with advanced power save modes like ultra low power micro controllers. The power good output may be used for power sequencing and/or power on reset.

The device features a typical quiescent current of 22 µA in normal mode and 4.8 µA in sleep mode. In sleep mode, the efficiency at very low load currents can be increased by as much as 20%. In shutdown mode, the shutdown current is less than 2 µA and the output is actively discharged.

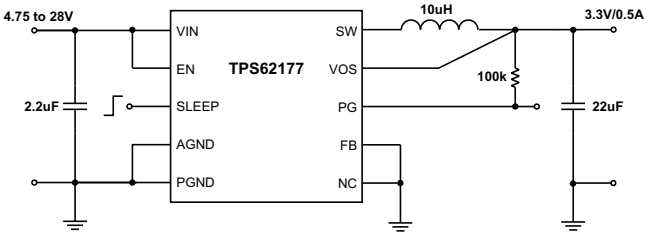
The TPS6217x, available in an adjustable and a fixed output voltage version, is packaged in a small 2-mm × 3-mm 10-pin WSON package.

Device Information(1)

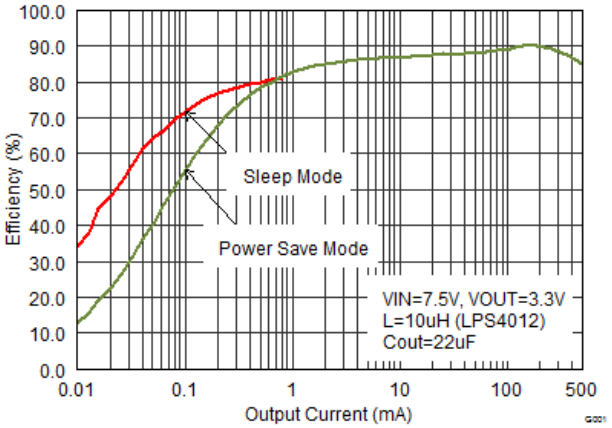
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6217x	WSON (10)	2.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2014) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (November 2012) to Revision B — **Page**

- Added to SLEEP description in TERMINAL FUNCTIONS table ... 3
- Changed *Sleep Mode Operation* section ... 11
- Changed Micro Controller Power Supply section information and Figure 54 ... 24
- Changed Figure 55 ... 24

Changes from Original (October 2012) to Revision A — **Page**

- Added Start-up Mode to High-Side MOSFET Current Limit in ELECTRICAL CHARACTERISTICS ... 5
- Changed Table 2 ... 14

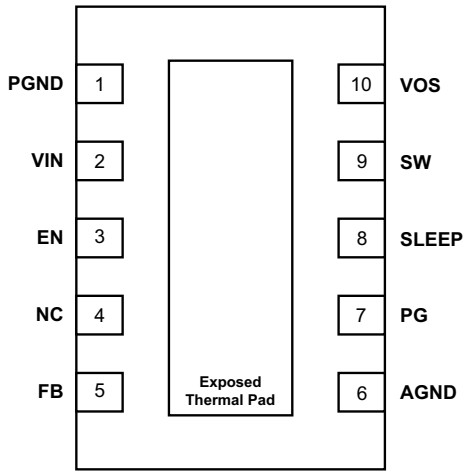
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5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	PACKAGE DESIGNATOR CODE	PACKAGE MARKING
TPS62175	Adjustable	DQC	62175
TPS62177	Fixed, 3.3 V	DQC	62177

6 Pin Configuration and Functions

DQC Package
10-Pin WSON
Top View



Pin Functions

PIN (1)		I/O	DESCRIPTION
NAME	NO.		
PGND	1	—	Power ground connection
VIN	2	I	Supply voltage for the converter
EN	3	I	Enable input (High = enabled, Low = disabled)
NC	4	—	This pin is recommended to be connected to AGND but can left be floating
FB	5	I	Voltage feedback of adjustable version. Connect resistive divider to this pin. TI recommends connecting FB to AGND for fixed voltage versions for improved thermal performance.
AGND	6	—	Analog ground connection
PG	7	O	Output power good (open drain, requires pullup resistor)
SLEEP	8	I	Sleep mode input (High = normal operation, Low = sleep mode operation). Can be operated dynamically during operation. If sleep mode is not used, connect to VOUT.
SW	9	O	Switch node, connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
VOS	10	I	Output voltage sense pin and connection for the control loop circuitry.
Exposed Thermal Pad	—	—	Must be connected to AGND and PGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application and Implementation* sections.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	–0.3	30	V
	EN, SW	–0.3	V_{IN} + 0.3	
	FB, PG, VOS, SLEEP, NC	–0.3	7	
Power good sink current	PG		10	mA
Temperature	Operating junction temperature, T_J	–40	125	°C
	Storage temperature, T_{stg}	–65	150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{IN}	4.75		28	V
Operating free air temperature, T_A	–40		85	°C
Operating junction temperature, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6217x DQC [WSON] 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Over free-air temperature range (T_A = –40°C to 85°C) and V_{IN} = 4.75 V to 28 V. Typical values at V_{IN} = 12 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		4.75		28	V
I_Q	Operating quiescent current	EN = High, SLEEP = High, I_{OUT} = 0 mA, device not switching		22	36	µA
I_{Q_SLEEP}	Sleep mode quiescent current	EN = High, SLEEP = Low, I_{OUT} = 0 mA, device not switching		4.8	10	µA
I_{SD}	Shutdown current	EN = Low, current into VIN pin		1.5	5	µA
V_{UVLO}	Undervoltage lockout threshold	Rising input voltage	4.5	4.6	4.7	V
		Falling input voltage		2.9		V
T_{SD}	Thermal shutdown temperature	Rising junction temperature		150		°C
	Thermal shutdown hysteresis			20		
CONTROL (EN, PG, SLEEP)						
V_H	High level input threshold voltage (EN, SLEEP)		0.9			V
V_L	Low level input threshold voltage (EN, SLEEP)				0.3	V
I_{LKG_EN}	Input leakage current (EN)	EN = V_{IN}		5	300	nA
I_{LKG_SLEEP}	Input leakage current (SLEEP)	V_{SLEEP} = 3.3 V		1.4		µA
V_{TH_PG}	Power good threshold voltage	Rising (%V_{OUT})	93%	96%	99%	
		Falling (%V_{OUT})	87%	90%	93%	
V_{OL_PG}	Power good output low voltage	I_{PG} = –2 mA			0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG} = 5 V		5	300	nA
POWER SWITCH						
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN} ≥ 6 V		850	1430	mΩ
	Low-side MOSFET ON-resistance	V_{IN} ≥ 6 V		320	530	mΩ
I_{LIMF}	High-side MOSFET current limit	Normal operation	800	1000	1200	mA
		Start-up mode	450	525	600	
OUTPUT						
V_{OUT}	Output voltage range (TPS62175)	V_{IN} ≥ V_{OUT}	1		6	V
V_{REF}	Internal reference voltage			0.8		V
I_{OUT_SLEEP}	Output current in sleep mode	SLEEP = Low, V_{OUT} = 3.3 V, L = 10 µH	15			mA
I_{LKG_FB}	Input leakage current (FB)	V_{FB} = 0.8 V		1	100	nA

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Electrical Characteristics (continued)

Over free-air temperature range (T_A = –40°C to 85°C) and V_{IN} = 4.75 V to 28 V. Typical values at V_{IN} = 12 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage accuracy(1)	TPS62175 (adjustable V_{OUT}), $V_{IN} \geq V_{OUT}$ +1 V	PWM mode		–1.8%		1.8%	
			Power save mode, L = 10 µH	$V_{OUT} \geq 2.5$ V, C_{OUT} = 22 µF	–1.8%		3%	
				$V_{OUT} < 2.5$ V, C_{OUT} = 44 µF	–1.8%		3.7%	
			Sleep mode, $I_{OUT} \leq$ 15 mA	C_{OUT} = 22 µF, L = 10 µH	–1.6%		2.9%	
		TPS62177 (3.3 V fixed V_{OUT})	PWM mode		–2%		2%	
			Power save mode,	C_{OUT} = 22 µF, L = 10 µH	–2%		2.9%	
			Sleep mode, $I_{OUT} \leq$ 15 mA		–1.6%		2.7%	
	Output discharge resistance	EN = Low				175		Ω
	Load regulation	V_{OUT} = 3.3 V, PWM mode operation				0.02		%/A
	Line regulation	V_{OUT} = 3.3 V, I_{OUT}= 500 mA, PWM mode operation				0.015		%/V

(1) The output voltage accuracy in Power Save and Sleep Mode can be improved by increasing the output capacitor value, reducing the output voltage ripple (see *Application and Implementation* section).

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7.6 Typical Characteristics

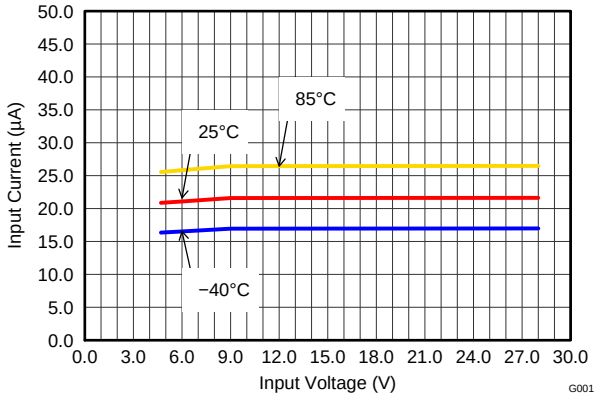


Figure 1. Quiescent Current

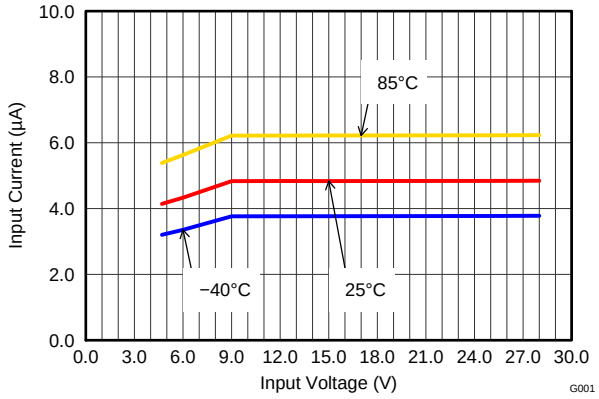


Figure 2. Quiescent Current (Sleep Mode)

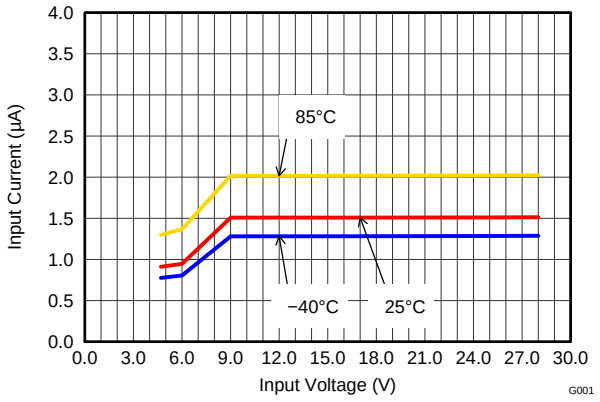


Figure 3. Shutdown Current

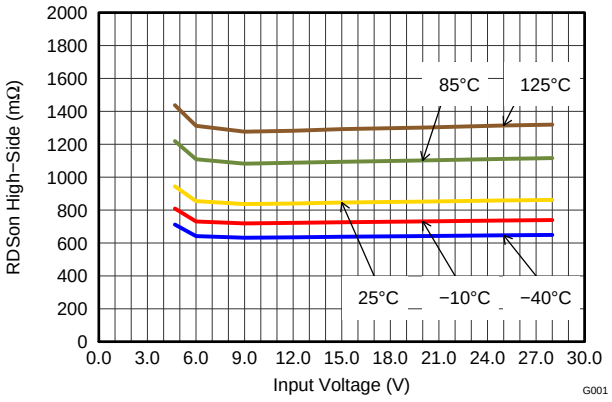


Figure 4. High-Side Switch

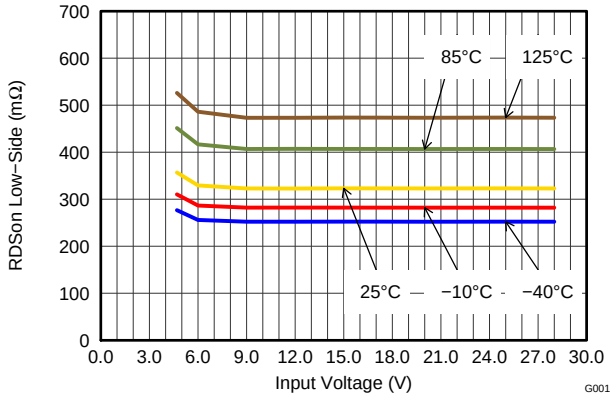


Figure 5. Low-Side Switch

8 Detailed Description

8.1 Overview

The TPS6217x synchronous switch mode power converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless Transition into Power Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode, and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors. The DCS-Control topology supports pulse width modulation (PWM) mode for medium and heavy load conditions and a power save mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 1 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters power save mode to sustain high efficiency down to very light loads. In power save mode the switching frequency decreases linearly with the load current. Because DCS-Control™ supports both operation modes within one single building block, the transition from PWM to power save mode is seamless without effects on the output voltage. Fixed output voltage versions provide smallest solution size and lowest current consumption, requiring only 3 external components. An internal current limit supports nominal output currents of up to 500 mA. The TPS6217x offer both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagrams

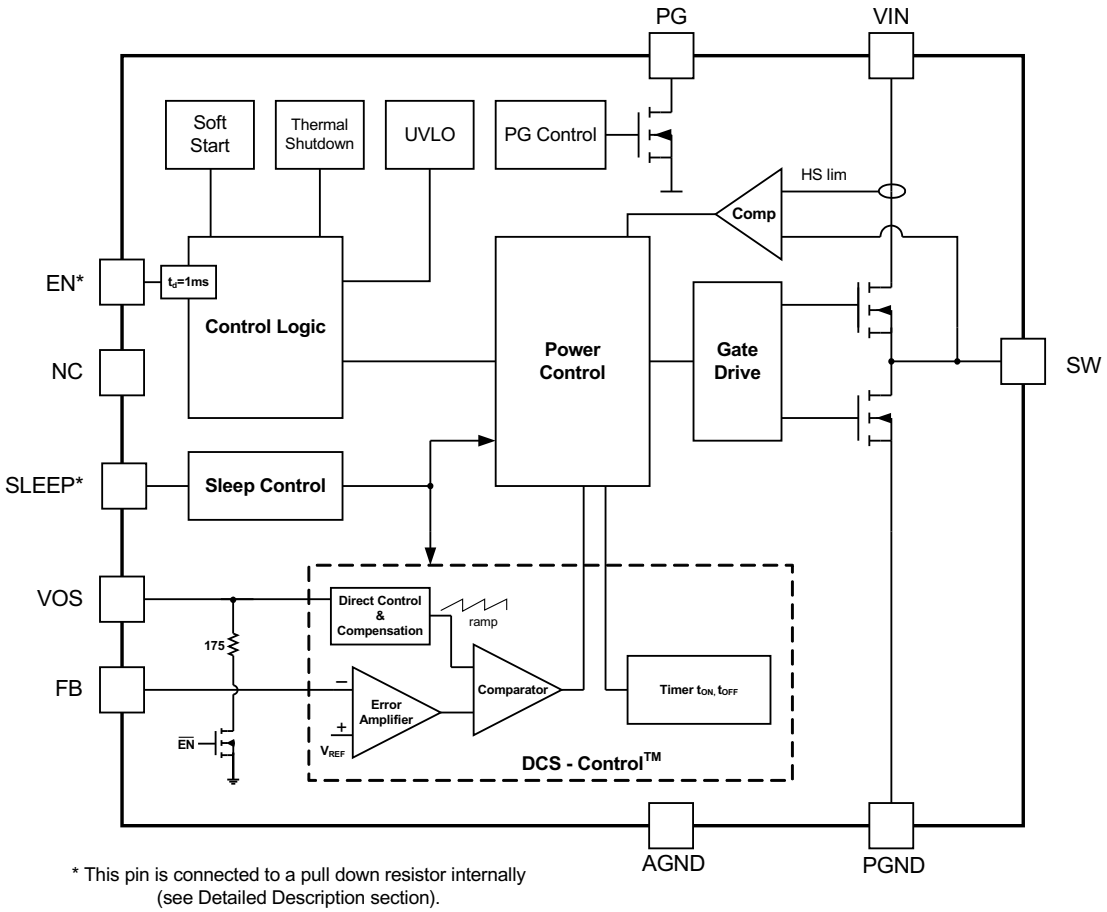


Figure 6. TPS62175 (Adjustable Output Voltage)

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Functional Block Diagrams (continued)

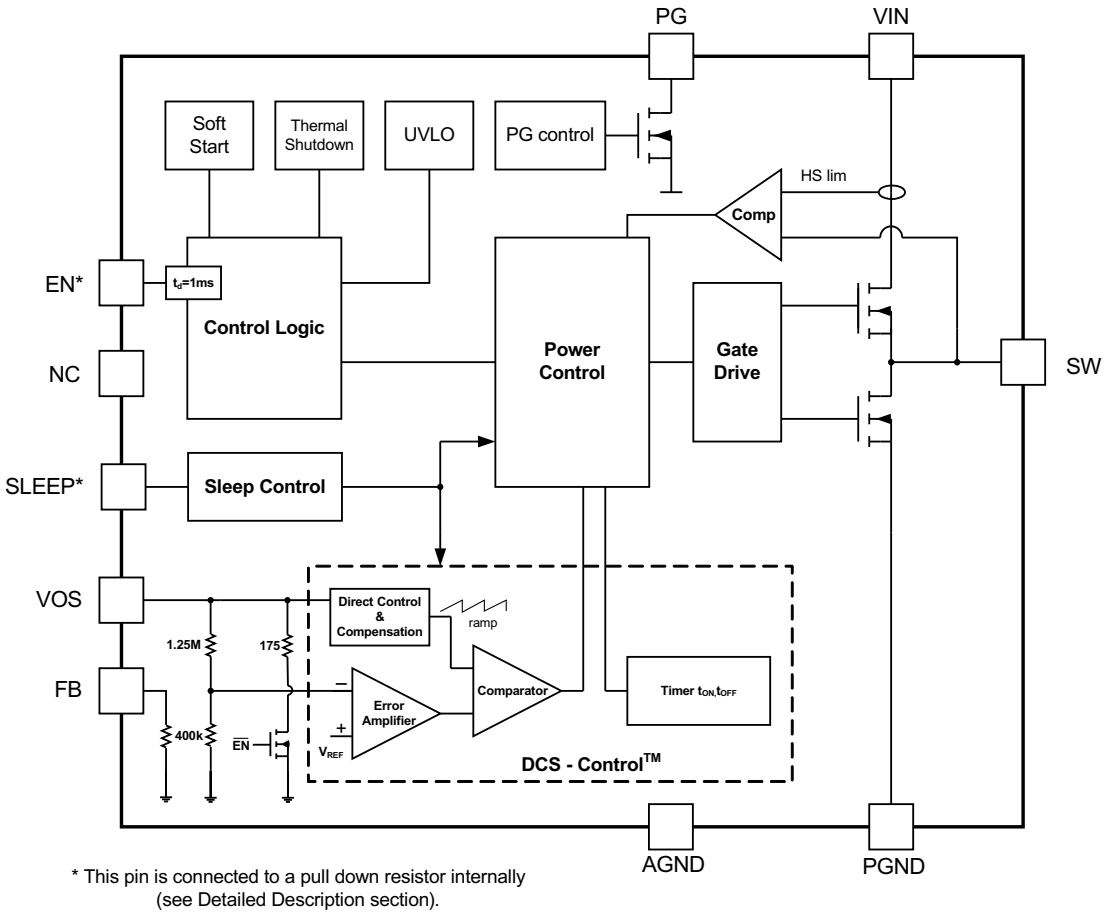


Figure 7. TPS62177 (Fixed Output Voltage)

8.3 Feature Description

8.3.1 Enable/Shutdown (EN)

The device can be switched ON/OFF by pulling the EN pin to High (operation) or Low (shutdown). If EN is pulled to High, the device starts operation after a delay of about 1 ms (typical). This helps to ensure a monotonic start-up sequence, which makes the device ideally suited to control the power on sequence of micro controllers.

During shutdown, the internal MOSFETs as well as the entire control circuitry are turned off and the current consumption is typically 1.5 µA. The EN pin is connected through a 400-kΩ pulldown resistor, keeping the logic level low, if the pin is floating. The resistor is disconnected when EN is set High.

8.3.2 Output Discharge

The output is actively discharged through a 175-Ω (typical) resistor on the VOS pin when the device is turned off by EN, UVLO or thermal shutdown.

8.3.3 Current Limit and Short Circuit Protection

The TPS6217x devices are protected against heavy load and short circuit events. If a current limit situation is detected, the device switches off. The off-time is maintained longer as the output voltage becomes lower. At heavy overloads the low-side MOSFET stays on until the inductor current returns to zero. Then the high-side MOSFET turns on again (see Figure 50 and Figure 51).

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Feature Description (continued)

8.3.4 Power Good (PG)

The TPS6217x has a built-in power good (PG) function to indicate that the output reached regulation. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor (to any voltage less than 7 V). It can sink 2 mA of current and maintain its specified logic low level of 0.3 V. It is held low when the device is turned off by EN, UVLO or thermal shutdown.

If the PG pin is not used, it may be left floating or connected to AGND.

8.3.5 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout function prevents misoperation by turning the device off. The undervoltage lockout threshold is set to 4.6 V (typically) for rising V_{IN}. To cover for possible input voltage drops, when using high impedance sources or batteries, the falling threshold is set to typically 2.9 V, allowing monotonic start-up sequence under such conditions. For input voltages below the minimum V_{IN} of 4.75 V and above the falling UVLO threshold of 2.9 V, the device still functions with a current limit and regulation capability but the electrical characteristics are no longer specified.

8.3.6 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typical), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes Low. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shutdown temperature.

8.4 Device Functional Modes

8.4.1 Soft Start

The internal soft start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to High and the device starts switching, V_{OUT} rises with a slope of typically 10 mV/µs. The internal current limit is reduced to typically 525 mA during start-up. Thereby the output current is less than 500 mA during that time (see Figure 41). The start-up sequence ends when the device achieves regulation; then, the device runs with the full current limit of typically 1 A, providing full output current.

The TPS6217x can monotonically start into a prebiased output.

8.4.2 Pulse Width Modulation (PWM) Operation

The TPS6217x operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of about 1 MHz. The switching frequency in PWM is set by an internal timer circuit. The frequency variation is controlled and depends on V_{IN} and V_{OUT}. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous conduction mode (DCM).

8.4.3 Power Save Mode Operation

The TPS6217x built in power save mode is entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation by keeping the on-time fixed and reducing the switching frequency by incorporating pause time. The device remains in power save mode as long as the inductor current is discontinuous. The on-time, in steady-state PWM operation, can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 1\mu s \quad (1)$$

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Device Functional Modes (continued)

In case Equation 1 yields a lower value, the device maintain an on-time of about 80 ns to limit switching losses. This minimum on-time is used in power save mode. While the peak inductor current in Power Save Mode can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \quad (2)$$

The switching frequency is calculated as follows:

$$f_{PSM} = \frac{2 \cdot I_{OUT}}{t_{ON}^2 \frac{V_{IN}}{V_{OUT}} \left[\frac{V_{IN} - V_{OUT}}{L} \right]} \quad (3)$$

8.4.4 Sleep Mode Operation

In sleep mode operation, the typical quiescent current is reduced from 22 µA to 4.8 µA to significantly increase the efficiency at load currents of typically less than 1 mA (see Figure 1 and Figure 2). It is designed to be enabled and disabled during operation by pulling the SLEEP pin High or Low by the host (processor). Ultralow power micro controllers in deep sleep or hibernating mode may set their output pins floating. Therefore, the TPS6217x have a pulldown resistor internally connected to the SLEEP pin, to keep a logic low level, when the sleep input signal goes high impedance. But, if the sleep signal goes directly from logic High to High Impedance, the low level detection must be ensured considering the leakage of the micro controller's sleep signal. An external pulldown resistor, on the SLEEP pin, may be required. Connect the SLEEP pin to VOUT, not VIN, to disable sleep mode, because the pin's voltage rating is limited to 7 V maximum.

The output voltage is regulated with a fixed switching scheme, using a fixed on-time of about twice the minimum on-time of Equation 1 (compare Figure 48 and Figure 49) and the minimum off-time. A new pulse is initiated once the output voltage falls below its regulation threshold. Sleep mode is limited with its dynamic response and current capabilities. However, the device can deliver temporarily more than 15 mA while still in sleep mode, to allow micro controllers to wake up and drive the sleep signal High, exiting sleep mode.

Continuously operating with a too high current in sleep mode causes the output voltage to drop until the PG pin goes Low. As a safety feature, the device then returns to normal operation automatically, avoiding a complete collapse of V_{OUT}. Once the load current decreases again, the device re-enters sleep mode operation. Certainly, this is not a recommended operation mode and sleep mode should be entered or exited by using the SLEEP pin logic.

Sleep mode is not entered until soft-start is complete.

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Device Functional Modes (continued)

8.4.5 100% Mode Operation

The duty cycle of the buck converter is given by D = V_{OUT}/V_{IN} and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input to output voltage differences, for example, for longest operation time of battery-powered applications.

The minimum input voltage to maintain output voltage regulation can be calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \quad (4)$$

where

- I_{OUT} is the output current
- $R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET
- R_L is the DC resistance of the inductor used

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6217x is a high-efficiency synchronous step-down DC-DC converter, based on the DCS-Control topology.

With a wide operating input voltage range of 4.75 V to 28 V, the device is ideally suited for systems powered from multi cell Li-Ion as well as 12 V and even higher intermediate supply rails, providing up to 500-mA output current.

9.2 Typical Application

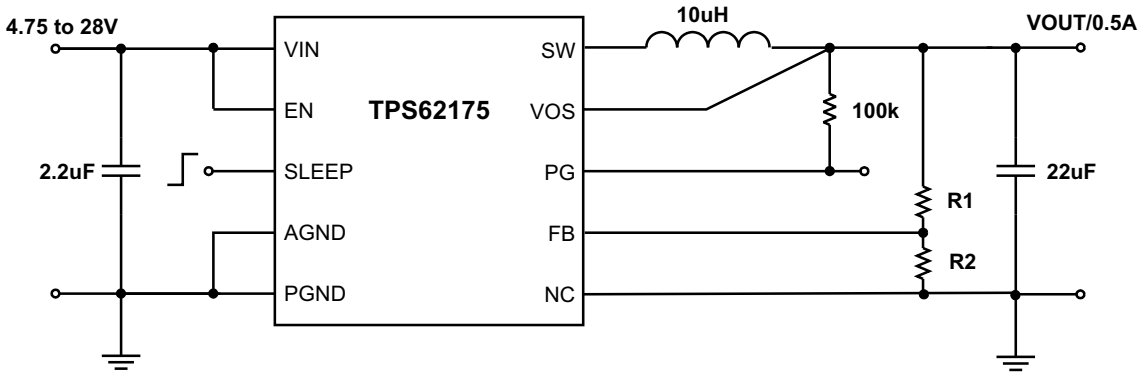


Figure 8. Adjustable 0.5-A Power Supply

9.2.1 Design Requirements

The device operates for an input voltage range of 4.75 V to 28 V. The output voltage is adjustable, using an external resistive divider, or internally fixed.

The graphs were generated using the setup according to Figure 8. Table 1 shows the list of components used for the setup.

9.2.2 Detailed Design Procedures

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	28 V, 0.5-A Step-Down Converter, WSON	TPS62175DQC, Texas Instruments
L1	10 uH, (4 × 4 × 1.2) mm	LPS4012, Coilcraft
Cin	2.2 µF, 50 V, Ceramic, 0805, X5R	Standard
Cout	22 µF, 6.3 V, Ceramic, 0805, X5R	Standard
R1	depending on V_{OUT}	
R2	depending on V_{OUT}	
R3	100 kΩ, Chip, 0603, 1/16 W, 1%	Standard

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9.2.2.1 Programming the Output Voltage

While the output voltage of the TPS62175 is adjustable, the TPS62177 is programmed to a fixed output voltage of 3.3 V. For the fixed output voltage version, the FB pin is pulled low internally by a 400-kΩ resistor. TI recommends connecting the FB pin to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 1 V to 6 V by using a resistive divider. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 5. TI recommends choosing resistor values that allow a current of at least 5 uA. Lower resistor values are recommended to increase noise immunity. For applications requiring lowest current consumption, the use of the fixed-output voltage version is recommended.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (5)$$

As a safety feature, the device clamps the output voltage at the VOS pin to typically 7.4 V, if the FB pin gets opened.

9.2.2.2 External Component Selection

The external components must fulfill the needs of the application, but also the stability criteria of the device's control loop. The TPS6217x is optimized to work within a wide range of external components. The LC output filter's inductance and capacitance must be considered together, creating a double pole that is responsible for the corner frequency of the converter. Table 2 shows the recommended output filter components.

Table 2. Recommended LC Output Filter Combinations(1)

	10 µF	22 µF	47 µF	100 µF	200 µF	400 µF
6.8 µH						
10 µH		√(2)	√	√	√	
22 µH				√	√	
33 µH						

(1) The values in the table are nominal values. Variations of typically ±20% due to tolerance, saturation and DC bias are assumed.
(2) This LC combination is the standard value and recommended for most applications. For output voltages of ≤2 V, TI recommends an output capacitance of at least 2 × 22 uF.

9.2.2.2.1 Output Filter and Loop Stability

The TPS6217x devices are internally compensated and are stable with LC output filter combinations recommended in *Table 2*. Further information on other values and loop stability can be found in *Optimizing the TPS62175 Output Filter* (SLVA543).

9.2.2.2.2 Inductor Selection

The inductor selection is determined by several effects like inductor ripple current, output ripple voltage, PWM-to-Power Save Mode transition point and efficiency. In addition, the inductor selected must be rated for appropriate saturation current and DC resistance (DCR). Equation 6 and Equation 7 calculate the maximum inductor current under static load conditions.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \quad (6)$$

$$\Delta I_{L(\max)} = \frac{V_{OUT}}{\eta} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(\max)} \cdot \eta} \right) \cdot \frac{1}{L_{(\min)} \cdot f_{SW}}$$

where

- ΔI_L is the peak to peak inductor ripple current

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- η is the converter efficiency (see efficiency figures)
- L(min) is the minimum inductor value
- f_{SW} is the actual PWM switching frequency (7)

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. TI recommends a margin of about 20% to cover possible load transient overshoot. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and solution size as well. The inductors listed in Table 3 have been tested with the TPS6217x.

Table 3. List of Inductors

TYPE	INDUCTANCE (µH])	CURRENT (A)(1)	DCR (mΩ)	DIMENSIONS (LENGTH x WIDTH x HEIGHT) mm	MANUFACTURER
LPS4012-103MLC	10 µH, ±20%	1.1	350 (maximum)	4 x 4 × 1.2	Coilcraft
LPS4018-103MLC	10 µH, ±20%	1.3	200 (maximum)	4 x 4 × 1.8	Coilcraft
VLS4012ET-100M	10 µH, ±20%	0.99	190 (typical)	4 x 4 × 1.2	TDK
VLCF4020T-100MR85	10 µH, ±20%	0.85	168 (typical)	4 × 4 × 2	TDK
74437324100	10 µH, ±20%	1.5	215 (typical)	4.5 × 4.1 × 1.8	Wuerth
744025100	10 µH, ±20%	1	190 (maximum)	2.8 × 2.8 × 2.8	Wuerth
IFSC-1515AH-01	10 µH, ±20%	1.3	135 (typical)	3.8 × 3.8 × 1.8	Vishay
ELL-4LG100MA	10 µH, ±20%	0.8	200 (typical)	3.8 × 3.8 × 1.8	Panasonic

(1) I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

9.2.2.2.3 Output Capacitor Selection

The recommended value for the output capacitor is 22 uF. To maintain low output voltage ripple during large load transients, for output voltages less than 2 V, TI recommends 2 × 22 µF output capacitors. The architecture of the TPS6217x allows the use of ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended with an X7R or X5R dielectric. Larger capacitance values have the advantage of smaller output voltage ripple and a tighter DC output accuracy in power save mode.

NOTE

In power save mode, the output voltage ripple and accuracy depends on the output capacitance and the inductor value. The larger the capacitance the lower the output voltage ripple and the better the output voltage accuracy. The same relation applies to the inductor value.

9.2.2.2.4 Input Capacitor Selection

Typically, 2.2 µF is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage during transient events and also decouples the converter from the supply. TI recommends a low ESR, multilayer, X5R or X7R dielectric, ceramic capacitor for best filtering, which should be placed between VIN and PGND as close as possible to those pins.

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value must be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

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9.2.3 Application Curves

V_{IN}=12 V, V_{OUT} = 3.3 V, T_J=25°C, unless otherwise noted

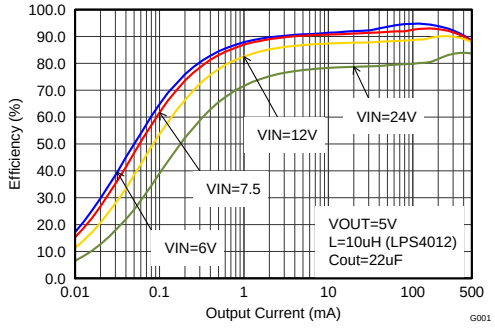


Figure 9. Efficiency vs Load Current

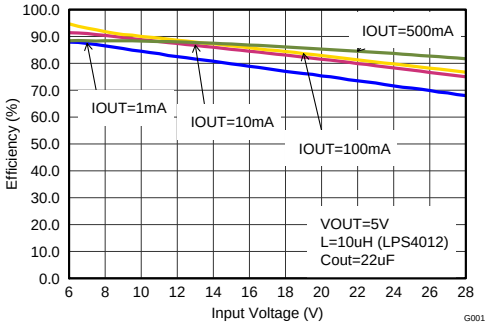


Figure 10. Efficiency vs Input Voltage

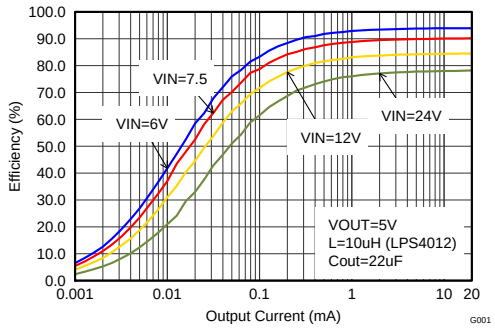


Figure 11. Efficiency vs Load Current (Sleep Mode)

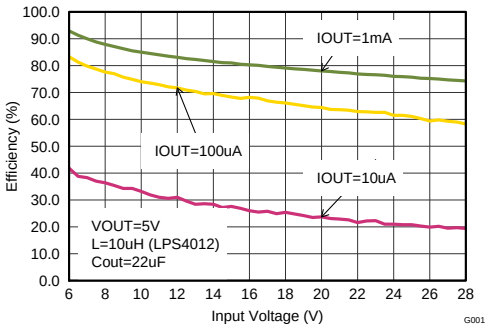


Figure 12. Efficiency vs Input Voltage (Sleep Mode)

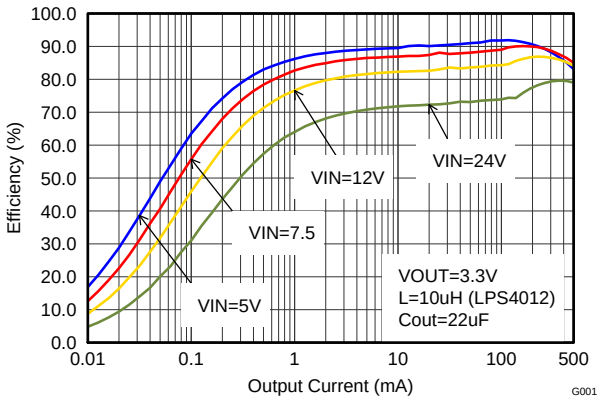


Figure 13. Efficiency vs Load Current

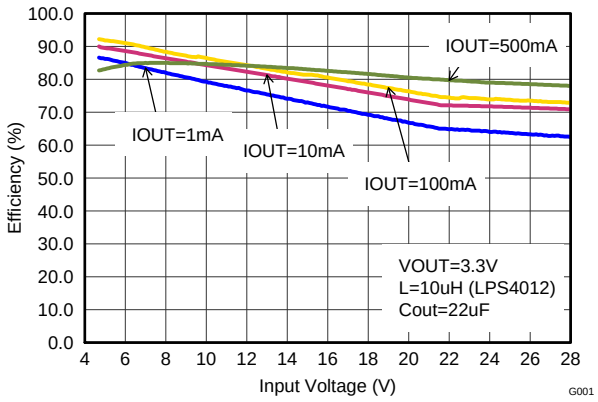


Figure 14. Efficiency vs Input Voltage

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V_{IN}=12 V, V_{OUT} = 3.3 V, T_J=25°C, unless otherwise noted

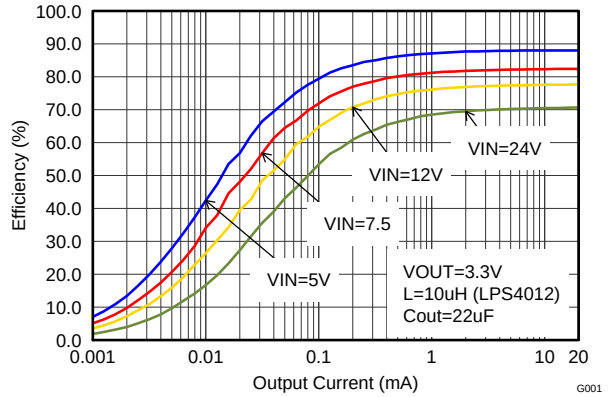


Figure 15. Efficiency vs Load Current (Sleep Mode)

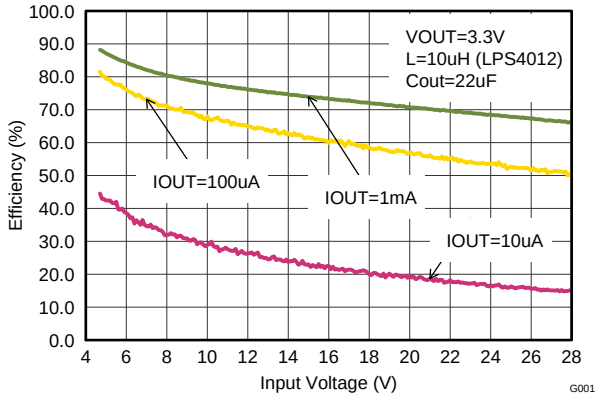


Figure 16. Efficiency vs Input Voltage (Sleep Mode)

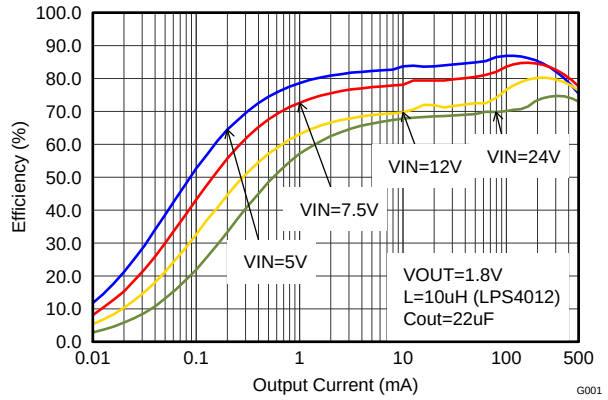


Figure 17. Efficiency vs Load Current

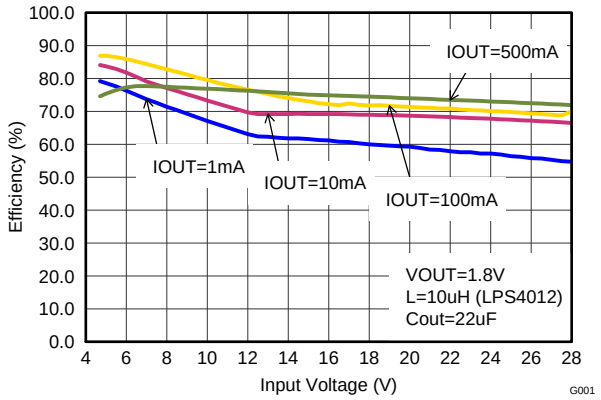


Figure 18. Efficiency vs Input Voltage

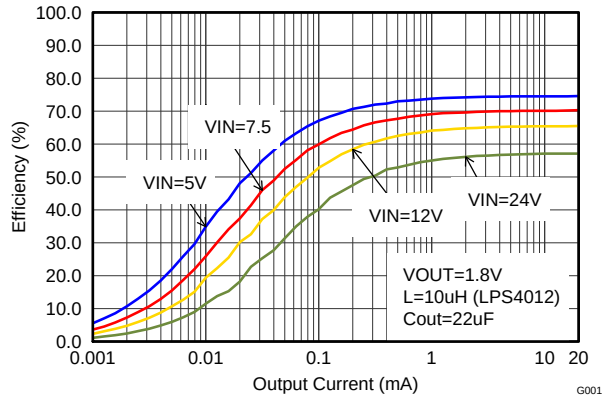


Figure 19. Efficiency vs Load Current (Sleep Mode)

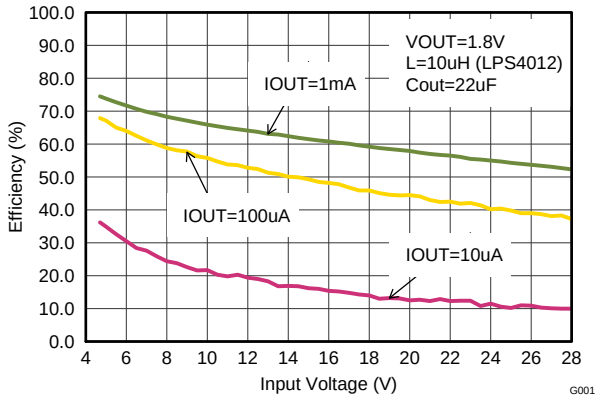


Figure 20. Efficiency vs Input Voltage (Sleep Mode)

V_{IN}=12 V, V_{OUT} = 3.3 V, T_J=25°C, unless otherwise noted

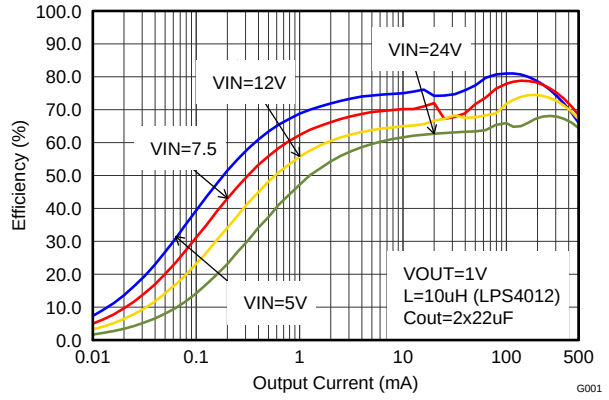


Figure 21. Efficiency vs Load Current

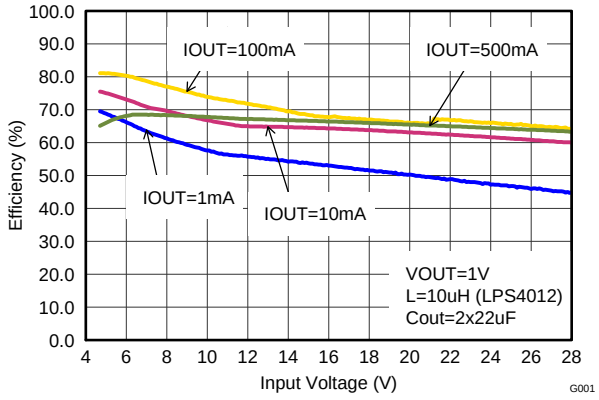


Figure 22. Efficiency vs Input Voltage

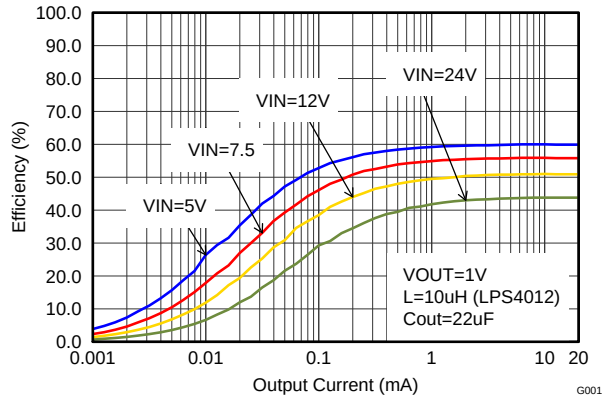


Figure 23. Efficiency vs Load Current (Sleep Mode)

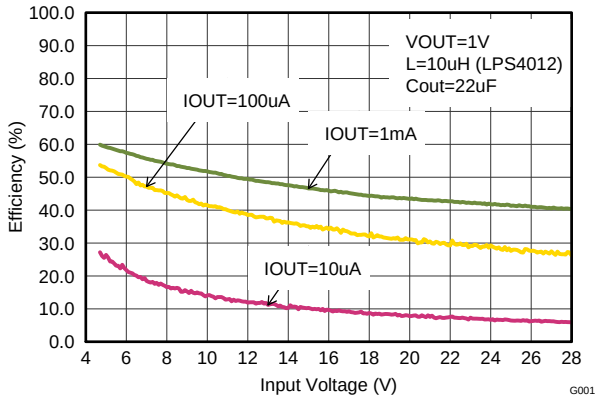


Figure 24. Efficiency vs Input Voltage (Sleep Mode)

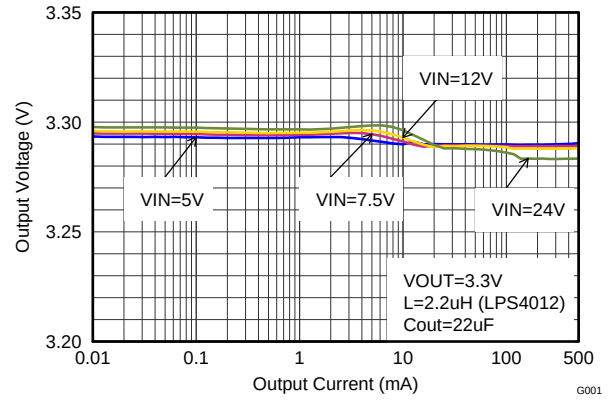


Figure 25. Output Voltage Accuracy (Load Regulation)

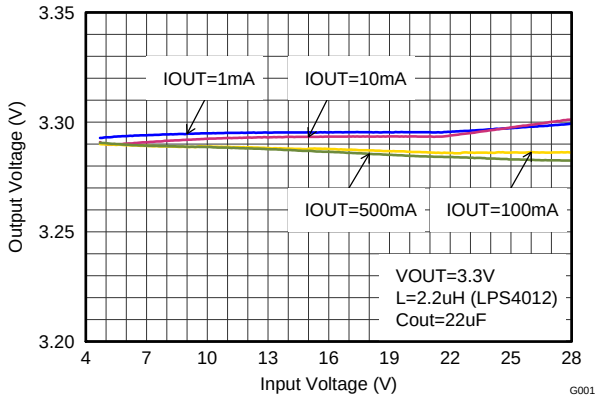


Figure 26. Output Voltage Accuracy (Line Regulation)

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V_{IN}=12 V, V_{OUT} = 3.3 V, T_J=25°C, unless otherwise noted

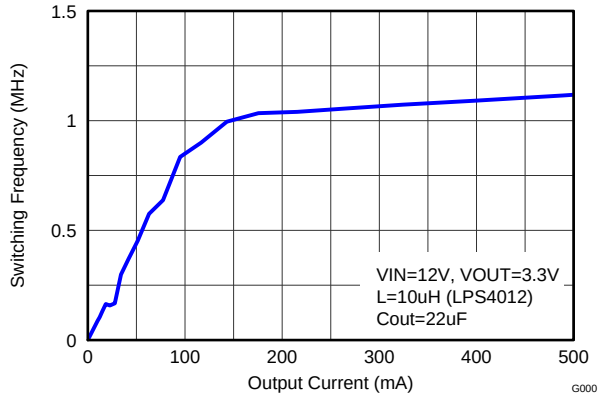


Figure 27. Switching Frequency

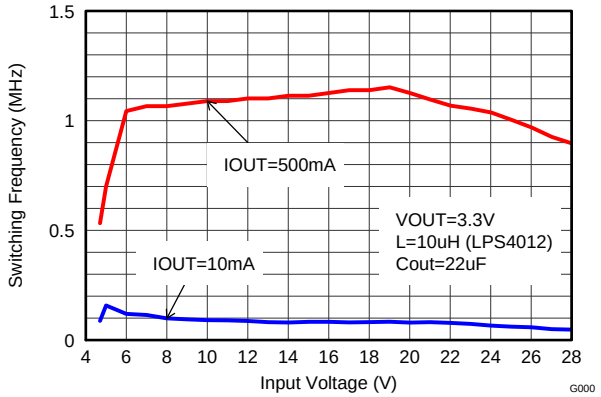


Figure 28. Switching Frequency

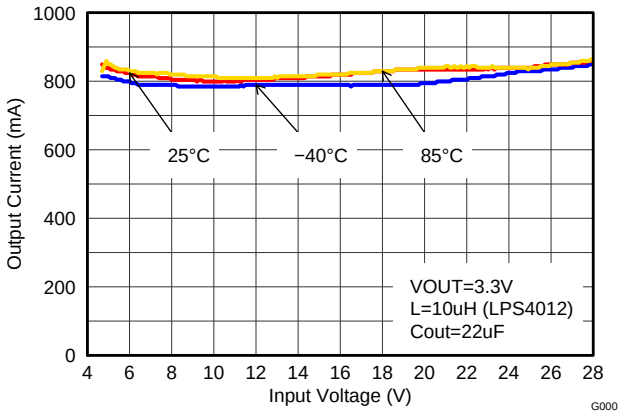


Figure 29. Maximum Output Current

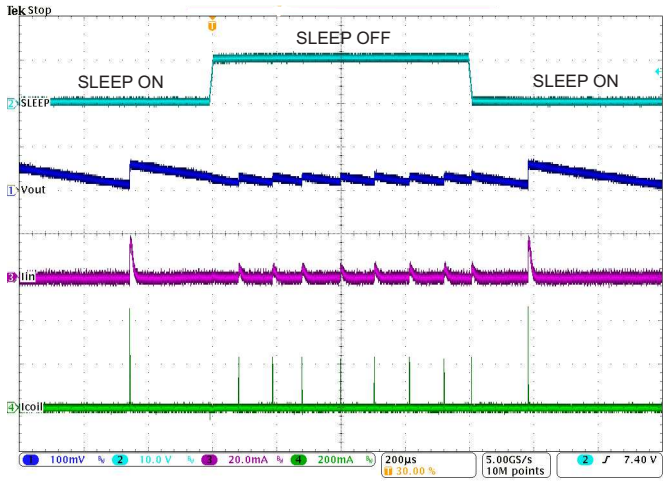


Figure 30. Sleep Mode Entry/Exit, I_{OUT} = 1 mA

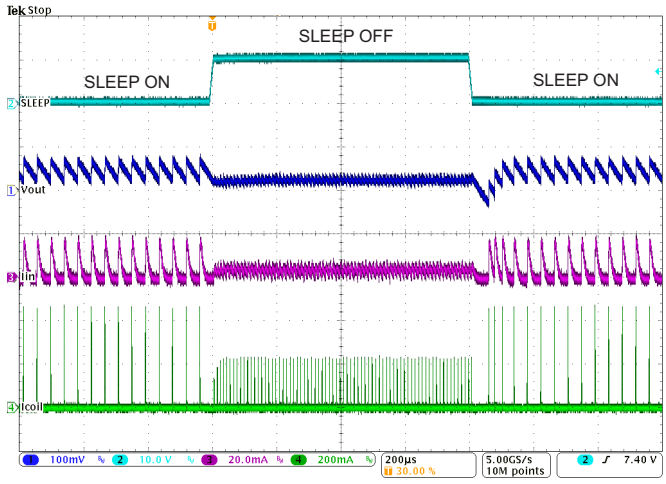


Figure 31. Sleep Mode Entry/Exit, I_{OUT} = 10 mA

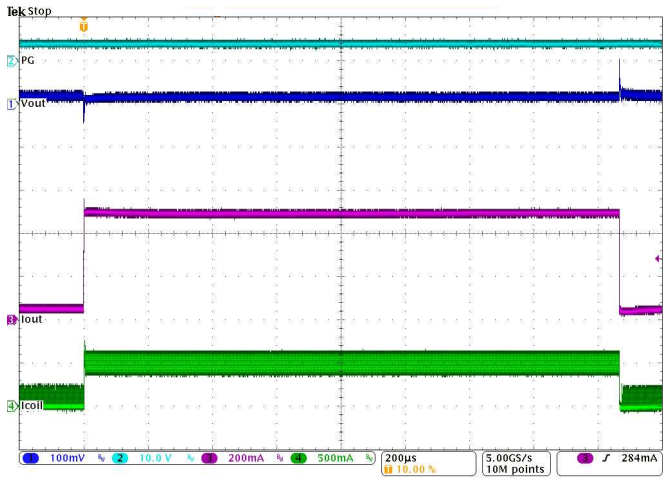


Figure 32. Load Transient Response, PWM Mode, I_{OUT} (200 mA to 500 mA)

V_{IN}=12 V, V_{OUT} = 3.3 V, T_J=25°C, unless otherwise noted

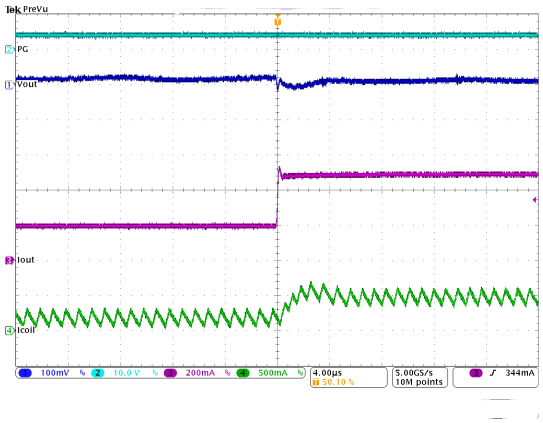


Figure 33. Load Transient Response, PWM Mode, I_{OUT} (200 mA to 500 mA), Rising Edge

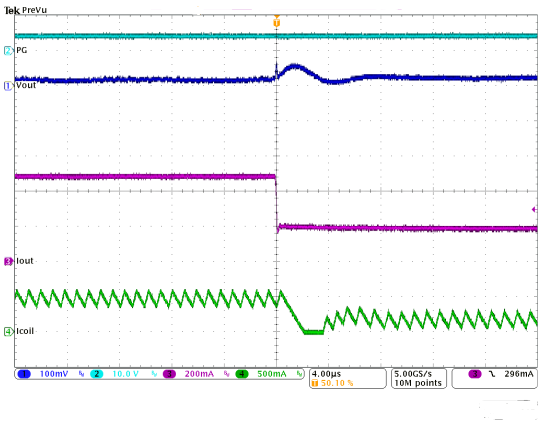


Figure 34. Load Transient Response, PWM Mode, I_{OUT} (200 mA to 500 mA), Falling Edge

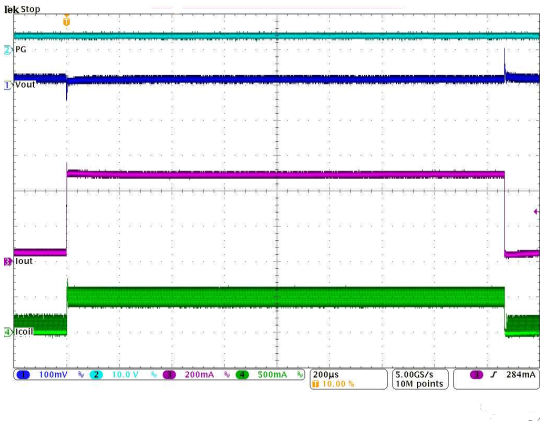


Figure 35. Load Transient Response, Power Save Mode, I_{OUT} (50 mA to 500 mA)

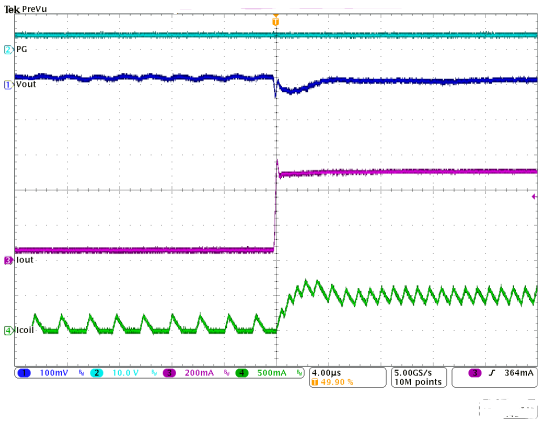


Figure 36. Load Transient Response, Power Save Mode, I_{OUT} (50 mA to 500 mA), Rising Edge

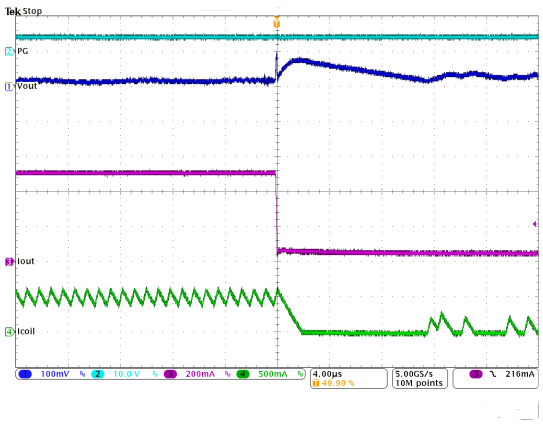


Figure 37. Load Transient Response, Power Save Mode, I_{OUT} (50 mA to 500 mA), Falling Edge

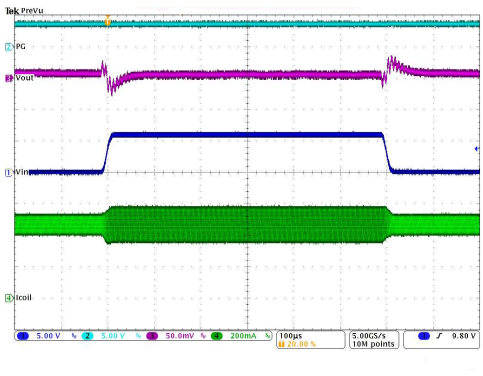


Figure 38. Line Transient Response, PWM Mode, V_{IN} (6 V to 12 V), I_{OUT} = 500 mA

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V_{IN}=12 V, V_{OUT} = 3.3 V, T_J=25°C, unless otherwise noted

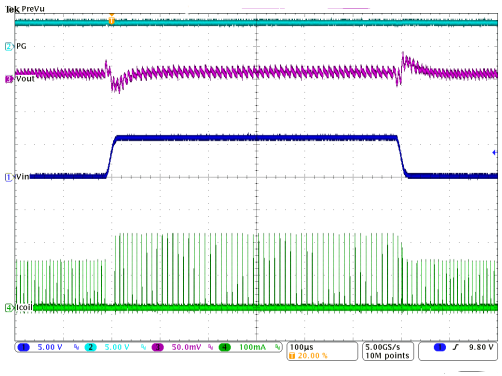


Figure 39. Line Transient Response, Power Save Mode, V_{IN} (6 V to 12 V), I_{OUT} = 10 mA

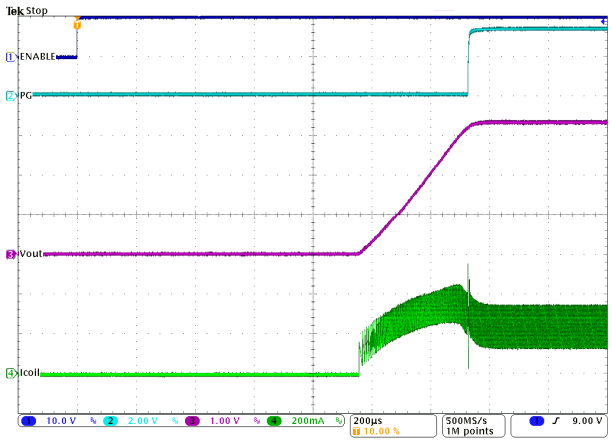


Figure 40. Start-Up (PWM Mode), I_{OUT} = 250 mA

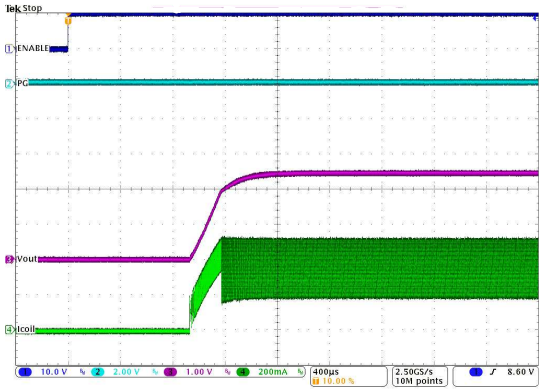


Figure 41. Start-Up Current Limit, R_{LOAD} = 6.6 Ω

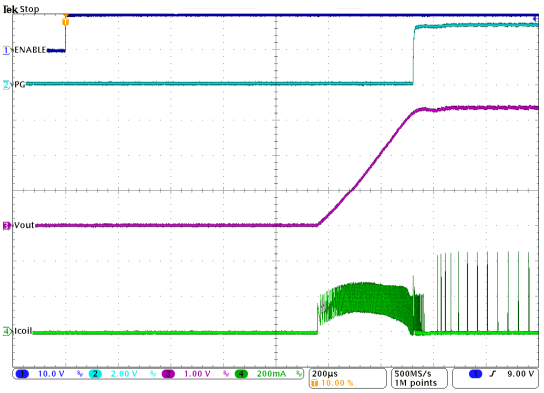


Figure 42. Start-Up (Sleep Mode), I_{OUT} = 10 mA

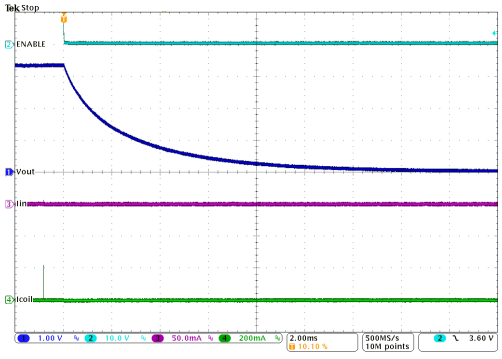


Figure 43. Output Discharge Function (No Load)

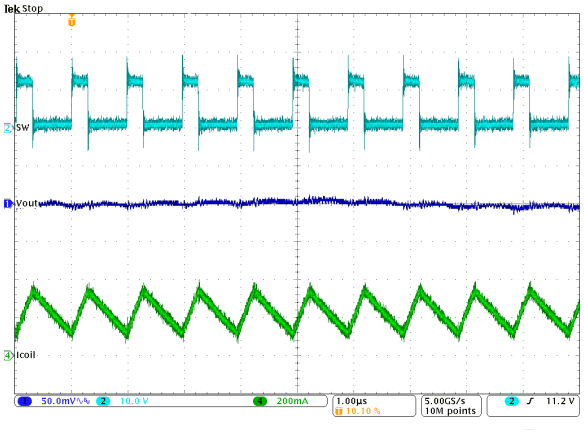


Figure 44. Typical Operation in PWM Mode, I_{OUT} = 250 mA

V_{IN}=12 V, V_{OUT} = 3.3 V, T_J=25°C, unless otherwise noted

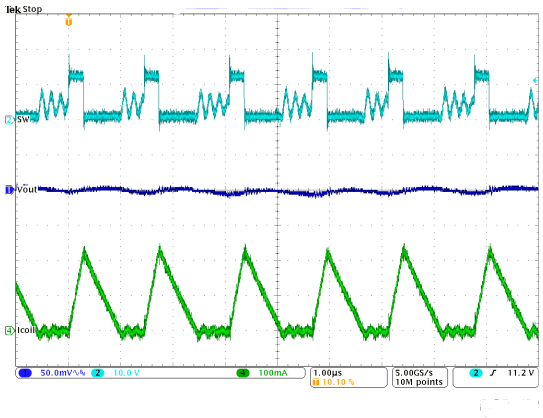


Figure 45. Typical Operation in Power Save Mode, I_{OUT} = 75 mA

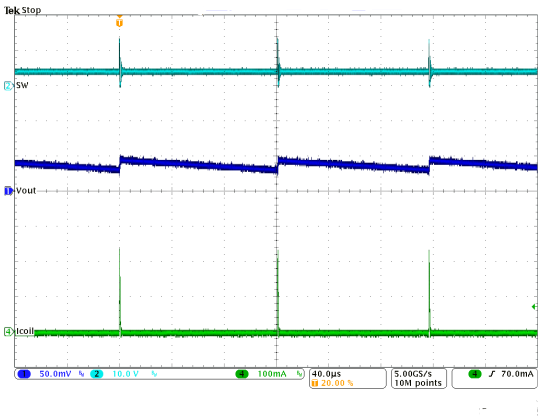


Figure 46. Typical Operation in Power Save Mode, I_{OUT} = 1 mA

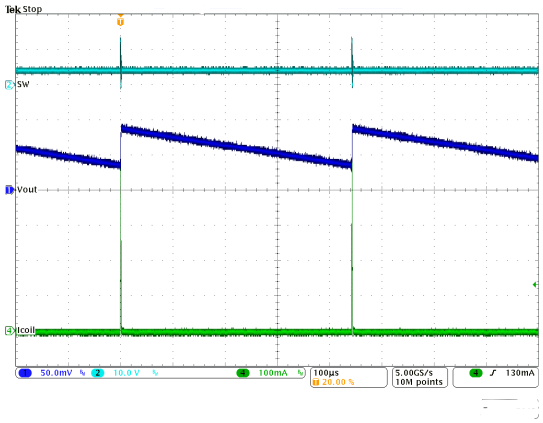


Figure 47. Typical Operation in Sleep Mode, I_{OUT} = 1 mA

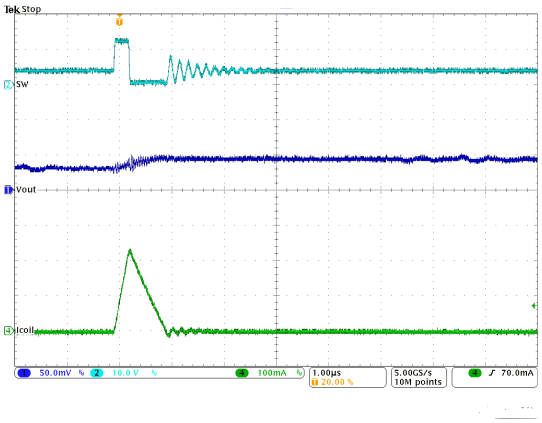


Figure 48. Typical Operation in Power Save Mode, I_{OUT} = 1 mA (Single Pulse)

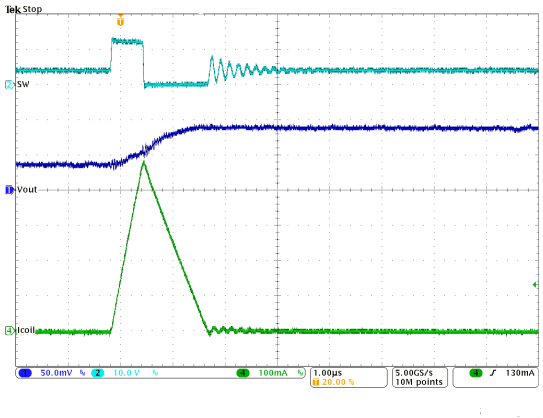


Figure 49. Typical Operation in Sleep Mode, I_{OUT} = 1 mA (Single Pulse)

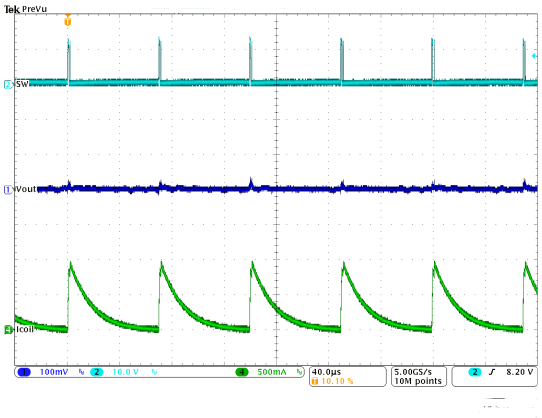


Figure 50. Short Circuit While Running

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V_{IN}=12 V, V_{OUT} = 3.3 V, T_J=25°C, unless otherwise noted

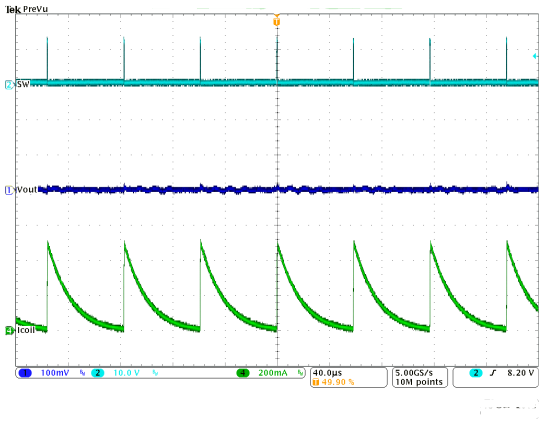


Figure 51. Short Circuit From Start-Up

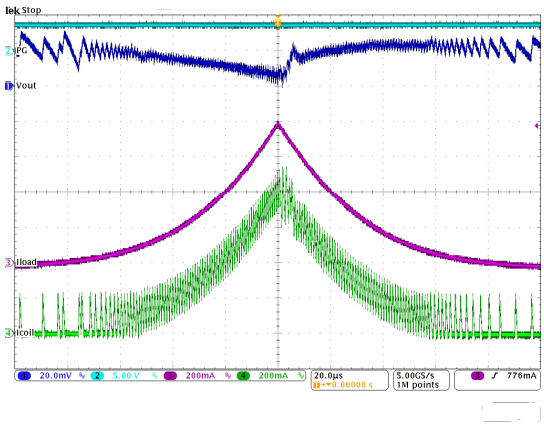


Figure 52. Triangular Load Sweep With Mode Transitions (Power Save Mode - PWM Mode - Power Save Mode)

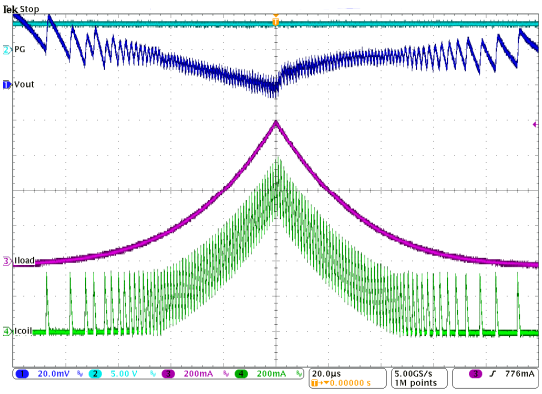


Figure 53. Triangular Load Sweep With Mode Transitions (Power Save Mode - PWM Mode - Power Save Mode), V_{IN} = 24 V

9.3 System Examples

9.3.1 Microcontroller Power Supply

The TPS6217x can be used advantageously as the power supply rail for microcontrollers with low current power save modes. Figure 54 shows the connection of TPS62177 to the Tiva C Series TM4C123x ARM Cortex™ - M4 MCUs (TM4C123x MCUs), using its hibernate mode signal to control sleep mode operation. More information is found in the Application Report, *Powering Tiva™ C Series Microcontrollers Using the High Efficiency DCS-Control™ Topology* (SPMA066).

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System Examples (continued)

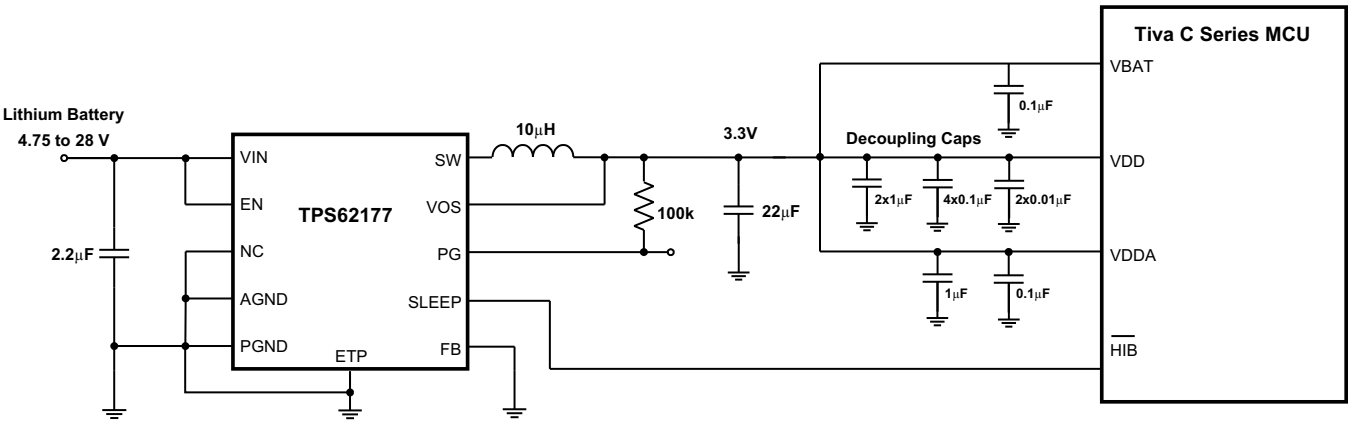


Figure 54. Microcontroller Power Supply With Sleep Mode

9.3.2 Inverting Power Supply

The TPS6217x can be used as inverting power supply by rearranging external circuitry as shown in Figure 55. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} must be limited to the maximum operating voltage of 28 V.

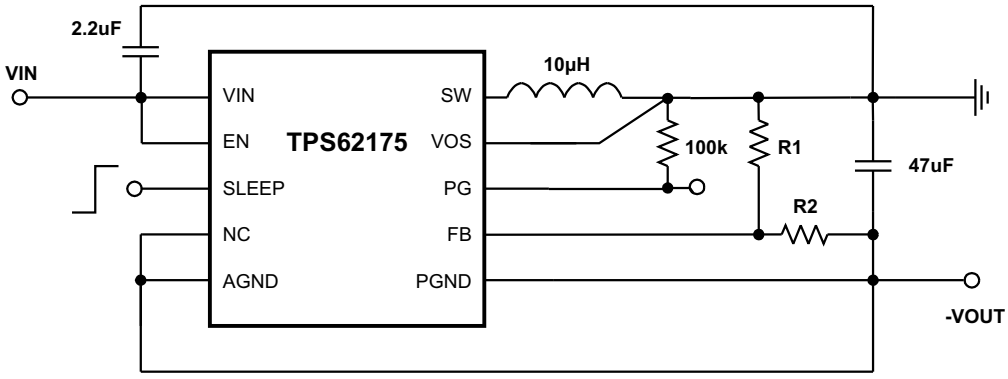


Figure 55. Inverting Buck-Boost Converter

More information about using TPS62175 as inverting buck-boost converter can be found in the Application Note, *Using the TPS62175 in an Inverting Buck Boost Topology* (SLVA542).

9.3.3 TPS62175 Adjustable Output Voltages

The following example circuits show typical schematics for commonly used output voltage values using the adjustable device version TPS62175.

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System Examples (continued)

9.3.3.1 5-V / 0.5-A Power Supply

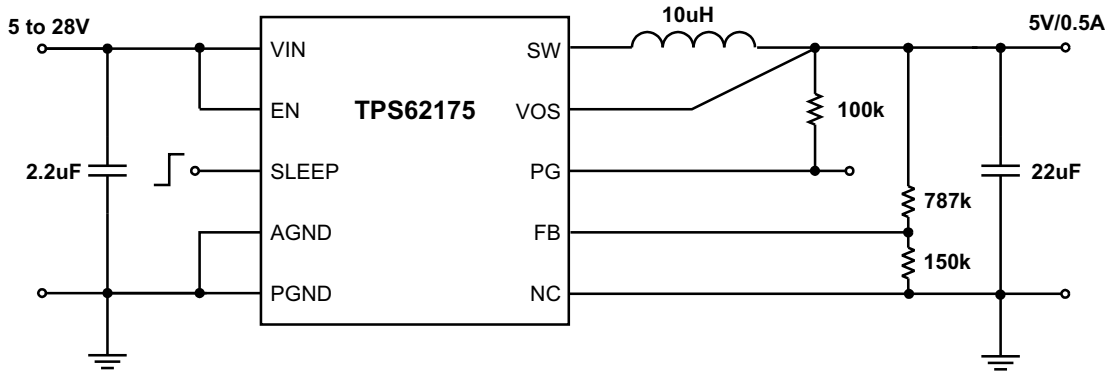


Figure 56. 5-V / 0.5-A Power Supply

9.3.3.2 2.5-V / 0.5-A Power Supply

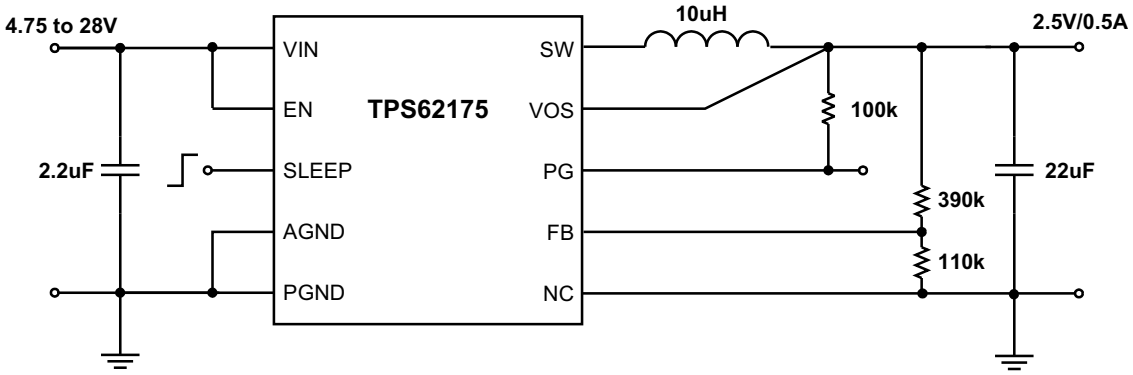


Figure 57. 2.5-V / 0.5-A Power Supply

9.3.3.3 1.8-V / 0.5-A Power Supply

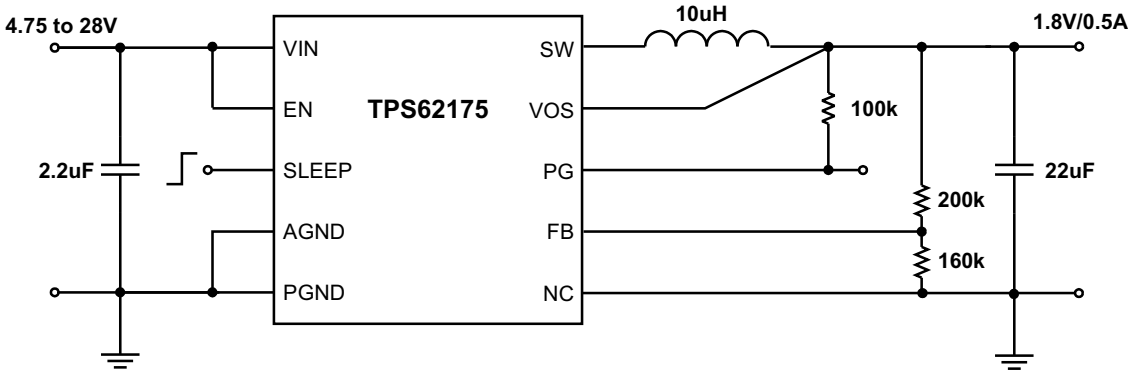


Figure 58. 1.8-V / 0.5-A Power Supply

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System Examples (continued)

9.3.3.4 1.2-V / 0.5-A Power Supply

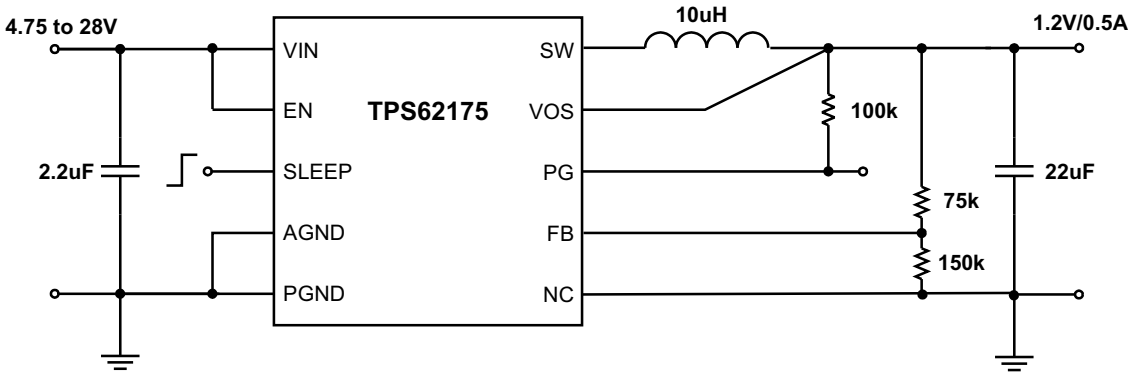


Figure 59. 1.2-V / 0.5-A Power Supply

9.3.3.5 1-V / 0.5-A Power Supply

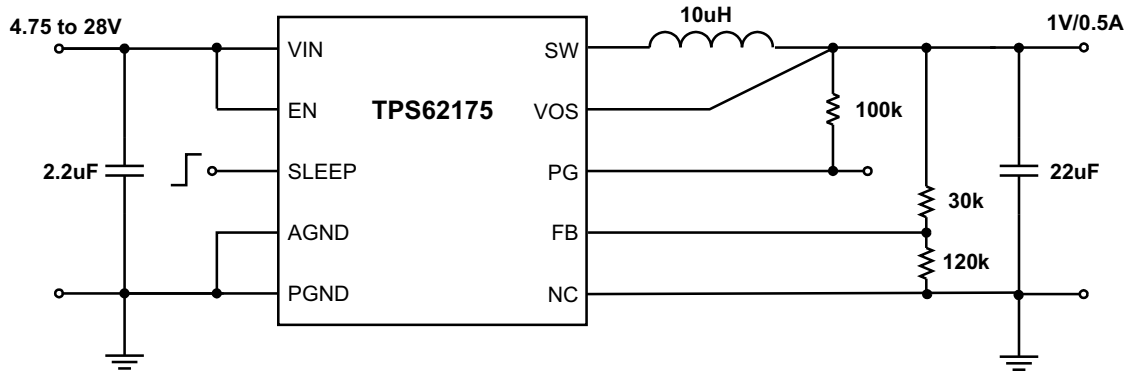


Figure 60. 1-V / 0.5-A Power Supply

9.3.4 TPS62177 Fixed 3.3-V / 0.5-A Power Supply

The following example circuit shows the typical schematic for fixed output voltage using the device version TPS62177.

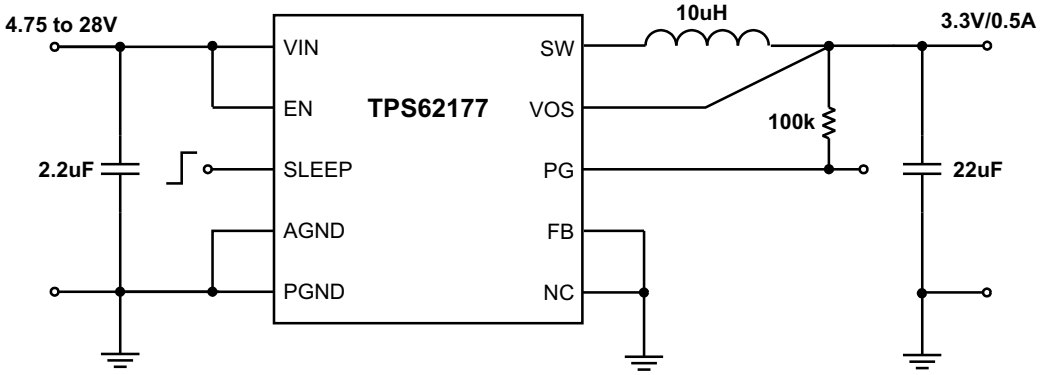


Figure 61. 3.3-V / 0.5-A Power Supply

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10 Power Supply Recommendations

The TPS6217x device family has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS6217x.

11 Layout

11.1 Layout Guidelines

The input capacitor needs to be placed as close as possible to the IC pins (VIN, PGND). The inductor should be placed close to the SW pin and connect directly to the output capacitor - minimizing the loop area between the SW pin, inductor, output capacitor and PGND pin. Also, sensitive nodes like FB and VOS should be connected with short wires, not nearby high dv/dt signals (for example, SW). The feedback resistors, R_1 and R_2, should be placed close to the IC and connect directly to the AGND and FB pins.

A proper layout is critical for the operation of a switch mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6217x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity. See Figure 62 for the recommended layout of the TPS62175, which is implemented on the EVM. Information can be found in the EVM Users Guide, *TPS62175EVM-098 Evaluation Module* (SLVU743). Alternatively, the EVM Gerber data are available for download here, SLVC453.

11.2 Layout Example

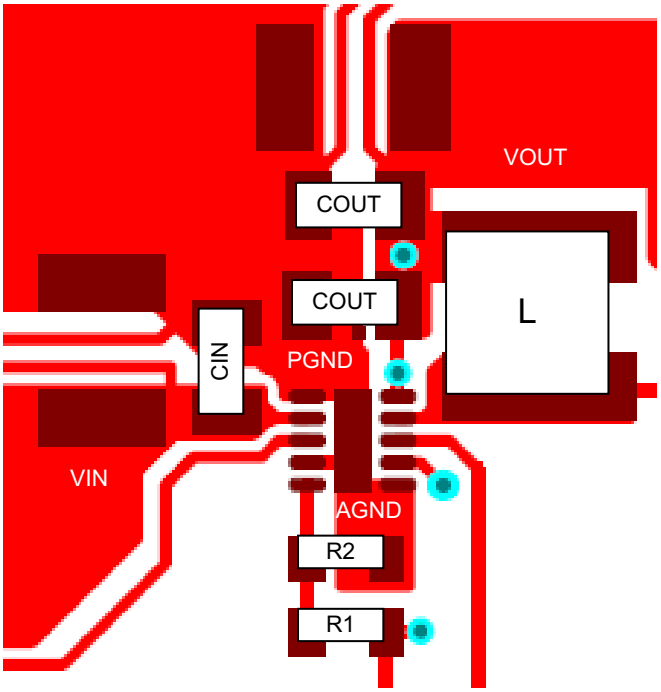


Figure 62. Layout Example Recommendation

The exposed thermal pad must be soldered to AGND and on the circuit board for mechanical reliability and to achieve appropriate power dissipation.

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11.3 Thermal Information

The TPS6217x is designed for a maximum operating junction temperature (T_J) of 125°C. Therefore the maximum output power is limited by the power losses. Because the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, TI recommends using top layer metal to connect the device with wide and thick metal lines (see Figure 62). Internal ground layers can connect to vias directly under the IC for improved thermal performance.

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017), and *Semiconductor and IC Package Thermal Metrics* (SPRA953).

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

Refer to the following documents for more information:

- *Optimizing the TPS62175 Output Filter*, SLVA543
- *Powering Tiva™ C Series Microcontrollers Using the High Efficiency DCS-Control™ Topology*, SPMA066
- *Using the TPS62175 in an Inverting Buck Boost Topology*, SLVA542
- *TPS62175EVM-098 Evaluation Module*, SLVU743
- *Semiconductor and IC Package Thermal Metrics*, SPRA953
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*, SZZA017

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62175	Click here	Click here	Click here	Click here	Click here
TPS62177	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

DCS-Control, E2E are trademarks of Texas Instruments.
ARM Cortex is a trademark of ARM Limited.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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12.7 Glossary

SLYZ022 — *TI Glossary*.

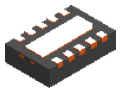
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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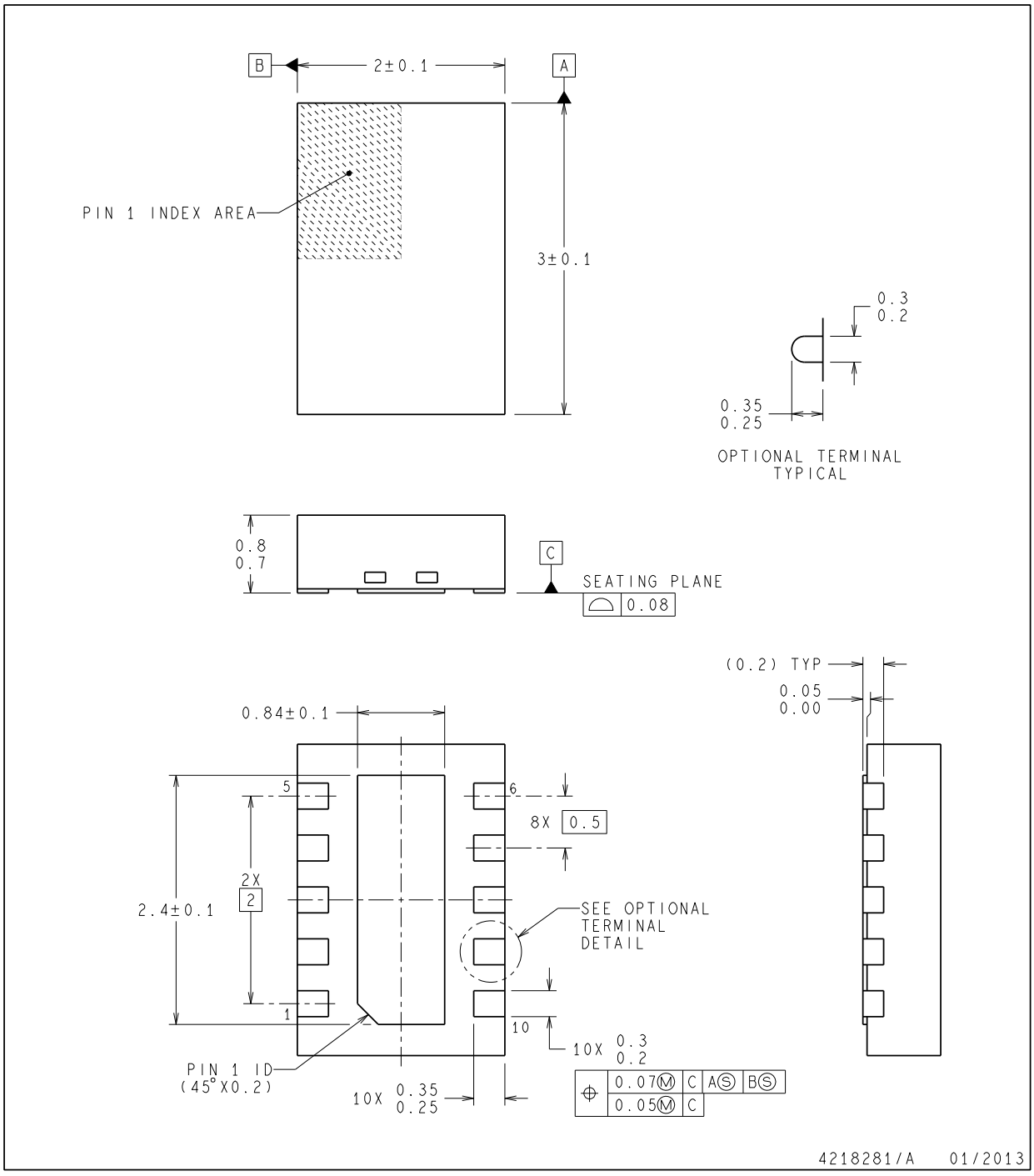
MECHANICAL DATA



DQC0010A

WSON - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK-NO LEAD)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN PARENTHESIS ARE FOR REFERENCE ONLY.
2. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
3. THE PACKAGE THERMAL PAD MUST BE SOLDERED TO THE PRINTED CIRCUIT BOARD FOR THERMAL AND MECHANICAL PERFORMANCE.
4. R-PWSON-N10.

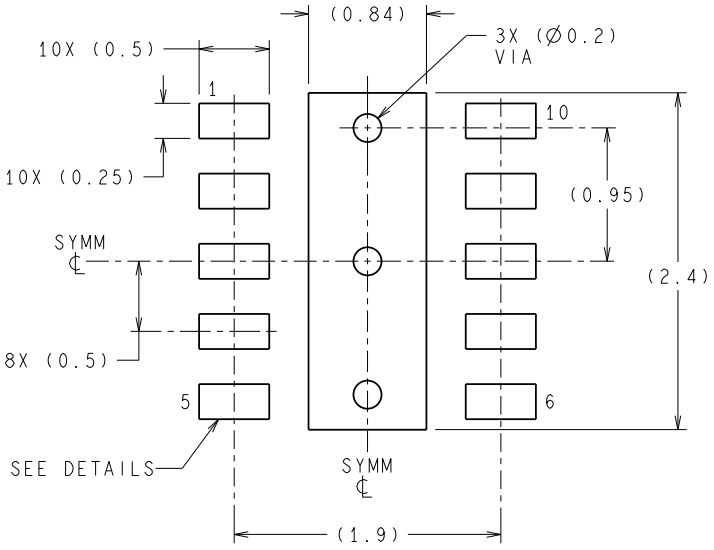
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MECHANICAL DATA

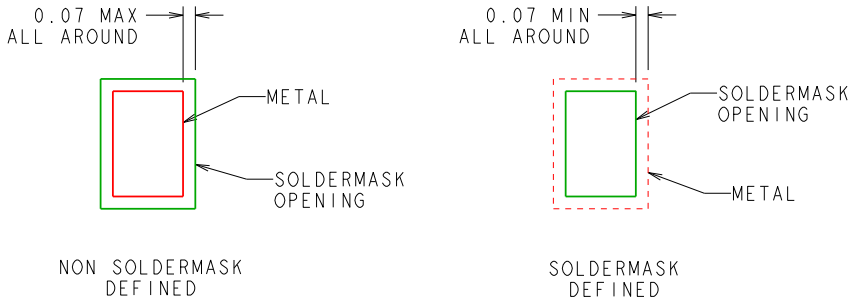
DQC0010A

WSON - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK-NO LEAD)



RECOMMENDED LAND PATTERN



SOLDERMASK DETAILS

4218281/A 01/2013

NOTES: 1. FOR PCB LAYOUT AND ASSEMBLY CONSIDERATIONS PLEASE REFER TO SLUA271 APPLICATION REPORT AVAILABLE AT www.ti.com.

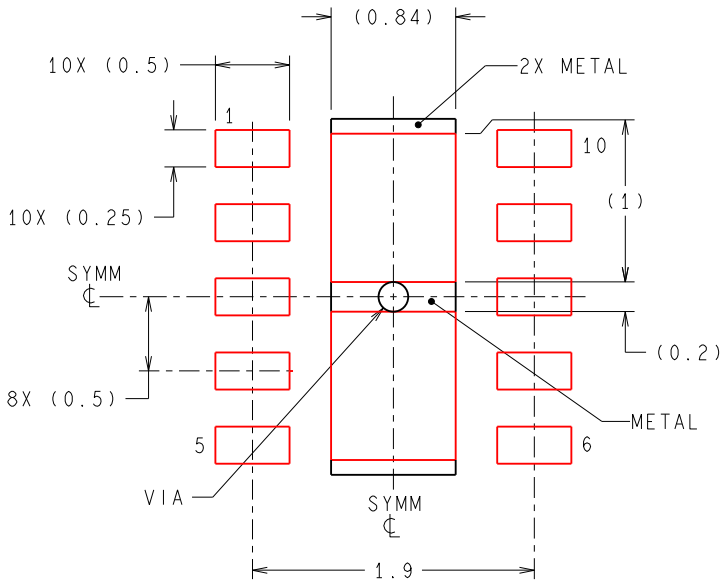
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MECHANICAL DATA

DQC0010A

WSON - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK-NO LEAD)



RECOMMENDED SOLDERPASTE
EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA

4218281/A 01/2013

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62175DQCR	ACTIVE	WSON	DQC	10	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	62175	Samples
TPS62175DQCT	ACTIVE	WSON	DQC	10	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	62175	Samples
TPS62177DQCR	ACTIVE	WSON	DQC	10	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	62177	Samples
TPS62177DQCT	ACTIVE	WSON	DQC	10	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	62177	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

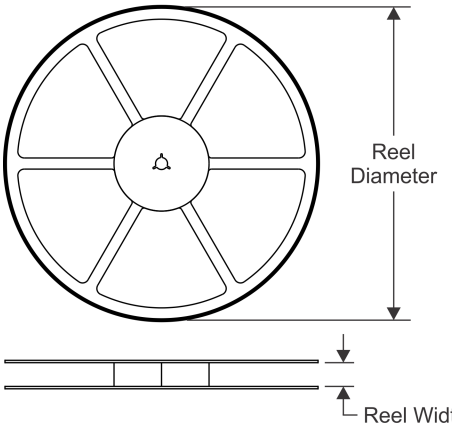
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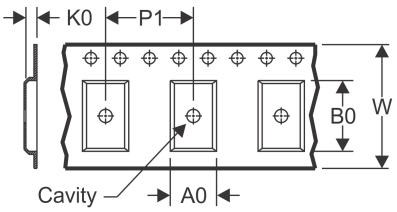
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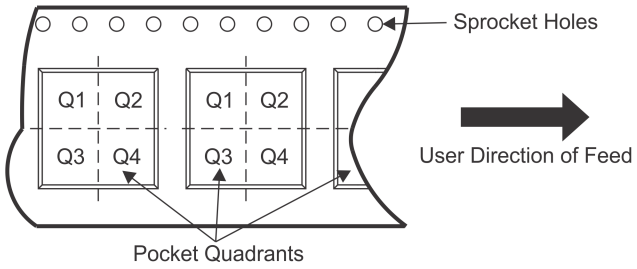


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

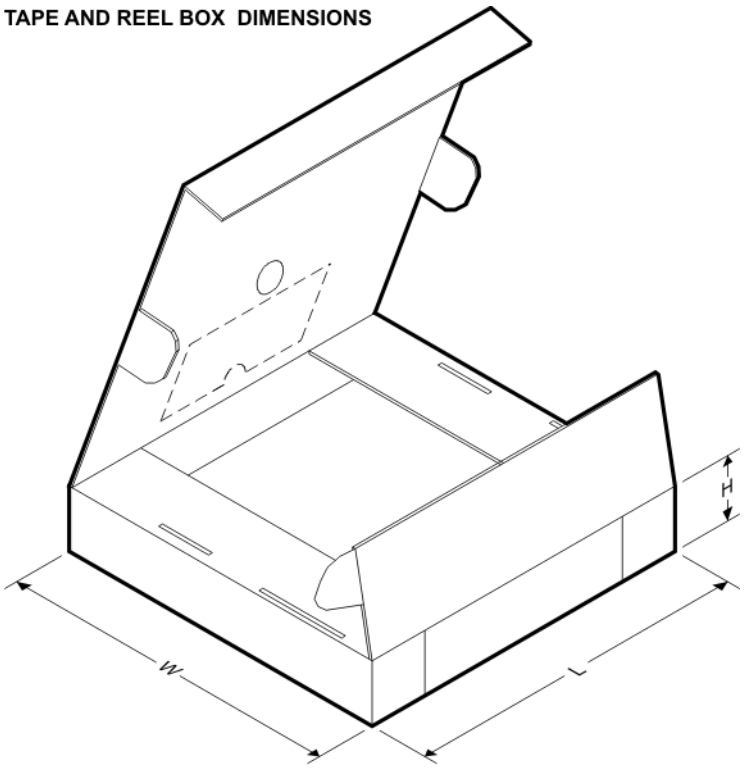
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62175DQCR	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS62175DQCT	WSON	DQC	10	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS62177DQCR	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS62177DQCT	WSON	DQC	10	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62175DQCR	WSON	DQC	10	3000	210.0	185.0	35.0
TPS62175DQCT	WSON	DQC	10	250	210.0	185.0	35.0
TPS62177DQCR	WSON	DQC	10	3000	210.0	185.0	35.0
TPS62177DQCT	WSON	DQC	10	250	210.0	185.0	35.0

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