TPS62060EVM-663

This user's guide describes the characteristics, operation, and use of the TPS62060 evaluation module (EVM). The TPS62060EVM-663 is a fully assembled and tested platform for evaluating the performance of the TPS62060 1.6-A step-down converter. This document includes schematic diagrams, printed-circuit board (PCB) layout, bill of materials, and test data. Throughout this document, the abbreviations *EVM*, *TPS62060EVM*, and the term *evaluation module* are synonymous with the TPS62060EVM-663 unless otherwise noted.

Contents

1 Introduction 3
2 Electrical Performance Specifications 3
3 TPS62060EVM Schematic 4
4 Connector and Test Point Descriptions 5
5 Test Configuration 6
6 TPS62060EVM Test Data 7
7 TPS62060EVM Thermal Performance 14
8 TPS62060EVM Assembly Drawings and Layout 15
9 Bill of Materials 19

List of Figures

1 TPS62060EVM Schematic 4
2 Hardware Board Connection 6
3 TPS62060 Efficiency vs Load Current, PFM Mode 7
4 TPS62060 Efficiency vs Load Current 8
5 TPS62060 Start-up Into 2.2-Ω Load 8
6 TPS62060 Start-up With No Load 9
7 TPS62060 Shutdown Into 2.2-Ω Load 10
8 TPS62060 Shutdown With No Load 10
9 TPS62060 Output Voltage Ripple, PFM Mode 11
10 TPS62060 Output Voltage Ripple, PWM Mode 11
11 TPS62060 Input Voltage Ripple 12
12 TPS62060 Gain and Phase vs Frequency 12
13 TPS62060 Gain and Phase vs Frequency 13
14 TPS62060 Transient Response, PFM Mode 13
15 TPS62060 Transient Response, PWM Mode 14
16 TPS62060EVM Thermal Performance 14
17 TPS62060EVM Component Placement, Top View 15
18 TPS62060EVM Top-Side Copper, Top View 16
19 TPS62060EVM Internal Layer 1, X-Ray View From Top 17
20 TPS62060EVM Internal Layer 2, X-Ray View From Top 18
21 TPS62060EVM Bottom-Side Copper, Bottom View 19

List of Tables

1 TPS62060EVM Performance Characteristics 3

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2 TPS62060EVM Bill of Materials 19

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1 Introduction

The TPS62060EVM-663 is a fully assembled and tested PCB for evaluating the TPS62060 1.6-A step-down converter.

1.1 Features

- Input voltage range: 2.7 V to 6 V
- Adjustable output voltage: 0.8 V to VIN
- Up to 1.6-A output current
- Power Save mode/ 3-MHz fixed-PWM mode
- Clock dithering

1.2 TPS62060 Applications

The TPS62060 step-down converters are ideal for these applications:

- POL
- Notebooks, pocket personal computers
- Portable media players
- DSP supply

2 Electrical Performance Specifications

Table 1 summarizes the TPS62060EVM performance specifications.

Table 1. TPS62060EVM Performance Characteristics

Parameter	Symbol	Notes and Conditions	Min	Typ	Max	Units
Input Characteristics						
Input Voltage	VIN		2.7		6	V
Input Undervoltage Lockout (UVLO)	V_{IN_UVLO}	Falling	1.73	1.78	1.83	V
		Rising	1.9	1.95	1.99	V
Output Characteristics						
Line Regulation				0		%/V
Load Regulation				–0.5		%/A
Output Current	I_{OUT}	VIN = 2.7 V to 6 V			1600	mA
Forward Current Limit High-Side and Low Side MOSFET	I_{LIMF}	VIN = 2.7 V to 6 V	1800	2250	2700	mA
Systems Characteristics						
Switching Frequency	f_{SW}	VIN = 2.7 V to 6 V, MODE = High	2600	3000	3400	kHz
Peak Efficiency	η_{pk}	VIN = 3.3 V, MODE = Low			91.0	%
Full Load Efficiency	η	VIN = 5 V, VOUT = 1.8 V, I_{OUT} = 1600 mA		83.3		%

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3 TPS62060EVM Schematic

Figure 1 shows the TPS62060EVM schematic.

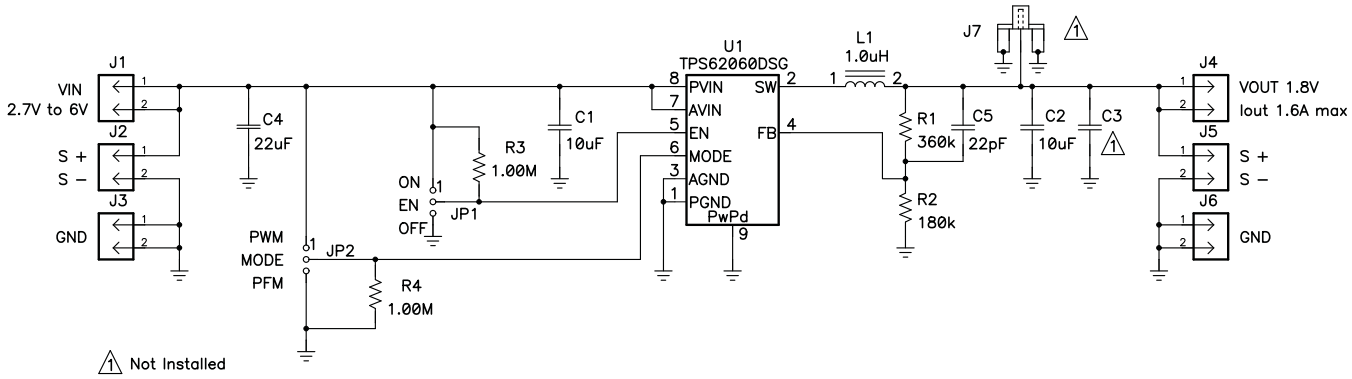


Figure 1. TPS62060EVM Schematic

NOTE: Figure 1 is provided for reference only. See the bill of materials (Table 2) for specific component values.

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4 Connector and Test Point Descriptions

4.1 Enable Jumpers/Switches: TPS62060EVM

4.1.1 J1 – VIN

This header is the positive connection to the input power supply. The power supply must be connected between J1 and J3 (GND). Twist the leads to the input supply, and keep them as short as possible. The input voltage must be between 2.7 V and 6 V.

4.1.2 J2 – S+/S–

J2 S+/S– are the sense connections for the input of the converter. Connect a voltmeter, or the sense connection of a power supply or oscilloscope, to this header.

4.1.3 J3 – GND

This header is the return connection to the input power supply. Connect the power supply between J3 and J1 (VIN). Twist the leads to the input supply, and keep them as short as possible. The input voltage must be between 2.7 V and 6 V.

4.1.4 J4 – VOUT

This header is the positive output of the step-down converter. The output voltage of the TPS62060 is adjustable with feedback resistors R1 and R2. On the EVM, the output voltage is set to 1.8 V by default.

NOTE: A feed-forward capacitor C5 is required. Refer to the TPS62060 data sheet (SLVSA95) for detailed information.

4.1.5 J5 – S+/S–

J5 S+/S– are the sense connections for the output of the converter. Connect a voltmeter, or the sense connection of an electronic load or oscilloscope, to this header.

4.1.6 J6 – GND

J6 is the return connection of the converter. A load can be connected between J6 and J4 (V_{OUT}). The converter is capable of carrying a load current up to 1600 mA.

4.1.7 JP1 – EN

This jumper enables/disables the TPS62060 on the EVM. Shorting jumper JP1 between the center pin and *On* turns on the unit. Shorting the jumper between center pin and *Off* turns off the unit. A 1-MΩ pullup resistor is connected between VIN and EN. Removing jumper JP1 turns on the converter.

4.1.8 JP2 – MODE

This jumper enables/disables the power-saving mode under light loads. Shorting jumper JP2 between the center pin and PWM disables the power-saving mode. If the power-save mode is disabled, the converter operates in forced PWM mode over the entire load current range. Shorting the jumper between the center pin and PFM enables the power-saving mode. The device operates in power-saving mode under light load conditions. See the TPS62060 data sheet (SLVSA95) for a detailed description of this configuration. A 1-MΩ pulldown resistor is connected between GND and MODE. By removing JP2, the converter operates in power-saving mode under light-load conditions.

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4.1.9 J7 – VOUT (SMA)

This SMA connector is connected to the output voltage of the TPS62060. It can be used to easily analyze the noise spectrum of the output voltage with a spectrum analyzer. By default, J7 is not assembled on the EVM.

5 Test Configuration

5.1 Hardware Setup

Figure 2 illustrates a typical hardware test configuration.

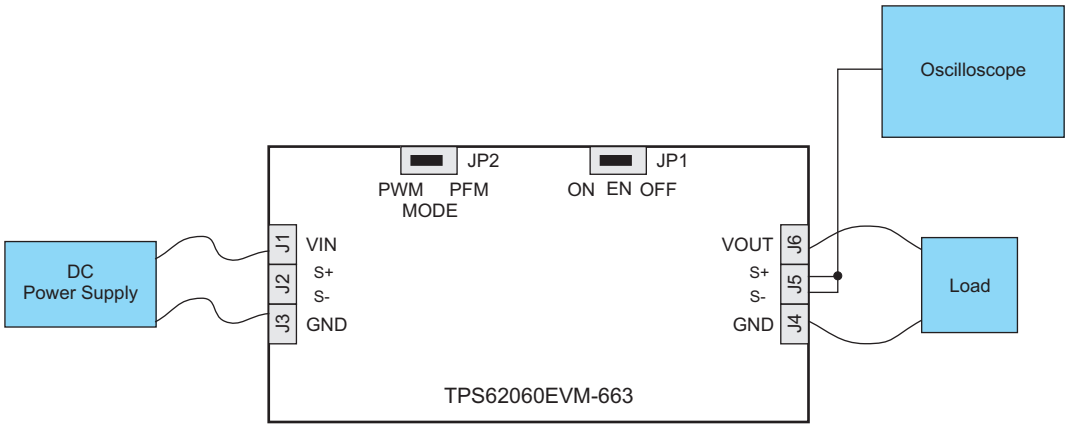


Figure 2. Hardware Board Connection

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5.2 Testing Procedure

Follow these procedures when configuring the EVM for testing.

CAUTION

Many of the components on the TPS62060EVM-663 are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD-handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap, bootstraps, or mats at an approved ESD workstation. An electrostatic smock and safety glasses also are recommended.

1. Connect a dc power supply between J1 and J3 on the TPS62060EVM. Note that the input voltage must be between 2.7 V and 6 V. Keep the wires from the input power supply to the EVM as short as possible and twisted.
2. Connect a dc voltmeter or oscilloscope to J5, the output sense connection of the EVM.
3. A load can be connected between J4 and J6 on the TPS62060EVM.
4. To enable the converter, connect the shorting bar on JP1 between EN and ON located on the TPS62060EVM.
5. The TPS62060EVM has a feature to allow the user to switch between Power-Save mode under light loads and forced PWM mode; this feature is enabled or disabled with jumper JP2.

6 TPS62060EVM Test Data

Figure 3 through Figure 15 present typical performance curves for the TPS62060EVM. Actual performance data can be affected by measurement techniques and environmental variables; therefore, these curves are presented for reference and may differ from actual results obtained by some users.

6.1 Efficiency

Figure 3 and Figure 4 show the typical efficiency performance for the TPS62060EVM.

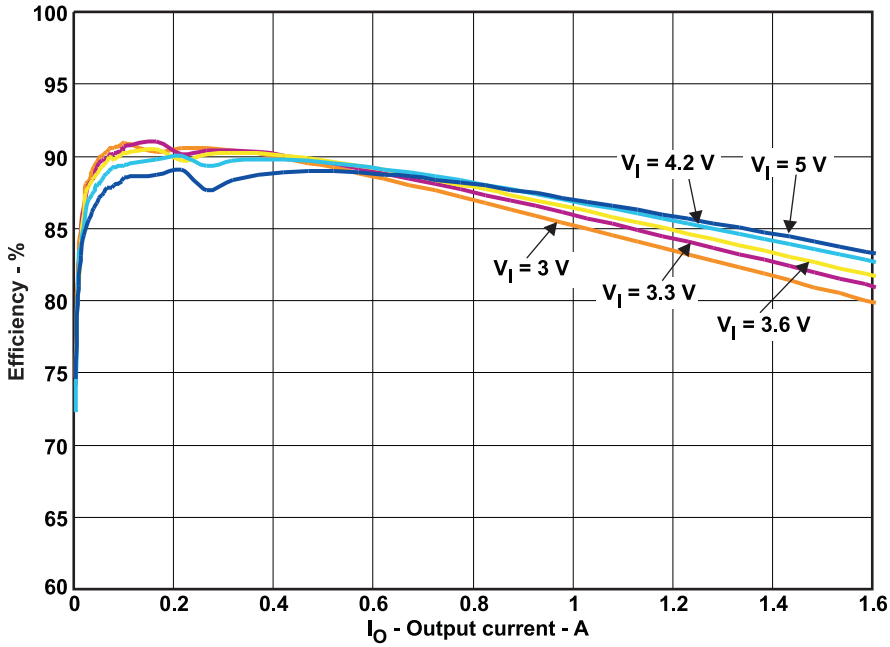


Figure 3. TPS62060 Efficiency vs Load Current, PFM Mode

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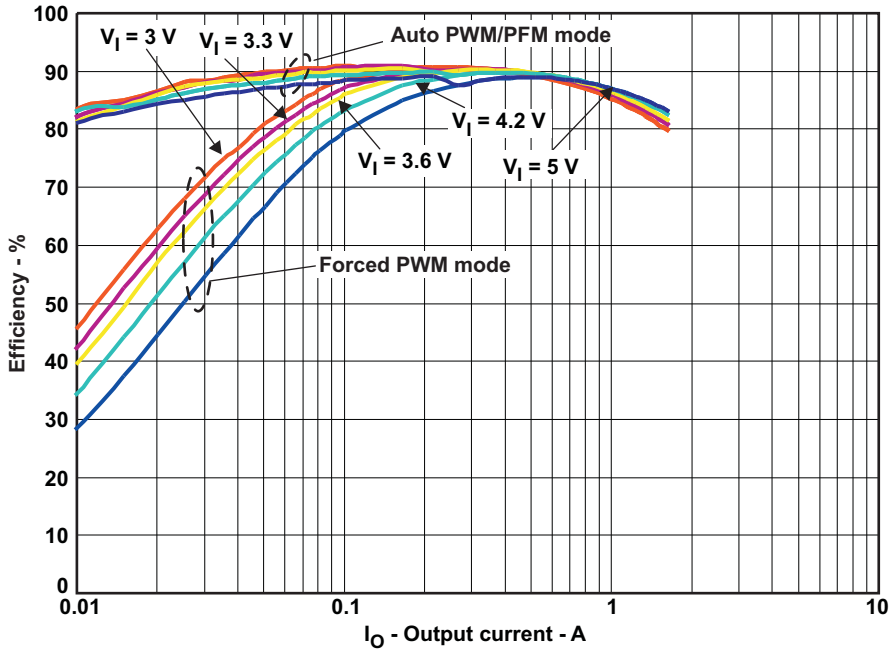
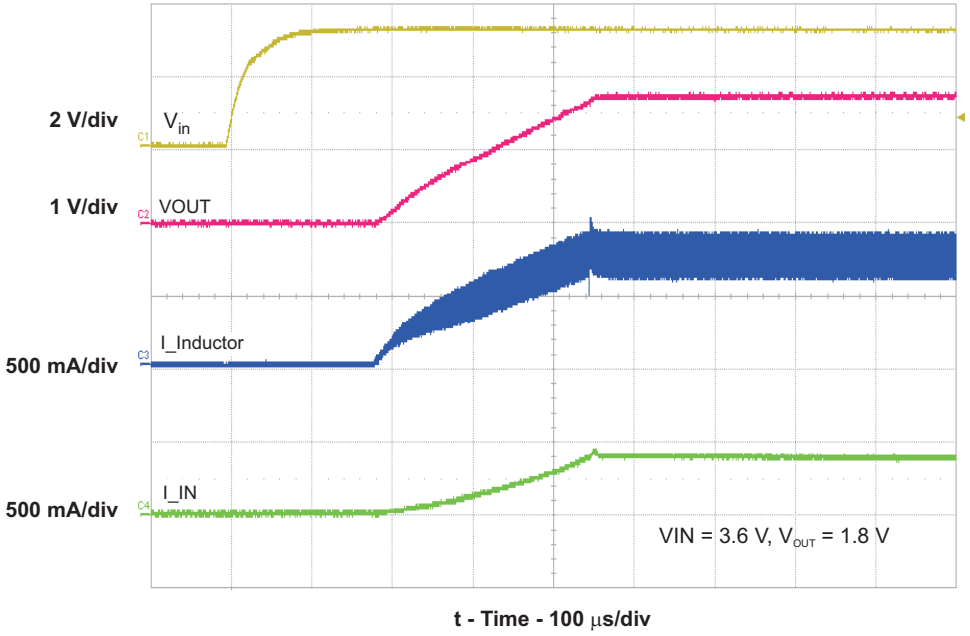


Figure 4. TPS62060 Efficiency vs Load Current

6.2 Start-up

Figure 5 and Figure 6 show the typical start-up performance for the TPS62060EVM.



Conditions: VIN = 3.6 V, V_{OUT} = 1.8 V

Figure 5. TPS62060 Start-up Into 2.2-Ω Load

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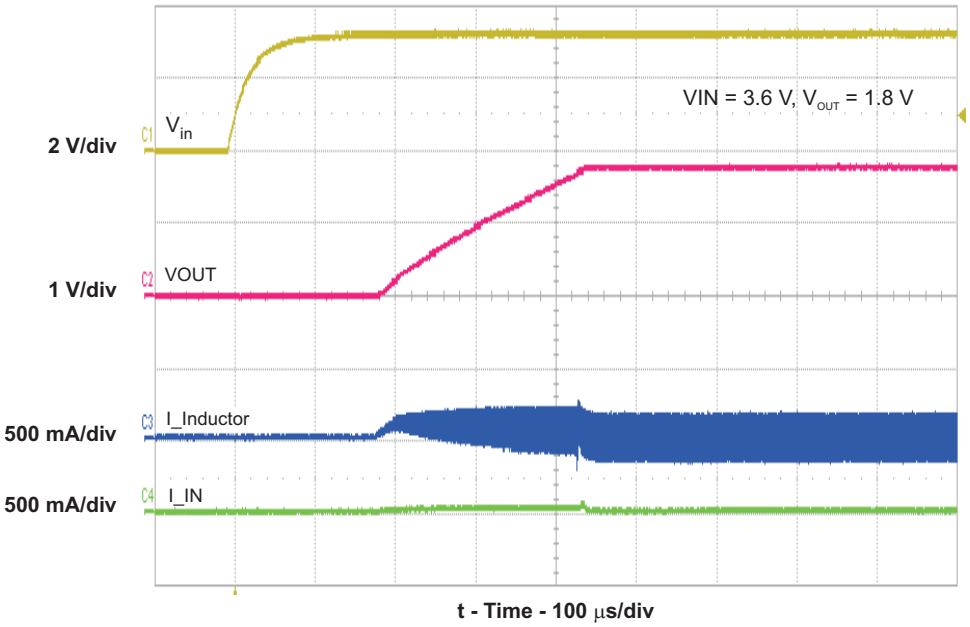
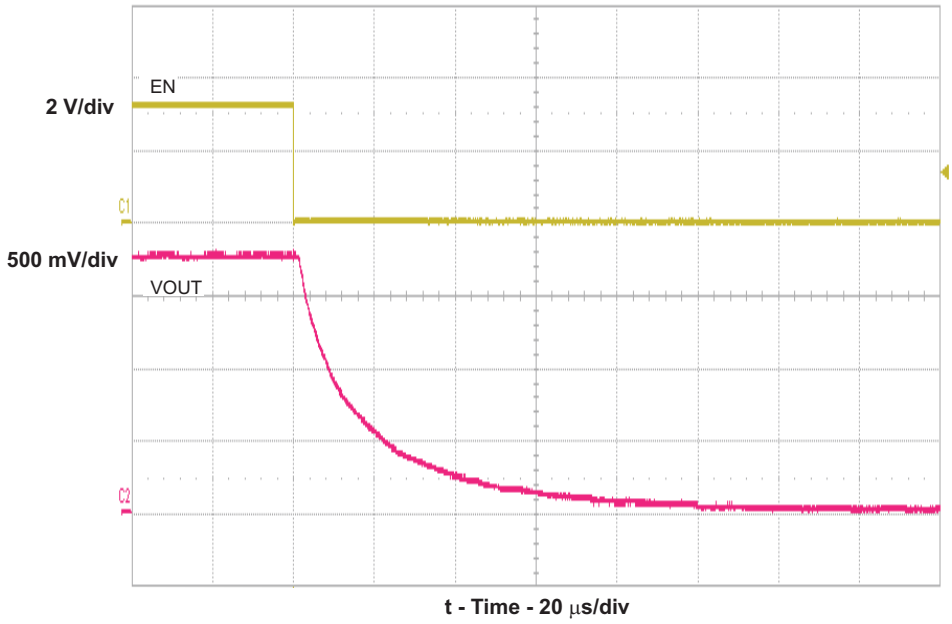


Figure 6. TPS62060 Start-up With No Load

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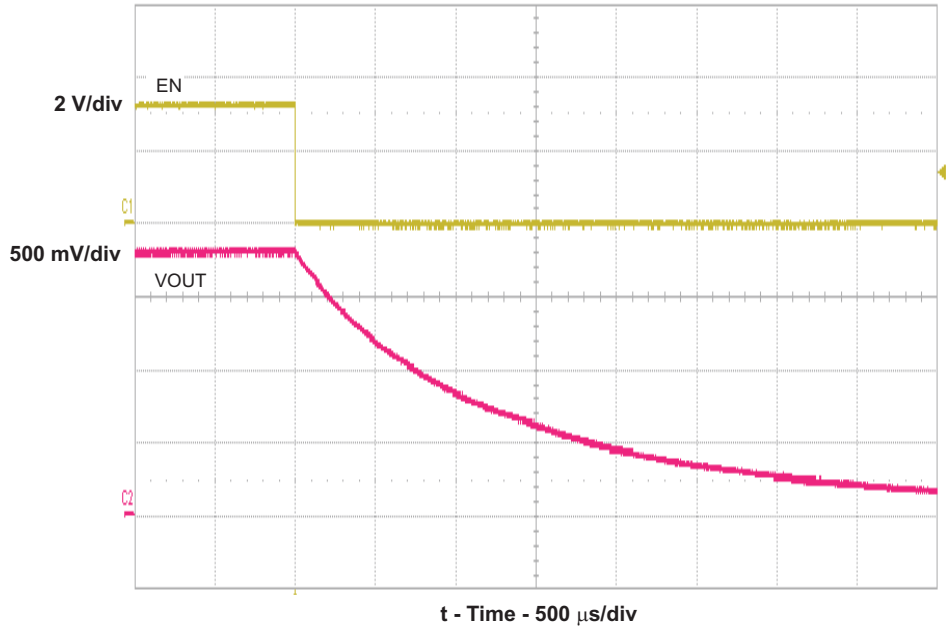
6.3 Shutdown

Figure 7 and Figure 8 illustrate the typical shutdown behavior for the TPS62060EVM.



Conditions: VIN = 3.6 V, V_{OUT} = 1.8 V

Figure 7. TPS62060 Shutdown Into 2.2-Ω Load



Conditions: VIN = 3.6 V, V_{OUT} = 1.8 V

Figure 8. TPS62060 Shutdown With No Load

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6.4 Output Voltage Ripple

Figure 9 and Figure 10 show the typical output voltage ripple for the TPS62060EVM in PFM and PWM modes, respectively.

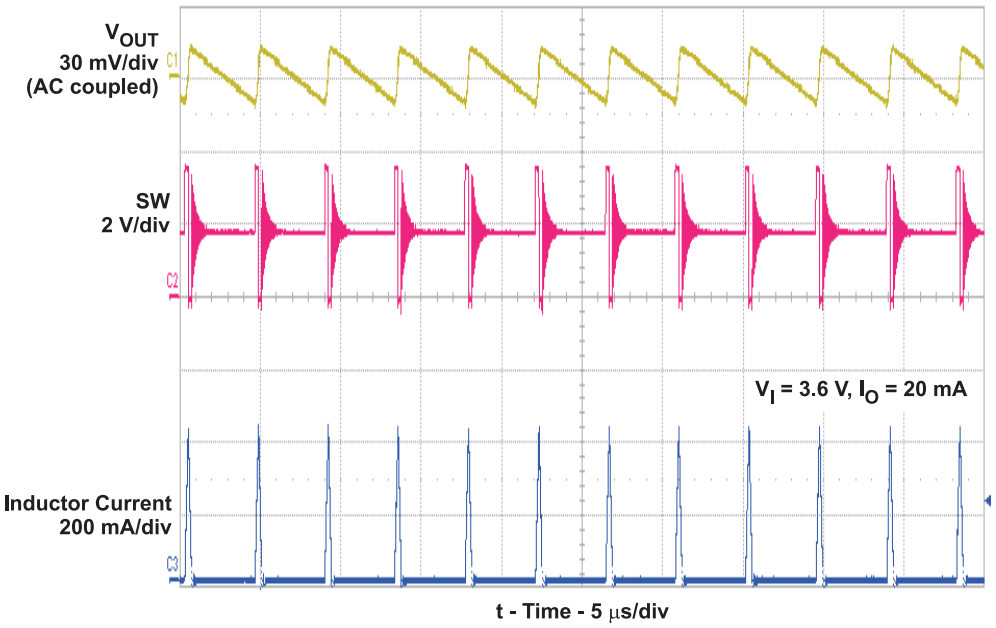


Figure 9. TPS62060 Output Voltage Ripple, PFM Mode

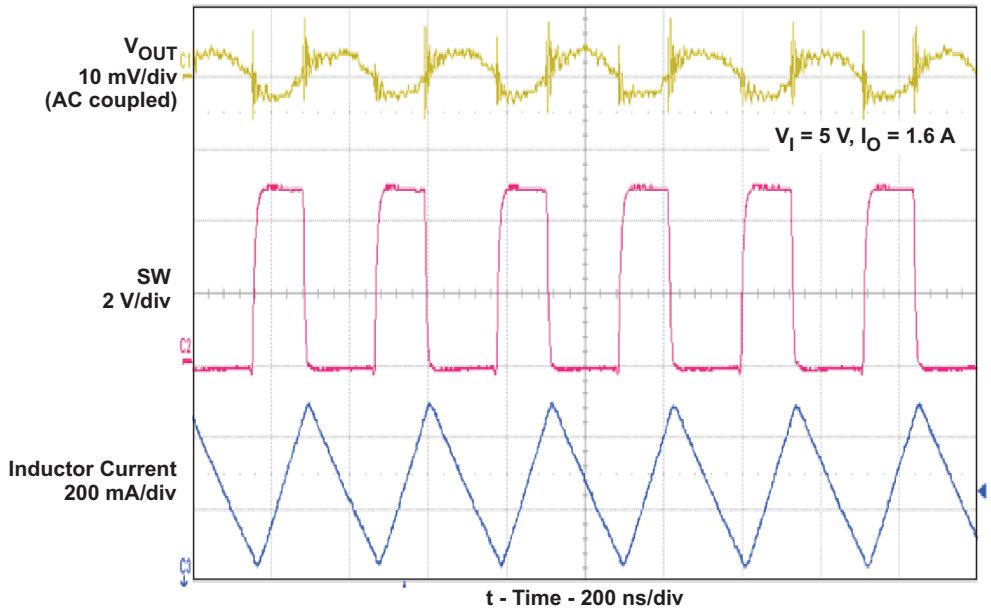


Figure 10. TPS62060 Output Voltage Ripple, PWM Mode

6.5 Input Voltage Ripple

Figure 11 shows the typical input voltage ripple for the TPS62060EVM at 3.6 V in and 1.6 A load.

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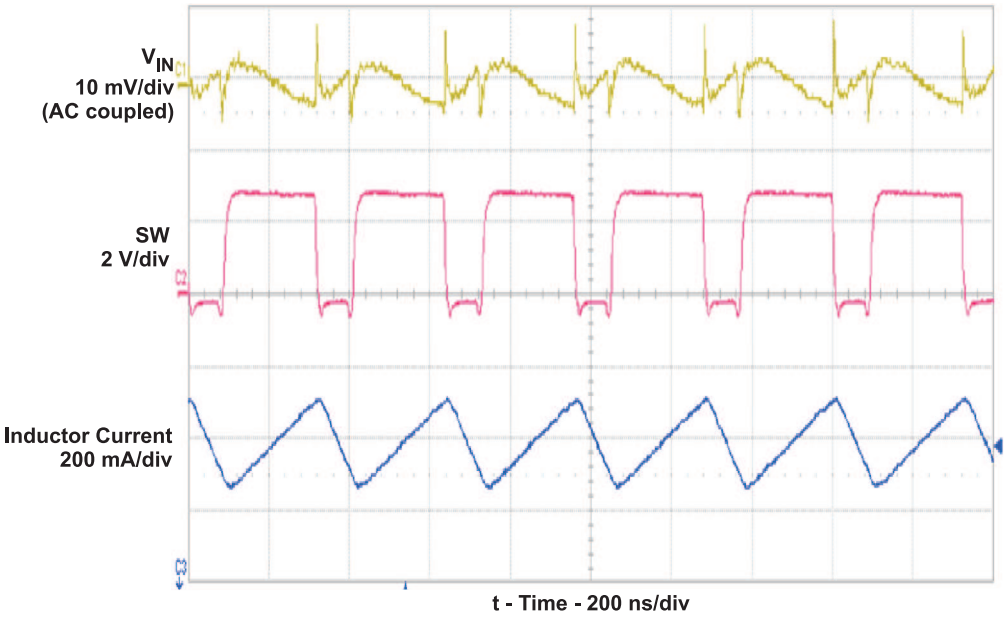
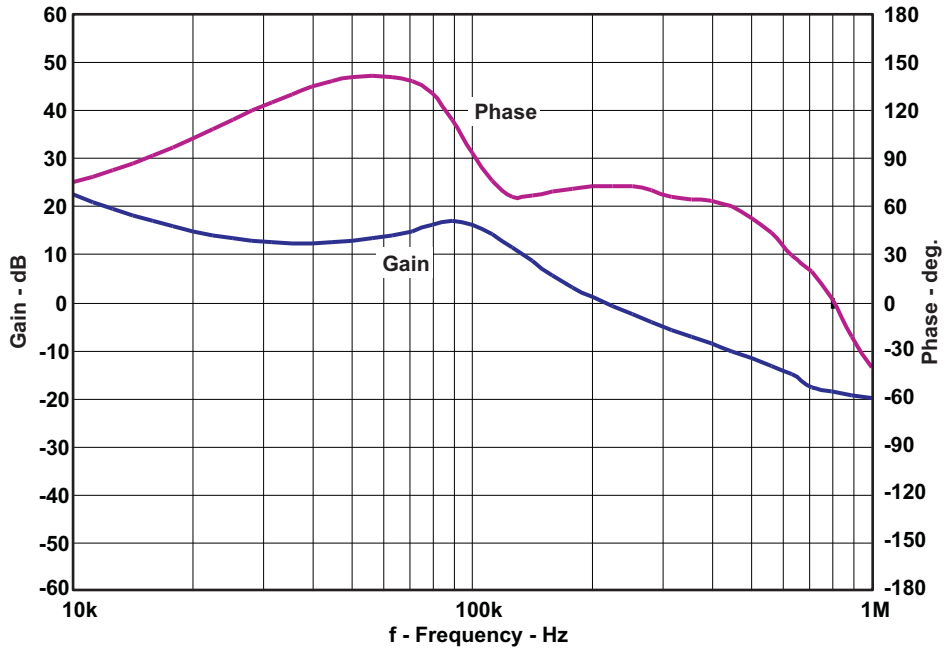


Figure 11. TPS62060 Input Voltage Ripple

6.6 Control Loop Bode Diagrams

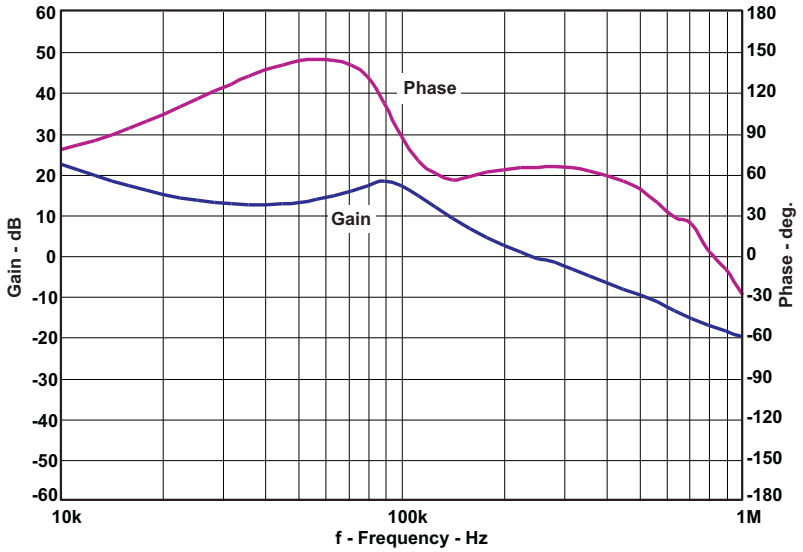
Figure 12 and Figure 13 illustrate typical TPS62060EVM gain and phase performance versus frequency at VIN = 3.6 V and 5 V, respectively.



Conditions: VIN = 3.6 V, VOUT = 1.8 V, I_{OUT} = 1.6 A; bandwidth: 213 kHz, phase margin: 73°

Figure 12. TPS62060 Gain and Phase vs Frequency

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Conditions: VIN = 5 V, VOUT = 1.8 V, I_{OUT} = 1.6 A; bandwidth: 241 kHz, phase margin: 66°

Figure 13. TPS62060 Gain and Phase vs Frequency

6.7 Transient Performance

Figure 14 and Figure 15 show the load transient response of the TPS62060EVM in PFM and PWM modes, respectively.

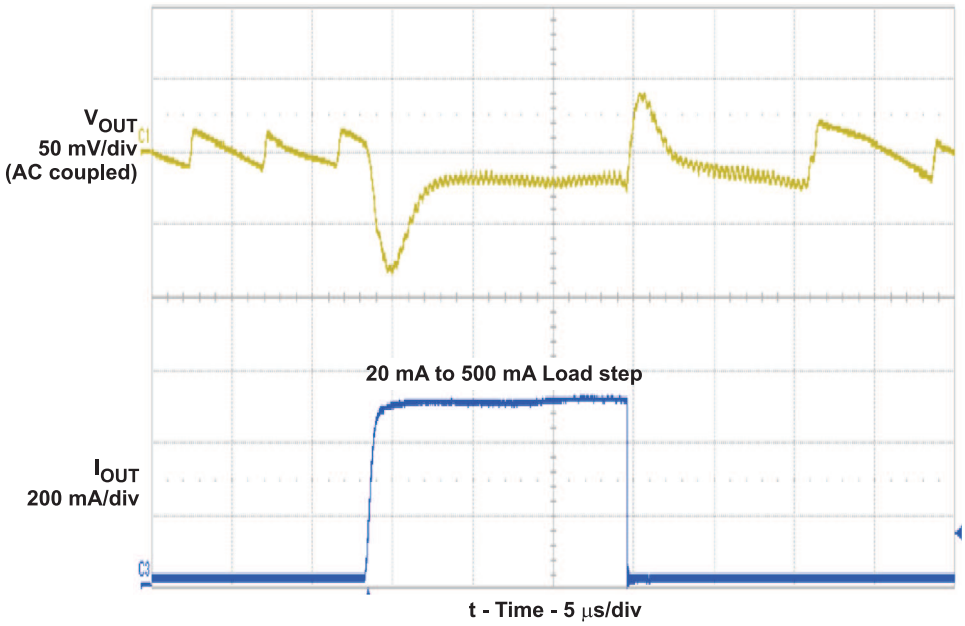


Figure 14. TPS62060 Transient Response, PFM Mode

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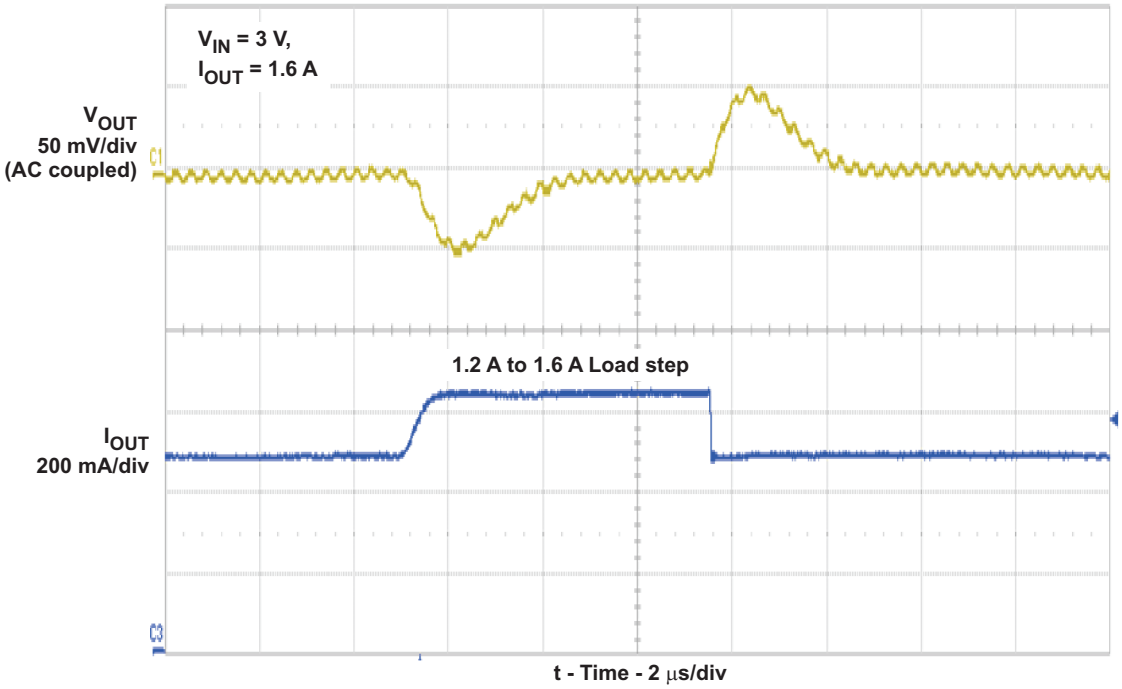


Figure 15. TPS62060 Transient Response, PWM Mode

7 TPS62060EVM Thermal Performance

Figure 16 shows a thermal picture of the TPS62060EVM operating at the full rated load of 1.6 A at an input voltage of 3 V.

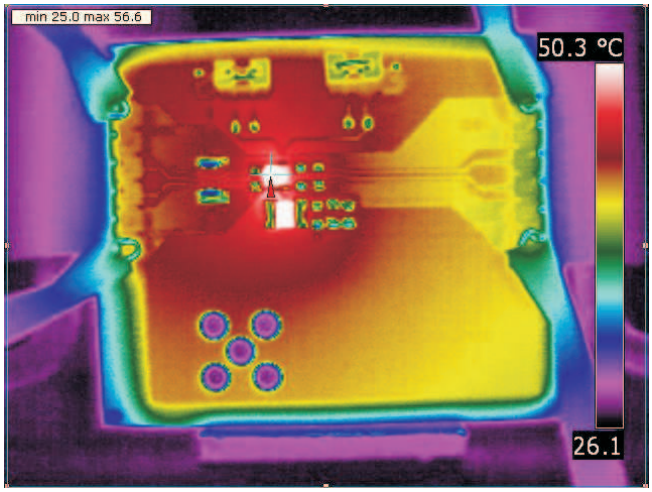


Figure 16. TPS62060EVM Thermal Performance

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8 TPS62060EVM Assembly Drawings and Layout

Figure 17 through Figure 21 show the design of the TPS62060EVM-663 printed-circuit board. This EVM has been designed using a four-layer, 1-ounce, copper-clad PCB (1.8 in.by 1.5 in.) with all components in an active area on the top side of the board. All active traces are routed on the top and bottom layers to allow the user to easily view, probe, and evaluate the TPS62060 control integrated circuit (IC) in a practical, double-sided application environment. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS62060EVM-663 PCBs.

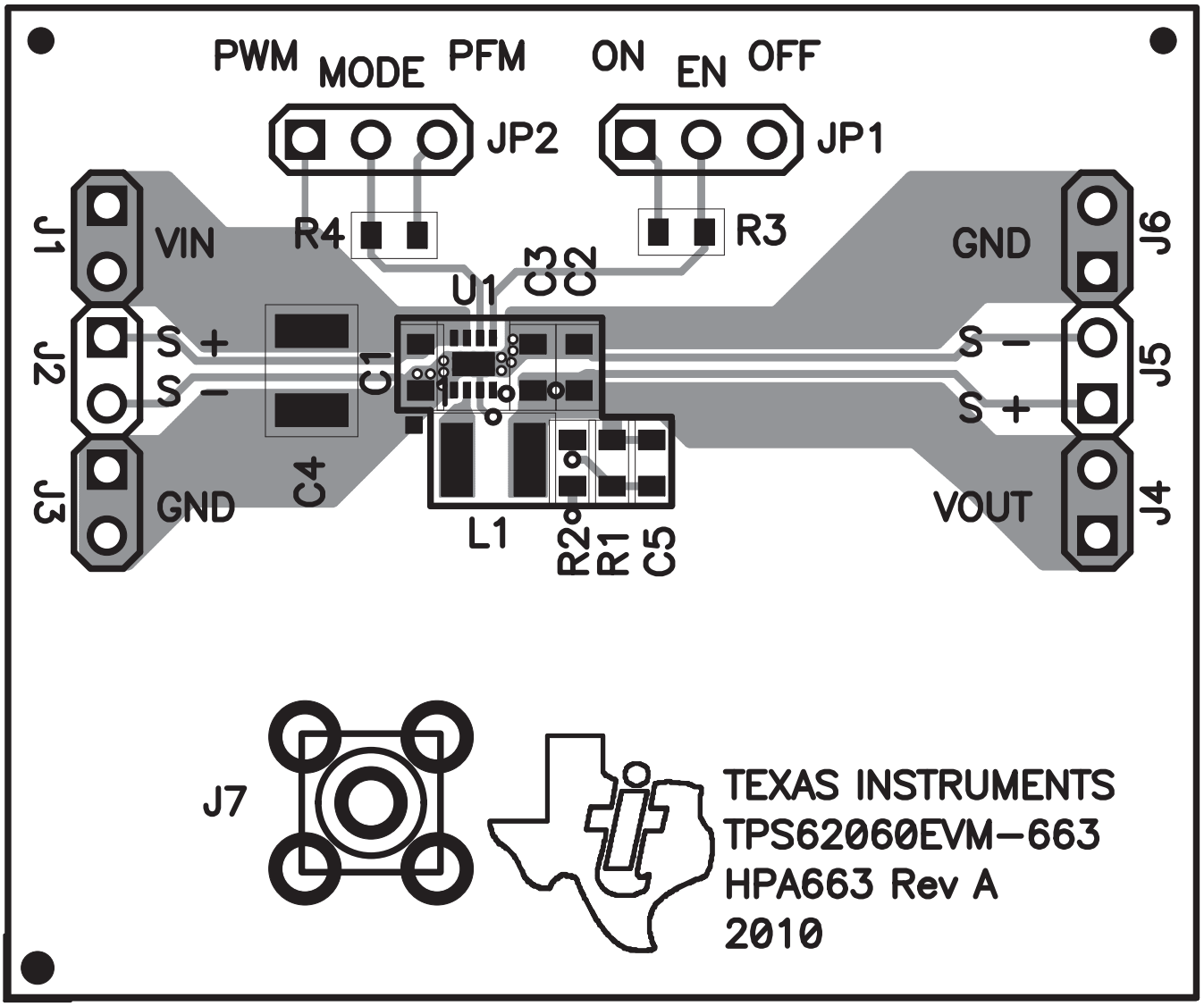


Figure 17. TPS62060EVM Component Placement, Top View

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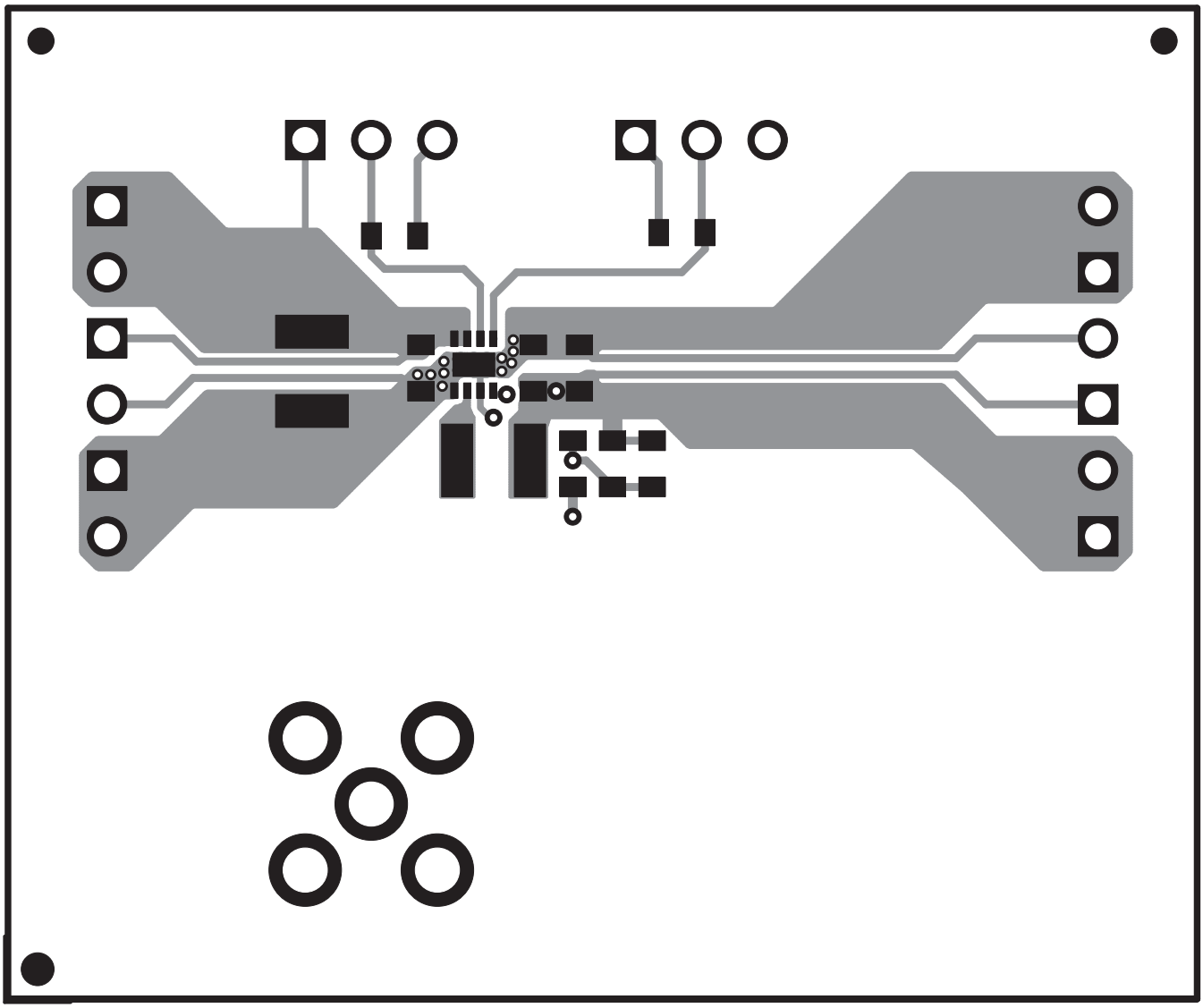


Figure 18. TPS62060EVM Top-Side Copper, Top View

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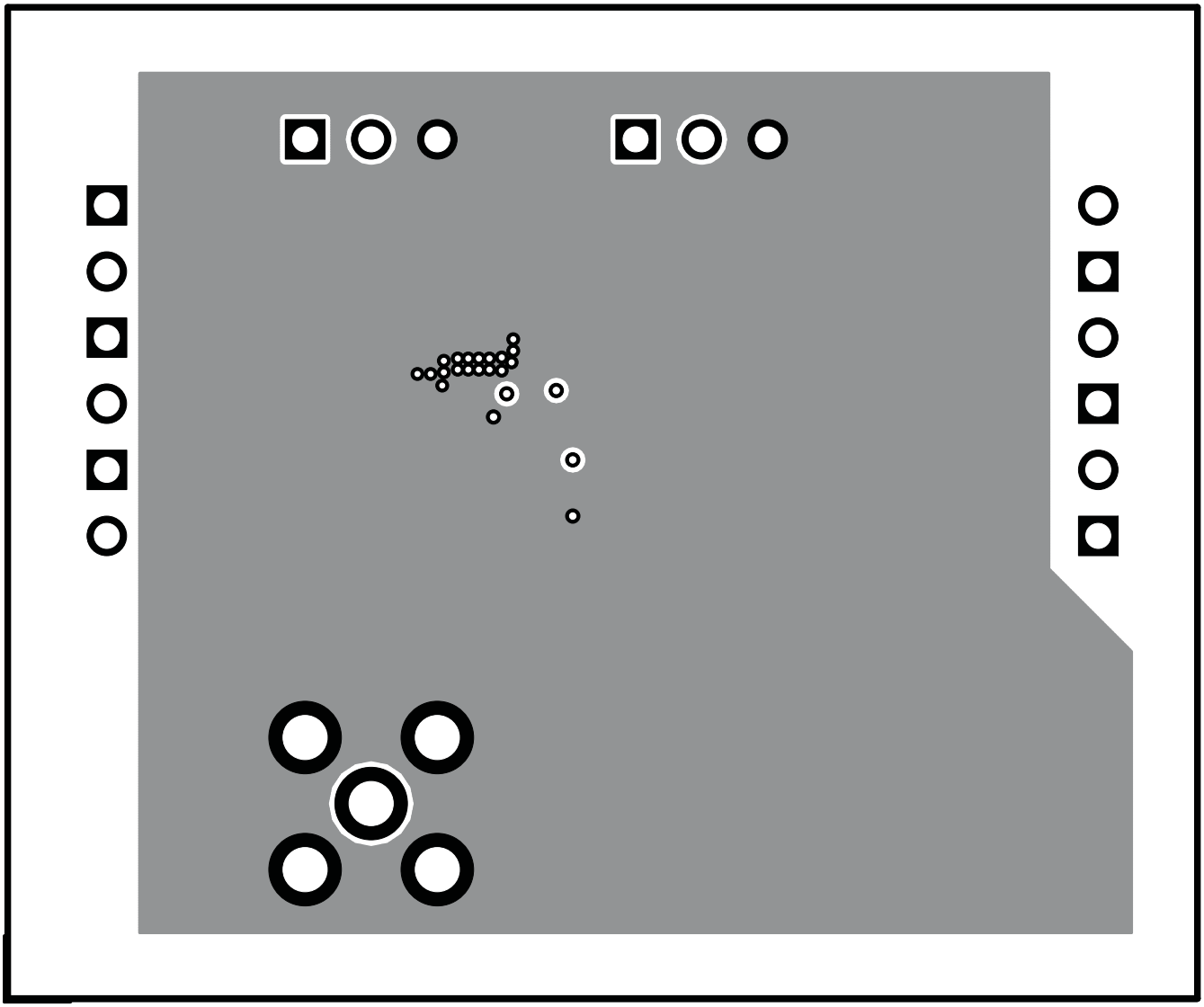


Figure 19. TPS62060EVM Internal Layer 1, X-Ray View From Top

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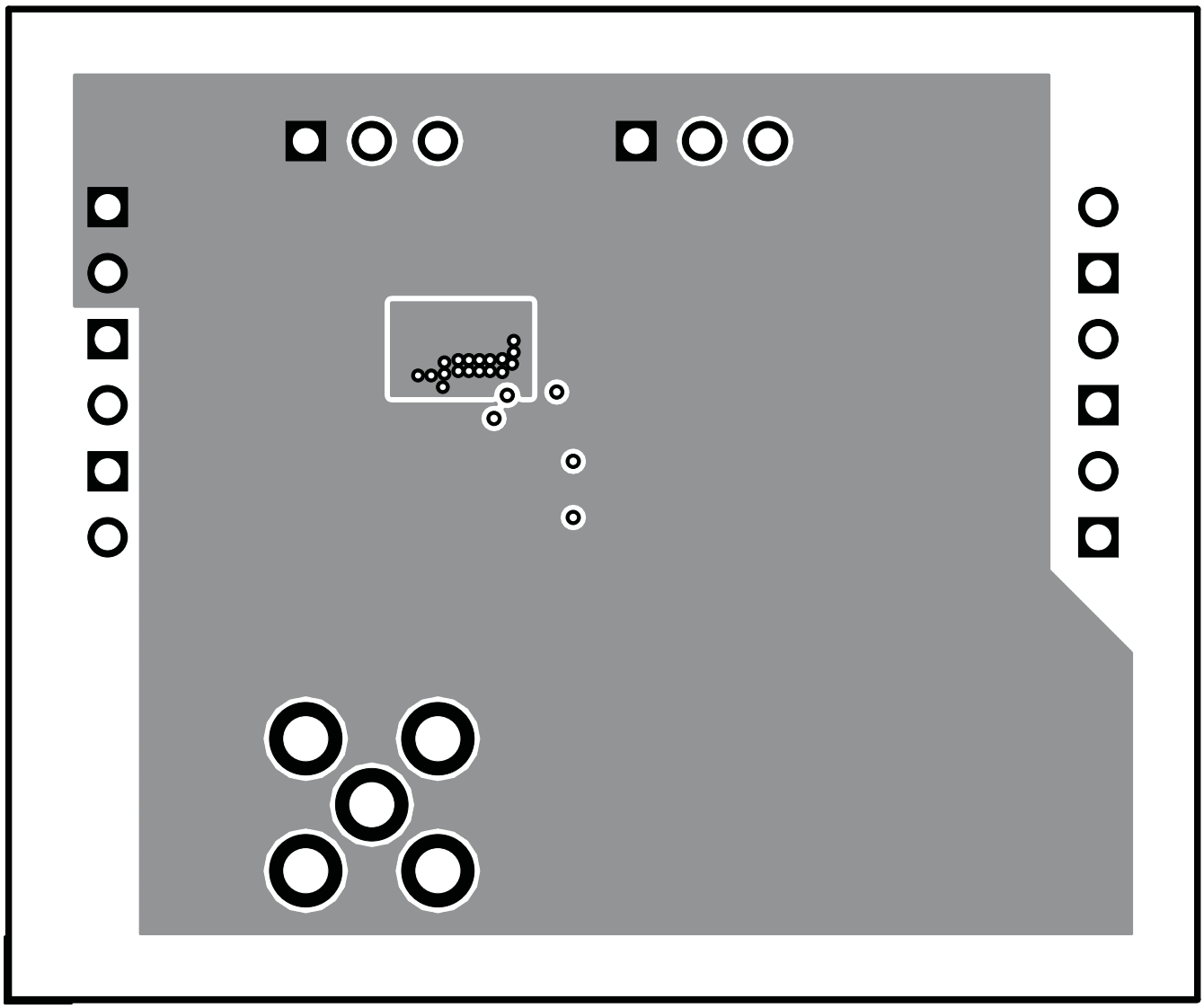


Figure 20. TPS62060EVM Internal Layer 2, X-Ray View From Top

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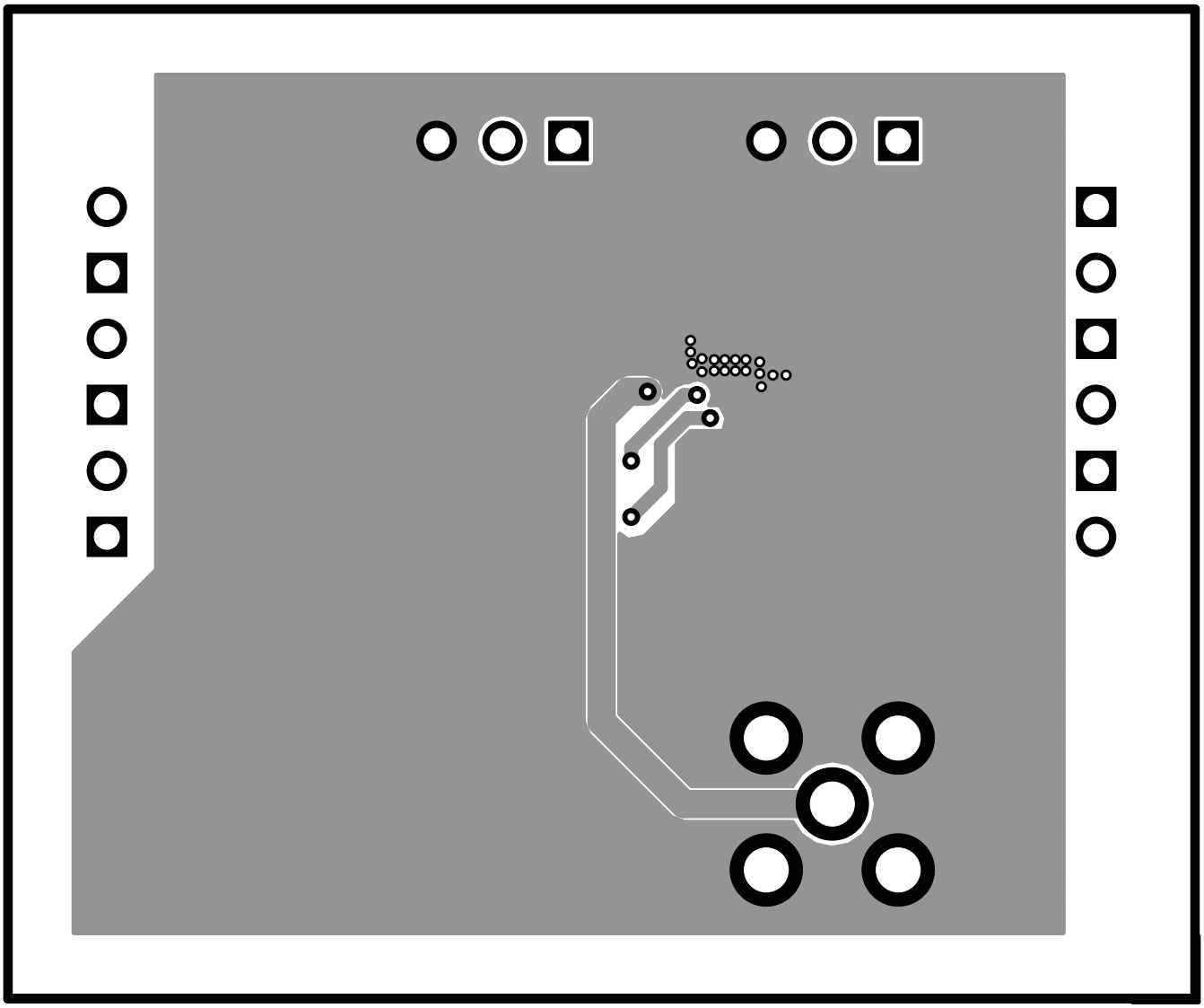


Figure 21. TPS62060EVM Bottom-Side Copper, Bottom View

9 Bill of Materials

Table 2 lists the bill of materials for the TPS62060EVM.

Table 2. TPS62060EVM Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C2	10uF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	Std	Std
1	C4	22uF	Capacitor, Ceramic, 10V, X5R, 20%	1210	Std	Std
1	C5	22pF	Capacitor, Ceramic, 50V, NPO, 5%	0603	Std	Std
1	L1	1.0 uH	Inductor, SMT Multi-layer, 1.8A, 40 milliohm	3225	MIPS3225D1R0	FDK
1	R1	360k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	180k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R3, R4	1.00M	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS62060DSG	IC, Step-Down Converter, 3MHz, 1.6A	SON-8	TPS62060DSG	TI

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2.7 V to 6 V and the output voltage range of 0.8 V to 6 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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