TEXAS INSTRUMENTS

TPS6200xEVM

Low-Power, DC-DC EVM for High-Efficiency, Step-Down Converters

User's Guide

June 2003

Power Management Products

SLVU038B

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM with an input voltage between 1.8 V and 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

About This Manual

This user's guide describes the TPS6200xEVM low-power, dc-dc evaluation module for high-efficiency, step-down converters.

How to Use This Manual

- ❑ Chapter 1 Introduction
- ❑ Chapter 2 Evaluation With the TPS6200xEVM
- ❑ Chapter 3 PCB Layout

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

- ❑ TPS62000 data sheet (literature number SLVS294)

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Chapter 1

Introduction

The Texas Instruments low-power dc-dc EVMs for high-efficiency step-down converters, TPS62000 to TPS62007, help designers evaluate these devices. The EVMs make it possible to evaluate different modes of the devices as well as the device performance.

The TPS6200x EVM is available as the TPS62000 (SLVP168–001) adjustable version set to 2.5 V and the TPS62007 (SLVP168–002), which is a fixed 3.3 V version.

If any other output voltage needs to be evaluated, the TPS62000 adjustable version can easily be set up to provide an output voltage between 0.8 V and V_I by adjusting the external resistor divider. Refer to the data sheet (SLVS294) for various fixed voltage options available for the TPS6200x. The TPS6200x has an input voltage range between 2 V and 5.5 V with an output current up to 600 mA.

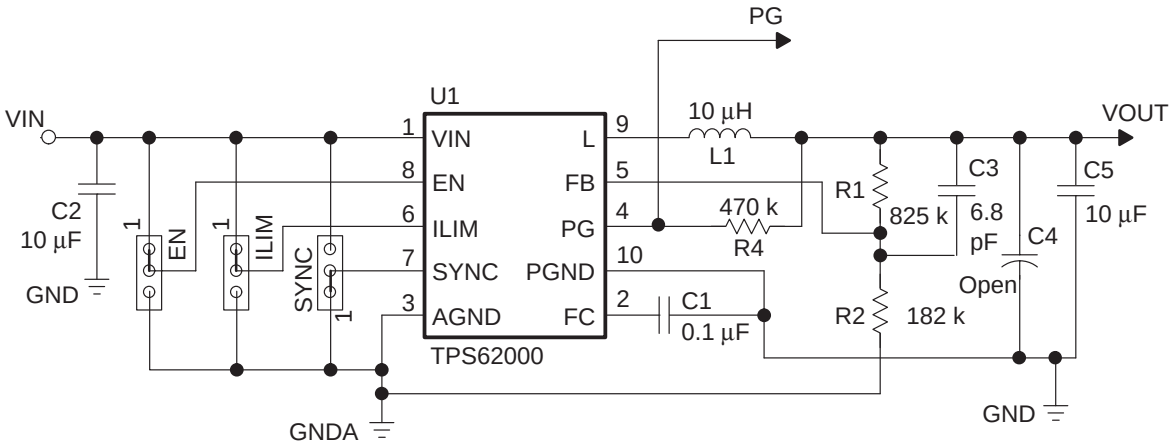
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1.1 SLVP168-001 EVM Schematic

Figure1–1 shows the SLVP168-001 EVM schematic diagram.

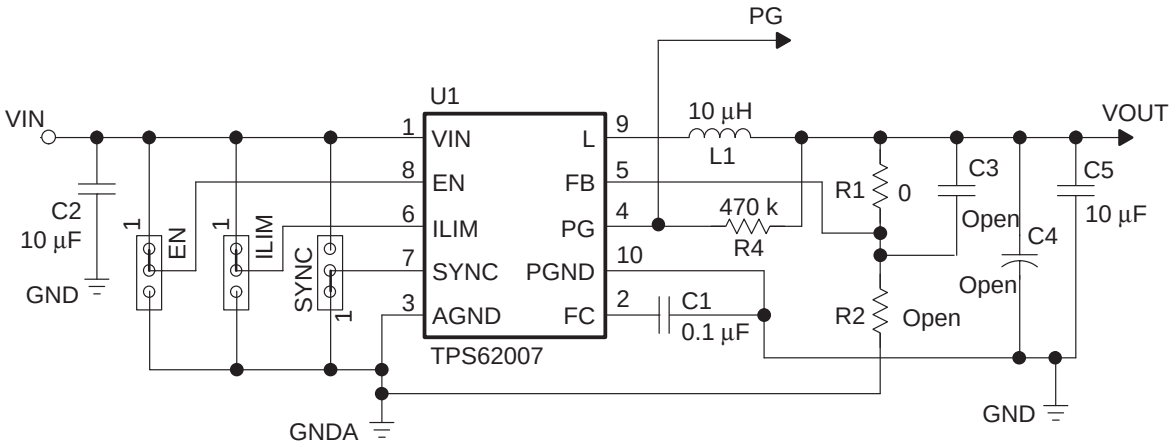
Figure 1–1. TPS62000 (SLVP168-001) EVM Schematic Diagram



1.2 SLVP168-002 EVM Schematic

Figure1–2 shows the SLVP168-002 EVM schematic diagram.

Figure 1–2. TPS62007 (SLVP168-002) EVM Schematic Diagram



1.3 SLVP168 Bill of Materials

Table 1–1 lists materials required for the SLVP168 EVM.

Table 1–1. SLVP168 EVM Bill of Materials

Ref Des	–001	–002	Description	Size	Manufacturer	Part Number
C1	1	1	Capacitor, ceramic, 0.1-µF, 16-V, X7R, 10%	1206	muRata	GRM319R71C104KA01
C2, C5	2	2	Capacitor, ceramic, 10-µF, 6.3 V, X5R, 10%	1206	Taiyo Yuden	JMK316BJ106KL
C3	1	0	Capacitor, ceramic, 6.8-pF, 50-V, C0G, 10%	805	muRata	GRM2165C1H6R8DD01
C4	0	0	Open			
JP1, JP2, JP3	3	3	Header, 3-pin, 100 mil spacing (36-pin strip)	0.100 x 3	Sullins	PTC36SAAN
L1	1	1	Inductor, 10 µH, 1.3-A, 65 mΩ		Sumida	CDRH5D28–100
R1	1	0	Resistor, chip, 825-kΩ, 1/16-W, 1%	1206	Std	Std
	0	1	Resistor, chip, 0-Ω, 1/16-W, 1%	1206	Std	Std
R2	1	0	Resistor, chip, 182-kΩ, 1/16-W, 1%	1206	Std	Std
R4	1	1	Resistor, chip, 470-kΩ, 1/16-W, 5%	1206	Std	Std
VIN, VOUT, PG	3	3	Test point, red, 1 mm	0.038	Farnell	240–345
GND, GNDA	2	2	Test point, black, 1 mm	0.038	Farnell	240–333
U1	1	0	IC, high-efficiency, step-down converter, adj V	DGS10	TI	TPS62000DGS
	0	1	IC, high-efficiency, step-down converter, 3.3-V	DGS10	TI	TPS62007DGS
	1	1	PCB		Any	SLVP168
	3	3	Shunt, 100-mil, black	0.100	3M	929950–00

1.4 EVM Ordering Information

Table 1–2. EVM Ordering Information

EVM Number	Description
TPS62000EVM-168	Adjustable output voltage version set to 2.5 V
TPS62007EVM-168	3.3-V Fixed output voltage version

1.5 Setup of the EVMs

It is important to establish all connections to the EVM before the power supply connected to the EVM is turned on.

1) Connect a power supply (2 V to 5.5 V, depending on the output voltage of the EVM) to the VIN pin and GND pin.
2) Connect a voltmeter to the VOUT pin and the GND1 pin.
3) Verify that the jumper, EN, is across pin 1 and pin 2.
4) Verify that the jumper, ILIM, is across pin 1 and pin 2.
5) Verify that the jumper, SYNC, is across pin 1 and pin 2.
6) Turn on the power supply and verify the output voltage.

Chapter 2

Evaluation With the TPS6200xEVM

This chapter details the evaluation process and features of the EVM. For this purpose, a load is connected to the output pin VOUT and GND1, which allows the load current to be adjusted between 0 mA and 600 mA.

For accurate output voltage and input voltage measurements, it is important to measure the voltage on the input and output voltage terminals with kelvin contacts or with a voltmeter connected directly to the input voltage or output voltage terminals. This eliminates any measurement errors related to voltage drops along the input and output terminal wires connected to the power supply or load.

The EVM has additional pads to allow the user to assemble an additional output capacitor, C4, onto the PCB for further evaluation purposes.

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2.1 Enable (EN) Jumper

This jumper is used to enable the device. Connecting the EN pin to VIN (e.g. set jumper, EN, across pin 1 and pin 2) enables the part.

2.2 Synchronization (SYNC) Jumper

This jumper is used to force the device into low noise fixed frequency pulse width modulation (PWM) mode by setting the jumper across pin 2 and pin 3. Setting the jumper across pin 1 and pin 2 enables the power save mode where the device enters a pulse frequency modulation mode (PFM) at light to medium load currents, thus reducing quiescent current and switching frequency to a minimum to achieve highest efficiency over the entire load current range. The operation of the different modes can be best observed by monitoring the L pin (pin 9), which is connected to the inductor.

Additionally an external clock between 500 kHz and 1 MHz with a CMOS logic level signal can be applied to pin 2 in order to synchronize the converter to an external clock.

2.3 Current Limit (ILIM) Jumper

Connecting the jumper across pin 1 and pin 2 will force the device to operate with a typical switch current limit of 1200 mA. Connecting the jumper across pin 2 and pin 3 forces a typical switch current limit 600 mA for low current applications. This reduces the short circuit current and allows the use of the smallest inductor size.

2.4 Power Good (PG) Pin

The PG pin is an open drain output with a pullup resistor, R4, connected to the output. The signal on this pin goes high as soon as the output voltage is greater than typically 94.5% of the nominal voltage. The signal goes low as soon as the output voltage falls below typically 92% of the nominal value.

Chapter 3

PCB Layout

As for all switch mode power supplies, the PCB layout is a very important step in the power supply design process. The following figures show the layout for the adjustable and fixed output voltage EVMs. Please refer to the data sheet (SLVS294) for further layout guidelines.

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3.1 PCB Layout

Figure 3–1. Component Placement

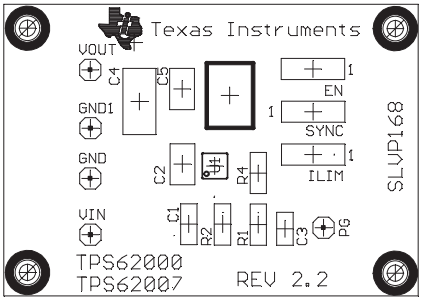
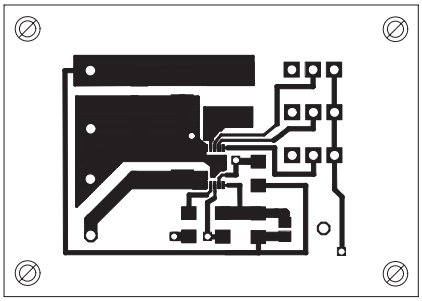
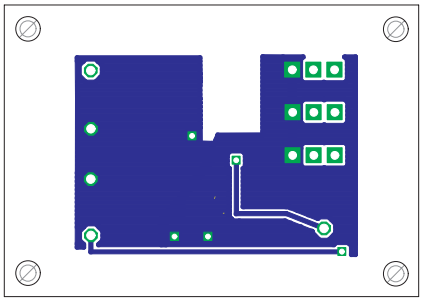


Figure 3–2. Top and Bottom Layers



TOP LAYER



BOTTOM LAYER