TPS61194 High-Performance Four-Channel LED Driver

1 Features

- Input Voltage Operating Range 4.5 V to 40 V
- Four High-Precision Current Sinks
  - Current Matching 1% (Typical)
  - LED String Current up to 100 mA per Channel
  - Outputs can be Combined Externally for Higher Current per String
- High Dimming Ratio of 10 000:1 at 100 Hz
- Integrated Boost/SEPIC Converter for LED String Power
  - Output Voltage up to 45 V
  - Switching Frequency 300 kHz to 2.2 MHz
  - Switching Synchronization Input
  - Spread Spectrum for Lower EMI
- Extensive Fault Detection Features
  - Fault Output
  - Input Voltage OVP and UVLO
  - Open and Shorted LED Fault Detection
  - Thermal Shutdown
- Minimum Number of External Components

2 Applications

- Industrial Backlighting Systems in Control Panels
- Industrial PC
- Test and Measurement Equipment

3 Description

The TPS61194 is a high-efficiency, low-EMI, easy-to-use LED driver with flexibility to support a wide range of applications. It has four high-precision current sinks that can be combined for higher current capability.

The TPS61194 has an integrated DC-DC supporting both boost and SEPIC mode operation. The converter has adaptive output voltage control based on the LED current sink headroom voltages. This feature minimizes the power consumption by adjusting the voltage to lowest sufficient level in all conditions. For EMI control the DC-DC converter supports spread spectrum for switching frequency and an external synchronization with dedicated pin.

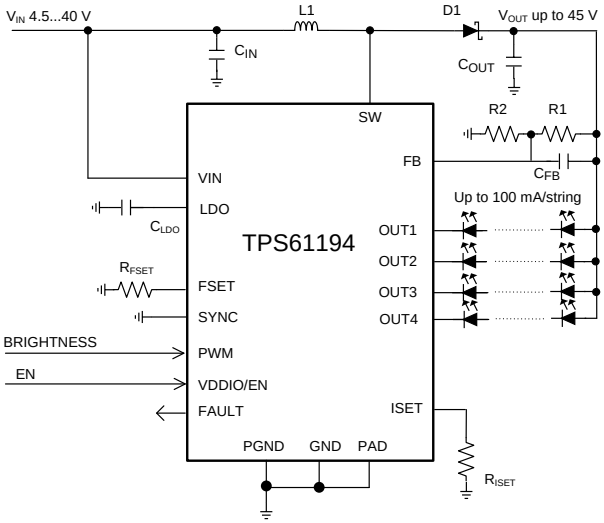
The TPS61194 has wide input voltage range from 4.5 V to 40 V for robust support of different types of applications. The TPS61194 integrates extensive fault detection features. The device supports PWM brightness dimming ratio of 10 000:1 for 100-Hz input PWM frequency.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61194	HTSSOP (20)	6.50 mm × 4.40 mm

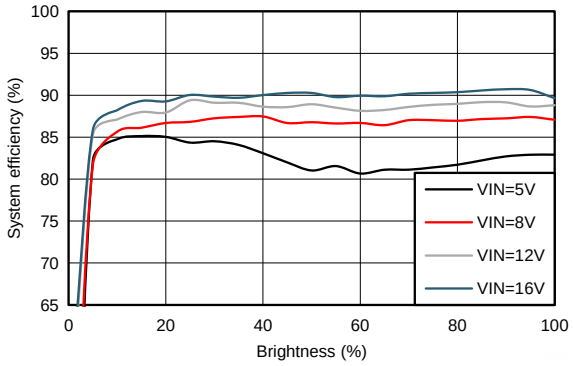
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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System Efficiency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2016) to Revision C — **Page**

- Enhanced pin descriptions for pins 3, 10 and 16 in *Pin Functions* ... 3
- Deleted "I_{OUT} = 100 mA" from $t_{ON/OFF}$ row of Table 7.9 ... 6
- Changed "0.5" from MAX to TYP column in $t_{ON/OFF}$ row of Table 7.9 ... 6
- Added table note 1 for Tables 7.9 and 7.10 ... 6
- Deleted "Initial DC-DC voltage is about 88% of $V_{MAX\ BOOST}$." from *Integrated DC-DC Converter*; change wording in last sentence before equation 1. ... 12
- Changed eq. 1; added "K" eq definitions for eq. 1 and paragraph after Fig. 9 ... 12
- Added new paragraph before *Internal LDO* ... 14
- Deleted "Dimming ratio is calculated as ratio between the input PWM period and minimum on/off time (0.5 µs). " from *Brightness Control* ... 14

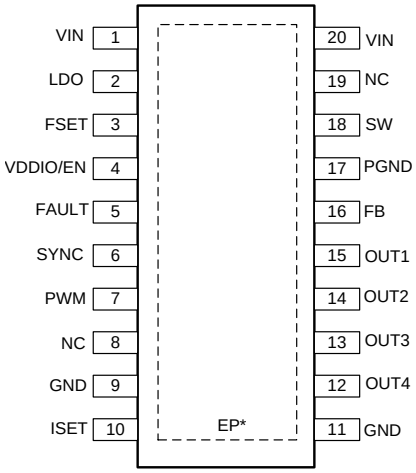
Changes from Revision A (January 2016) to Revision B — **Page**

- Deleted wording of several items in *Features* ... 1
- Changed "Output Current" to "LED String Current" and "High Dimming Ratio of 10 000:1 at 200 Hz" to "High Dimming Ratio of 10 000:1 at 100 Hz" ... 1
- Deleted last sentence in first para of *Description* - moved to last sentence of last para ... 1
- "PWM brightness dimming ratio of 10 000:1 for 200-Hz" to "PWM brightness dimming ratio of 10 000:1 for 100-Hz" ... 1
- Added footnotes to *ESD Ratings* ... 4
- Added 2 new LED Current graphs ... 9

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5 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP With Exposed Thermal Pad
Top View



*EXPOSED PAD

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VIN	A	Input power pin
2	LDO	A	Output of internal LDO; connect a 1-μF decoupling capacitor between this pin and noise-free GND.
3	FSET	A	Boost or SEPIC switching frequency setting resistor; for normal operation, resistor value from 24 kΩ to 219 kΩ must be connected between this pin and ground.
4	VDDIO/EN	I	Enable input for the device as well as supply input (VDDIO) for digital pins
5	FAULT	OD	Fault signal output. If unused, the pin may be left floating.
6	SYNC	I	Input for synchronizing boost. If synchronization is not used, connect this pin to GND to disable spread spectrum or to VDDIO/EN to enable spread spectrum.
7	PWM	I	PWM dimming input.
8	NC	—	No connect
9	GND	G	Ground.
10	ISET	A	LED current setting resistor; for normal operation, resistor value from 24 kΩ to 129 kΩ must be connected between this pin and ground.
11	GND	G	Ground
12	OUT4	A	Current sink output This pin must be connected to GND if not used.
13	OUT3	A	Current sink output This pin must be connected to GND if not used.
14	OUT2	A	Current sink output This pin must be connected to GND if not used.
15	OUT1	A	Current sink output This pin must be connected to GND if not used.
16	FB	A	Boost or SEPIC feedback input; for normal operation this pin must be connected to the middle of a resistor divider between V_{OUT} and ground using feedback resistor values from 5 kΩ to 150 kΩ.
17	PGND	G	DC-DC (boost or SEPIC) power ground
18	SW	A	DC-DC (boost or SEPIC) switch pin
19	NC	A	No connect
20	VIN	A	Input power pin

(1) A: Analog pin, G: Ground pin, P: Power pin, I: Input pin, I/O: Input/Output pin, O: Output pin, OD: Open Drain pin

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Voltage on pins	VIN, SW, FB	–0.3	50	V
	OUT1, OUT2, OUT3, OUT4	–0.3	45	
	LDO, SYNC, FSET, ISET, PWM, VDDIO/EN, FAULT	–0.3	5.5	
Continuous power dissipation(3)		Internally Limited		
Ambient temperature range T_A(4)		–40	125	°C
Junction temperature range T_J(4)		–40	150	°C
Maximum lead temperature (soldering)			See(5)	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typical) and disengages at T_J = 145°C (typical).
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 150°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.
(5) For detailed soldering specifications and information, refer to the *PowerPAD™ Thermally Enhanced Package* .

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per JESD22-A114, JS-001(1)		±2000	V
		Charged-device model (CDM), per JESD22-C101(2)	All other pins	±500	
			Corner pins (1,10,11,20)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on pins	VIN	4.5	45	V
	SW	0	45	
	OUT1, OUT2, OUT3, OUT4	0	40	
	FB, FSET, LDO, ISET, VDDIO/EN, FAULT	0	5.25	
	SYNC, PWM	0	VDDIO/EN	

(1) All voltages are with respect to the potential at the GND pins.

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6.4 Thermal Information

THERMAL METRIC(1)		TPS61194 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	44.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.2	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

6.5 Electrical Characteristics(1)(2)

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Standby supply current	Device disabled, $V_{VDDIO/EN}$ = 0 V, V_{IN} = 12 V		4.5	20	µA
	Active supply current	V_{IN} = 12 V, V_{OUT} = 26 V, output current 80 mA/channel, converter f_{SW} = 300 kHz		5	12	mA
V_{POR_R}	Power-on reset rising threshold	LDO pin voltage			2.7	V
V_{POR_F}	Power-on reset falling threshold	LDO pin voltage	1.5			V
T_{TSD}	Thermal shutdown threshold		150	165	175	°C
T_{TSD_HYST}	Thermal shutdown hysteresis			20		°C

(1) All voltages are with respect to the potential at the GND pins.
(2) Minimum and maximum limits are specified by design, test, or statistical analysis.

6.6 Internal LDO Electrical Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LDO}	Output voltage	V_{IN} = 12 V	4.15	4.3	4.55	V
V_{DR}	Dropout voltage		120	300	430	mV
I_{SHORT}	Short circuit current			50		mA

6.7 Protection Electrical Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	VIN OVP threshold voltage		41	42	44	V
V_{UVLO}	VIN UVLO			4		V
V_{UVLO_HYST}	VIN UVLO hysteresis			100		mV
	LED short detection threshold		5.6	6	7	V

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6.8 Current Sinks Electrical Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKAGE}$	Leakage current	Outputs OUT1 to OUT4 , V_{OUTx} = 45 V		0.1	5	µA
I_{MAX}	Maximum current	OUT1, OUT2, OUT3, OUT4		100		mA
I_{OUT}	Output current accuracy	I_{OUT} = 100 mA	−5%		5%	
I_{MATCH}	Output current matching (1)	I_{OUT} = 100 mA, PWM duty =100%		1%	5%	
V_{SAT}	Saturation voltage (2)	I_{OUT} = 100 mA		0.4	0.7	V

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUTx), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Matching number is calculated: (MAX-MIN)/AVG. The typical specification provided is the most likely norm of the matching figure for all parts. LED current sinks were characterized with 1-V headroom voltage. Note that some manufacturers have different definitions in use.
(2) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1 V.

6.9 PWM Brightness Control Electrical Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM}	PWM input frequency		100		20 000	Hz
$t_{ON/OFF}$	Minimum on/off time (1)			0.5		µs

(1) This specification is not ensured by ATE.

6.10 Boost and SEPIC Converter Characteristics

T_J = −40°C to +125°C (unless otherwise noted).
Unless otherwise specified: V_{IN} = 12 V, $V_{EN/VDDIO}$ = 3.3 V, L = 22 µH, C_{IN} = 2 × 10-µF ceramic and 33-µF electrolytic, C_{OUT} = 2 × 10-µF ceramic and 33-µF electrolytic, D = NRVB460MFS, f_{SW} = 300 kHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5		40	V
V_{OUT}	Output voltage		6		45	
f_{SW_MIN}	Minimum switching frequency (central frequency if spread spectrum is enabled)	Defined by R_{FSET} resistor		300		kHz
f_{SW_MAX}	Maximum switching frequency (central frequency if spread spectrum is enabled)			2 200		kHz
V_{OUT}/V_{IN}	Conversion ratio				10	
T_{OFF}	Minimum switch OFF time (1)	f_{SW} ≥ 1.15 MHz			55	ns
I_{SW_MAX}	SW current limit		1.8	2	2.2	A
R_{DSON}	FET R_{DSON}	Pin-to-pin		240	400	mΩ
f_{SYNC}	External SYNC frequency		300		2 200	kHz
$t_{SYNC_ON_MIN}$	External SYNC minimum on time (1)			150		ns
$t_{SYNC_OFF_MIN}$	External SYNC minimum off time (1)			150		ns

(1) This specification is not ensured by ATE.

6.11 Logic Interface Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT VDDIO/EN						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.65			
I_I	Input current		−1	5	30	µA
LOGIC INPUT SYNC/FSET, PWM						

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Logic Interface Characteristics (continued)

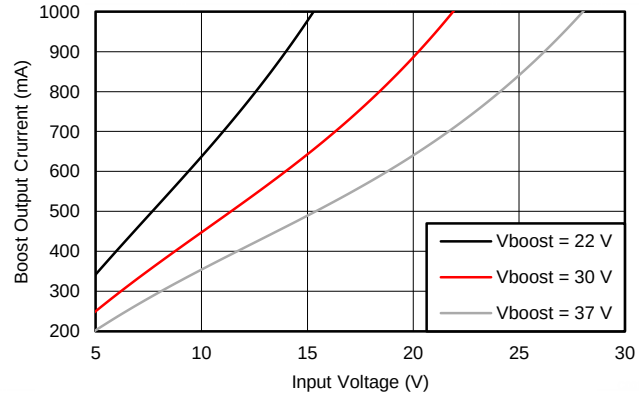
T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low level				0.2 × VDDIO/EN	V
V_{IH}	Input high level		0.8 × VDDIO/EN			
I_I	Input current		−1		1	μA
LOGIC OUTPUT FAULT						
V_{OL}	Output low level	Pullup current 3 mA		0.3	0.5	V
$I_{LEAKAGE}$	Output leakage current	V = 5.5 V			1	μA

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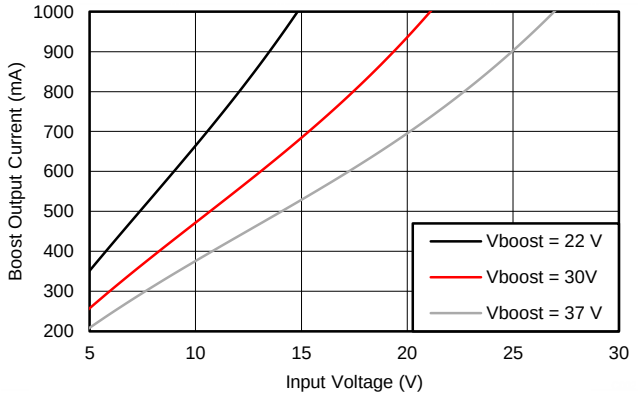
6.12 Typical Characteristics

Unless otherwise specified: D = NRVB460MFS, T = 25°C



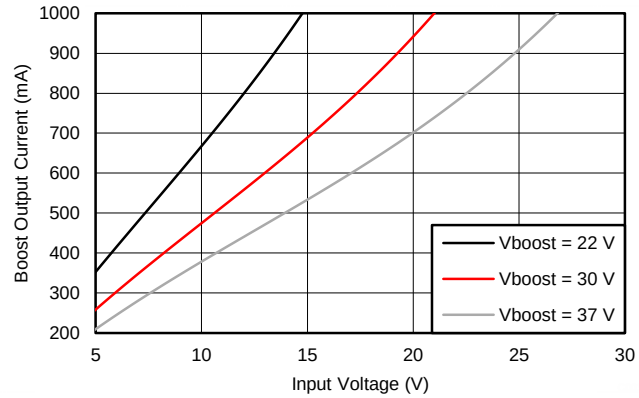
f_{SW} = 300 kHz L = 33 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 33 µF + 2 × 10 µF (ceramic)

Figure 1. Maximum Boost Current



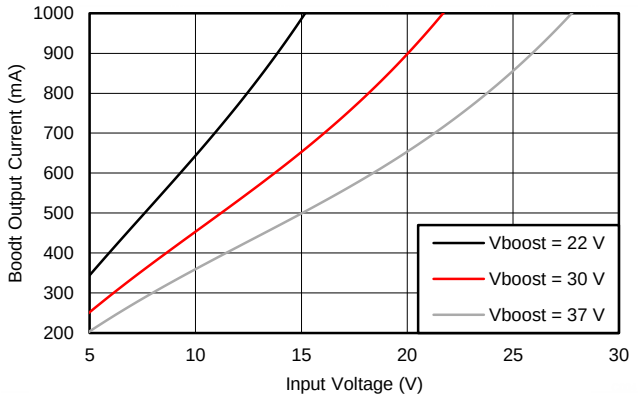
f_{SW} = 800 kHz L = 15 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 2 ×10 µF (ceramic)

Figure 2. Maximum Boost Current



f_{SW} = 1.5 MHz L = 8.2 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 2 × 10 µF (ceramic)

Figure 3. Maximum Boost Current



f_{SW} = 2.2 MHz L = 4.7 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 2 × 10 µF (ceramic)

Figure 4. Maximum Boost Current

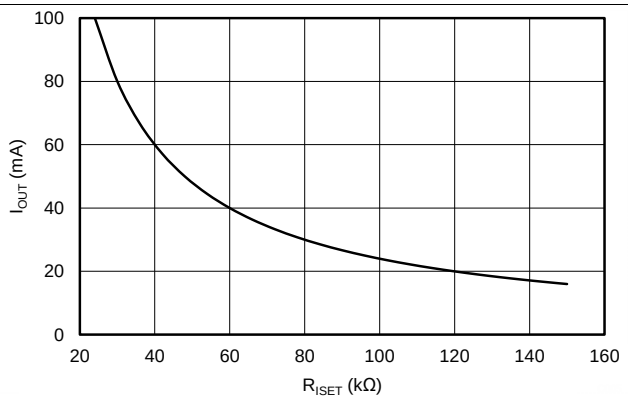


Figure 5. LED Current vs R_{ISET}

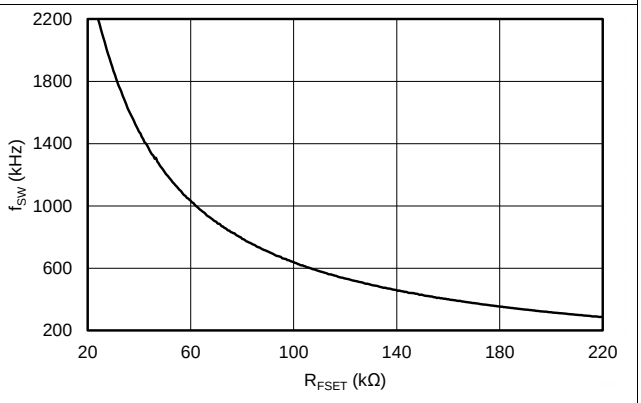


Figure 6. Boost Switching Frequency f_{SW} vs R_{FSET}

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Typical Characteristics (continued)

Unless otherwise specified: D = NRVB460MFS, T = 25°C

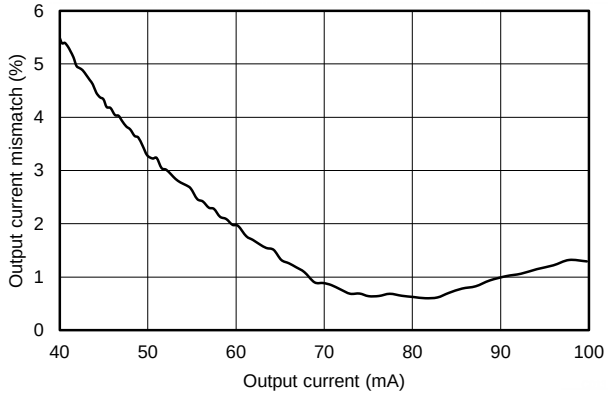
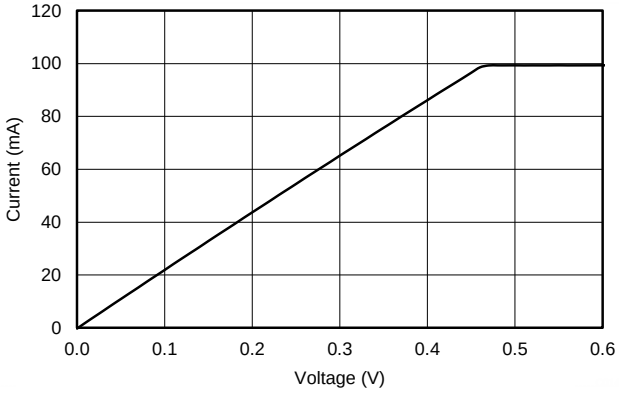


Figure 7. LED Current Sink Matching



R_{ISET} = 24 kΩ

Figure 8. LED Current Sink Saturation Voltage

7 Detailed Description

7.1 Overview

The TPS61194 is a highly integrated LED driver for medium-sized LCD backlight applications. It includes a DC-DC with an integrated FET, supporting both boost and SEPIC modes, an internal LDO enabling direct connection to battery without need for a pre-regulated supply and four LED current sinks. The VDDIO/EN pin provides the supply voltage for digital IOs (PWM and SYNC inputs) and at the same time enables the device.

The switching frequency on the DC-DC converter is set by a resistor connected to the FSET pin. The maximum voltage of the DC-DC is set by a resistive divider connected to the FB pin. For the best efficiency the output voltage is adapted automatically to the minimum necessary level needed to drive the LED strings. This is done by monitoring LED output voltage drop in real time. For EMI reduction and control two optional features are available:

- Spread spectrum, which reduces EMI noise around the switching frequency and its harmonic frequencies
- DC-DC can be synchronized to an external frequency connected to SYNC pin

The four constant current outputs OUT1, OUT2, OUT3, and OUT4 provide LED current up to 100 mA.Value for the current per OUT pin is set with a resistor connected to ISET pin. Current sinks that are not used must be connected to ground. Grounded current sink is disabled and excluded from adaptive voltage detection loop.

Brightness is controlled with the PWM input. Frequency range for the input PWM is from 100 Hz to 20 kHz. LED output PWM follows the input PWM so the output frequency is equal to the input frequency.

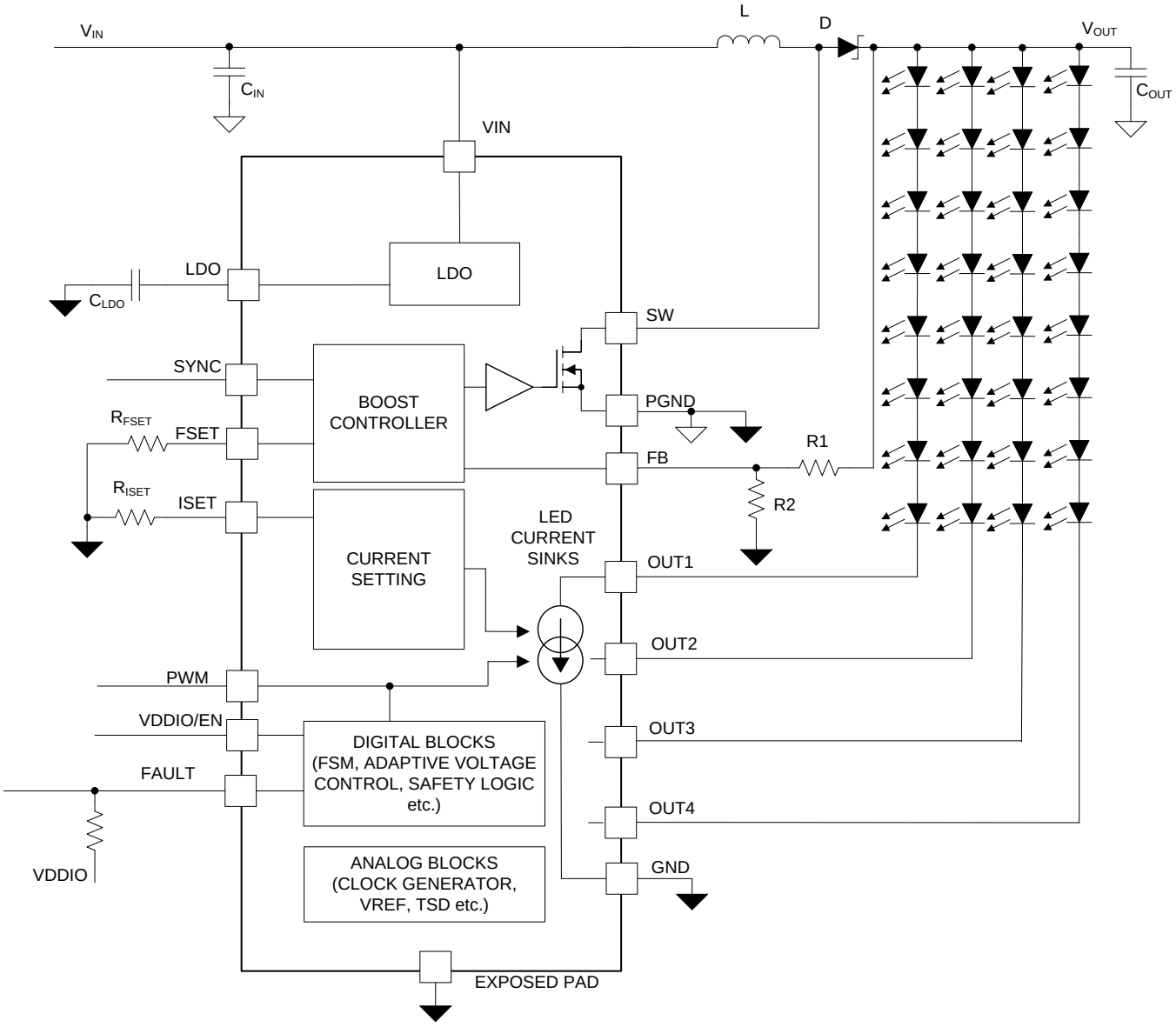
TPS61194 has extensive fault detection features :

- Open-string and shorted LED detections
  - LED fault detection prevents system overheating in case of open or short in some of the LED strings
- V_{IN} input overvoltage protection
  - Threshold sensing from VIN pin
- V_{IN} input undervoltage protection
  - Threshold sensing from VIN pin
- Thermal shutdown in case of die overtemperature

Fault condition is indicated through the FAULT output pin.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integrated DC-DC Converter

The TPS61194 DC-DC converter generates supply voltage for the LEDs and can operate in boost mode or in SEPIC mode. The maximum output voltage V_{OUT_MAX} is defined by an external resistive divider (R1, R2).

V_{OUT_MAX} voltage should be chosen based on the maximum voltage required for LED strings. Recommended maximum voltage is about 30% higher than maximum LED string voltage. DC-DC output voltage is adjusted automatically based on LED current sink headroom voltage. Maximum, minimum, and initial boost voltages can be calculated with Equation 1:

$$V_{BOOST} = \left(\frac{V_{BG}}{R2} + K \times 0.0387 \right) \times R1 + V_{BG} \quad (1)$$

where

- V_{BG} = 1.2 V
- R2 recommended value is 130 kΩ
- Resistor values are in kΩ
- K = 1 for maximum adaptive boost voltage (typical)
- K = 0 for minimum adaptive boost voltage (typical)
- K = 0.88 for initial boost voltage (typical)

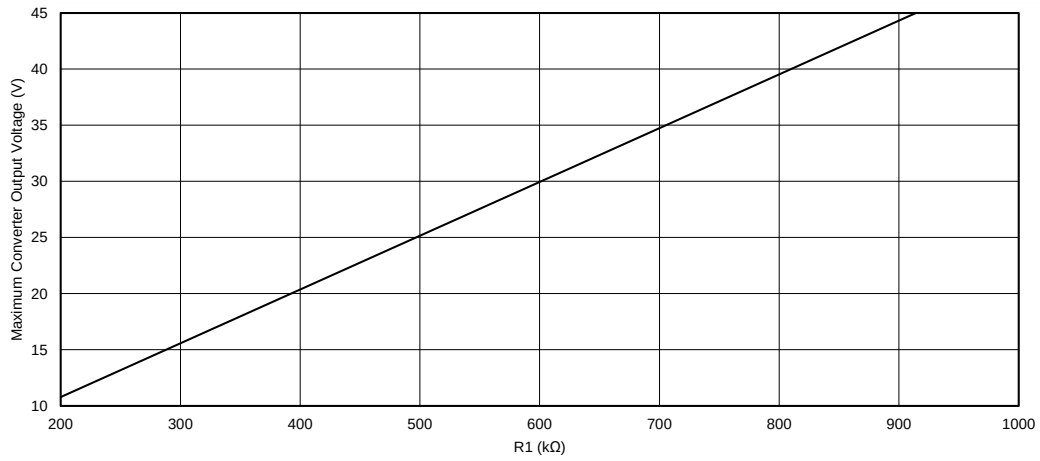


Figure 9. Maximum Converter Output Voltage vs R1 Resistance

Alternatively, a T-divider can be used if resistance less than 100 kΩ is required for the external resistive divider. Refer to *Using the TPS61194xEVM Evaluation Module* for details.

The converter is a current mode DC-DC converter, where the inductor current is measured and controlled with the feedback. Switching frequency is adjustable between 250 kHz and 2.2 MHz with R_{FSET} resistor as Equation 2:

$$f_{SW} = 67600 / (R_{FSET} + 6.4) \quad (2)$$

where

- f_{SW} is switching frequency, kHz
- R_{FSET} is frequency setting resistor, kΩ

In most cases lower frequency has higher system efficiency. DC-DC internal parameters are chosen automatically according to the selected switching frequency (see Table 2) to ensure stability. In boost mode a 15-pF capacitor C_{FB} must be placed across resistor R1 when operating in 300-kHz to 500-kHz range (see *Typical Application for 4 LED Strings*). When operating in the 1.8-MHz to 2.2-MHz range C_{FB} = 4.7 pF.

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Feature Description (continued)

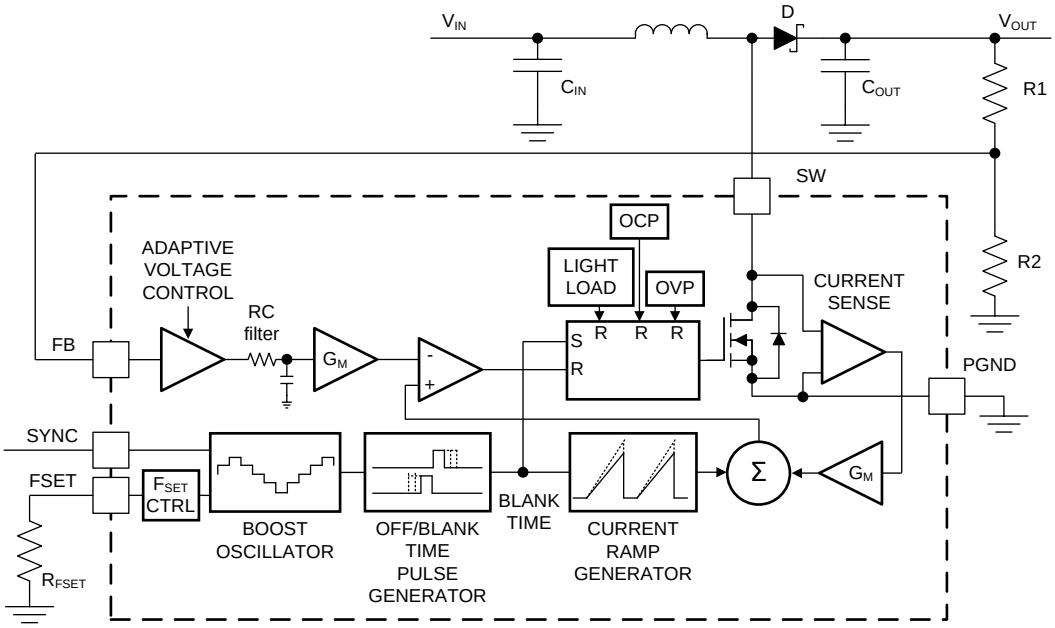


Figure 10. Boost Block Diagram

DC-DC can be driven by an external SYNC signal between 300 kHz and 2.2 MHz. If the external synchronization input disappears, DC-DC continues operation at the frequency defined by R_{FSET} resistor. When external frequency disappears and SYNC pin level is low, converter continues operation without spread spectrum immediately. If SYNC remains high, converter continues switching with spread spectrum enabled after 256 µs.

External SYNC frequency must be 1.2 to 1.5 times higher than the frequency defined by R_{FSET} resistor. Minimum frequency setting with R_{FSET} is 250 kHz to support 300-kHz switching with external clock.

The optional spread spectrum feature (±3% from central frequency, 1-kHz modulation frequency) reduces EMI noise at the switching frequency and its harmonic frequencies. When external synchronization is used, spread spectrum is not available.

Table 1. DC-DC Synchronization Mode

SYNC PIN INPUT	MODE
Low	Spread spectrum disabled
High	Spread spectrum enabled
300 to 2200 kHz frequency	Spread spectrum disabled, external synchronization mode

Table 2. DC-DC Parameters(1)

RANGE	FREQUENCY (kHz)	TYPICAL INDUCTANCE (µH)	TYPICAL BOOST INPUT AND OUTPUT CAPACITORS (µF)	MINIMUM SWITCH OFF TIME (ns)(2)	BLANK TIME (ns)	CURRENT RAMP (A/s)	CURRENT RAMP DELAY (ns)
1	300 to 480	33	2 ×10 (cer.) + 33 (electr.)	150	95	24	550
2	480 to 1150	15	10 (cer.) + 33 (electr.)	60	95	43	300
3	1150 to 1650	10	3 × 10 (cer.)	40	95	79	0
4	1650 to 2200	4.7	3 × 10 (cer.)	40	70	145	0

(1) Parameters are for reference only
(2) Due to current sensing comparator delay the actual minimum off time is 6 ns (typical) longer than in the table.

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The converter SW pin DC current is limited to 2 A (typical). To support short-term transient condition the current limit is automatically increased to 2.5 A for a short period of 1.5 seconds when a 2-A limit is reached.

NOTE

Application condition where the 2-A limit is exceeded continuously is not allowed. In this case the current limit would be 2 A for 1.5 seconds followed by 2.5-A limit for 1.5 seconds, and this 3-second period repeats.

To keep switching voltage within safe levels there is a 48-V limit comparator in the event that FB loop is broken.

7.3.2 Internal LDO

The internal LDO regulator converts the input voltage at VIN to a 4.3-V output voltage for internal use. Connect a minimum of 1-µF ceramic capacitor from LDO pin to ground, as close to the LDO pin as possible.

7.3.3 LED Current Sinks

7.3.3.1 Output Configuration

TPS61194 detects LED output configuration during start-up. Any current sink output connected to ground is disabled and excluded from the adaptive voltage control of the DC-DC and fault detections.

7.3.3.2 Current Setting

Maximum current for the LED outputs is controlled with external R_{ISET} resistor. R_{ISET} value for target maximum current can be calculated using Equation 3:

$$R_{ISET} = 2342 / (I_{OUT} – 2.5) \quad (3)$$

where

- R_{ISET} is current setting resistor, kΩ
- I_{LED} is output current per output, mA

7.3.3.3 Brightness Control

TPS61194 controls the brightness of the display with conventional PWM. Output PWM directly follows the input PWM. Input PWM frequency can be in the range of 100 Hz to 20 kHz.

7.3.4 Protection and Fault Detections

The TPS61194 has fault detection for LED open and short, VIN input overvoltage protection (VIN_OVP) , VIN undervoltage lockout (VIN_UVLO), and thermal shutdown (TSD).

7.3.4.1 Adaptive DC-DC Voltage Control and Functionality of LED Fault Comparators

Adaptive voltage control function adjusts the DC-DC output voltage to the minimum sufficient voltage for proper LED current sink operation. The current sink with highest V_F LED string is detected and DC-DC output voltage adjusted accordingly. DC-DC adaptive control voltage step size is defined by maximum voltage setting, $V_{STEP} = (V_{OUT_MAX} – V_{OUT_MIN)} / 256$. Periodic down pressure is applied to the target voltage to achieve better system efficiency.

Every LED current sink has 3 comparators for the adaptive DC-DC control and LED fault detections. Comparator outputs are filtered, filtering time is 1 µs.

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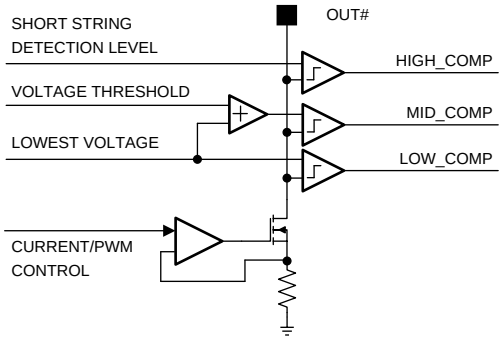


Figure 11. Comparators for Adaptive Voltage Control and LED Fault Detection

Figure 12 shows different cases which cause DC-DC voltage increase, decrease, or generate faults. In normal operation voltage at all the OUT# pins is between LOW_COMP and MID_COMP levels, and boost voltage stays constant. LOW_COMP level is the minimum for proper LED current sink operation, 1.1 × V_{SAT} + 0.2 V (typical). MID_COMP level is 1.1 × V_{SAT} + 1.2 V (typical) so typical headroom window is 1 V.

When voltage at all the OUT# pins increases above MID_COMP level, DC-DC voltage adapts downwards.

When voltage at any of the OUT# pins falls below LOW_COMP threshold, DC-DC voltage adapts upwards. In the condition where DC-DC voltage reaches the maximum and there are one or more outputs still below LOW_COMP level, an open LED fault is detected.

HIGH_COMP level, 6 V typical, is the threshold for shorted LED detection. When the voltage of one or more of the OUT# pins increases above HIGH_COMP level and at least one of the other outputs is within the normal headroom window, shorted LED fault is detected.

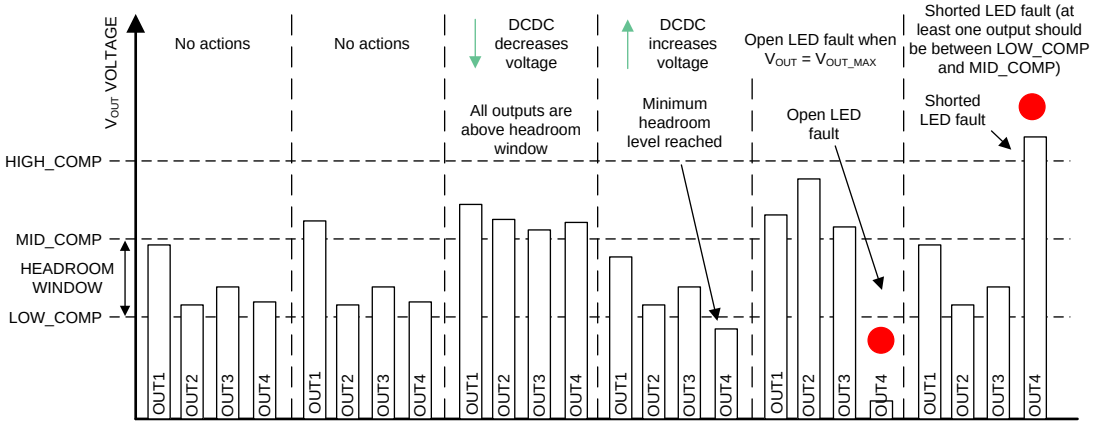


Figure 12. Protection and DC-DC Voltage Adaptation Algorithms

7.3.4.2 Overview of the Fault/Protection Schemes

A summary of the TPS61194fault detection behavior is shown in Table 3. Detected faults (excluding LED open or short) cause device to enter FAULT_RECOVERY state. In FAULT_RECOVERY the DC-DC and LED current sinks of the device are disabled, and the FAULT pin is pulled low. The device recovers automatically and enters normal operating mode (ACTIVE) after a recovery time of 100 ms if the fault condition has disappeared. When recovery is succesful, FAULT pin is released.

If a LED fault is detected, the device continues normal operation and only the faulty string is disabled. The fault is indicated via the FAULT pin which can be released by toggling VDDIO/EN pin low for a short period of 2 µs to 20 µs. LEDs are turned off for this period but the device stays in ACTIVE mode. If VDDIO/EN is low longer, the device goes to STANDBY and restarts when EN goes high again.

Table 3. Fault Detections

FAULT/ PROTECTION	FAULT NAME	THRESHOLD	FAULT PIN	FAULT_ RECOVERY STATE	ACTION
VIN overvoltage protection	VIN_OVP	1. V_{IN} > 42 V 2. V_{OUT} > V_{SET_DCDC} + 6..10 V. V_{SET_DCDC} is voltage value defined by logic during adaptation	Yes	Yes	1. Overvoltage is monitored from the beginning of soft start. Fault is detected if the duration of overvoltage condition is 100 µs minimum. 2. Overvoltage is monitored from the beginning of normal operation (ACTIVE mode). Fault is detected if over-voltage condition duration is 560 ms minimum (t_{filter}). After the first fault, detection filter time is reduced to 50 ms for following recovery cycles. When the device recovers and has been in ACTIVE mode for 160 ms, filter time is increased back to 560 ms .
VIN undervoltage lockout	VIN_UVLO	Falling 3.9 V Rising 4 V	Yes	Yes	Detects undervoltage condition at VIN pin. Sensed in all operating modes. Fault is detected if undervoltage condition duration is 100 µs minimum.
Open LED fault	OPEN_LED	LOW_COMP threshold	Yes	No	Detected if the voltage of one or more current sinks is below threshold level, and DC-DC adaptive control has reached maximum voltage. Open string is removed from the DC-DC voltage control loop and current sink is disabled. Fault pin is released by toggling VDDIO/EN pin. If VDDIO/EN is low for a period of 2 µs to 20 µs, LEDs are turned off for this period but device stays ACTIVE. If VDDIO/EN is low longer, device goes to STANDBY and restarts when EN goes high again.
Shorted LED fault	SHORT_LED	Shorted string detection level 6 V	Yes	No	Detected if the voltage of one or more current sinks is above shorted string detection level and at least one OUTx voltage is within headroom window. Shorted string is removed from the DC-DC voltage control loop and current sink is disabled. Fault pin is released by toggling VDDIO/EN pin. If VDDIO/EN is low for a period of 2…20 µs, LEDs are turned off for this period but device stays ACTIVE. If VDDIO/EN is low longer, device goes to STANDBY and restarts when EN goes high again..
Thermal protection	TSD	165ºC Thermal shutdown hysteresis 20ºC	Yes	Yes	Thermal shutdown is monitored from the beginning of soft start. Die temperature must decrease by 20ºC for device to recover.

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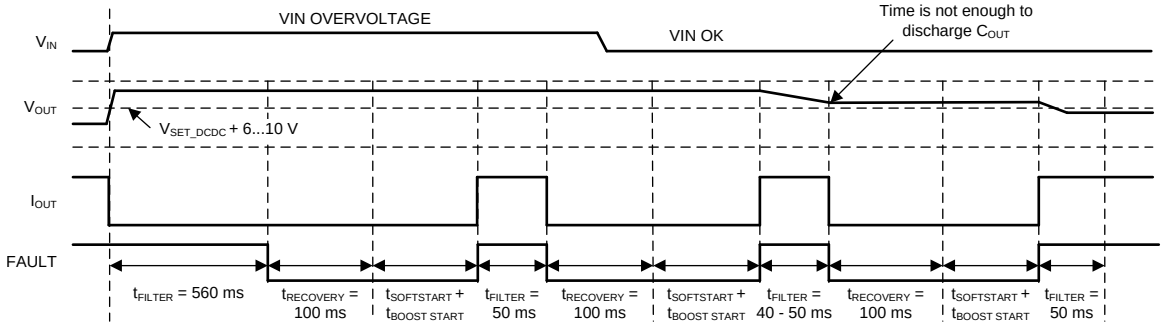


Figure 13. V_{IN} Overvoltage Protection (DC-DC OVP)

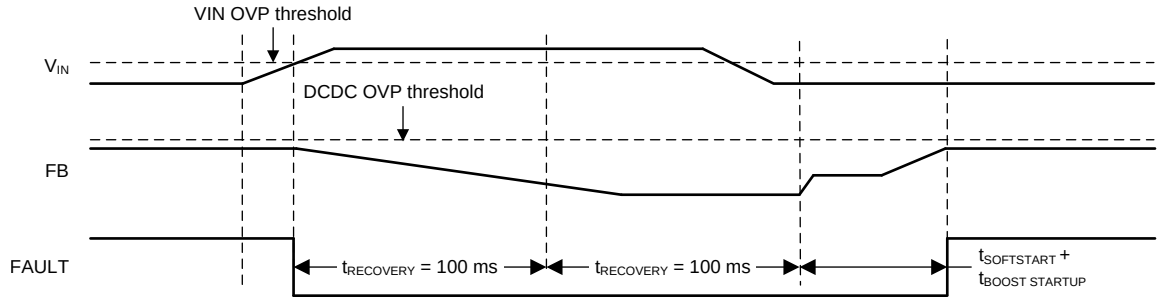


Figure 14. V_{IN} Overvoltage Protection (V_{IN} OVP)

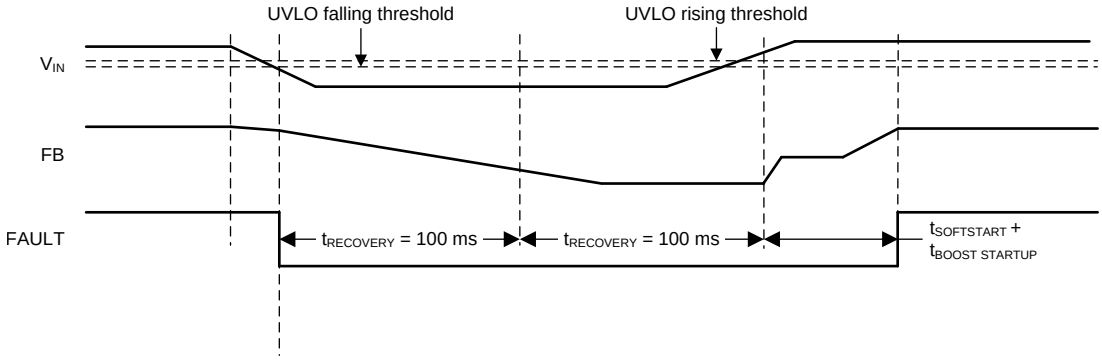


Figure 15. V_{IN} Undervoltage Lockout

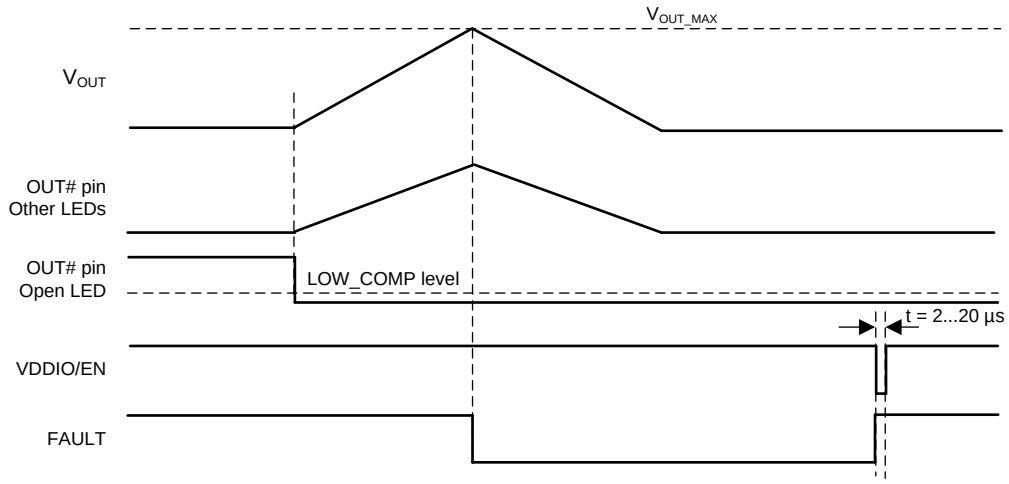


Figure 16. LED Open Fault

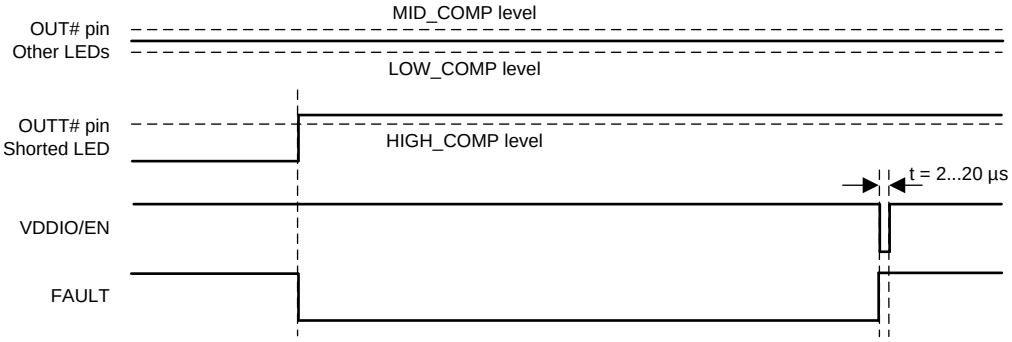


Figure 17. LED Short Fault

7.4 Device Functional Modes

7.4.1 Device States

The TPS61194 enters STANDBY mode when the internal LDO output rises above the power-on reset level, $V_{LDO} > V_{POR}$. In STANDBY mode the device is able to detect VDDIO/EN signal. When VDDIO/EN is pulled high, the device powers up. After start LED outputs are sensed to detect grounded outputs. Grounded outputs are disabled and excluded from the adaptive voltage control loop of the DC-DC.

If a fault condition is detected, the device enters FAULT_RECOVERY state. Faults that cause the device to enter FAULT_RECOVERY are listed in Table 3. When LED open or short is detected, the faulty string is disabled, but device stays in ACTIVE mode.

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Device Functional Modes (continued)

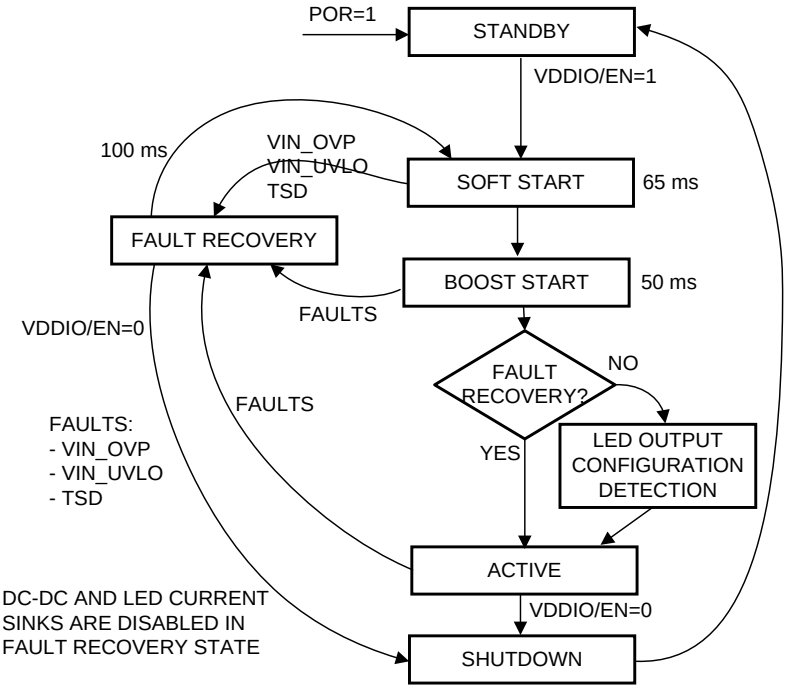


Figure 18. State Diagram

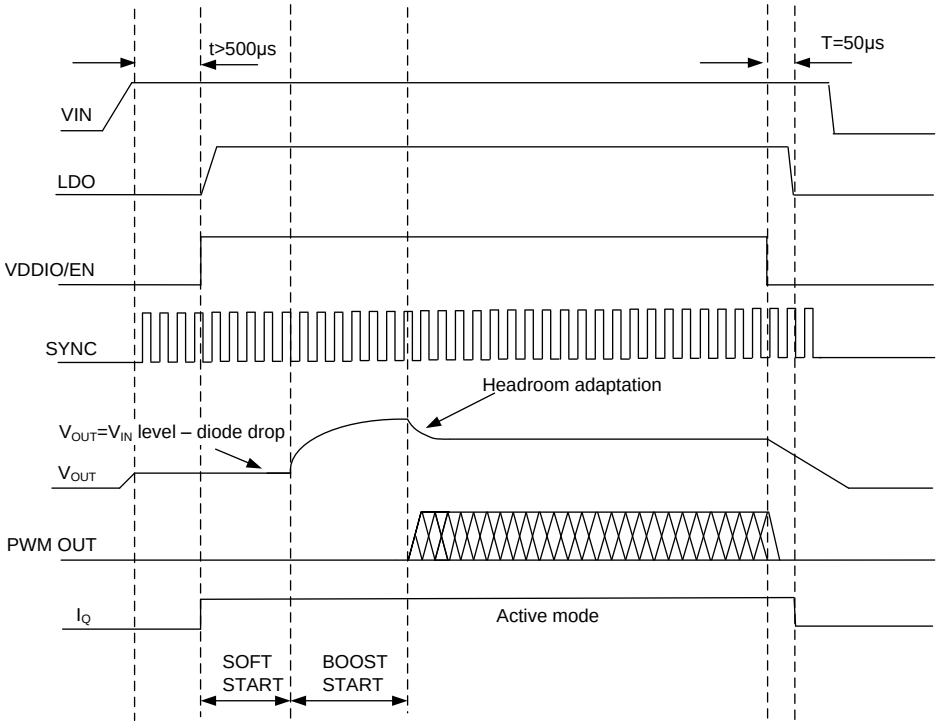


Figure 19. Timing Diagram for the Typical Start-Up and Shutdown

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61194 supports input voltage range from 4.5 V to 40 V. Device internal circuitry is powered from the integrated LDO.

The TPS61194 uses a simple four-wire control:

- VDDIO/EN for enable
- PWM input for brightness control
- SYNC pin for boost synchronisation (optional)
- FAULT output to indicate fault condition (optional)

8.2 Typical Applications

8.2.1 Typical Application for 4 LED Strings

Figure 20 shows the typical application for TPS61194 which supports 4 LED strings, 80 mA per string, , with a boost switching frequency of 300 kHz.

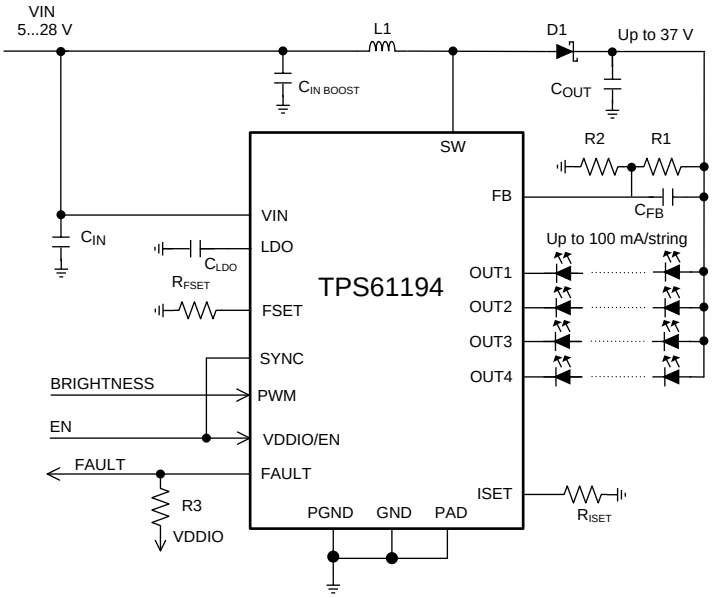


Figure 20. Four Strings 80 mA per String Configuration

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Typical Applications (continued)

8.2.1.1 Design Requirements

DESIGN PARAMETER	VALUE
V_{IN} voltage range	4.5 V – 28 V
LED string	4P8S LEDs (30 V)
LED string current	100 mA
Maximum boost voltage	37 V
Boost switching frequency	300 kHz
External boost sync	not used
Boost spread spectrum	enabled
L1	33 µH
C_{IN}	100 µF, 50 V
$C_{IN\ BOOST}$	2 × (10-µF, 50-V ceramic) + 33-µF, 50-V electrolytic
C_{OUT}	2 × (10-µF, 50-V ceramic) + 33-µF, 50-V electrolytic
C_{FB}	15 pF
C_{LDO}	1 µF, 10 V
R_{ISET}	24 kΩ
R_{FSET}	210 kΩ
R1	750 kΩ
R2	130 kΩ
R3	10 kΩ

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

There are two main considerations when choosing an inductor; the inductor must not saturate, and the inductor current ripple must be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and are preferred. The saturation current must be greater than the sum of the maximum load current, and the worst case average-to-peak inductor current. Equation 4 shows the worst case conditions

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE} \quad \text{For Boost}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ and } D' = (1 - D)$$

- I_{RIPPLE} - peak inductor current
- I_{OUTMAX} - maximum load current
- V_{IN} - minimum input voltage in application
- L - min inductor value including worst case tolerances
- f - minimum switching frequency
- V_{OUT} - output voltage
- D - Duty Cycle for CCM Operation (4)

As a result, the inductor should be selected according to the I_{SAT}. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit. A saturation current rating of at least 2.5 A is recommended for most applications. See Table 2 for recommended inductance value for the different switching frequency ranges. The inductor's resistance should be less than 300 mΩ for good efficiency.

See detailed information in *Understanding Boost Power Stages in Switch Mode Power Supplies*. *Power Stage Designer™ Tool* can be used for the boost calculation: http://www.ti.com/tool/powerstage-designer.

8.2.1.2.2 Output Capacitor Selection

A ceramic capacitor with 2 × $V_{MAX\ BOOST}$ or more voltage rating is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Capacitance recommendations for different switching frequencies are shown in Table 2. To minimize audible noise of ceramic capacitors their physical size should typically be minimized.

8.2.1.2.3 Input Capacitor Selection

A ceramic capacitor with 2 × $V_{IN\ MAX}$ or more voltage rating is recommended for the input capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Capacitance recommendations for different boost switching frequencies are shown in Table 2.

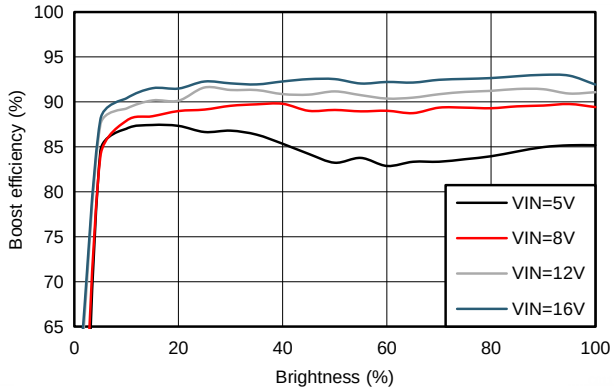
8.2.1.2.4 LDO Output Capacitor

A ceramic capacitor with at least 10-V voltage rating is recommended for the output capacitor of the LDO. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Typically a 1-µF capacitor is sufficient.

8.2.1.2.5 Diode

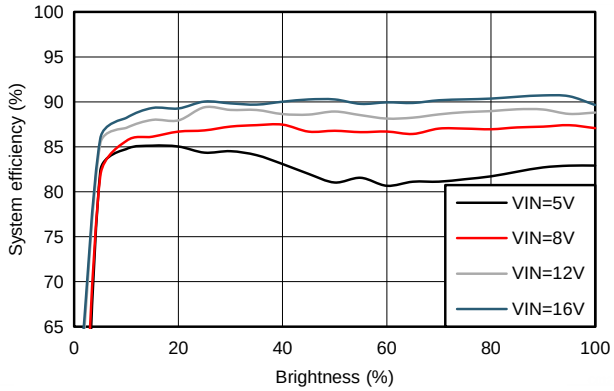
A Schottky diode should be used for the boost output diode. Do not use ordinary rectifier diodes because slow switching speeds and long recovery times degrade the efficiency and the load regulation. Diode rating for peak repetitive current should be greater than inductor peak current (up to 3 A) to ensure reliable operation in boost mode. Average current rating should be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. Choose a reverse breakdown voltage of the Schottky diode significantly larger than the output voltage.

8.2.1.3 Application Curves



Load 4 strings, 8 LEDs per string f_{sw}=300 kHz, 33 µH
100 mA/string for V_{IN} = 12 V and V_{IN} = 16 V
60 mA/string for V_{IN} = 8 V
50 mA/string for V_{IN} = 5 V

Figure 21. Boost Efficiency



Load 4 strings, 8 LEDs per string f_{sw}=300 kHz, 33 µH
100 mA/string for V_{IN} = 12 V and V_{IN} = 16 V
60 mA/string for V_{IN} = 8 V
50 mA/string for V_{IN} = 5 V

Figure 22. System Efficiency

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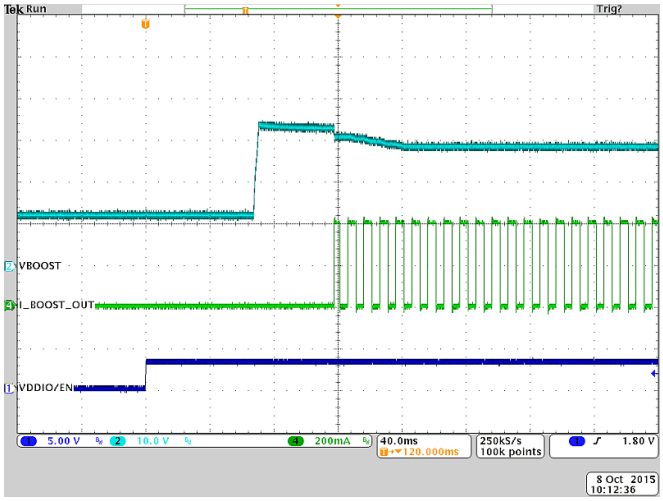


Figure 23. Typical Start-Up

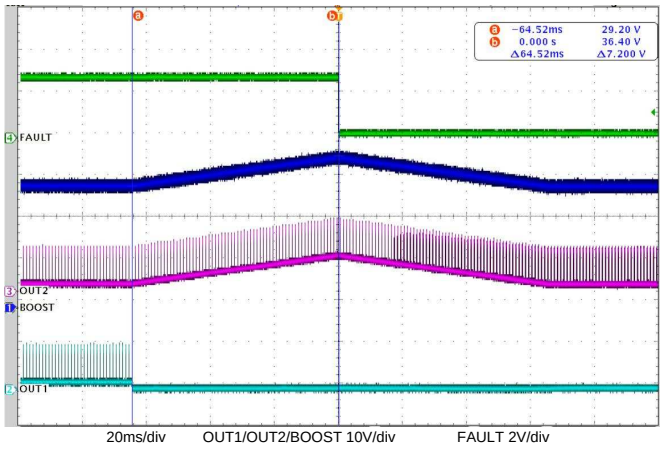


Figure 24. Open LED Fault

8.2.2 SEPIC Mode Application

When LED string voltage can be above or below V_{IN} voltage, SEPIC configuration can be used. In this example, two separate coils are used for SEPIC. This can enable lower height external components to be used, compared to a coupled coil solution. On the other hand, coupled coil typically maximizes the efficiency. Also, in this example, an external clock is used to synchronize SEPIC switching frequency. External clock input can be modulated to spread switching frequency spectrum.

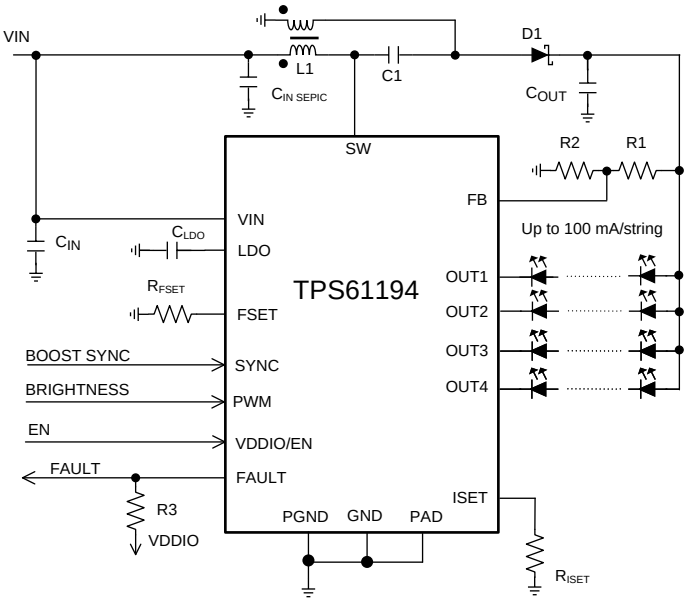


Figure 25. SEPIC Mode, 4 Strings, 100 mA per String Configuration

8.2.2.1 Design Requirements

DESIGN PARAMETER	VALUE
V_{IN} voltage range	4.5 V – 30 V
LED string	4P2S LEDs (7.2 V)
LED string current	100 mA
Maxmum output voltage	10 V
SEPIC switching frequency	2.2 MHz
External sync for SEPIC	used
Spread spectrum	Internal spread spectrum disabled (external sync used)
L1, L2	10 µH
C_{IN}	10 µF 50 V
$C_{IN\ SEPIC}$	2 × 10-µF, 50-V ceramic + 33 µF 50-V electrolytic
C1	10-µF 50-V ceramic
C_{OUT}	2 × 10-µF, 50-V ceramic + 33 µF 50-V electrolytic
C_{LDO}	1 µF, 10 V
R_{ISET}	24 kΩ
R_{FSET}	
R1	184 kΩ
R2	130 kΩ
R3	10 kΩ

8.2.2.2 Detailed Design Procedure

In SEPIC mode the maximum voltage at the SW pin is equal to the sum of the input voltage and the output voltage. Because of this, the maximum sum of input and output voltage must be limited below 50 V. See *Detailed Design Procedure* for general external component guidelines. Main differences of SEPIC compared to boost are described below.

Power Stage Designer™ Tool can be used for modeling SEPIC behavior: http://www.ti.com/tool/powerstage-designer. For detailed explanation on SEPIC see Texas Instruments Analog Applications Journal *Designing DC/DC Converters Based on SEPIC Topology* (SLYT309).

8.2.2.2.1 Inductor

In SEPIC mode, currents flowing through the coupled inductors or the two separate inductors L1 and L2 are the input current and output current, respectively. Values can be calculated using *Power Stage Designer™ Tool* or using equations in SLYT309.

8.2.2.2.2 Diode

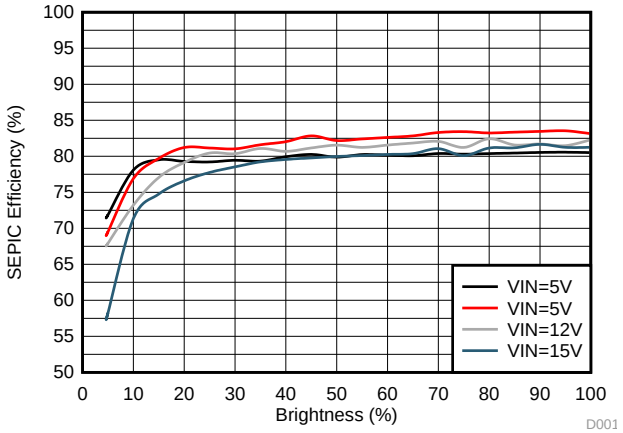
In SEPIC mode diode peak current is equal to the sum of input and output currents. Diode rating for peak repetitive current should be greater than SW pin current limit (up to 3 A for transients) to ensure reliable operation in boost mode. Average current rating should be greater than the maximum output current. Diode voltage rating must be higher than sum of input and output voltages.

8.2.2.2.3 Capacitor C1

Ti recommends a ceramic capacitor with low ESR. Diode voltage rating must be higher than maximum input voltage.

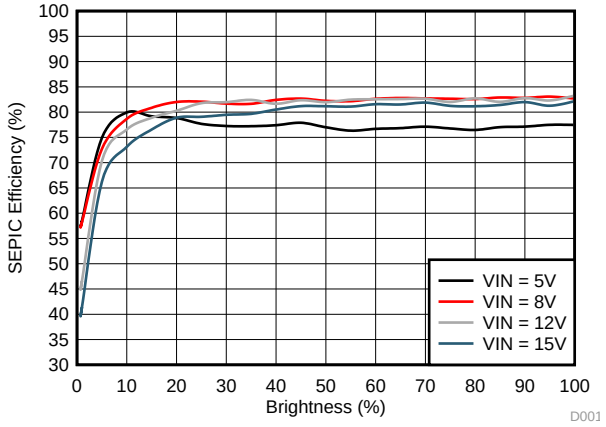
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8.2.2.3 Application Curves



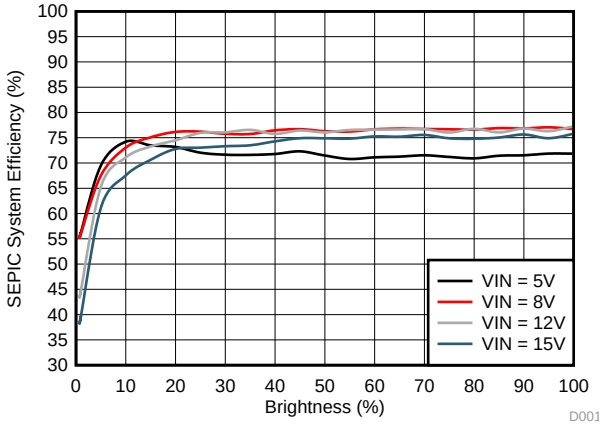
Load 100mA per string, 3 strings, 2 LEDs per string
f_{sw} = 2.2 MHz
2 × 10 µH, IHLP2525BDER100M

Figure 26. SEPIC Efficiency



Load 100mA per string, 4 strings, 2 LEDs per string
f_{sw} = 2.2 MHz
2 × 10 µH, IHLP2525BDER100M

Figure 27. SEPIC Efficiency



Load 100mA/string, 4 strings, 2 LEDs per string
f_{sw} = 2.2 MHz
2 x 10 µH, IHLP2525BDER100M

Figure 28. System Efficiency

9 Power Supply Recommendations

The resistance of the input supply rail must be low enough so that the input current transient does not cause too high drop at TPS61194 VIN pin. If the input supply is connected by using long wires additional bulk capacitance may be required in addition to the ceramic bypass capacitors in the V_{IN} line.

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10 Layout

10.1 Layout Guidelines

Figure 29 is a layout recommendation for TPS61194 used to demonstrate the principles of a good layout. This layout can be adapted to the actual application layout if or where possible. It is important that all boost components are close to the chip, and the high current traces must be wide enough. By placing boost components on one side of the chip it is easy to keep the ground plane intact below the high current paths. This way other chip pins can be routed more easily without splitting the ground plane. Bypass LDO capacitor must be placed as close as possible to the device.

Here are some main points to help the PCB layout work:

- Current loops need to be minimized:
  - For low frequency the minimal current loop can be achieved by placing the boost components as close as possible to the SW and PGND pins. Input and output capacitor grounds must be close to each other to minimize current loop size.
  - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High-frequency return currents find a route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the *positive*current route in the ground plane, if the ground plane is intact under the route.
- The GND plane must be intact under the high current boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
- Current loops when the boost switch is conducting and not conducting must be on the same direction in optimal case.
- Inductors must be placed so that the current flows in the same direction as in the current loops. Rotating inductor 180° changes current direction.
- Use separate power and noise-free grounds. Power ground is used for boost converter return current and noise-free ground for more sensitive signals, such as LDO bypass capacitor grounding as well as grounding the GND pin of the device.
- Boost output feedback voltage to LEDs must be taken out *after* the output capacitors, not straight from the diode cathode.
- Place LDO 1-µF bypass capacitor as close as possible to the LDO pin.
- Input and output capacitors require strong grounding (wide traces, many vias to GND plane).
- If two output capacitors are used they must have symmetrical layout to get both capacitors working ideally.
- Output ceramic capacitors have a DC-bias effect. If the output capacitance is too low, it can cause boost to become unstable on some loads, and this increases EMI. DC-bias characteristics should be obtained from the component manufacturer; they are not taken into account on component tolerance. TI recommends X5R/X7R capacitors.

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10.2 Layout Example

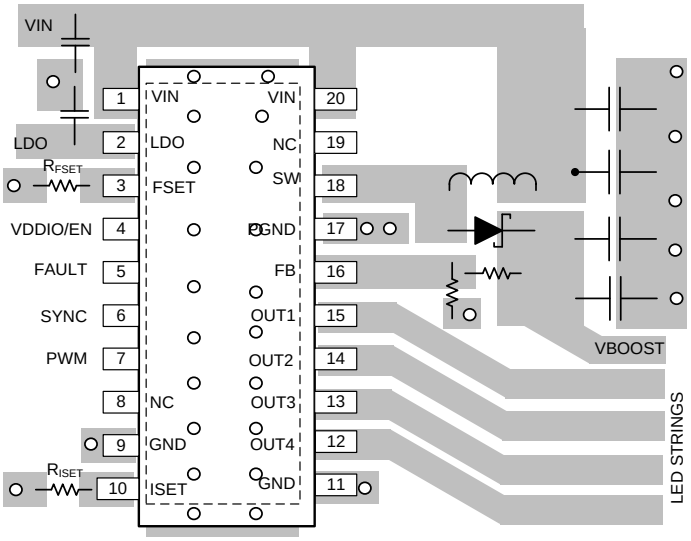


Figure 29. TPS61194 Boost Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

Power Stage Designer™ Tool can be used for both boost and SEPIC: http://www.ti.com/tool/powerstage-designer

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package*
- *Understanding Boost Power Stages in Switch Mode Power Supplies*
- *Designing DC-DC Converters Based on SEPIC Topology*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

Power Stage Designer, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61194PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS61194	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS61194 :

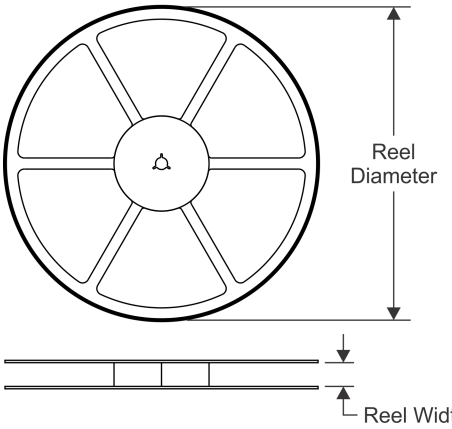
- Automotive: TPS61194-Q1

NOTE: Qualified Version Definitions:

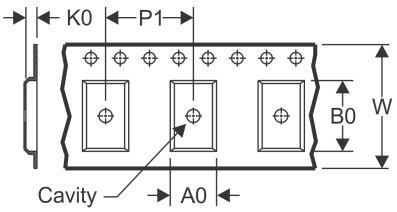
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

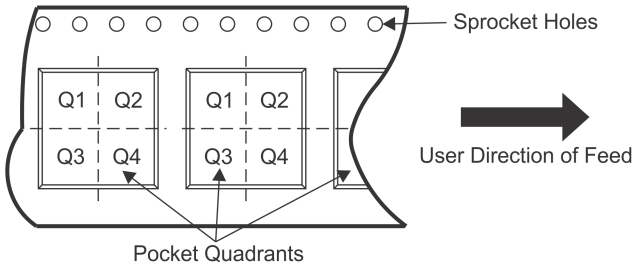


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

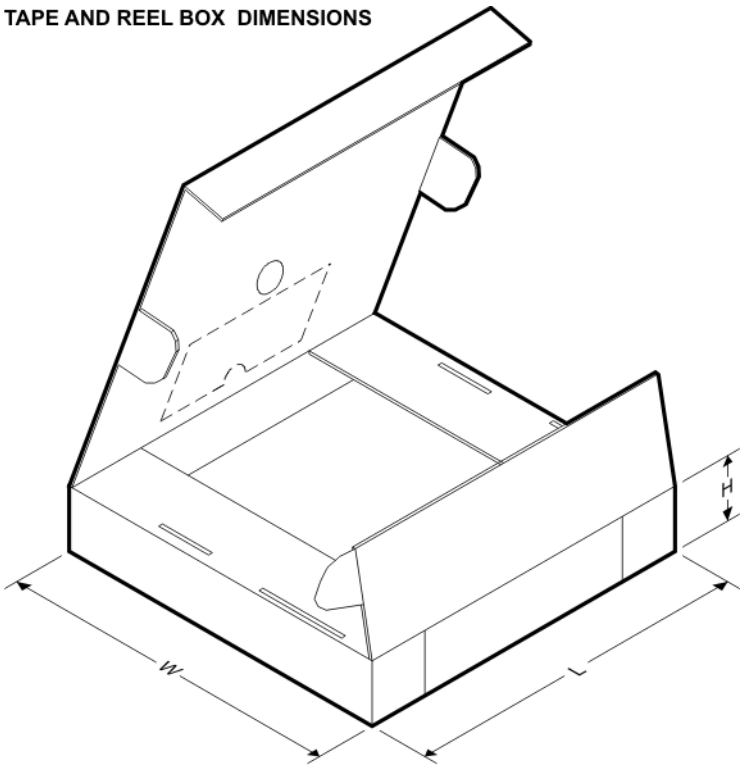
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61194PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

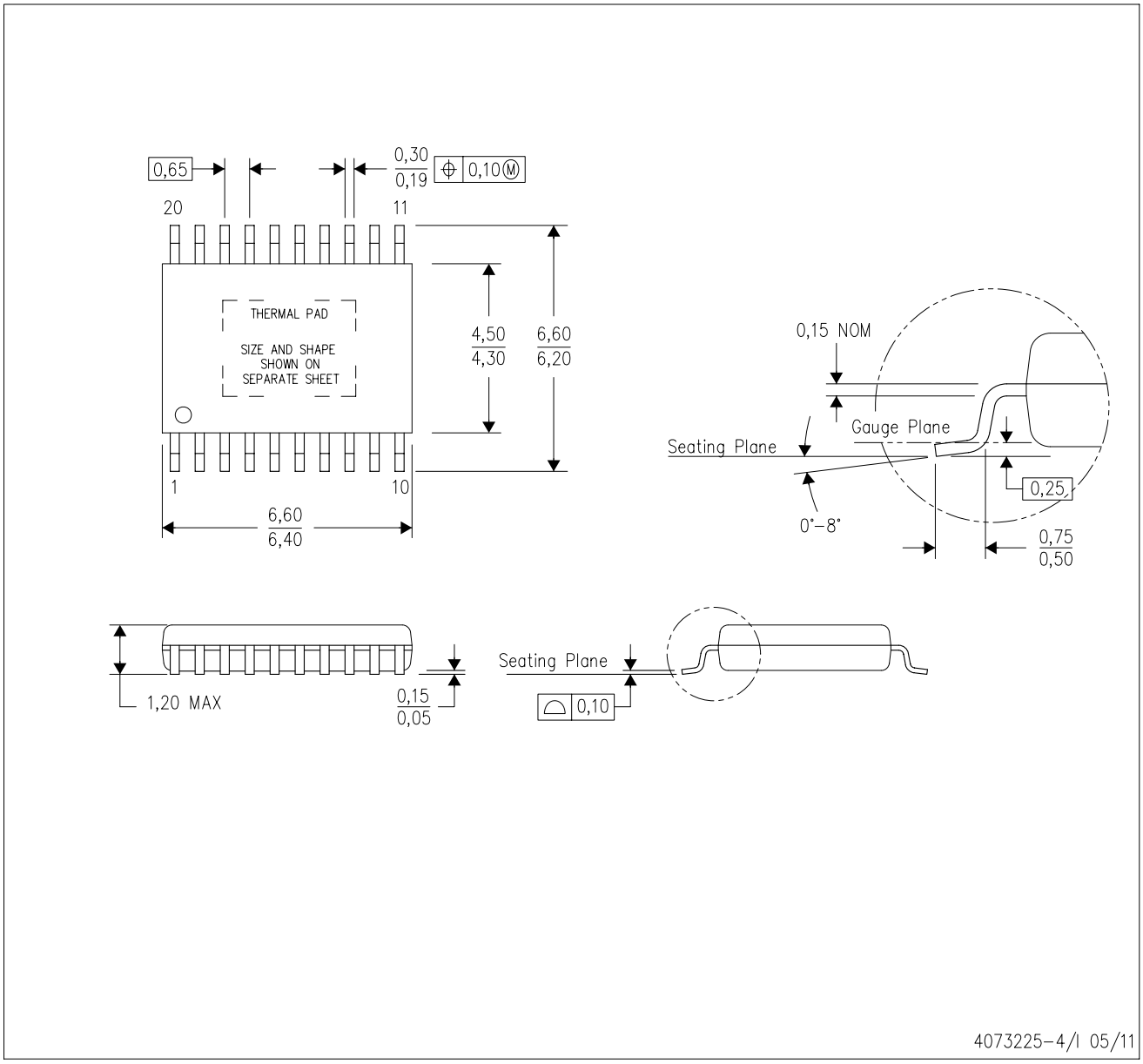
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61194PWPR	HTSSOP	PWP	20	2000	367.0	367.0	38.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

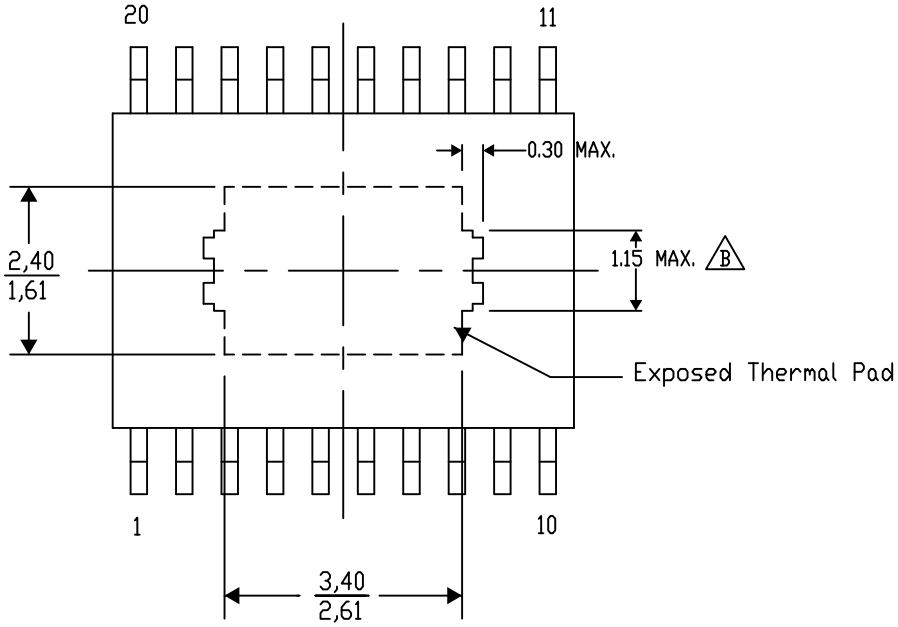
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

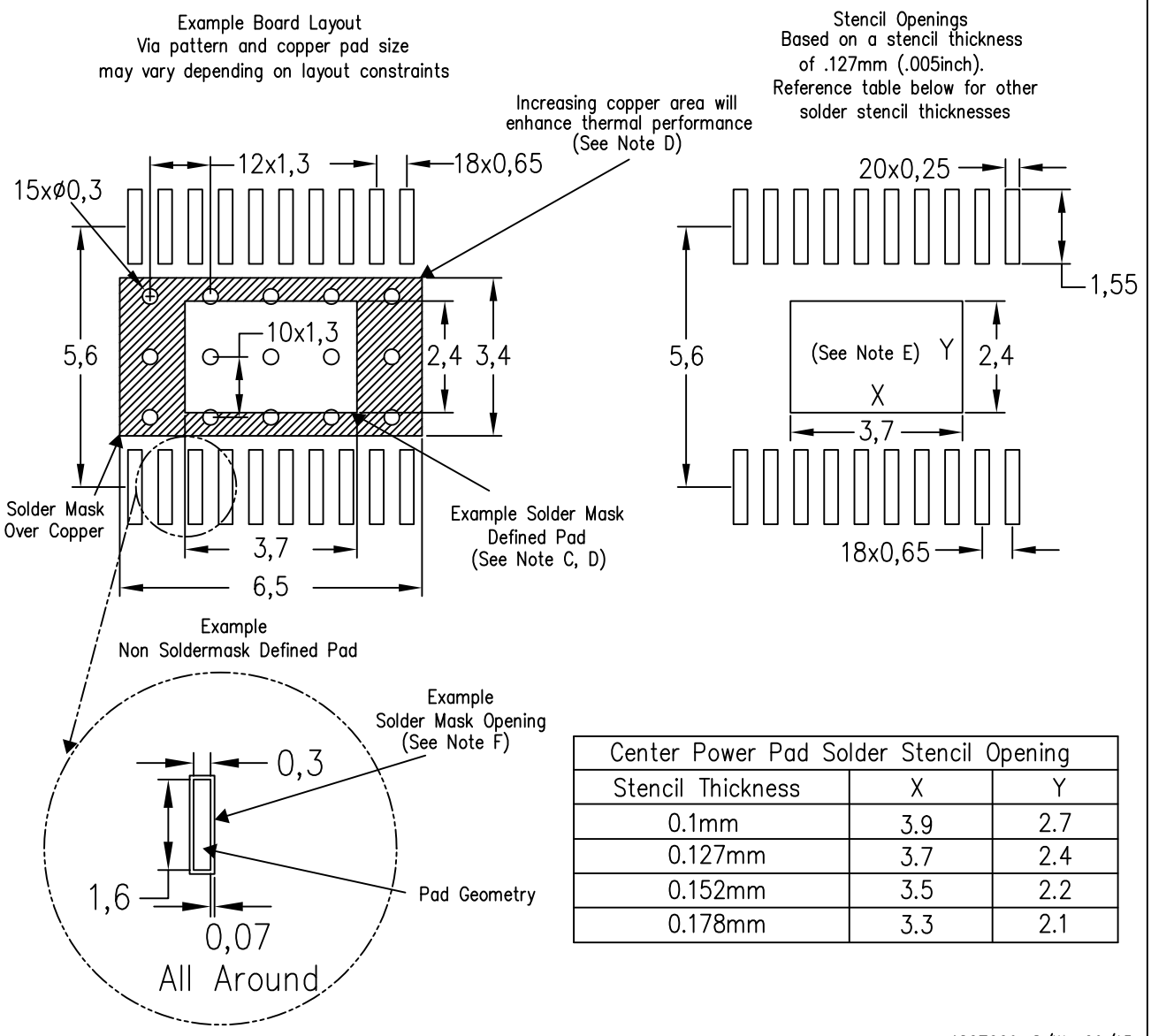
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61194PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS61194	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
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OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

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OTHER QUALIFIED VERSIONS OF TPS61194 :

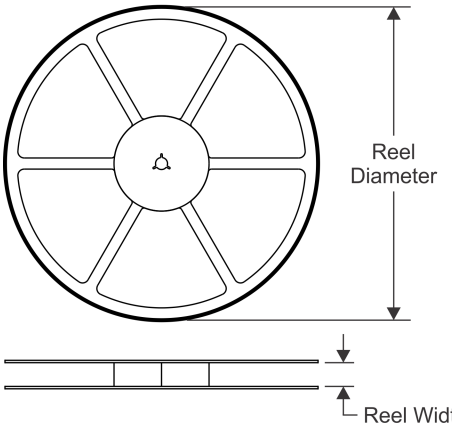
- Automotive: TPS61194-Q1

NOTE: Qualified Version Definitions:

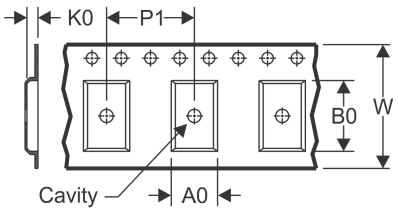
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

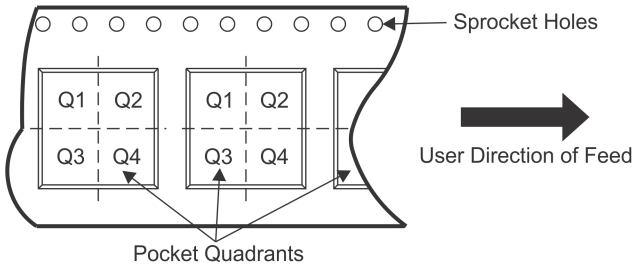


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

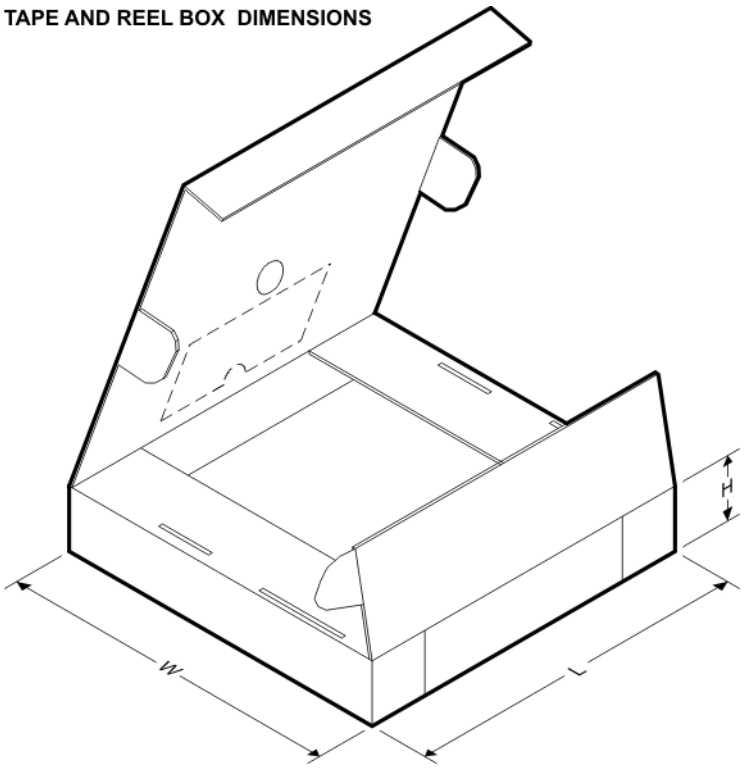
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61194PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61194PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

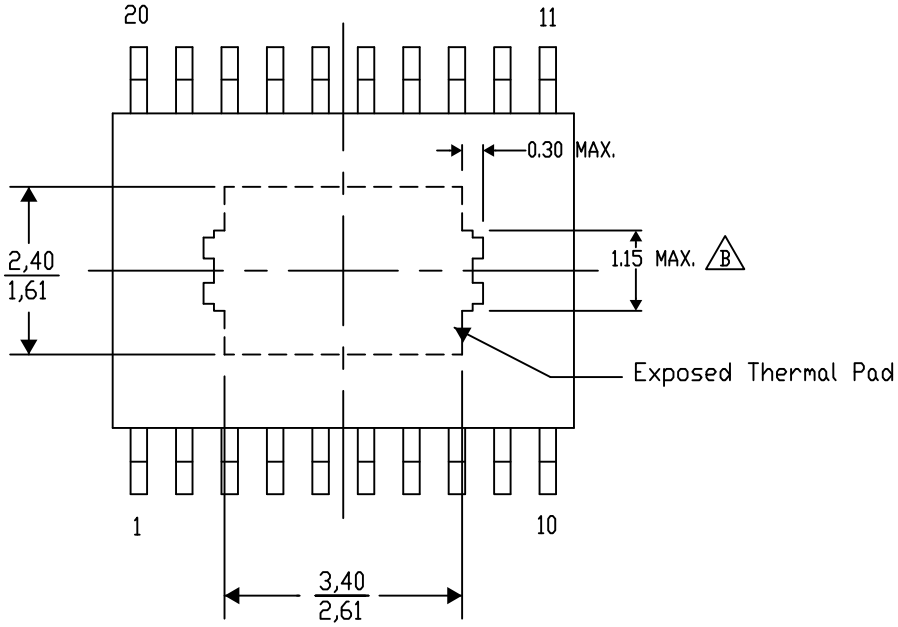
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

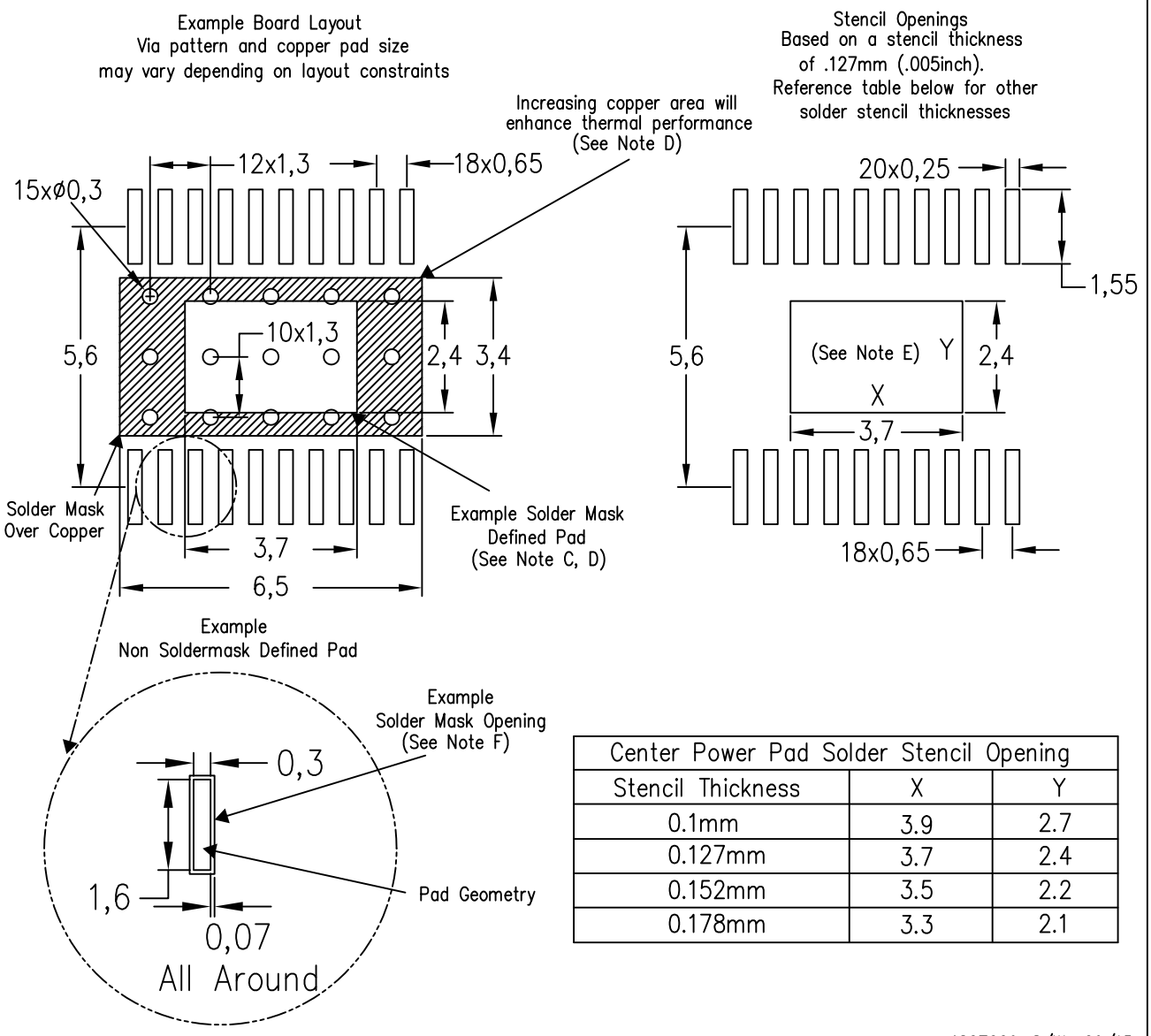
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
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C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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