TPS56921EVM-188, 9-A, SWIFT™ Regulator Evaluation Module

This user's guide contains information for the TPS56921EVM-188 evaluation module (PWR188) as well as for the TPS56921 dc/dc converter. Also included are the performance specifications, the schematic, and the bill of materials for the TPS56921EVM-188.

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1 Introduction

1.1 Background

The TPS56921 dc/dc converter is designed to provide up to a 9-A output. The TPS56921 implements split-input power rails with separate input voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 17 V whereas the control input (VIN) is rated for 4.5 V to 17 V. The TPS56921EVM-188 provides both inputs but is designed and tested using the PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS56921 regulator. The switching frequency is externally set at a nominal 500 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS56921 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS56921 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS56921 provides adjustable slow start, tracking, and undervoltage lockout inputs. The absolute maximum input voltage is 20 V for the TPS56921EVM-188.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS56921EVM-188	VIN = 4.5 V to 17 V	0 A to 9 A

1.2 Performance Specification Summary

A summary of the TPS56921EVM-188 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.1 V, unless otherwise specified. The TPS56921EVM-188 is designed and tested for V_{IN} = 4.5 V to 17 V with the VIN and PVIN pins connect together with the JP1 jumper. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS56921EVM-188 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range (PVIN = VIN)			4.5	12	17	V
V_{IN} start voltage (internal UVLO)				4.0		V
V_{IN} stop voltage (internal UVLO)				3.85		V
Output voltage setpoint				1.1		V
Output current range	V_{IN} = 8 V to 17 V		0		9	A
Line regulation	I_O = 4.5 A, V_{IN} = 4.5 V to 17 V			±0.01		%
Load regulation	V_{IN} = 12 V, I_O = 0 A to 9 A			±0.18		%
Load transient response	I_O = 2.25 A to 6.75 A	Voltage change		–90		mV
		Recovery time		100		µs
	I_O = 6.75 A to 2.25 A	Voltage change		90		mV
		Recovery time		100		µs
Loop bandwidth	V_{IN} = 12 V, I_O = 4 A			50.1		kHz
Phase margin	V_{IN} = 12 V , I_O = 4 A			63		°
Input ripple voltage	I_O = 9 A, measured with 330 µF added capacitance at J2			300		mVPP
Output ripple voltage	I_O = 8 A			10		mVPP
Output rise time				4		ms
Operating frequency				500		kHz
Maximum efficiency	TPS56921EVM-188, V_{IN} = 5 V, I_O = 1.6 A			88.1		%

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1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS56921. Some modifications can be made to this module.

1.3.1 Output Voltage Setpoint

The output voltage of the EVM is set either externally using a voltage divider or internally using the integrated I²C™ interface. The external adjustment of the output voltage is set by the resistor divider network of R10 and R11. R10 is fixed at 10 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R11. Changing the value of R11 can change the output voltage in the range of 0.72 V to 1.48 V. The value of R11 for a specific output voltage can be calculated using Equation 1.

$$R11 = \frac{10\,k\Omega \times 0.8\,V}{V_{OUT} - 0.8V} \quad (1)$$

The output voltage can also be set using the optional VID control using the I²C interface. The EVM is designed so that the J3 connector is compatible with the HPA665-001 USB2ANY interface. Using that control and USB2ANY_GUI software allows the output voltage to be programmed to any of 77 preset voltages from 0.72 V to 1.48 V. See the TPS56921 datasheet for a complete description of the available codes. With the software running and the cable attached, confirm the connection by clicking the "Read" button under "Firmware Revision". The firmware revision number will be returned if the connection is good. Set up the interface by selecting "Speed = _400kHz", "Address = _7Bits" and "Pull Ups = OFF" in the "I2C" section. Click on "Set I2C". In the "3.3V/5.0V" section set "3.3V = ON" and "5.0V = OFF". Click on "Set", then click on "Get Status". "GOOD" should be returned for both 3.3 V and 5.0 V. To communicate with the TPS56921EVM-188, in the "Single-Register" section set "I2C Address = 34". In the "Register Address" field, enter the data byte for the voltage you wish to set. Ignore the "Byte to Write" field. Click on "Write" to send the data.

Table 3. Ideal VOUT versus Code

Code	Binary	VOUT	Code	Binary	VOUT	Code	Binary	VOUT
0	0000000	0.720	26	0011010	0.980	52	0110100	1.240
1	0000001	0.730	27	0011011	0.990	53	0110101	1.250
2	0000010	0.740	28	0011100	1.000	54	0110110	1.260
3	0000011	0.750	29	0011101	1.010	55	0110111	1.270
4	0000100	0.760	30	0011110	1.020	56	0111000	1.280
5	0000101	0.770	31	0011111	1.030	57	0111001	1.290
6	0000110	0.780	32	0100000	1.040	58	0111010	1.300
7	0000111	0.790	33	0100001	1.050	59	0111011	1.310
8	0001000	0.800	34	0100010	1.060	60	0111100	1.320
9	0001001	0.810	35	0100011	1.070	61	0111101	1.330
10	0001010	0.820	36	0100100	1.080	62	0111110	1.340
11	0001011	0.830	37	0100101	1.090	63	0111111	1.350
12	0001100	0.840	38	0100110	1.100	64	1000000	1.360
13	0001101	0.850	39	0100111	1.110	65	1000001	1.370
14	0001110	0.860	40	0101000	1.120	66	1000010	1.380
15	0001111	0.870	41	0101001	1.130	67	1000011	1.390
16	0010000	0.880	42	0101010	1.140	68	1000100	1.400
17	0010001	0.890	43	0101011	1.150	69	1000101	1.410
18	0010010	0.900	44	0101100	1.160	70	1000110	1.420
19	0010011	0.910	45	0101101	1.170	71	1000111	1.430
20	0010100	0.920	46	0101110	1.180	72	1001000	1.440
21	0010101	0.930	47	0101111	1.190	73	1001001	1.450
22	0010110	0.940	48	0110000	1.200	74	1001010	1.460
23	0010111	0.950	49	0110001	1.210	75	1001011	1.470
24	0011000	0.960	50	0110010	1.220	76	1001100	1.480
25	0011001	0.970	51	0110011	1.230	>76	>1001100	Illegal / Special

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1.3.2 Slow-Start Time

The slow-start time can be adjusted by changing the value of C5. Use Equation 2 to calculate the required value of C5 for a desired slow-start time

$$C5(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)} \quad (2)$$

The EVM is set for a slow-start time of 5.7 ms using C5 = 0.01 µF.

1.3.3 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R1 and R2. The EVM is set to use the internal UVLO and R1 and R2 are not populated. Use Equation 3 and Equation 4 to calculate required resistor values for different start and stop voltages.

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (3)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (4)$$

1.3.4 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected using a jumper across JP1. The single input voltage is supplied at J2. If desired, these two input voltage rails may be separated by removing the jumper across JP1. Two input voltages must then be provided at both J1 and J2.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS56921EVM-188 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS56921EVM-188 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 4 A must be connected to J2 through a pair of 20-AWG wires. The jumper across JP1 must be in place. See Section 1.3.4 for split-input voltage rail operation. The load must be connected to J4 through a pair of 20-AWG wires. The maximum load current capability must be 9 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP3 provides a place to monitor the V_{IN} input voltages with TP4 providing a convenient ground reference. TP9 is used to monitor the output voltage with TP10 as the ground reference.

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Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	VIN input voltage connector. Not normally used.
J2	PVIN input voltage connector. (See Table 1 for V_{IN} range.)
J3	I^2C interface connector.
J4	V_{OUT}, 1.1 V at 9 A maximum
JP1	PVIN to VIN jumper. Normally closed to tie VIN to PVIN for common rail voltage operation.
JP2	2-pin header for enable. Connect EN to ground to disable, open to enable.
JP3	I^2C interface pull up jumper for SDA.
JP4	I^2C interface pull up jumper for SCL.
JP5	I^2C interface grounding jumper for A0.
JP6	I^2C interface grounding jumper for A1.
JP7	PWRGD pull up to Vin. (1)
TP1	VIN test point at VIN connector.
TP2	GND test point at VIN connector.
TP3	PVIN test point at PVIN connector.
TP4	GND test point at PVIN connector.
TP5	PWRGD test point.
TP6	PH test point.
TP7	COMP pin test point.
TP8	Analog GND test point.
TP9	Test point in voltage divider network at VO. Used for loop response measurements when output voltage is set using I^2C control.
TP10	Test point in voltage divider network. Used for loop response measurements when output voltage is set using external resistor divider network.
TP11	Output voltage test point at VOUT connector.
TP12	GND test point at VOUT connector.

(1) Absolute maximum voltage for PWRGD is 6 V. Do not use JP7 to connect to VIN for input voltages above 6 V.

2.2 Efficiency

Figure 1 shows the efficiency for the TPS56921EVM-188 at an ambient temperature of 25°C.

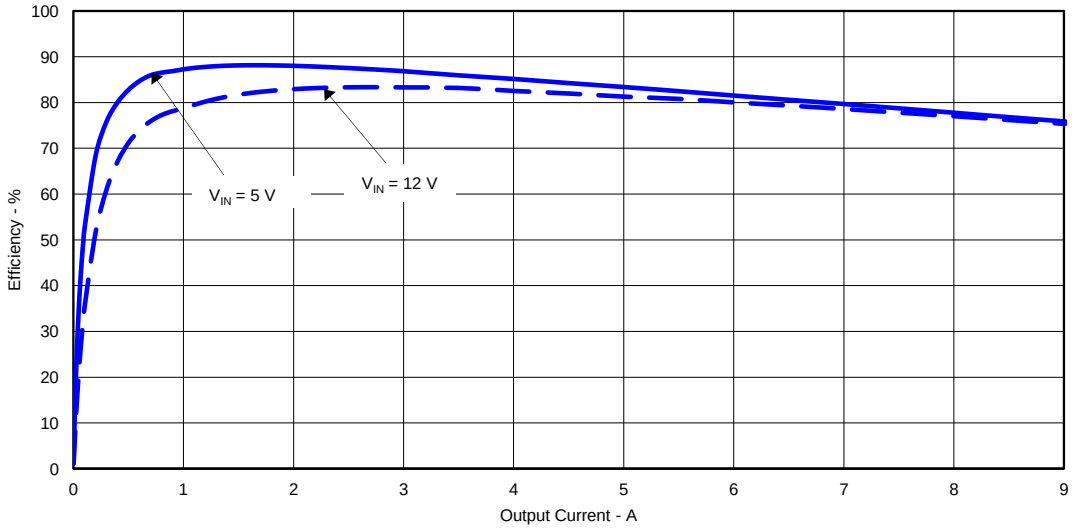

Figure 1. TPS56921EVM-188 Efficiency

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Figure 2 shows the efficiency for the TPS56921EVM-188 using a semi-log scale to more easily show efficiency at lower output currents. The ambient temperature is 25°C.

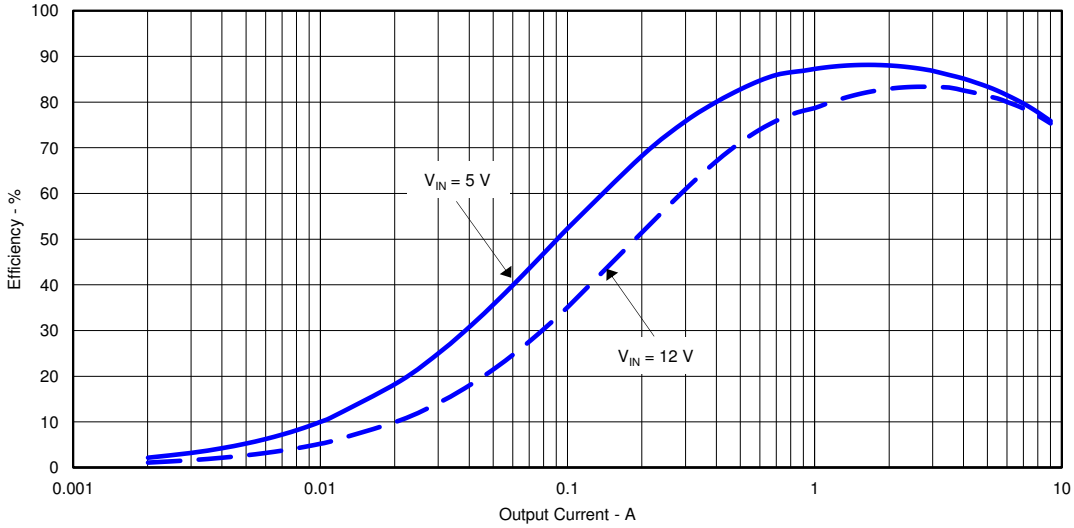

Figure 2. TPS56921EVM-188 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 3 shows the load regulation for the TPS56921EVM-188.

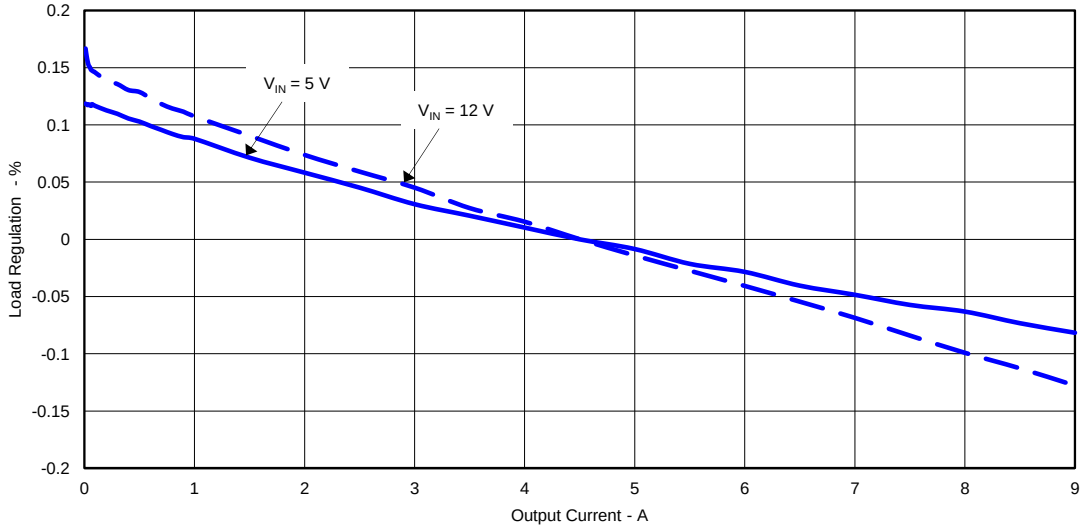

Figure 3. TPS56921EVM-188 Load Regulation

Measurements are given for an ambient temperature of 25°C.

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2.4 Output Voltage Line Regulation

Figure 4 shows the line regulation for the TPS56921EVM-188.

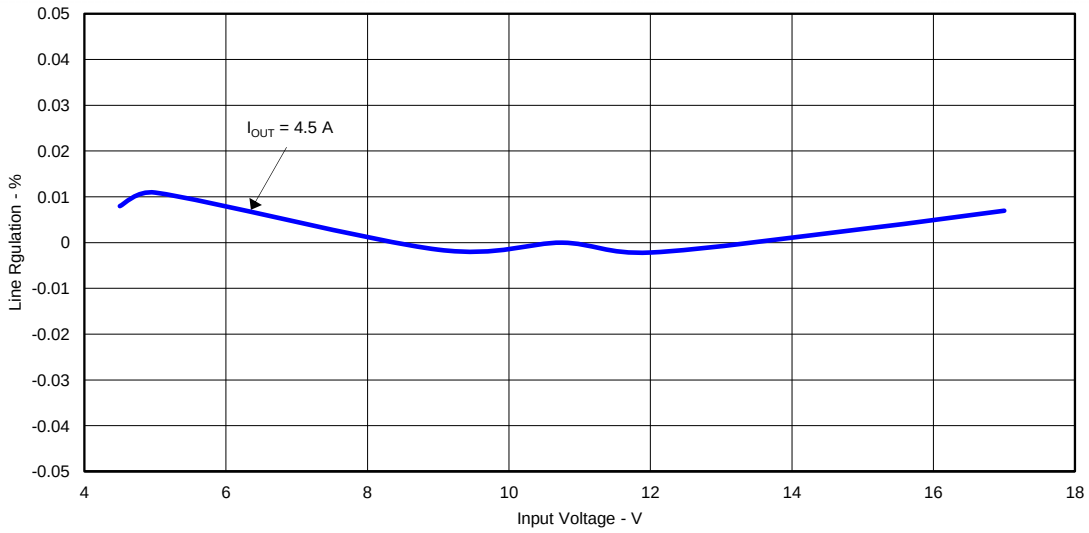

Figure 4. TPS56921EVM-188 Line Regulation

2.5 Load Transients

Figure 5 shows the TPS56921EVM-188 response to load transients. The current step is from 25% to 75% of maximum rated load at 12-V input. The current step slew rate is 100 mA/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

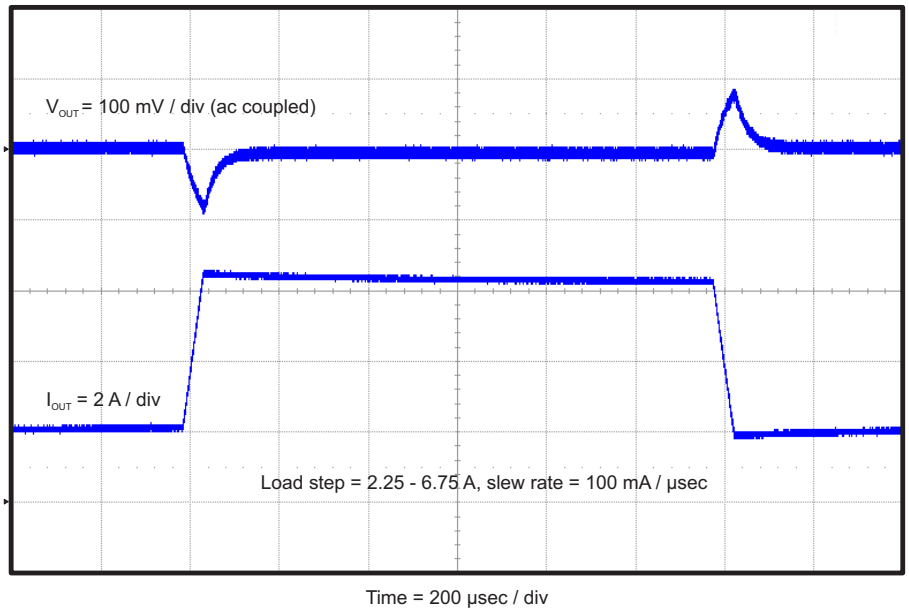

Figure 5. TPS56921EVM-188 Transient Response

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2.6 Loop Characteristics

Figure 6 shows the TPS56921EVM-188 loop-response characteristics when the output voltage is set by the external resistor divider network. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 4 A.

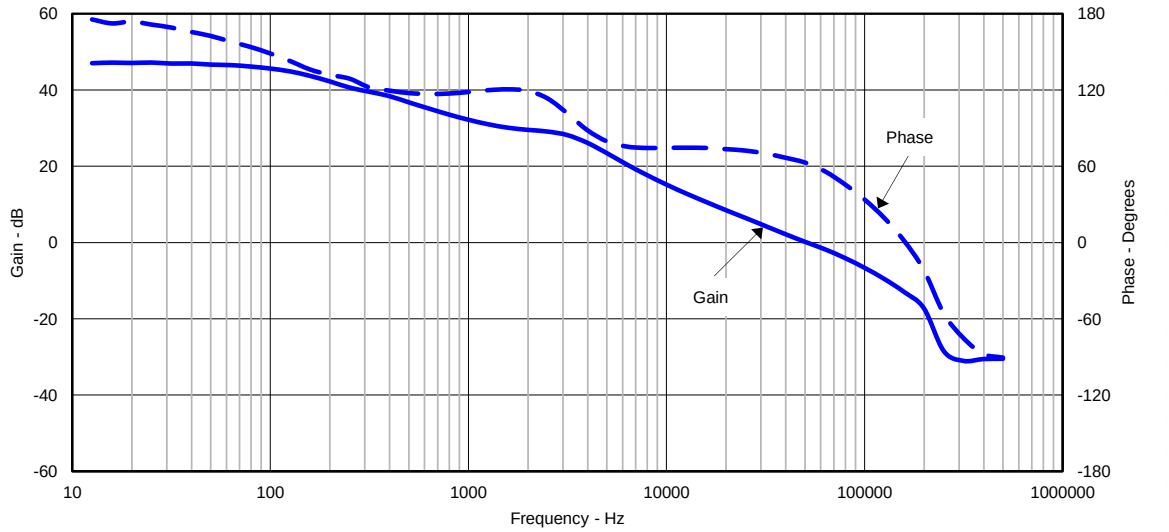

Figure 6. TPS56921EVM-188 Loop Response, V_{OUT} Set by Resistor Divider

Figure 7 shows the TPS56921EVM-188 loop-response characteristics when the output voltage is set by the external resistor divider network. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 4 A.

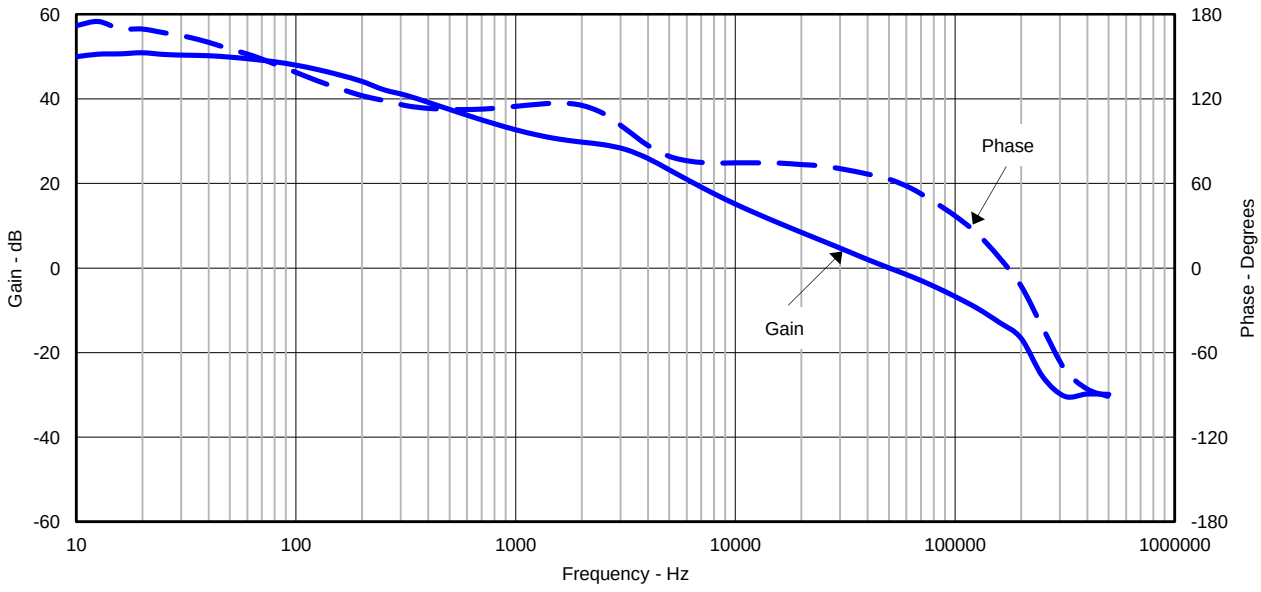

Figure 7. TPS56921EVM-188 Loop Response, V_{OUT} Set by I^2C Interface

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2.7 Output Voltage Ripple

Figure 8 shows the TPS56921EVM-188 output voltage ripple. The output current is the rated full load of 9 A and V_{IN} = 12 V. The ripple voltage is measured directly across the output capacitors.

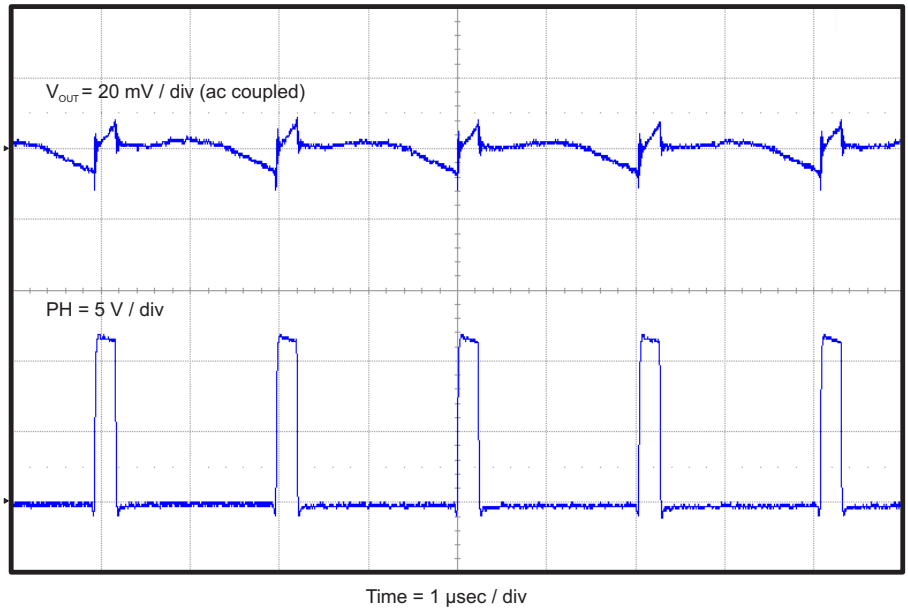

Figure 8. TPS56921EVM-188 Output Ripple

2.8 Input Voltage Ripple

Figure 9 shows the TPS56921EVM-188 input voltage. The output current is the rated full load of 9 A and V_{IN} = 12 V. The ripple voltage is measured directly across the input capacitors.

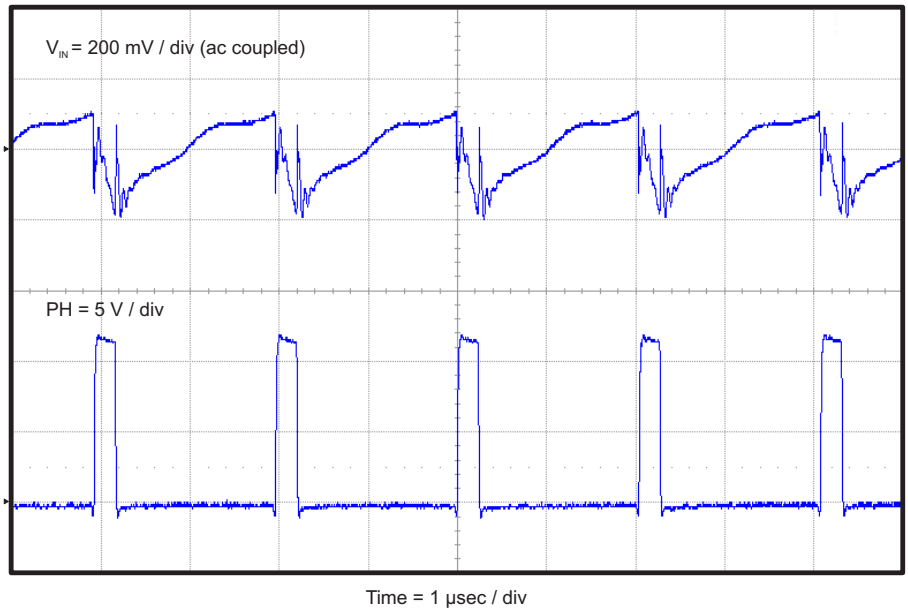

Figure 9. TPS56921EVM-188 Input Ripple

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2.9 Powering Up

Figure 10 and Figure 11 show the start-up waveforms for the TPS56921EVM-188. In Figure 10, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1 and R2 resistor divider network. In Figure 11, the input voltage is initially applied and the output is inhibited by using a jumper at JP2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.1 V. The input voltage for these plots is 12 V and the load is 1 Ω. Figure 12 shows a detailed view of the output voltage ramp up.

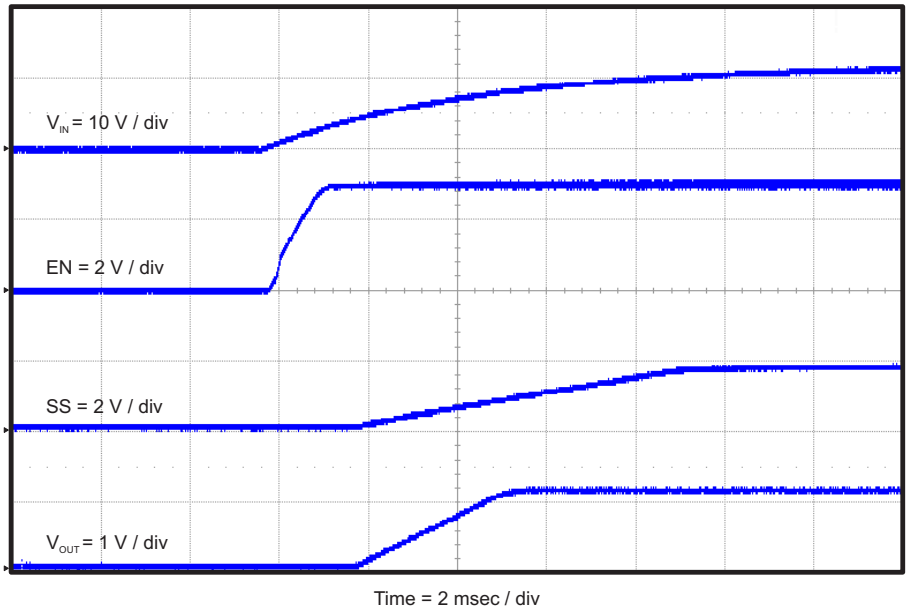

Figure 10. TPS56921EVM-188 Start-Up Relative to V_{IN}

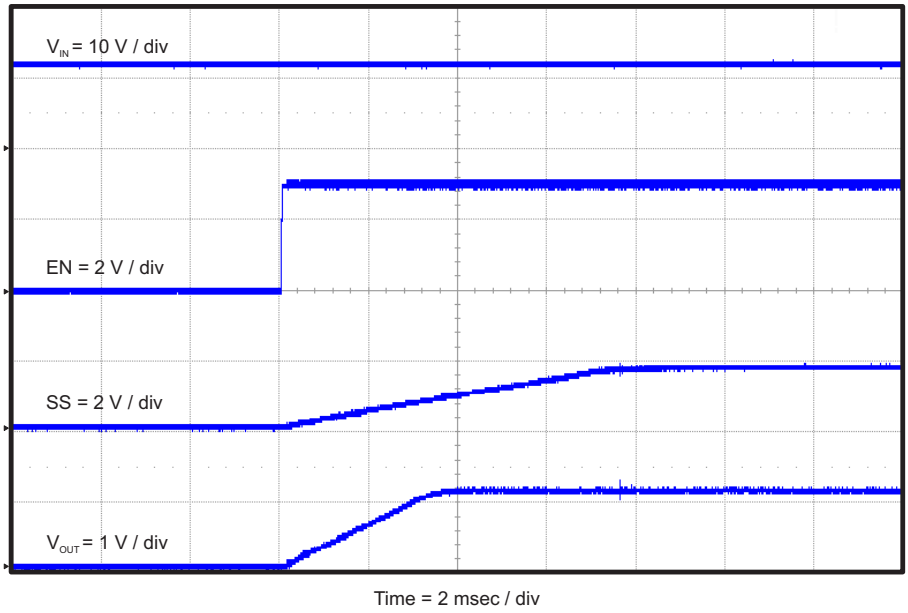

Figure 11. TPS56921EVM-188 Start-Up Relative to Enable

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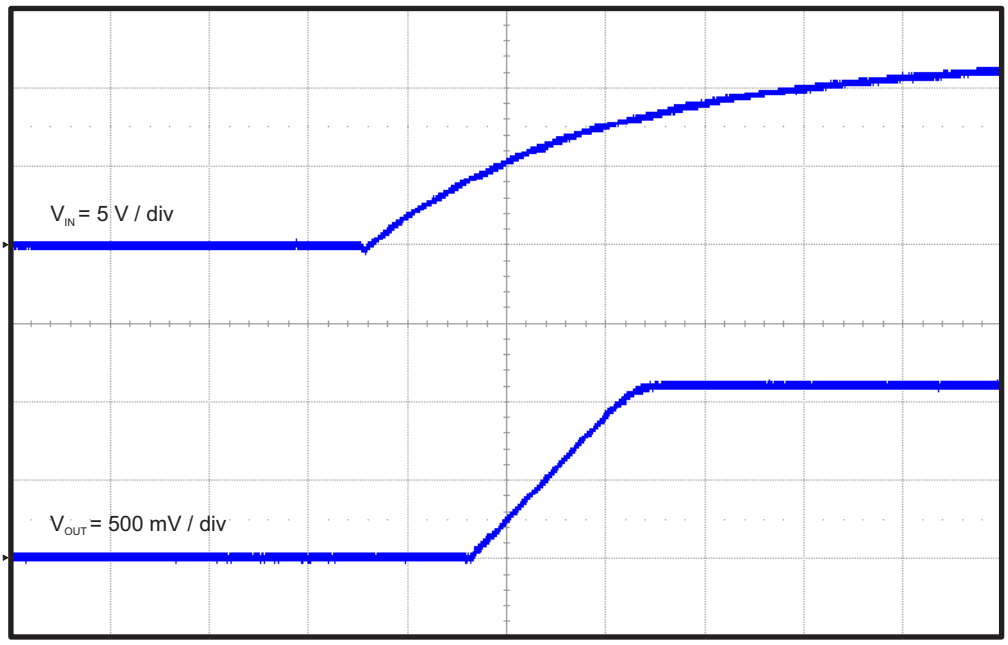

Figure 12. TPS56921EVM-188 Start-Up Relative to V_{IN} Detail

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3 Board Layout

This section provides a description of the TPS56921EVM-188 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS56921EVM-188 is shown in Figure 13 through Figure 17. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for PVIN, VIN, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS56921 and a large area filled with ground. The internal layer-1 is dedicated to a power ground plane. the internal layer-2 contains an analog ground fill area. This analog ground is used as a return for the I^2C interface as well as for sensitive analog circuits for RT, SS, EN, COMP and VSENSE. The analog ground is connected to the main power ground at one place to inhibit circulating currents. This connection is made at the via near TP7. Internal layer-2 also contains additional fill areas for PVIN and V_{OUT}, as well as connections to the I^2C interface connector at J3. The bottom layer contains a power ground plane only. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board including nine vias directly under the TPS56921 and 12 vias directly adjacent to the TPS56921device to provide a thermal path from the top-side ground area to the internal layer-1 and bottom-side ground planes.

The input decoupling capacitors (C1,C2, C3 and C4) and bootstrap capacitor (C8) are all located as close to the IC as possible. Additionally, the voltage setpoint resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the J4 output connector. For the TPS56921, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply.

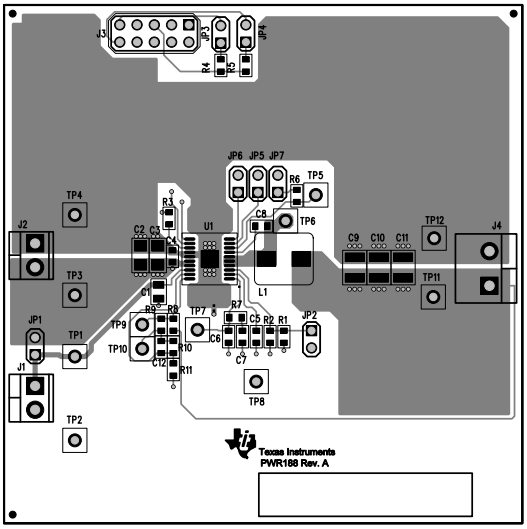

Figure 13. TPS56921EVM-188 Top-Side Assembly

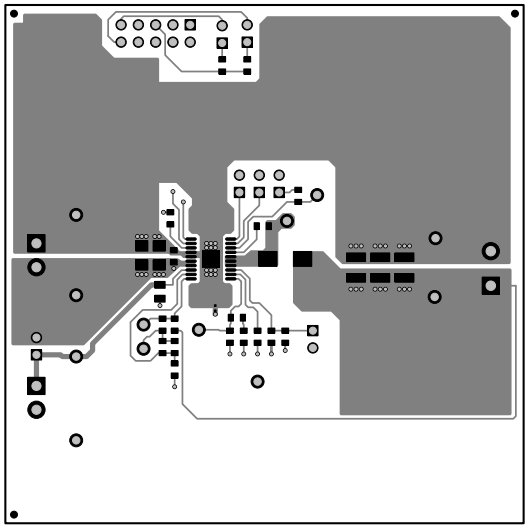

Figure 14. TPS56921EVM-188 Top-Side Layout

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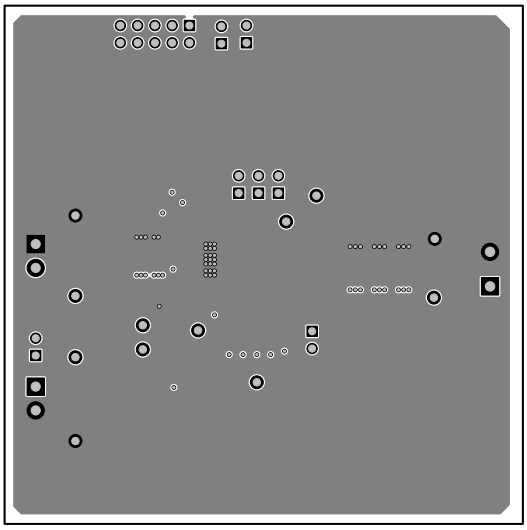

Figure 15. TPS56921EVM-188 Internal Layer-1 Layout

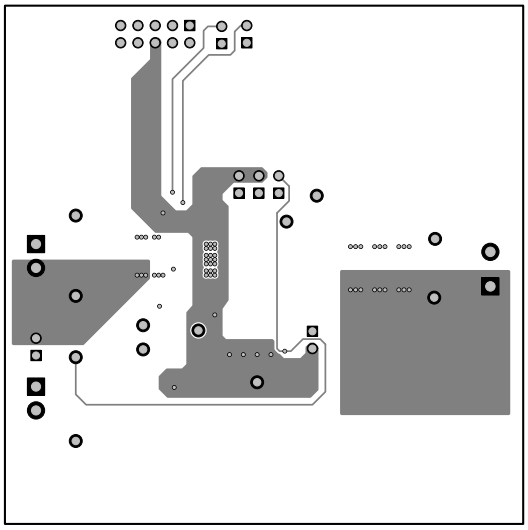

Figure 16. TPS56921EVM-188 Internal Layer-2 Layout

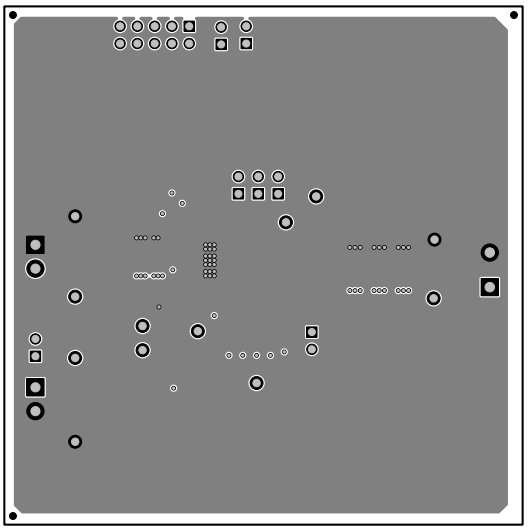

Figure 17. TPS56921EVM-188 Bottom-Side Layout

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4 Schematic and Bill of Materials

This section presents the TPS56921EVM-188 schematic and bill of materials.

4.1 Schematic

Figure 18 is the schematic for the TPS56921EVM-188.

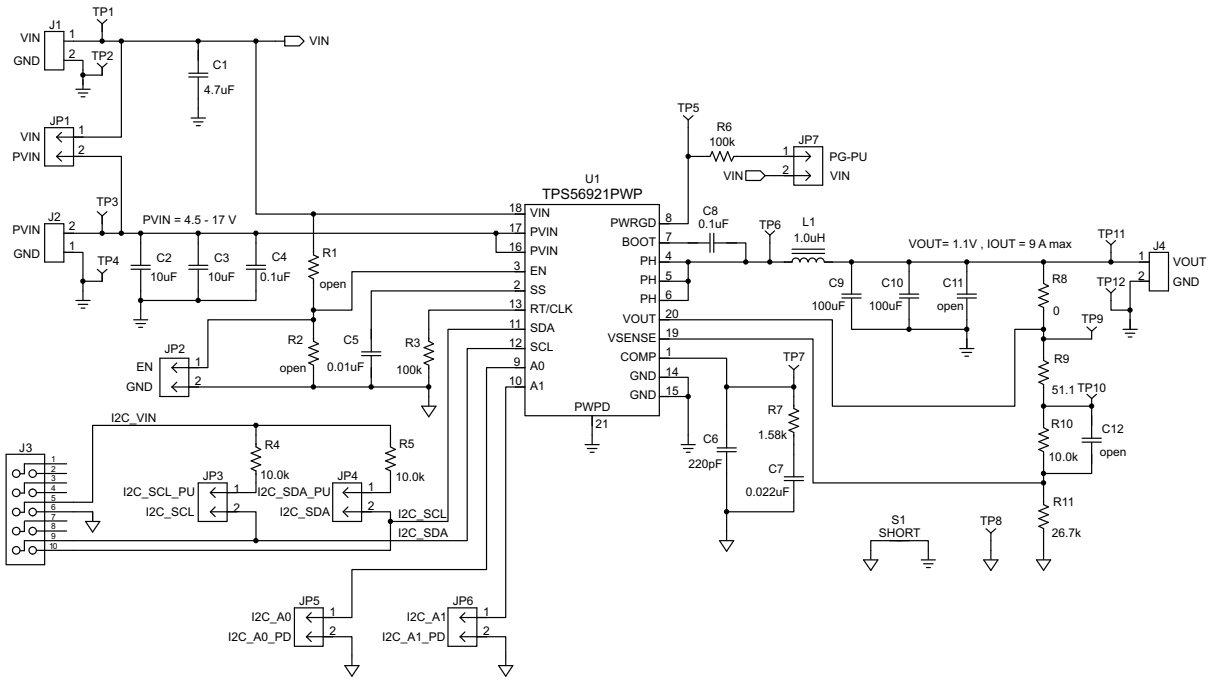

Figure 18. TPS56921EVM-188 Schematic

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4.2 Bill of Materials

Table 5 presents the bill of materials for the TPS56921EVM-188.

Table 5. TPS56921EVM-188 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	4.7uF	Capacitor, Ceramic, 25V, X5R, 10%	805	Std	Std
2	C2, C3	10uF	Capacitor, Ceramic, 25V, X5R, 10%	1206	Std	Std
2	C4, C8	0.1uF	Capacitor, Ceramic, 25V, X5R, 10%	603	Std	Std
1	C5	0.01uF	Capacitor, Ceramic, 25V, X7R, 10%	603	Std	Std
1	C6	220pF	Capacitor, Ceramic, 50V, NPO, 5%	603	Std	Std
1	C7	0.022uF	Capacitor, Ceramic, 50V, X7R, 10%	603	Std	Std
2	C9, C10	100uF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	Std	Std
0	C11	open	Capacitor, Ceramic	1210	Std	Std
0	C12	open	Capacitor, Ceramic	603	Std	Std
7	JP1, JP2, JP3, JP4, JP5, JP6, JP7	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
2	J1, J2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
1	J3	PEC05DAAN	Header, Male 2x5-pin, 100mil spacing	0.100 inch x 5 X 2	PEC05DAAN	Sullins
1	J4	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
1	L1	1.0uH	Inductor, Power Choke	7.0 x 6.9 mm	744311100	Wurth Elektronik
0	R1	open	Resistor, Chip, 1/16W, 1%	603	Std	Std
0	R2	open	Resistor, Chip, 1/16W, 1%	603	Std	Std
2	R3, R6	100k	Resistor, Chip, 1/16W, 1%	603	Std	Std
3	R4, R5, R10	10.0k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R7	1.58k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R8	0	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R9	51.1	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R11	26.7k	Resistor, Chip, 1/16W, 1%	603	Std	Std
3	TP1, TP3,TP11	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
4	TP2, TP4 ,TP8, TP12	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
5	TP5, TP6, TP7, TP9, TP10	5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	U1	TPS56921PWP	IC, 4.5V to 17V Input, 9A Synchronous Step Down SWIFTConverter With VID Control	HTSSOP	TPS56921PWP	TI
7	--		Shunt, 100-mil, Black	0.100	929950-00	3M
1	--		Label (See Note 5)	1.25 x 0.25 inch	THT-13-457-10	Brady
1	--		PCB, 3" x 3" x 0.062"		PWR188	Any

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 4.5 V to 17 V and the output voltage range of 0.6 V to 5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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