User's Guide
SLVUBD0–January 2018

TPS563249EVM-031 17-V, 3-A, Regulator Evaluation Module

This user's guide contains information for the TPS563249 as well as support documentation for the TPS563249EVM-031 evaluation module. Included are the performance specifications, schematic, and the bill of materials (BOM) of the TPS563249EVM-031.

Contents

1 Introduction 2
2 Performance Specification Summary 2
3 Modifications 3
4 Test Setup 3
4.1 Input/Output Connections 3
4.2 Start-Up Procedure 4
5 Board Layout 5
6 Schematic, Bill of Materials, and Reference 6
6.1 Schematic 6
6.2 Bill of Materials 7

List of Figures

1 Top Layer 5
2 Bottom Layer 6
3 TPS563249EVM-031 Schematic Diagram 6

List of Tables

1 Input Voltage and Output Current Summary 2
2 TPS563249EVM-031 Performance Specifications Summary 2
3 Recommended Component Values 3
4 Connection and Test Points 4
5 Bill of Materials 7

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1 Introduction

The TPS563249 is a single, adaptive on-time, D-CAP3™ mode, synchronous buck converter requiring a very low external component count. The D-CAP3 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 1.4 MHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS563249 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS563249 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS563249 dc/dc synchronous converter is designed to provide up to a 3-A output from an input voltage source of 4.5 V to 17 V. Rated input voltage and output current ranges for the evaluation module are given in Table 1.

The TPS563249EVM-031 evaluation module (EVM) is a single, synchronous buck converter providing 3.3 V at 3 A from 4.5-V to 17-V input. This user's guide describes the TPS563249EVM-031 performance.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage (V_{IN}) Range	Output Current (I_{OUT}) Range
TPS563249EVM-031	4.5 V to 17 V	0 A to 3 A

2 Performance Specification Summary

A summary of the TPS563249EVM-031 performance specifications is provided in Table 2. Specifications are given for an input voltage of 12 V and an output voltage of 3.3 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2. TPS563249EVM-031 Performance Specifications Summary

Specifications		Test Conditions	MIN	TYP	MAX	Unit
V_{IN}	Input voltage		4.5	12	17	V
CH1	Output voltage			3.3		V
	Operating frequency	V_{IN} = 12 V, I_{OUT} = 3 A		1.4		MHz
	Output current range		0		3	A

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3 Modifications

These evaluation modules are designed to provide access to the features of the TPS563249. Some modifications can be made to this module.

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.60 V. The value of R1 for a specific output voltage can be calculated using Equation 1.

$$V_{OUT} = 0.6 \times (1 + \frac{R1}{R2}) \quad (1)$$

Table 3 lists the R1 values for some common output voltages. Note that the values given in Table 3 are standard values and not the exact value calculated using Table 3.

Table 3. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C5 + C6 (µF)
			MIN	TYP	MAX	
1	6.65	10.0	0.33	0.56	1	10 to 44
1.05	7.5	10.0	0.33	0.56	1	10 to 44
1.2	10	10.0	0.33	0.68	1.5	10 to 44
1.5	15	10.0	0.47	0.82	1.5	10 to 44
1.8	20	10.0	0.56	1	2.2	10 to 44
2.5	31.6	10.0	0.68	1	2.2	10 to 44
3.3	45.3	10.0	0.82	1.5	3.3	10 to 44
5	73.2	10.0	1	1.5	3.3	10 to 44
6.5	97.6	10.0	1	2.2	3.3	10 to 44

4 Test Setup

This section describes how to properly connect, set up, and use the TPS563249EVM-031.

4.1 Input/Output Connections

The TPS563249EVM-031 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 3 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 3 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP6 is used to monitor the output voltage with TP7 as the ground reference.

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Table 4. Connection and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range)
J2	V_{OUT}, 3.3 V at 3-A maximum
JP1	EN control. Shunt EN to GND to disable, shunt EN to V_{IN} to enable.
TP1	V_{IN} positive monitor point
TP2	GND monitor test point
TP3	EN test point
TP4	Switch node test point
TP5	Test point for loop response measurements
TP6	V_{OUT} positive monitor point
TP7	GND monitor test point
TP8	GND monitor test point

4.2 Start-Up Procedure

Use the following steps during start-up:

1. Ensure that the jumper at JP1 (Enable control) pins 1 and 2 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate input voltage to VIN (J1-1) and GND (J1-2).
3. Move the jumper at JP1 (Enable control) from pins 1 and 2 (EN and GND), to pins 2 and 3 (EN and V_{IN}) enabling the output.

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5 Board Layout

This section provides a description of the TPS563249EVM-031, board layout, and layer illustrations.

The board layout for the TPS563249EVM-031 is shown in Figure 1, and Figure 2. The top layer contains the main power traces for V_{IN}, V_{OUT}, and ground. Also on the top layer are connections for the pins of the TPS563249 and a large area filled with ground. Most of the signal traces are also located on the top side. The input decoupling capacitors, C1, C2, and C3 are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. The bottom layer is a ground plane along with the switching node copper fill, signal ground copper fill and the feed back trace from the point of regulation to the top of the resistor divider network.

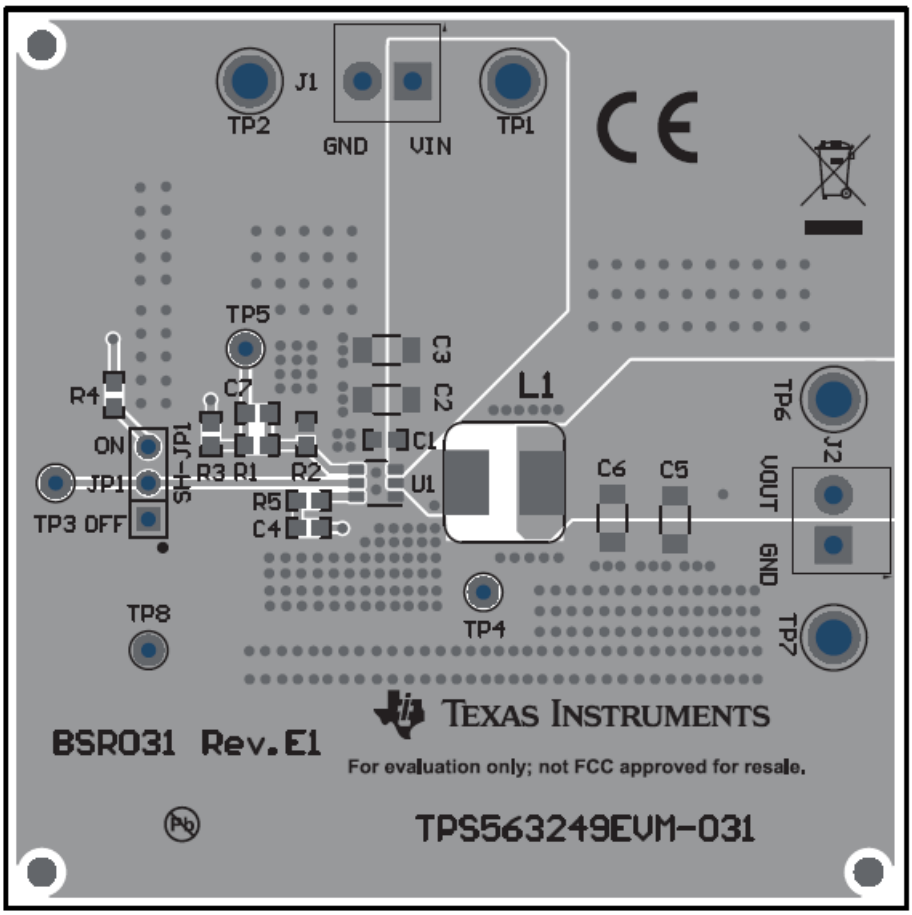


Figure 1. Top Layer

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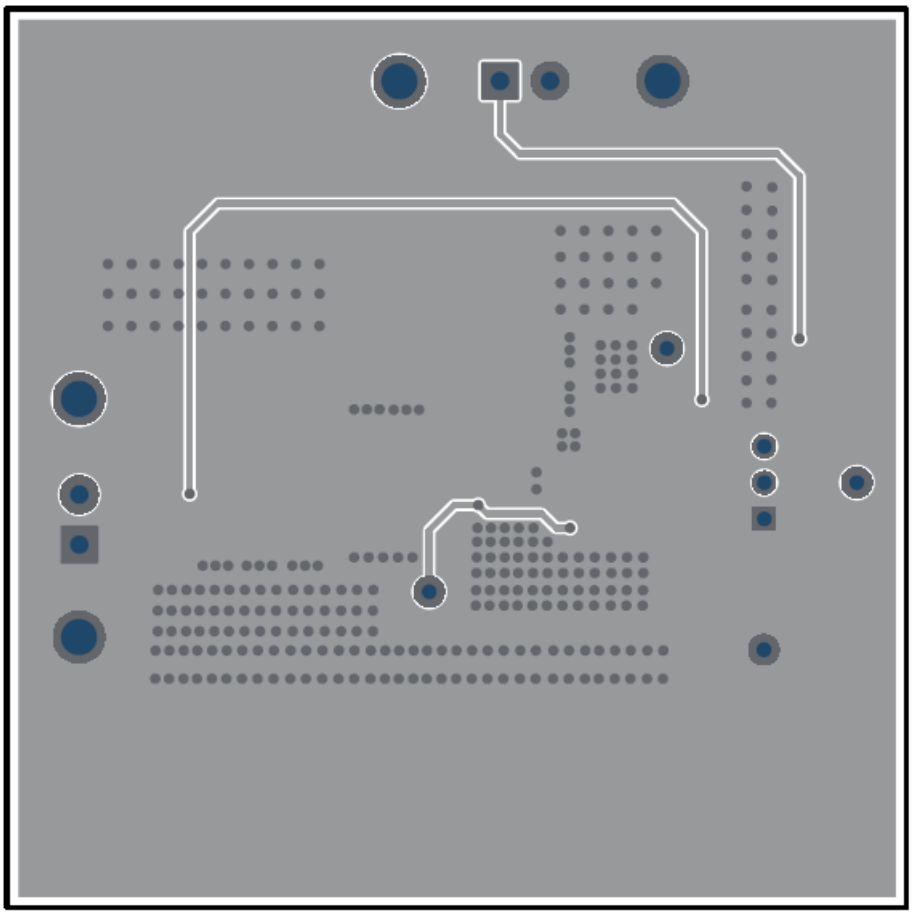


Figure 2. Bottom Layer

6 Schematic, Bill of Materials, and Reference

6.1 Schematic

Figure 3 is the schematic for the TPS563249EVM-031.

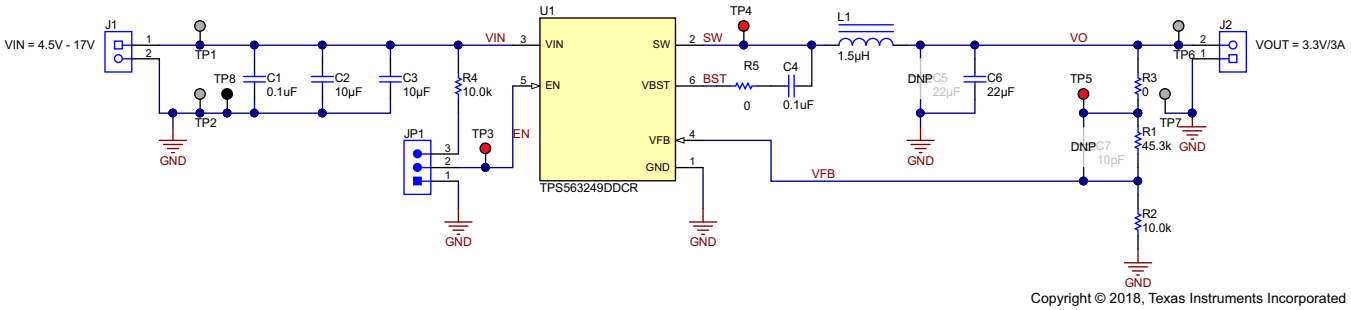


Figure 3. TPS563249EVM-031 Schematic Diagram

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6.2 Bill of Materials

Table 5 displays the TPS563249EVM-031 BOM.

Table 5. Bill of Materials(1)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		BSR031	Any	-	-
C1, C4	2	0.1uF	CAP, CERM, 0.1uF, 25V, ±10%, X5R, 0603	0603	GRM188R61E104KA01D	Murata		
C2, C3	2	10uF	CAP, CERM, 10 µF, 25 V,± 10%, X5R, 1206	1206	GRM31CR61E106KA12L	Murata		
C6	1	22uF	CAP, CERM, 22 µF, 10 V,± 10%, X7R, 1206	1206	GRM31CR71A226KE15L	Murata		
J1, J2	2		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology		
JP1	1		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions		
L1	1	1.5uH	Inductor, Shielded Drum Core, Superflux, 1.5 µH, 11 A, 0.0078 ohm, SMD	WE-HC4	744311150	Wurth Elektronik		
R1	1	45.3k	RES, 45.3 k ohm, 1%, 0.1W, 0603	0603	CRCW060345K3FKEA	Vishay-Dale		
R2, R4	2	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale		
R3, R5	2	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	ERJ-3GEY0R00V	Panasonic		
SH-JP1	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M	SNT-100-BK-G	Samtec
TP1, TP2, TP6, TP7	4		Terminal, Turret, TH, Double	Keystone1502-2	1502-2	Keystone		
TP3, TP4, TP5	3		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone		
TP8	1		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
U1	1		17 V, 3 A, 1.4 MHz Synchronous Step-Down Voltage Regulator, DDC0006A (SOT-23-T-6)		TPS563249DDCR	Texas Instruments	TPS563249DDCT	Texas Instruments
C5	0	22uF	CAP, CERM, 22 µF, 10 V,± 10%, X7R, 1206	1206	GRM31CR71A226KE15L	Murata		
C7	0	10pF	CAP, CERM, 10 pF, 100 V, ± 5%, C0G/NP0, 0603	0603	GRM1885C2A100JA01D	Murata		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A		

(1) Unless otherwise noted in the *Alternate Part Number* or *Alternate Manufacturer* columns, all parts may be substituted with equivalents.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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