TPS55330 集成式 5A 24V 升压/SEPIC/反激式 DC/DC 稳压器

1 特性

- 内部 5A、24V 低侧 MOSFET 开关
- 2.9 V 至 16 V 输入电压范围
- ±0.7% 基准电压
- 0.5mA 静态工作电流
- 2.7μA 关断电源电流
- 固定频率电流模式脉宽调制 (PWM) 控制
- 可在 100kHz 至 1.2MHz 之间进行频率调节
- 同步外部时钟功能
- 可调软启动时间
- 用于在轻负载时实现较高效率的脉冲跳跃模式
- 逐周期电流限制、热关断、和欠压闭锁 (UVLO) 保护
- QFN-16 (3mm × 3mm) 封装，带有 PowerPAD™
- 宽 T_J 运行范围：-40°C 至 +150°C
- 使用 TPS55330 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 3.3，5V，12V 功率转换
- 升压、SEPIC 和反激式拓扑结构
- 用于平板电脑和便携式个人电脑 (PC) 的霹雳 (Thunderbolt) 端口、电源扩展坞
- 工业电源系统
- 非对称用户数字环路 (ADSL) 调制解调器 (Modem)

3 说明

TPS55330 是一款单片非同步开关稳压器，此稳压器集成有一个 5A、24V 电源开关。此器件可配置成多种标准开关稳压器拓扑，包括升压、SEPIC 和隔离反激式。此器件具有宽输入电压范围，可支持 那些 输入电压来自多节电池或 3.3V、5V 和 12V 稳压电源轨的应用。

TPS55330 使用电流模式 PWM（脉宽调制）控制来调节输出电压，并具有一个内部振荡器。PWM 的开关频率由一个外部电阻器设定或者同步至一个外部时钟信号。用户可以在
100kHz 至 1.2MHz 之间对开关频率进行设定。

该器件在关闭状态下 具有 可编程软启动功能，用于限制启动时的浪涌电流；并且还内置有其它保护 特性，包括逐周期过流限制和热关断。

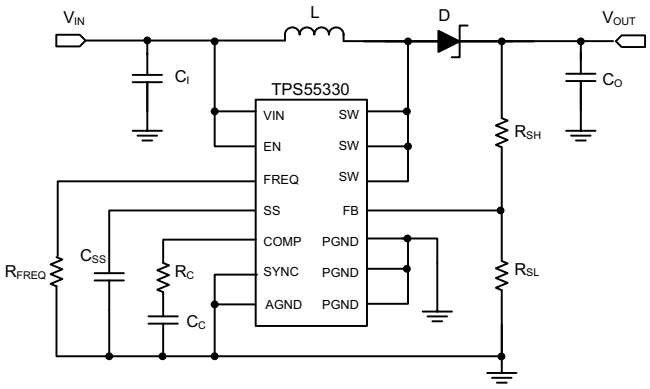
TPS55330 采用小型 3mm × 3mm 16 引脚 QFN 封装，该封装配有 PowerPAD 以增强散热性能。

器件信息(1)

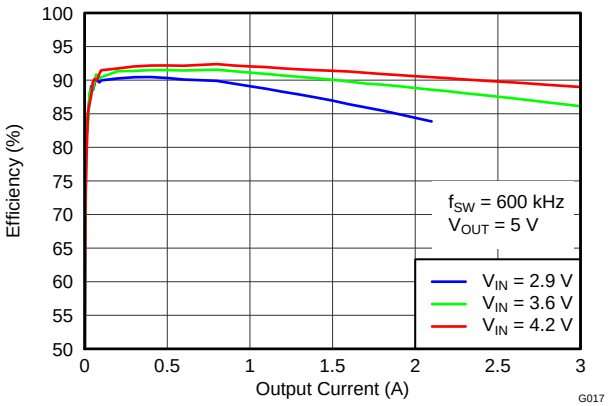
器件型号	封装	封装尺寸（标称值）
TPS55330	WQFN (16)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用（升压）



效率与输出电流间的关系



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 6
7 **Detailed Description** ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 9
7.3 Feature Description ... 9
7.4 Device Functional Modes ... 12
8 **Application and Implementation** ... 13
8.1 Application Information ... 13
8.2 Typical Application ... 13
9 **Power Supply Recommendations** ... 22
10 **Layout** ... 22
10.1 Layout Guidelines ... 22
10.2 Layout Example ... 22
10.3 Thermal Considerations ... 23
11 器件和文档支持 ... 24
11.1 器件支持 ... 24
11.2 接收文档更新通知 ... 24
11.3 社区资源 ... 24
11.4 商标 ... 24
11.5 静电放电警告 ... 24
11.6 术语表 ... 24
12 机械、封装和可订购信息 ... 25

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (October 2014) to Revision B **Page**

- 已添加 Webench 链接 ... 1
- Added text note under pin configuration diagram ... 3

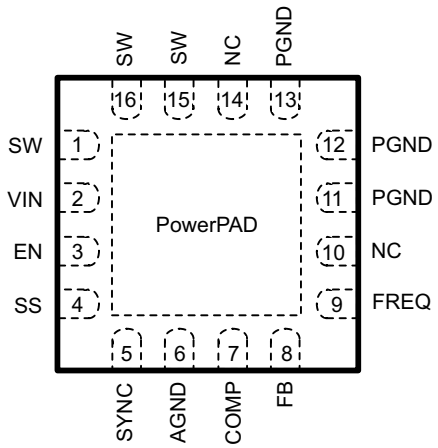
Changes from Original (May 2013) to Revision A **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Copyright © 2013–2019, Texas Instruments Incorporated

5 Pin Configuration and Functions

16-Pin RTE
QFN Package
Top View



TI recommends connecting NC with AGND.

Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
VIN	2	The input supply pin to the IC. Connect VIN to a supply voltage between 2.9 V and 16 V. It is acceptable for the voltage on the pin to be different from the boost power stage input.
SW	1, 15, 16	SW is the drain of the internal power MOSFET. Connect SW to the switched side of the boost or SEPIC inductor or the flyback transformer.
FB	8	Error amplifier input and feedback pin for positive voltage regulation. Connect to the center tap of a resistor divider to program the output voltage.
EN	3	Enable pin. When the voltage of this pin falls below the enable threshold for more than 1 ms, the IC turns off.
COMP	7	Output of the transconductance error amplifier. An external RC network connected to this pin compensates the regulator feedback loop.
SS	4	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start timing.
FREQ	9	Switching frequency program pin. An external resistor connected between the FREQ pin and AGND sets the switching frequency.
AGND	6	Signal ground of the IC.
PGND	11, 12, 13	Power ground of the IC. It is connected to the source of the internal power MOSFET switch.
SYNC	5	Switching frequency synchronization pin. An external clock signal can be used to set the switching frequency between 200 kHz and 1 MHz. If not used, this pin should be tied to AGND.
NC	10, 14	Reserved pin that must be connected to ground.
PowerPAD	17	Solder the PowerPAD to the AGND. If possible, use thermal vias to connect to internal ground plane for improved power dissipation.

Copyright © 2013–2019, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Supply voltages on pin VIN(2)	–0.3	18	V
	Voltage on pin EN(2)	–0.3	18	V
	Voltage on pins FB, FREQ, and COMP(2)	–0.3	3	V
	Voltage on pin SS(2)	–0.3	5	V
	Voltage on pin SYNC(2)	–0.3	7	V
	Voltage on pin SW(2)	–0.3	24	V
	Operating junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage range	2.9	16	V
V_{OUT}	Output voltage range	V_{IN}	22	V
V_{EN}	EN voltage range	0	16	V
V_{SYN}	External switching frequency logic input range	0	5	V
T_A	Operating free-air temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS55330 QFN 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	14.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2013–2019, Texas Instruments Incorporated

6.5 Electrical Characteristics

V_{IN} = 5 V, T_J = –40°C to +150°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.9		16	V
I_Q	Operating quiescent current into V_{IN}	Device non-switching, V_{FB} = 2 V		0.5		mA
I_{SD}	Shutdown current	EN = GND		2.7	10	µA
V_{UVLO}	Under-voltage lockout threshold	V_{IN} falling		2.5	2.7	V
V_{hys}	Under-voltage lockout hysteresis		120	140	160	mV
ENABLE AND REFERENCE CONTROL						
$V_{EN(r)}$	EN threshold voltage	EN rising input	0.9	1.08	1.30	V
$V_{EN(f)}$	EN threshold voltage	EN falling input	0.74	0.92	1.125	V
V_{ENh}	EN threshold hysteresis			0.16		V
R_{EN}	EN pulldown resistor		400	950	1600	kΩ
T_{off}	Shutdown delay, SS discharge	EN high to low		1.0		ms
V_{SYNh}	SYN logic high voltage		1.2			
V_{SYNl}	SYN logic low voltage				0.4	V
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		1.204	1.229	1.254	V
		T_A = 25°C	1.220	1.229	1.238	
I_{FB}	Voltage feedback input bias current	T_A = 25°C		1.6	20	nA
I_{sink}	Comp pin sink current	$V_{FB} = V_{REF}$ + 200 mV, V_{COMP} = 1 V		42		µA
I_{source}	Comp pin source current	$V_{FB} = V_{REF}$ – 200 mV, V_{COMP} = 1 V		42		µA
V_{CCLP}	Comp pin Clamp Voltage	High Clamp, V_{FB} = 1 V Low Clamp, V_{FB} = 1.5 V		3.1 0.75		V
V_{CTH}	Comp pin threshold	Duty cycle = 0%		1.04		V
G_{ea}	Error amplifier transconductance		240	360	440	µS
R_{ea}	Error amplifier output resistance			10		MΩ
f_{ea}	Error amplifier crossover frequency			500		kHz
FREQUENCY						
f_{SW}	Frequency	R_{FREQ} = 480 kΩ	75	94	130	kHz
		R_{FREQ} = 80 kΩ	460	577	740	
		R_{FREQ} = 40 kΩ	920	1140	1480	
D_{max}	Maximum duty cycle	V_{FB} = 1.0 V, R_{FREQ} = 80 kΩ	89%	96%		
V_{FREQ}	FREQ pin voltage			1.25		V
T_{min_on}	Minimum on pulse width	R_{FREQ} = 80 kΩ		77		ns
POWER SWITCH						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = 5 V V_{IN} = 3 V		60 70	110 120	mΩ
I_{LN_NFET}	N-channel leakage current	V_{DS} = 25 V, T_A = 25°C			2.1	µA
OCP and SS						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	5.25	6.6	7.75	A
I_{SS}	Soft-start bias current	V_{SS} = 0 V		6		µA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			165		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

Copyright © 2013–2019, Texas Instruments Incorporated

6.6 Typical Characteristics

V_{IN} = 5 V, T_A = 25°C (unless otherwise noted)

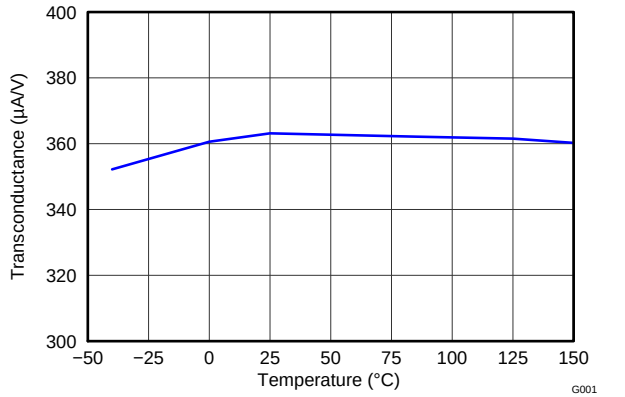


Figure 1. Error Amplifier Transconductance vs Temperature

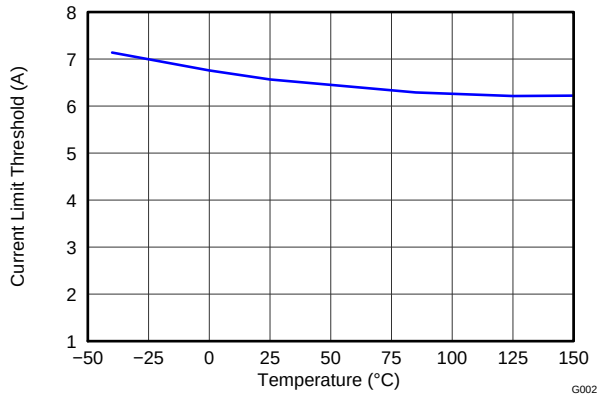


Figure 2. Switch Current Limit vs Temperature

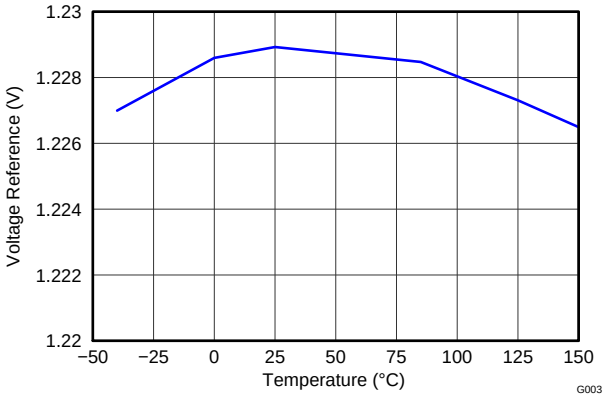


Figure 3. Feedback Voltage Reference vs Temperature

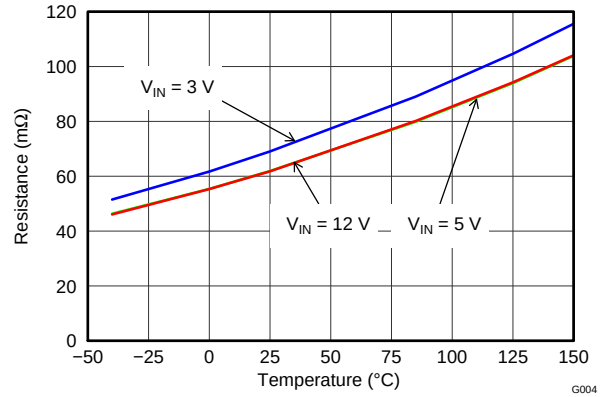


Figure 4. $R_{DS(ON)}$ vs Temperature

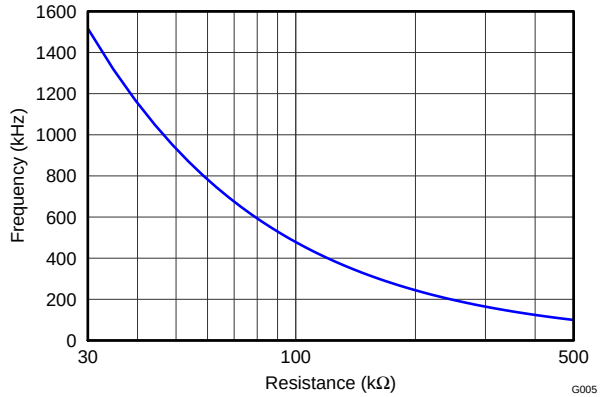


Figure 5. Frequency vs FREQ Resistance

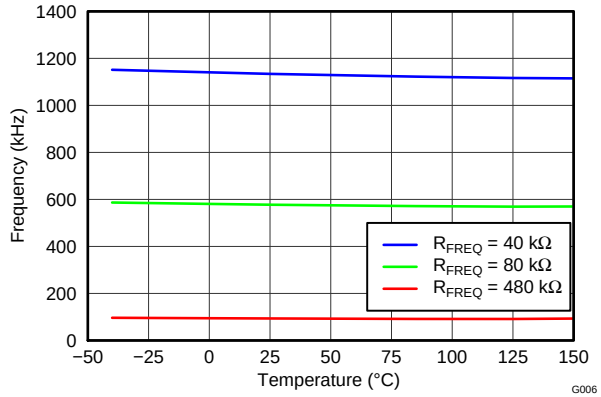


Figure 6. Frequency vs Temperature

Copyright © 2013–2019, Texas Instruments Incorporated

Typical Characteristics (continued)

V_{IN} = 5 V, T_A = 25°C (unless otherwise noted)

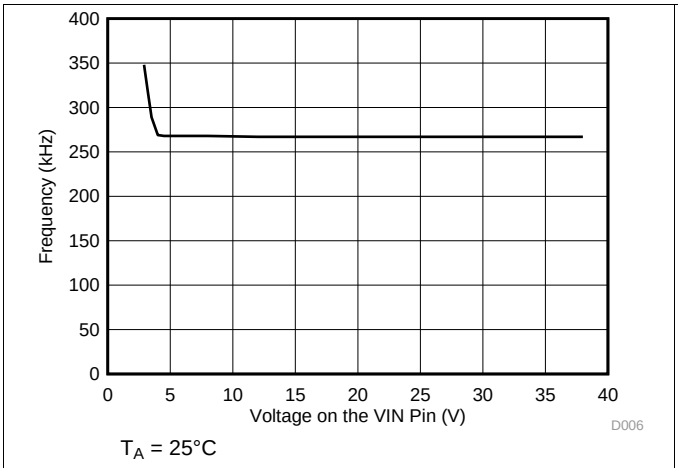


Figure 7. Minimum Switching Frequency for Quick Recovery from Frequency Foldback

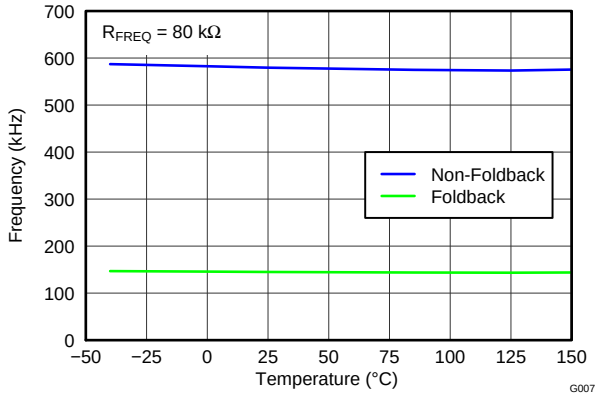


Figure 8. Non-Foldback Frequency vs Foldback Frequency

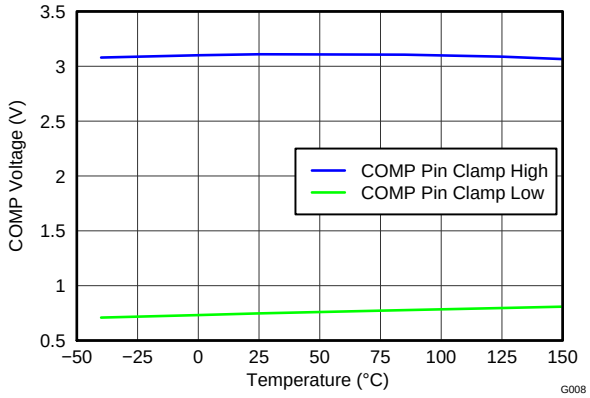


Figure 9. COMP Clamp Voltage vs Temperature

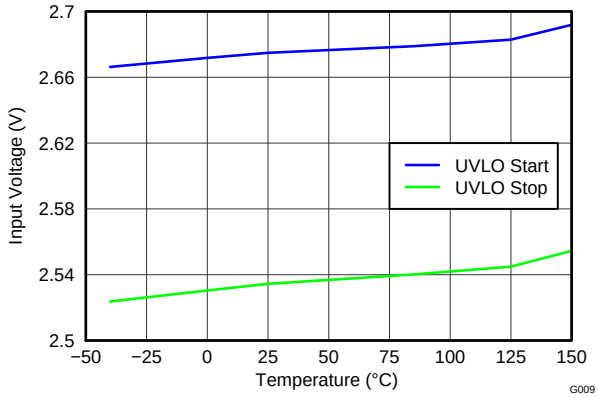


Figure 10. Input Voltage UVLO vs Temperature

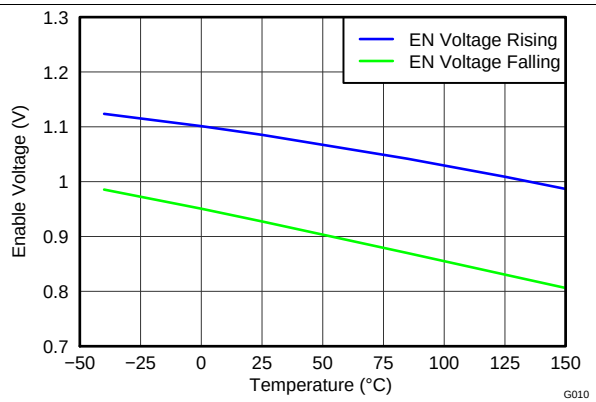


Figure 11. Enable Voltage vs Temperature

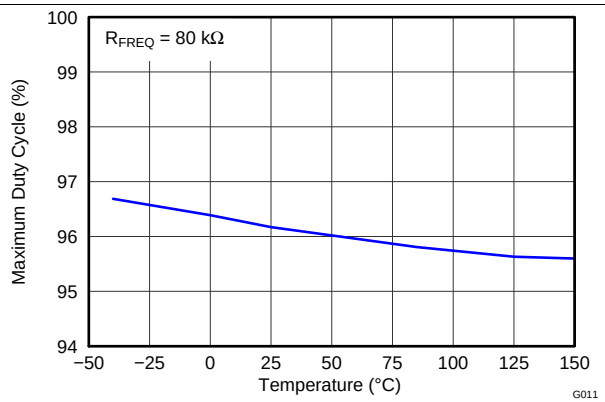


Figure 12. Maximum Duty Cycle vs Temperature

Copyright © 2013–2019, Texas Instruments Incorporated

Typical Characteristics (continued)

V_{IN} = 5 V, T_A = 25°C (unless otherwise noted)

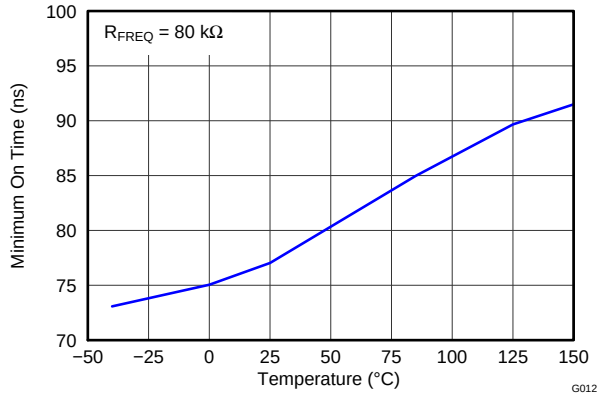


Figure 13. Minimum On Time vs Temperature

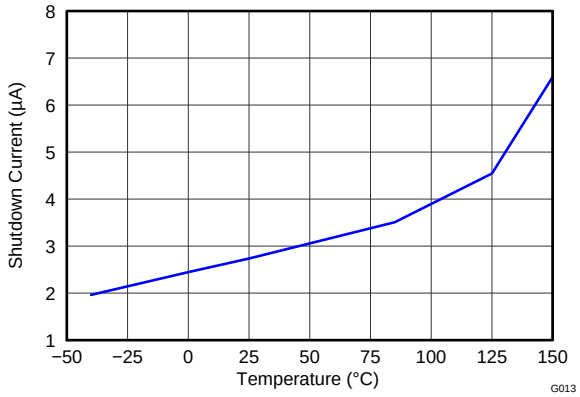


Figure 14. Shutdown Current vs Temperature

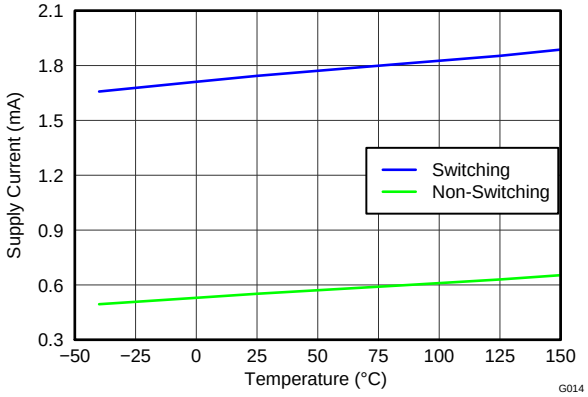


Figure 15. Supply Current vs Temperature

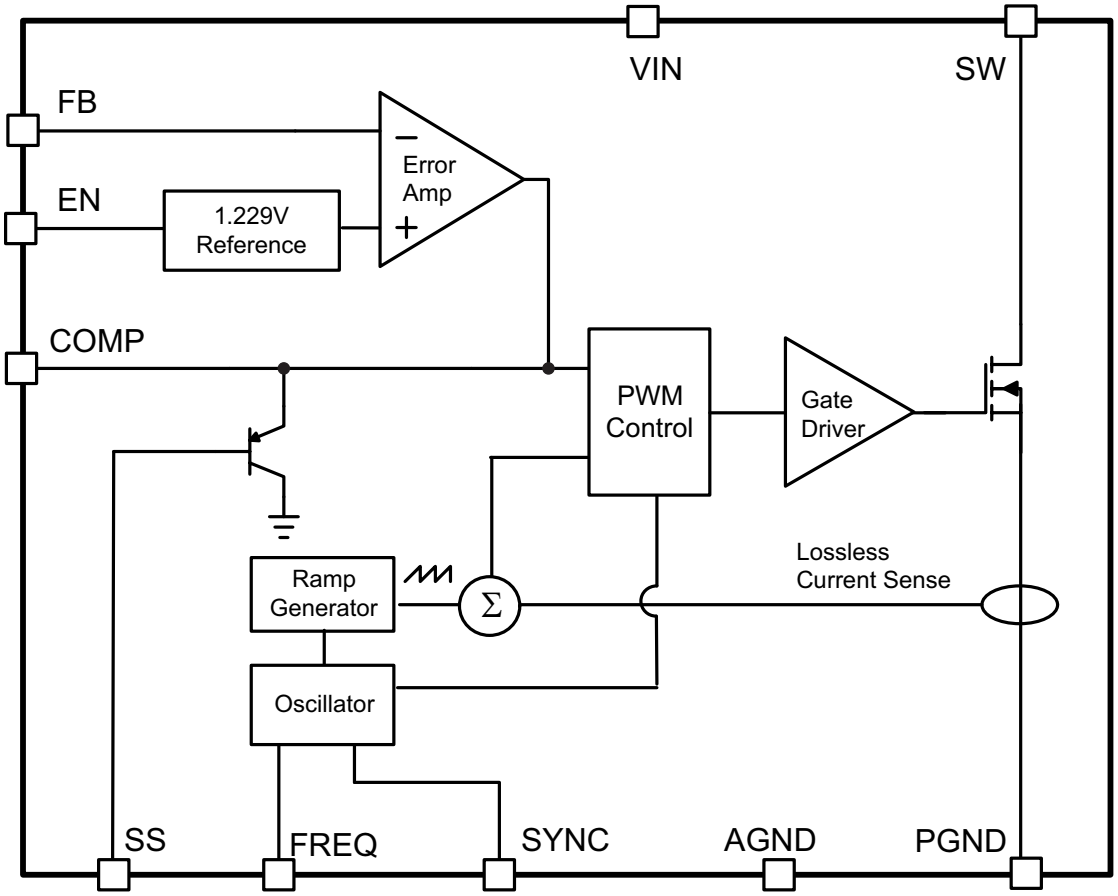
Copyright © 2013–2019, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The TPS55330 device is a monolithic nonsynchronous switching regulator with an integrated 5-A, 24-V power switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. The device has a wide input voltage range to support applications with input voltage from multicell batteries or regulated 3.3-V, 5-V, and 12-V power rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operation

If designed as a boost converter, the TPS55330 device regulates the output with current-mode pulse-width-modulation (PWM) control. The PWM-control circuitry turns on the switch at the beginning of each oscillator clock cycle. The input voltage is applied across the inductor and stores the energy as inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current reaches a threshold level set by the error amplifier output, the power switch turns off and the external Schottky diode is forward biased to allow the inductor current to flow to the output. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats every switching cycle. The duty cycle of the converter is determined by the PWM-control comparator which compares the error amplifier output and the current signal. The oscillator frequency is programmed by the external resistor or synchronized to an external clock signal.

Copyright © 2013–2019, Texas Instruments Incorporated

Feature Description (continued)

A ramp signal from the oscillator is added to the inductor current ramp to provide slope compensation. Slope compensation is required to avoid subharmonic oscillation that is intrinsic to peak-current mode control at duty cycles higher than 50%. If the inductor value is too small, the internal slope compensation may not be adequate to maintain stability.

The PWM control feedback loop regulates the FB pin to a reference voltage through a transconductance error amplifier. The output of the error amplifier is connected to the COMP pin. An external RC-compensation network connected to the COMP pin is chosen for feedback loop stability and optimum transient response.

7.3.2 Switching Frequency

The switching frequency is set by a resistor (R_{FREQ}) connected to the FREQ pin of the TPS55330. The relationship between the timing resistance R_{FREQ} and frequency is shown in the Figure 5. Do not leave this pin open. A resistor must always be connected from the FREQ pin to ground for proper operation. The resistor value required for a desired frequency can be calculated using Equation 1.

$$R_{FREQ}(k\Omega) = 57500 \times f_{sw}(kHz)^{-1.03} \quad (1)$$

For the given resistor value, the corresponding frequency can be calculated by Equation 2.

$$f_{sw}(kHz) = 41600 \times R_{FREQ}(k\Omega)^{-0.97} \quad (2)$$

The TPS55330 switching frequency can be synchronized to an external clock signal that is applied to the SYNC pin. The required logic levels of the external clock are shown in the specification table. The recommended duty cycle of the clock is in the range of 10% to 90%. A resistor must be connected from the FREQ pin to ground when the converter is synchronized to the external clock and the external clock frequency must be within ±20% of the corresponding frequency set by the resistor. For example, if the frequency programmed by the FREQ pin resistor is 600kHz, the external clock signal should be in the range of 480kHz to 720kHz.

With a switching frequency below 280 kHz (typical) after the TPS55330 enters frequency foldback as described in the section, if a load remains when the overcurrent condition is removed the output may not recover to the set value. For the output to return to the set value the load must be removed completely or the TPS55330 power cycled with the EN pin or VIN pin. Select a nominal switching frequency of 350 kHz for quicker recovery from frequency foldback.

7.3.3 Overcurrent Protection and Frequency Foldback

The TPS55330 provides cycle-by-cycle over-current protection that turns off the power switch once the inductor current reaches the over-current limit threshold. The PWM circuitry resets itself at the beginning of the next switch cycle. During an over-current event, the output voltage begins to droop as a function of the load on the output. When the FB voltage through the feedback resistors, drops lower than 0.9 V, the switching frequency is automatically reduced to 1/4 of the normal value. Figure 8 shows the non-foldback frequency with an 80kΩ timing resistor and the corresponding foldback frequency. The switching frequency does not return to normal until the over-current condition is removed and the FB voltage increases above 0.9 V. The frequency foldback feature is disabled during soft-start.

7.3.3.1 Minimum On-Time and Pulse Skipping

The TPS55330 PWM control system has a minimum PWM pulse width of 77ns (typical). This minimum on-time determines the minimum duty cycle of the PWM, for any set switching frequency. When the voltage regulation loop of the TPS55330 requires a minimum on-time pulse width less than 77ns, the IC enters pulse-skipping mode. In this mode, the device will hold the power switch off for several switching cycles to prevent the output voltage from rising above the desired regulated voltage. This operation typically occurs in light load conditions when the PWM operates in discontinuous conduction mode. Pulse skipping increases the output ripple as shown in Figure 22.

7.3.4 Voltage Reference and Setting Output Voltage

An internal voltage reference provides a precise 1.229 V voltage reference at the error amplifier non-inverting input. To set the output voltage, select the FB pin resistor R_{SH} and R_{SL} according to *Overcurrent Protection and Frequency Foldback*.

Copyright © 2013–2019, Texas Instruments Incorporated

Feature Description (continued)

$$V_{OUT} = 1.229\,V \times \left(\frac{R_{SH}}{R_{SL}} + 1 \right) \quad (3)$$

7.3.5 Soft-Start

The TPS55330 has a built-in soft-start circuit which significantly reduces the start-up current spike and output voltage overshoot. When the IC is enabled, an internal bias current source (6 µA typical) charges a capacitor (C_{SS}) on the SS pin. The voltage at the capacitor clamps the output of the internal error amplifier that determines the peak current and duty cycle of PWM controller. Limiting the peak switch current during start-up with a slow ramp on the SS pin will reduce in-rush current and output voltage overshoot. Once the capacitor reaches 1.8V, the soft-start cycle is completed and the soft-start voltage no longer clamps the error amplifier output. When the EN is pulled low for at least 1ms, the IC enters the shutdown mode and the SS capacitor is discharged through a 5kΩ resistor to prepare for the next soft-start sequence.

7.3.6 Slope Compensation

The TPS55330 has internal slope compensation to prevent subharmonic oscillations. The sensed current slope of boost converter can be expressed as Equation 4:

$$S_n = \frac{V_{IN}}{L} \times R_{SENSE} \quad (4)$$

The slope compensation dv/dt can be calculated using Equation 5.

$$S_e = \frac{0.32\,V / R_{FREQ}}{16 \times (1 - D) \times 6\,pF} + \frac{0.5\,\mu A}{6\,pF} \quad (5)$$

In a converter with current mode control, in addition to the output voltage feedback loop, the inner current loop including the inductor current sampling effect as well as the slope compensation on the small signal response should be taken into account, which can be modeled as seen in Equation 6:

$$He(s) = \frac{1}{1 + \frac{s \times \left[\left(1 + \frac{S_e}{S_n} \right) \times (1 - D) - 0.5 \right]}{f_{sw}} + \frac{s^2}{(\pi \times f_{sw})^2}} \quad (6)$$

where

- R_{SENSE} (15mΩ) is the equivalent current sense resistor
- R_{FREQ} is timing resistor used to set frequency
- D is the duty cycle

NOTE

If S_n << S_e, the converter operates in voltage mode control rather than current mode control, and Equation 6 is no longer valid.

7.3.7 Enable and Thermal Shutdown

The TPS55330 enters shutdown when the EN voltage is less than 0.68 V (min) for more than 1 ms. In shutdown, the input supply current for the device is less than 10 µA (max). The EN pin has an internal 950kΩ pull down resistor to disable the device if the pin is floating.

An internal thermal shutdown turns off the device when the junction temperature exceeds 165°C (typical). The device restarts when the junction temperature drops by 15°C.

Copyright © 2013–2019, Texas Instruments Incorporated

Feature Description (continued)

7.3.8 Undervoltage Lockout (UVLO)

An under-voltage lockout circuit prevents mis-operation of the device at input voltages below 2.5 V (typical). When the input voltage is below the UVLO threshold, the device remains off and the internal power MOSFET is turned off. The UVLO threshold is set below minimum operating voltage of 2.9 V to ensure that a transient VIN dip will not cause the device to reset. For the input voltages between UVLO threshold and 2.9 V, the device attempts to operate, but the electrical specifications are **not** ensured.

7.4 Device Functional Modes

7.4.1 Operation With V_I < 2.9 V (Minimum V_I)

The TPS55330 device operates with input voltages above 2.9 V. The typical UVLO voltage (turning off) is 2.5 V and the TPS55330 device remains off at input voltages lower than that point. For the input voltages between UVLO threshold and 2.9 V, the device attempts to operate, but the electrical specifications are **not** ensured.

7.4.2 Operation With EN Control

The enable rising-edge threshold voltage is 1.08 V (typical) with 0.16 V hysteresis (typical). With the EN pin held below the turn-off voltage the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. When the input voltage is above the UVLO threshold and the EN pin voltage increases above the rising edge threshold, the device becomes active. Switching enables and the soft-start sequence initiates. The TPS55330 device starts at the soft-start time determined by the external soft-start capacitor.

7.4.3 Operation at Light Loads

The device is designed to operate in high-efficiency pulse-skipping mode under light load conditions. Discontinuous-conduction-mode (DCM) operation initiates when the switch current falls to 0 A. During DCM operation, the catch diode stops conducting when the switch current falls to 0 A. The switching node (the SW pin) waveform takes on the characteristics of discontinuous-conduction-mode (DCM) operation. As the load decreases further and when the voltage-regulation loop of TPS55330 device requires an on-time pulse width less than the minimum PWM pulse width of 77 ns (typical), the IC enters pulse-skipping mode. In this mode, the device holds the power switch off for several switching cycles to prevent the output voltage from rising too much above the desired regulated voltage.

Copyright © 2013–2019, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS55330 device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. For example, the device configured in boost topology is widely used to convert a lower DC voltage to a higher DC voltage with a maximum available switching current of 5.25 A. Use the following design procedure to select component values for a boost converter design or SEPIC design for the TPS55330 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The following section provides a step-by-step design approach for configuring the TPS55330 as a voltage regulating boost converter, as shown in Figure 16. When configured as SEPIC or flyback converter, a different design approach is required.

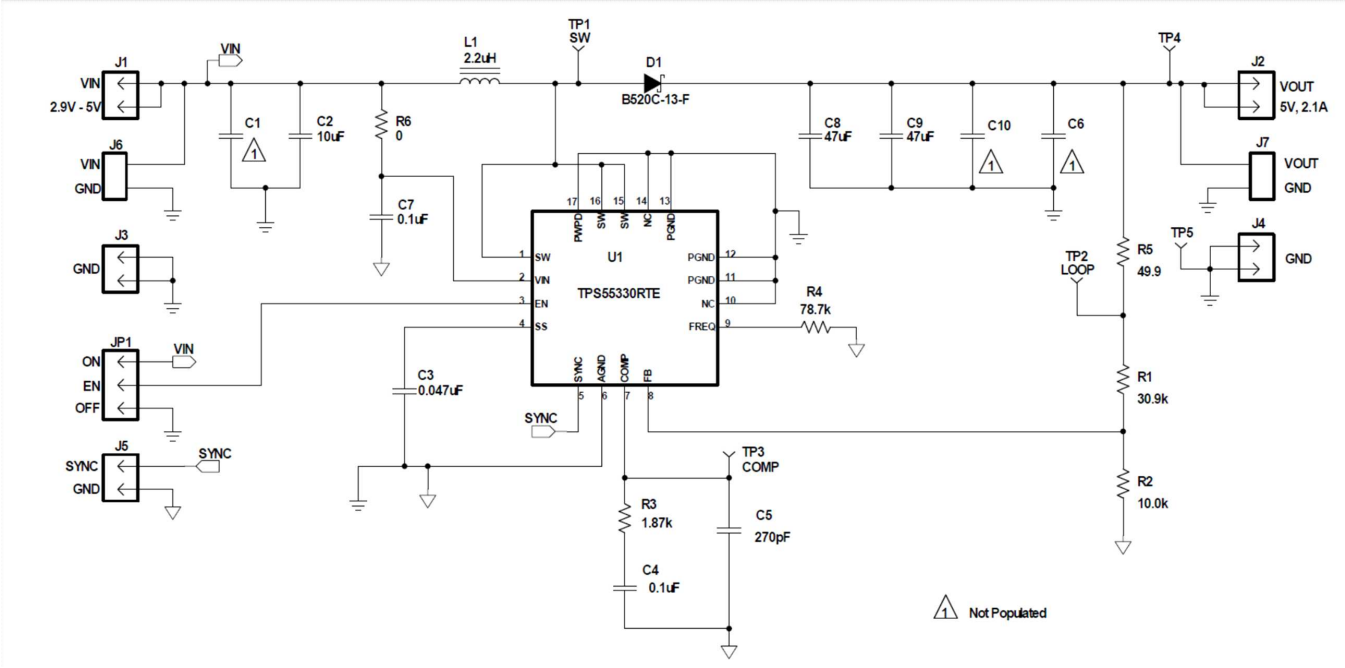


Figure 16. Boost Converter Application Schematic

8.2.1 Design Requirements

PARAMETER	VALUE
Output Voltage	5 V
Input Voltage	2.9 V to 4.2 V
Maximum Output Current	2.1 A
Transient Response 50% load step (ΔV_{OUT} = 3%)	200 mV
Output Voltage Ripple (0.5% of V_{OUT})	25 mV

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS55330 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Selecting the Switching Frequency (R4)

The first step is to decide on a switching frequency for the regulator. There are tradeoffs to consider for a higher or lower switching frequency. A higher switching frequency allows for lower valued inductor and smaller output capacitors leading to the smallest solution size. A lower switching frequency will result in a larger solution size but better efficiency. The user will typically set the frequency for the minimum tolerable efficiency to avoid excessively large external components.

A switching frequency of 600 kHz is a good trade-off between efficiency and solution size. The appropriate resistor value is found from the resistance versus frequency graph of Figure 5, or calculated using Equation 1. R4 is calculated to be 78.4 kΩ and the nearest standard value resistor of 78.7 kΩ is selected. A resistor must be placed from the FREQ pin to ground, even if an external oscillation is applied for synchronization.

8.2.2.3 Determining the Duty Cycle

The input to output voltage conversion ratio of the TPS55330 is limited by the worst case maximum duty cycle of 89% and the minimum duty cycle which is determined by the minimum on-time of 77 ns and the switching frequency. The minimum duty cycle can be estimated with Equation 7. With a 600 kHz switching frequency the minimum duty cycle is 4%.

$$D_{PS} = T_{ON}\ \text{min} \times f_{sw} \tag{7}$$

The duty cycle at which the converter operates is dependent on the mode in which the converter is running. If the converter is running in discontinuous conduction mode (DCM), where the inductor current ramps to zero at the end of each cycle, the duty cycle varies with changes of the load much more than it does when running in continuous conduction mode (CCM). In continuous conduction mode, where the inductor maintains a minimum dc current, the duty cycle is related primarily to the input and output voltages as computed in Equation 8. Assume a 0.5 V drop V_D across the Schottky rectifier. At the minimum input of 2.9 V, the duty cycle will be 47%. At the maximum input of 4.2 V, the duty cycle is 24%.

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} \tag{8}$$

At light loads the converter will operate in DCM. In this case the duty cycle is a function of the load, input and output voltages, inductance and switching frequency as computed in Equation 9. This can be calculated only after an inductance is chosen in the following section. While operating in DCM with very light load conditions the duty cycle demand will force the TPS55330 to operate with the minimum on time. The converter will then begin pulse skipping which can increase the output ripple.

$$D = \frac{\sqrt{2 \times (V_{OUT} + V_D - V_{IN}) \times L \times I_{OUT} \times f_{SW}}}{V_{IN}} \tag{9}$$

Copyright © 2013–2019, Texas Instruments Incorporated

All converters using a diode as the freewheeling or catch component have a load current level at which they transit from discontinuous conduction mode to continuous conduction mode. This is the point where the inductor current just falls to zero during the off-time of the power switch. At higher load currents, the inductor current does not fall to zero and diode and switch current assume a trapezoidal wave shape as opposed to a triangular wave shape. The load current boundary between discontinuous conduction and continuous conduction can be found for a set of converter parameters as shown in Equation 10.

$$I_{OUT(crit)} = \frac{(V_{OUT} + V_D - V_{IN}) \times V_{IN}^2}{2 \times (V_{OUT} + V_D)^2 \times f_{SW} \times L} \quad (10)$$

For loads higher than the result of the Equation 10, the duty cycle is given by Equation 8. For loads less than the results of Equation 10, the duty cycle is given Equation 9. For Equation 7 through Equation 10, the variable definitions are as follows.

- V_{OUT} is the output voltage of the converter in V
- V_D is the forward conduction voltage drop across the rectifier or catch diode in V
- V_{IN} is the input voltage to the converter in V
- I_{OUT} is the output current of the converter in A
- L is the inductor value in H
- f_{SW} is the switching frequency in Hz

Unless otherwise stated, the design equations that follow assume that the converter is running in continuous conduction mode, which typically results in a higher efficiency for the power levels of this converter.

8.2.2.4 Selecting the Inductor (L1)

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, DC resistance and saturation current. Considering inductor value alone is not enough. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, the effective inductance can fall to a fraction of the zero current value.

The minimum value of the inductor should be able to meet inductor current ripple (ΔI_L) requirement at worst case. In a boost converter, maximum inductor current ripple occurs at 50% duty cycle. For the applications where duty cycle is always smaller or larger than 50%, Equation 12 should be used with the duty cycle closest to 50% and corresponding input voltage to calculate the minimum inductance. For applications that need to operate with 50% duty cycle when input voltage is somewhere between the minimum and the maximum input voltage, Equation 13 should be used. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum input current ($I_{IN}DC = I_L avg$). The maximum input current can be estimated with Equation 11, with an estimated efficiency based on similar applications (η_{EST}). The inductor ripple current will be filtered by the output capacitor. Therefore, choosing high inductor ripple currents will impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value (K_{IND}) is at the discretion of the designer. However, the following guidelines may be used.

For CCM operation, it is recommended to use K_{IND} values in the range of 0.2 to 0.4. Choosing K_{IND} closer to 0.2 results in a larger inductance value, maximizes the converter's potential output current and minimizes EMI. Choosing K_{IND} closer to 0.4 results in a smaller inductance value, a physically smaller inductor, and improved transient response, but potentially worse EMI and lower efficiency. Using an inductor with a smaller inductance value may result in the converter operating in DCM. This reduces the boost converter's maximum output current, causes larger input voltage and output voltage ripple and reduced efficiency. For this design, choose K_{IND} = 0.3 and a conservative efficiency estimate of 85% with the minimum input voltage and maximum output current. Equation 12 is used with the minimum input voltage because this corresponds to duty cycle closest to 50%. The maximum input current is estimated at 4.53A and the minimum inductance is 1.68 µH. A standard value of 2.2 µH is chosen.

$$I_{IN}DC = \frac{V_{OUT} \times I_{OUT}}{\eta_{EST} \times V_{IN}\,min} \quad (11)$$

$$L_O\,min \geq \frac{V_{IN}}{I_{IN}DC \times K_{IND}} \times \frac{D}{f_{SW}} \quad , D \neq 50\%, V_{IN} \text{ with D closest to } 50\% \quad (12)$$

Copyright © 2013–2019, Texas Instruments Incorporated

$$L_O \min \geq \frac{(V_{OUT} + V_D)}{I_{IN}DC \times K_{IND}} \times \frac{1}{4 \times f_{SW}} \text{ , D=50\%} \quad (13)$$

After choosing the inductance, the required current ratings can be calculated. The inductor will be closest to its ratings with the minimum input voltage. The ripple with the chosen inductance is calculated with Equation 14. The RMS and peak inductor current can be found with Equation 15 and Equation 16. For this design the current ripple is 1.04 A, the RMS inductor current is 4.53 A, and the peak inductor current is 5.05 A. It is generally recommended for the peak inductor current rating of the selected inductor be 20% higher to account for transients during power up, faults or transient load conditions. The most conservative approach is to specify an inductor with a saturation current greater than the maximum peak current limit of the TPS55330. This helps to avoid saturation of the inductor. The chosen inductor is a Würth Elektronik 74437346022. It has a saturation current rating of 15 A, RMS current rating of 6.5 A, and typical DCR of 18 mΩ.

$$\Delta I_L = \frac{V_{IN} \min}{L_O} \times \frac{D \max}{f_{SW}} \quad (14)$$

$$I_L rms = \sqrt{(I_{IN}DC)^2 + \frac{\Delta I_L^{\,2}}{12}} \quad (15)$$

$$I_L peak = I_{IN}DC + \frac{\Delta I_L}{2} \quad (16)$$

The TPS55330 has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too small, the slope compensation may not be adequate, and the loop can be unstable.

8.2.2.5 Computing the Maximum Output Current

The over-current limit for the integrated power MOSFET limits the maximum input current and thus the maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output (I_{OUT}max). The current limit clamps the peak inductor current, therefore the ripple has to be subtracted to derive maximum DC current. Decreasing the K_{IND} or designing for a higher efficiency will increase the maximum output current. This can be evaluated with the chosen inductance or the chosen K_{IND}. This should be evaluated with the minimum input voltage and minimum peak current limit (I_{LIM}) of 5.25 A.

$$I_{OUT} \max = \frac{V_{IN} \min \times \left(I_{LIM} - \frac{\Delta I_L}{2} \right) \times \eta_{EST}}{V_{OUT}} = \frac{V_{IN} \min \times I_{LIM} \times \eta_{EST}}{\left(1 + \frac{K_{IND}}{2} \right) \times V_{OUT}} \quad (17)$$

In this design with 2.9 V input boosted to 5 V output and a 2.2 µH inductor with an assumed the Schottky forward voltage of 0.5 V and estimated efficiency of 80%, the maximum output current is 2.25 A. With the 4.2 V input and increased estimated efficiency of 90%, the maximum output current increases to 3.68 A.

8.2.2.6 Selecting the Output Capacitor (C8-C10)

At least 4.7 µF of ceramic type X5R or X7R capacitance is recommended at the output. The output capacitance is mainly selected to meet the requirements for the output ripple (V_{RIPPLE}) and voltage change during a load transient. Then the loop is compensated for the output capacitor selected. The output capacitance should be chosen based on the most stringent of these criteria. The output ripple voltage is related to the capacitance and equivalent series resistance (ESR) of the output capacitor. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by Equation 18. If high ESR capacitors are used it will contribute additional ripple. The maximum ESR for a specified ripple is calculated with Equation 19. ESR ripple can be neglected for ceramic capacitors but must be considered if tantalum or electrolytic capacitors are used. The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated by the Equation 20. Equation 21 can be used to calculate the RMS current that the output capacitor needs to support.

$$C_{OUT} \geq \frac{D \max \times I_{OUT}}{f_{SW} \times V_{RIPPLE}} \quad (18)$$

Copyright © 2013–2019, Texas Instruments Incorporated

$$ESR = \frac{\left(V_{RIPPLE} - \frac{D\max \times I_{OUT}}{f_{SW} \times C_{OUT}} \right)}{I_L peak} \quad (19)$$

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2 \times \pi \times f_{BW} \times \Delta V_{TRAN}} \quad (20)$$

$$I_{CO}rms = I_{OUT} \sqrt{\frac{D\max}{(1 - D\max)}} \quad (21)$$

Using Equation 18 for this design, the minimum output capacitance for the specified 25 mV output ripple is 66 µF. For a maximum transient voltage change (ΔV_{TRAN}) of 200 mV with a 1 mA load transient (ΔI_{TRAN}) and a 10 kHz control loop bandwidth (f_{BW}) with Equation 20, the minimum output capacitance is 84 µF. The most stringent criteria is the 66 µF for the required load transient. Equation 21 gives a 2 A RMS current in the output capacitor. The capacitor should also be properly rated for the desired output voltage.

Care must be taken when evaluating ceramic capacitors that derate under dc bias, aging and AC signal conditions. For example, larger form factor capacitors (in 1206 size) have self-resonant frequencies in the range of converter switching frequency. Self-resonance causes the effective capacitance to be significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can lose as much as 50% of the capacitance whan operated at the rated voltage. Therefore, allow margin in selected capacitor voltage rating to ensure adequate capacitance at the required output voltage. For this example, two 47 µF, 16 V 1210 X5R ceramic capacitors are used in parallel leading to a negligible ESR. Choosing 16 V capacitors instead of 6.3 V reduces the effects of DC bias and allows this example circuit to be rated for the maximum output voltage range of the TPS55330.

8.2.2.7 Selecting the Input Capacitors (C2, C7)

At least 4.7µF of ceramic input capacitance is recommended. Additional input capacitance may be required to meet ripple and/or transient requirements. High quality ceramic, type X5R or X7R are recommended to minimize capacitance variations over temperature. The capacitor must also have an RMS current rating greater than the maximum RMS input current of the TPS55330 calculated with Equation 22. The input capacitor must also be rated greater than the maximum input voltage. The input voltage ripple can be calculated with Equation 23.

$$I_{CI}rms = \frac{\Delta I_L}{\sqrt{12}} \quad (22)$$

$$V_I ripple = \frac{\Delta I_L}{4 \times f_{SW} \times C_{IN}} + \Delta I_L \times R_{CIN} \quad (23)$$

In the design example, the input RMS current is calculated to be 300 mA. The chosen input capacitor is a 10 µF, 25 V 1210 X7R with 3 mΩ ESR. Although one with a lower voltage rating can be used, a 25 V rated capacitor was chosen to limit the affects of dc bias and to allow it the circuit to be rated for the entire input range of the TPS55330. The input ripple is calculated to be 46 mV. An additional 0.1 µF, 50 V 0603 X5R is located close to the VIN and GND pins for extra decoupling.

8.2.2.8 Setting Output Voltage (R1, R2)

To set the output voltage in either DCM or CCM, select the values of R1 and R2 according to the following equations.

$$V_{OUT} = 1.229\,V \times \left(\frac{R1}{R2} + 1 \right) \quad (24)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{1.229\,V} - 1 \right) \quad (25)$$

Considering the leakage current through the resistor divider and noise decoupling into FB pin, an optimum value for R2 is around 10 kΩ. The output voltage tolerance depends on the V_{FB} accuracy and the tolerance of R1 and R2. In this example with a 5-V output using Equation 25, R1 is calculated to 30.7 kΩ. The nearest standard value of 30.9 kΩ is used.

Copyright © 2013–2019, Texas Instruments Incorporated

8.2.2.9 Setting the Soft-start Time (C7)

Choose the appropriate capacitor to set soft-start time and avoid overshoot. Increasing the soft-start time reduces the overshoot during start-up. A 0.047 µF ceramic capacitor is used in this example.

8.2.2.10 Selecting the Schottky Diode (D1)

The high switching frequency of the TPS55330 demands high-speed rectification for optimum efficiency. Ensure that the diode's average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the regulated output voltage. The diode must also be rated for the power dissipated which can be calculated with Equation 26.

$$P_D = V_D \times I_{OUT} \tag{26}$$

In this conservative design example, the diode is chosen to be rated for the maximum output current of 3.6 A. During normal operation with 2.1 mA output current and assuming a Schottky diode drop of 0.5 V, the diode must be capable of dissipating 1 W. The recommended minimum ratings for this design are a 20 V, 4 A diode. However to improve the flexibility of this design, a Diodes Inc B520-13-F in an SMC package is used with voltage and current ratings of 20 V and 5 A.

8.2.2.11 Compensating the Control Loop (R3, C4, C5)

The TPS55330 requires external compensation which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external resistor R3 and ceramic capacitor C4 are connected to the COMP pin to provide a pole and a zero, shown in the application circuit. This pole and zero, along with the inherent pole and zero of a boost converter, determine the closed loop frequency response. This is important for converter stability and transient response. Loop compensation should be designed for the minimum operating voltage.

The following equations summarize the loop equations for the TPS55330 configured as a CCM boost converter. They include the power stage output pole (f_{OUT}) and the right-half-plane zero (f_{RHPZ}) of a boost converter calculated with Equation 27 and Equation 28 respectively. When calculating f_{OUT} it is important to include the derating of ceramic output capacitors. In the example with an estimated 61 µF capacitance, these frequencies are calculated to 521 kHz and 2.2 kHz respectively. The DC gain (A) of the power stage is calculated with Equation 27 and is 39.9 dB in this design. The compensation pole (f_P) and zero (f_Z) generated by R3, C4 and internal transconductance amplifier are calculated with Equation 30 and Equation 31, respectively.

Most CCM boost converters will have a stable control loop if f_Z is set slightly above f_P through proper sizing of R3 and C4. A good starting point is C4 = 0.1 µF and R3 = 2kΩ. Increasing R3 or reducing C4 increases the closed loop bandwidth, and therefore improves the transient response. Adjusting R3 and C4 in opposite direction increases the phase and gain margin of the loop, which improves loop stability. It is generally recommended to limit the bandwidth of the loop to the lower of either 1/5 of the switching frequency f_{SW} or 1/3 the RHPZ frequency, f_{RHPZ} shown in Equation 28. The spreadsheet tool located in the TPS55330 product folder at SLVC430 can also be used to aid in compensation design.

$$f_{OUT} \approx \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \tag{27}$$

$$f_{RHPZ} \approx \frac{R_{OUT}}{2\pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \tag{28}$$

$$A = \frac{1.229}{V_{OUT}} \times G_{ea} \times 10M\Omega \times \frac{V_{IN}}{V_{OUT} \times R_{SENSE}} \times R_{OUT} \times \frac{1}{2} \tag{29}$$

$$f_P = \frac{1}{2\pi \times 10M\Omega \times C4} \tag{30}$$

$$f_Z = \frac{1}{2\pi \times R3 \times C4} \tag{31}$$

$$f_{co1} = \frac{f_{SW}}{5} \tag{32}$$

$$f_{co2} = \frac{f_{RHPZ}}{3} \tag{33}$$

Copyright © 2013–2019, Texas Instruments Incorporated

Where

- C_{OUT} is the equivalent output capacitor (C_{OUT}=C8+C9+C10)
- R_{OUT} is the equivalent load resistance (V_{OUT}/I_{OUT})
- Gea is the error amplifier transconductance located in the *Electrical Characteristics* table
- R_{SENSE} (15 mΩ, typical) is the sense resistor in the current control loop
- f_{co1} and f_{co2} are possible bandwidth.

An additional capacitor from the COMP pin to GND (C5) can be used to place a high frequency pole in the control loop. This is not always necessary with ceramic output capacitors. If a nonceramic output capacitor is used, there is an additional zero (f_{ZESR}) in the control loop which can be calculated with Equation 35. The value of C5 and the pole created by C5 can be calculated with Equation 36 and Equation 34 respectively. Finally if more phase margin is needed, an additional zero (f_{ZFF}) can be added by placing a capacitor (C_{FF}) in parallel with the top feedback resistor R1. TI recommendeds placing the zero at the target cross-over frequency or higher. The feed forward capacitor also adds a pole at a higher frequency. The recommended value of C_{FF} can be calculated with Equation 37.

$$f_{P2} = \frac{1}{2\pi \times R3 \times C5} \tag{34}$$

$$f_{ZESR} \approx \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{35}$$

$$C5 = \frac{R_{ESR} \times C_{OUT}}{R3} \tag{36}$$

$$C_{FF} = \frac{1}{2\pi \times R1 \times f_{ZFF} \times \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{37}$$

where R_{ESR} is the ESR of the output capacitor.

If a network measurement tool is available, the most accurate compensation design can be achieved following this procedure. The power stage frequency response is first measured using a network analyzer at the 3.6 V input and maximum 2.1 A load. This measurement is shown in Figure 17. In this design only one pole and one zero are used, so the maximum phase increase from the compensation will be 180 degrees. For a 60 degree phase margin, the power stage phase must be –120 degrees at its lowest point. Based on the target 10 kHz bandwidth, the measured power stage gain, $K_{PS}(f_{BW})$, is 13.3 dB and the phase is –87 degrees.

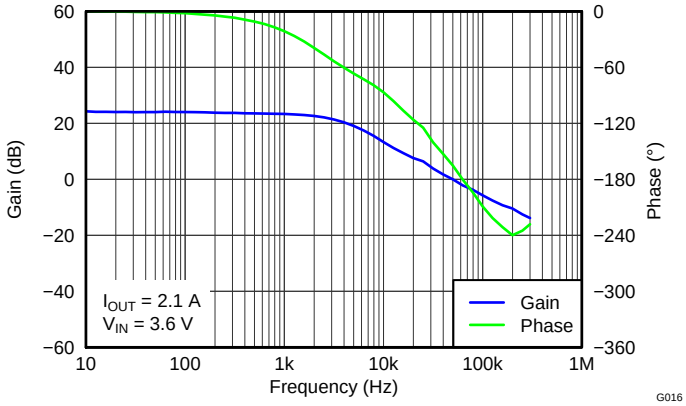


Figure 17. Power Stage Gain and Phase of the Boost Converter

R3 is then chosen to set the compensation gain to be the reciprocal of the power stage gain at the target bandwidth using Equation 38. C4 is then chosen to place a zero at 1/10 the target bandwidth with Equation 39. In this case R3 is calculated to be 1.87 kΩ, the nearest standard value 1.87 kΩ is used. C4 is calculated at 0.085 µF and the nearest standard value 0.100 µF is used. Although not necessary because this design uses all ceramic capacitors, a 270-pF capacitor is selected for C5 to add a high-frequency pole at a frequency 100 times the target bandwidth.

Copyright © 2013–2019, Texas Instruments Incorporated

$$R3 = \frac{1}{\left(Gea \times \frac{R2}{(R1 + R2)} \times 10^{\frac{K_{PS}(f_{BW})}{20}} \right)} \quad (38)$$

$$C4 = \frac{1}{2\pi \times R3 \times \frac{f_{BW}}{10}} \quad (39)$$

8.2.3 Application Curves

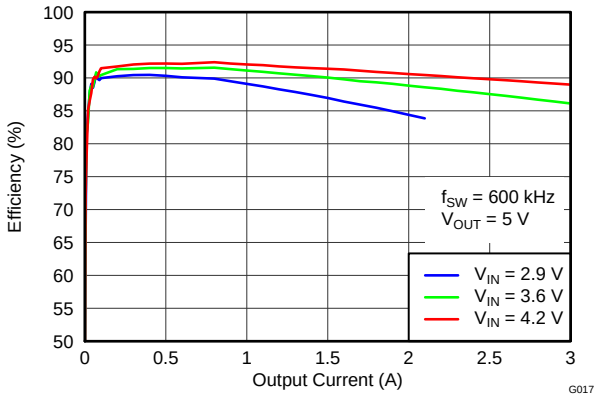


Figure 18. Efficiency vs Output Current

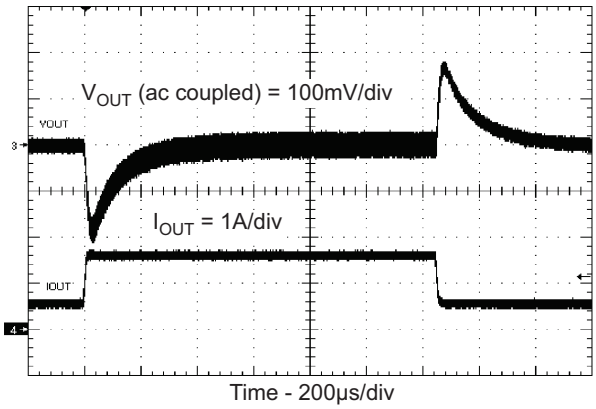


Figure 19. Load Transient Response

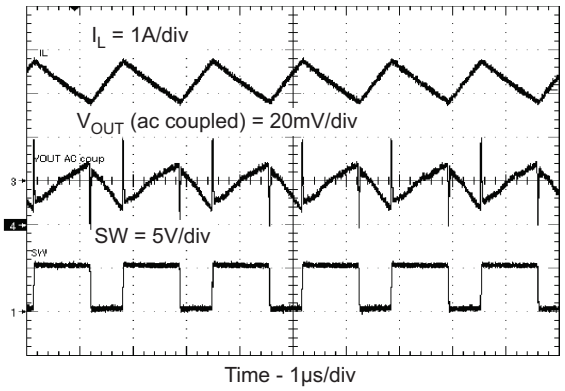


Figure 20. CCM PWM Operation

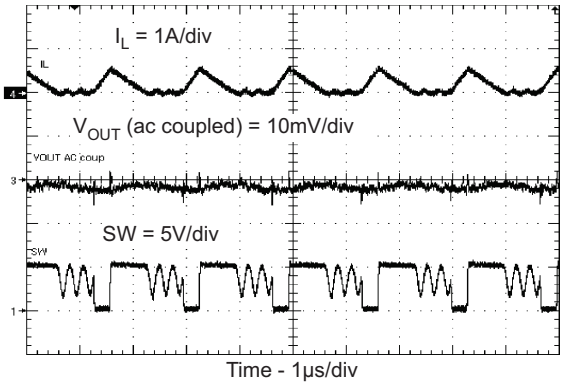


Figure 21. DCM PWM Operation

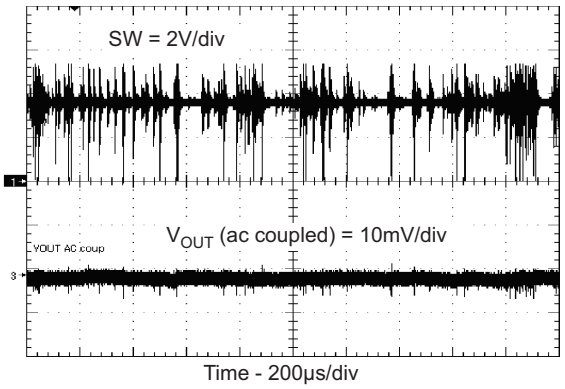


Figure 22. Pulse Skipping

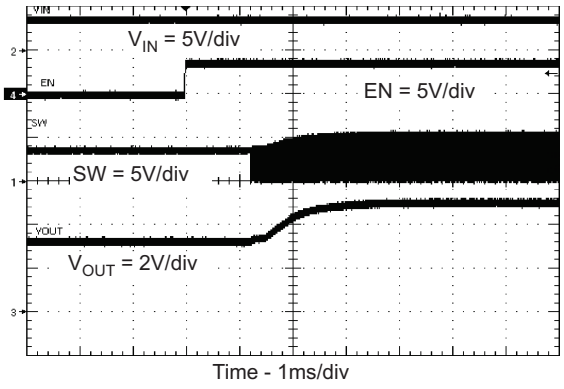


Figure 23. Start Up

Copyright © 2013–2019, Texas Instruments Incorporated

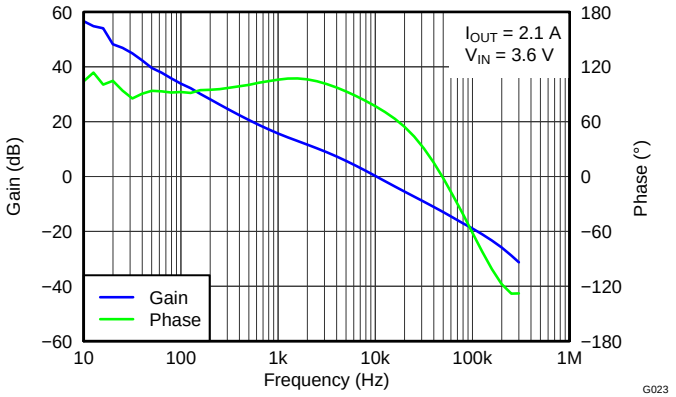


Figure 24. Closed-Loop Gain and Phase of the Boost Converter

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.9 V to 16 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS55330 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μF is a typical choice.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those with high frequency and high switch current, printed circuit board (PCB) layout is an important design step. If the layout is not carefully designed, the regulator can suffer from instability as well as noise problems. The following guidelines are recommended for good PCB layout.

- To prevent radiation of high frequency resonance problems, use proper layout of the high frequency switching path.
- Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling.
- The high current path including the internal MOSFET switch, Schottky diode, and output capacitor, contains nanosecond rise times and fall times. Keep these rise times and fall times as short as possible.
- Place the VIN bypass capacitor as close to the VIN pin and the AGND pin as possible to reduce the IC supply ripple.
- Connect the AGND and PGND pins to thermal pad directly on the same layer.

10.2 Layout Example

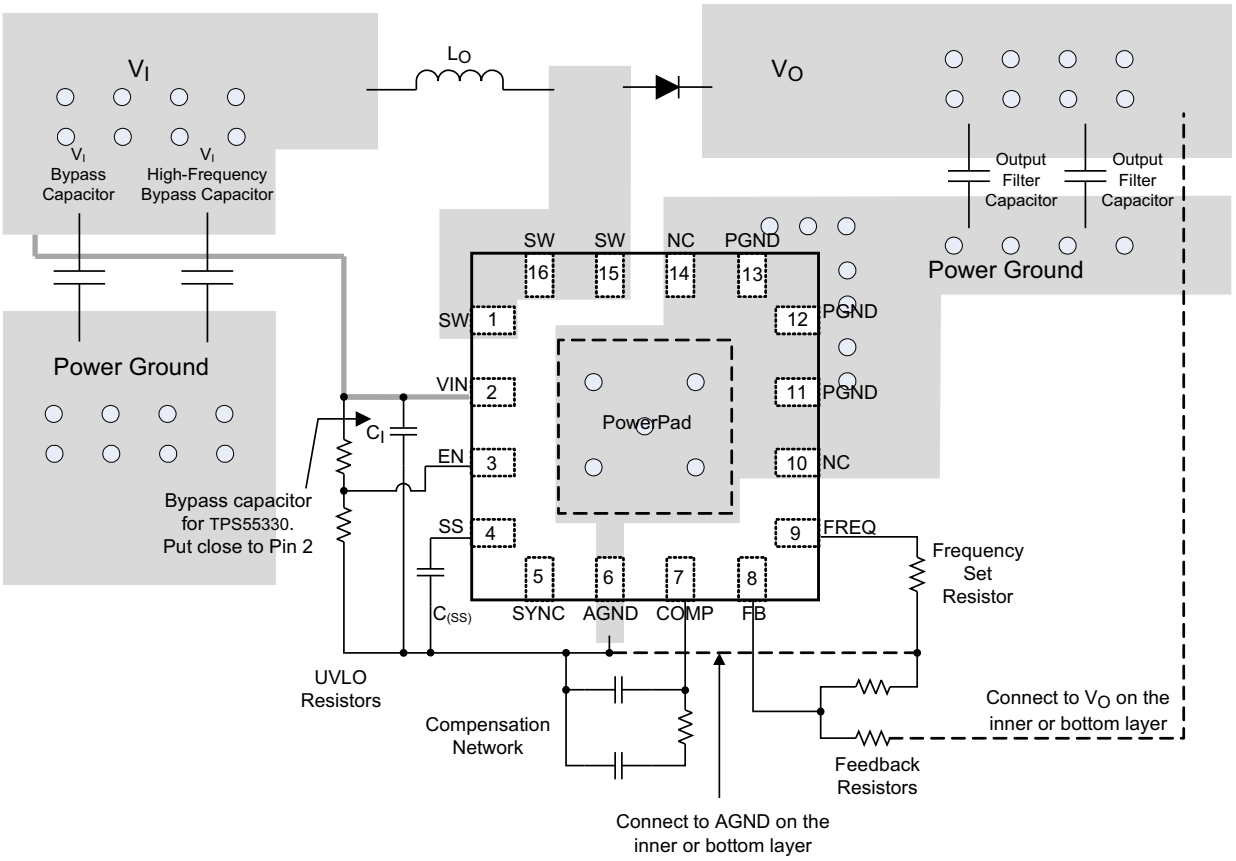


Figure 25. TPS55330 Example Board Layout

版权 © 2013–2019, Texas Instruments Incorporated

10.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. This restriction limits the power dissipation of the TPS55330. The TPS55330 features a thermally enhanced QFN package. This package includes a PowerPAD that improves the thermal capabilities of the package. The thermal resistance of the QFN package in any application greatly depends on the PCB layout and the PowerPAD connection. The PowerPAD must be soldered to the analog ground on the PCB. Use thermal vias underneath the PowerPAD to achieve good thermal performance.

版权 © 2013–2019, Texas Instruments Incorporated

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.1.2 开发支持

11.1.2.1 使用 WEBENCH® 工具创建定制设计

单击此处，使用 TPS55330 器件及其 WEBENCH® 电源设计器创建定制设计。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

版权 © 2013–2019, Texas Instruments Incorporated

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

版权 © 2013–2019, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS55330RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55330	Samples
TPS55330RTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55330	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

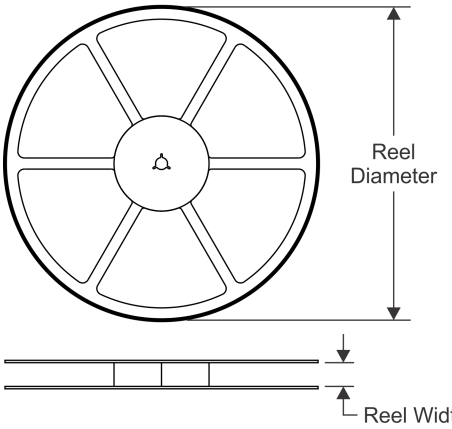
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

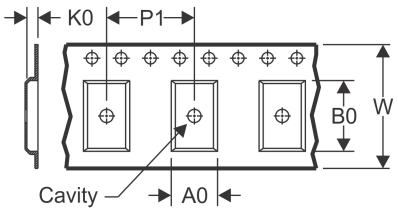
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

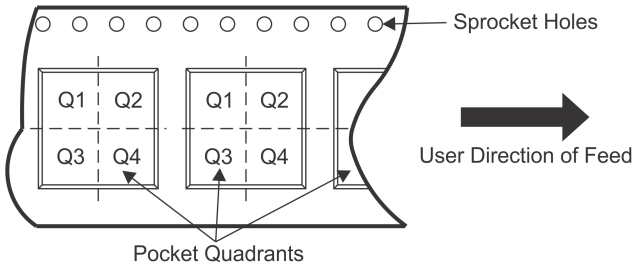


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

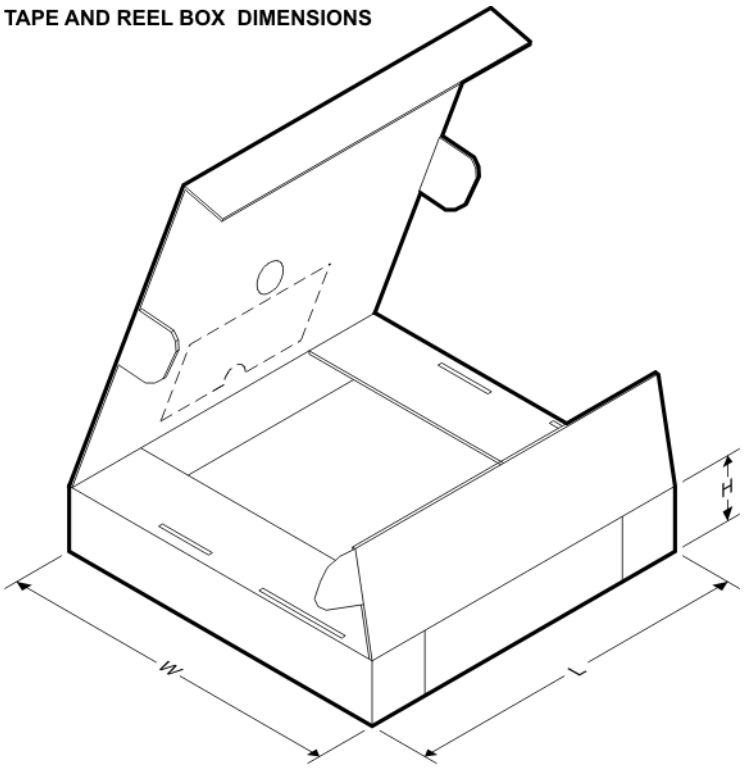
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55330RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS55330RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55330RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS55330RTET	WQFN	RTE	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

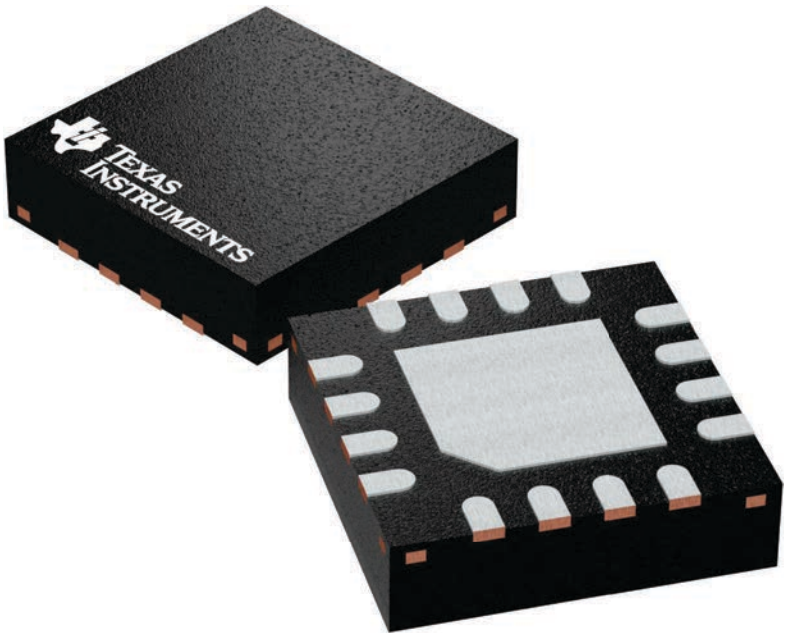
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

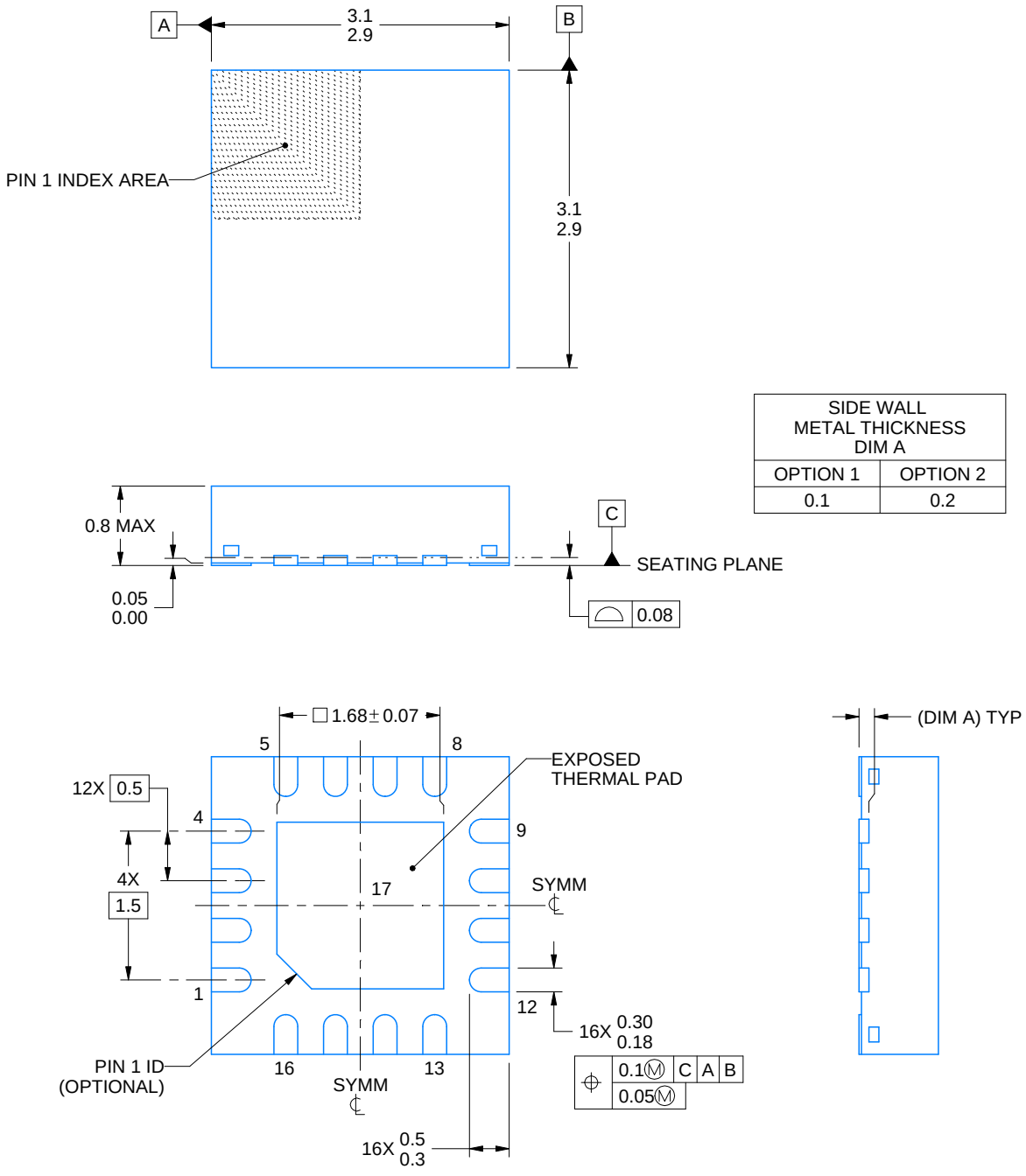


RTE0016C

PACKAGE OUTLINE

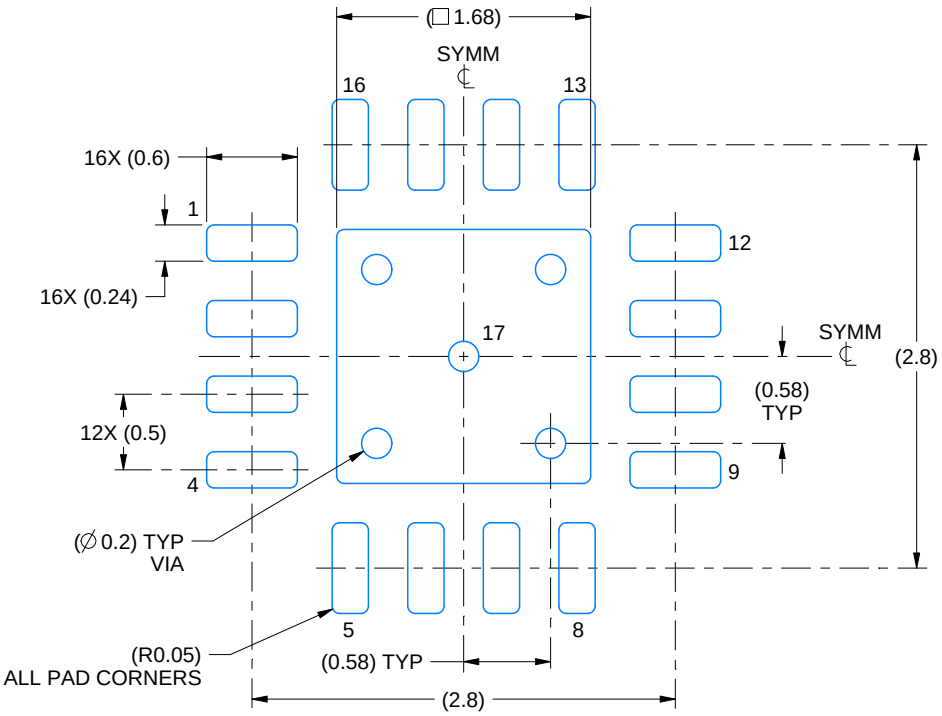
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

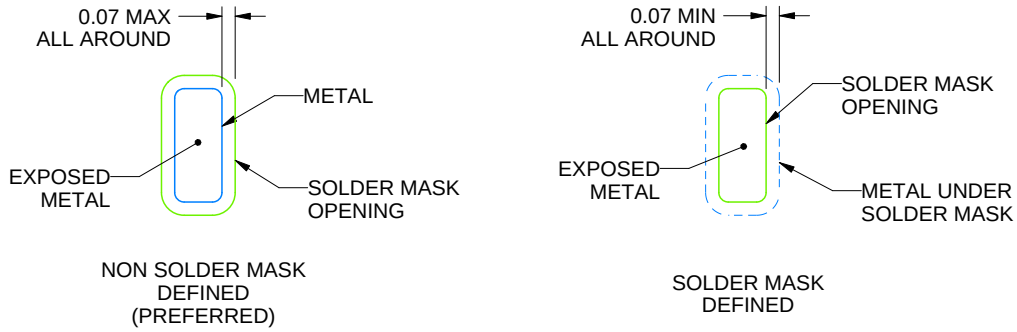


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

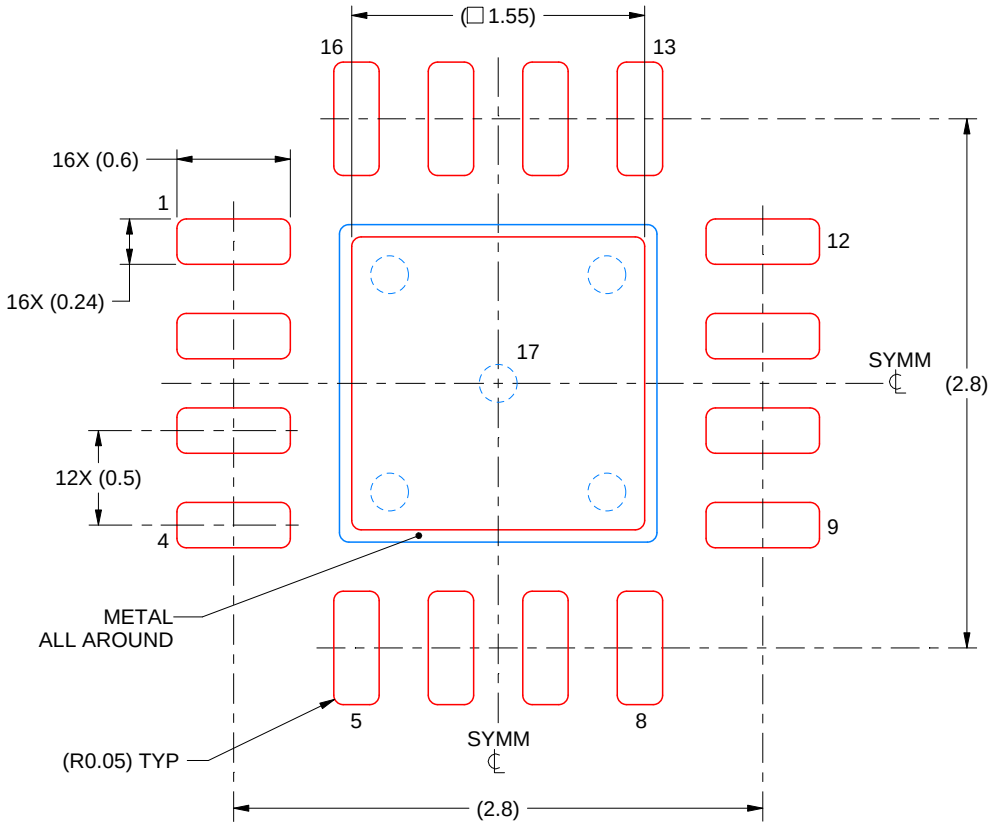


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022，德州仪器 (TI) 公司