User's Guide
SLVU278–December 2008

TPS54917EVM-367 9-A, SWIFT™ Regulator Evaluation Module

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1 Introduction

This user's guide contains background information for the TPS54917 as well as support documentation for the TPS54917EVM-367 evaluation module (HPA367). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54917EVM-367.

1.1 Background

The TPS54917 dc/dc converter is designed to provide up to a 9 A output from an input voltage source of 3 V to 4 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54917 regulator. The switching frequency is internally set at a nominal 1600 kHz. The both high-side and low-side MOSFETs are incorporated inside the TPS54917 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS54917 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54917 provides adjustable slow start, synchonization, enable and frequency adjust inputs along with a powergood output. The absolute maximum input voltage is 7 V for the TPS54917EVM-367.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54917EVM-367	VIN = 3 V to 4 V	0 A to 9 A

1.2 Performance Specification Summary

A summary of the TPS54917EVM-367performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 3.3 V and an output voltage of 1.8 V, unless otherwise specified. The TPS54917EVM-367is designed and tested for V_{IN} = 3 V to 4 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54917EVM-367Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			3	3.3	4	V
Output voltage set point				1.8		V
Output current range	V_{IN} = 3 V to 4V		0		9	A
Line regulation	I_O = 4.5 A, V_{IN} = 3 V to 4 V			±0.015%		
Load regulation	V_{IN} = 3.3 V, I_O = 0 A to 9A			±0.035%		
Load transient response	I_O = 2.2 A to 6.5 A	Voltage change		–40		mV
		Recovery time		250		µs
	I_O = 6.5 A to 2.2 A	Voltage change		40		mV
		Recovery time		250		µs
Loop bandwidth	V_{IN} = 3.3 V, I_O = 4.5 A			45		kHz
Phase margin	V_{IN} = 3.3 V , I_O = 4.5 A			75		°
Input ripple voltage	I_O = 9 A			140		mVpp
Output ripple voltage	I_O = 9 A			10		mVpp
Output rise time				8		ms
Operating frequency				1600		kHz
Maximum efficiency	V_{IN} = 3 V, I_O = 1.5 A			90%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54917. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R_2. Changing the value of R_2 can change the output voltage above 0.891 V. The value of R_2 for a specific output voltage can be calculated using Equation 1.

$$R_2 = 10\ k\Omega \times \frac{0.891\ V}{V_{OUT} - 0.891\ V} \quad (1)$$

Table 3 lists the R_2 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 160 ns, and the maximum duty cycle is less than 90%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Output Voltages Available

Output Voltage (V)	R_2 Value (kΩ)
1.2	28.7
1.8	10
2.5	3.74

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54917EVM-367evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The TPS54917EVM-367is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 7 A must be connected to J1 through a pair of 18 AWG wires. The load must be connected to J4 through a pair of 18 AWG wires. The maximum load current capability must be 9 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP2 provides a place to monitor the V_{IN} input voltages with TP5 providing a convenient ground reference. TP1 is used to monitor the output voltage with TP6 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	SYNC input. Connection for external synchronization clock.
J2	V_{OUT}, 1.8 V at 9 A maximum.
J3	V_{IN} (see Table 1 for V_{IN} range).
J4	2-pin header for enable. Connect EN to ground to disable, open to enable. Use to monitor SS/ENA voltage.
TP1	Output voltage test point at VOUT connector
TP2	V_{IN} test point at V_{IN} connector.
TP3	Test point between voltage divider network and output. Used for loop response measurements.
TP4	PH test point.
TP5	GND test point at V_{IN} connector.
TP6	GND test point at OUT connector.

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 1 A — 2.5 A and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPS54917EVM-367 at an ambient temperature of 25°C.

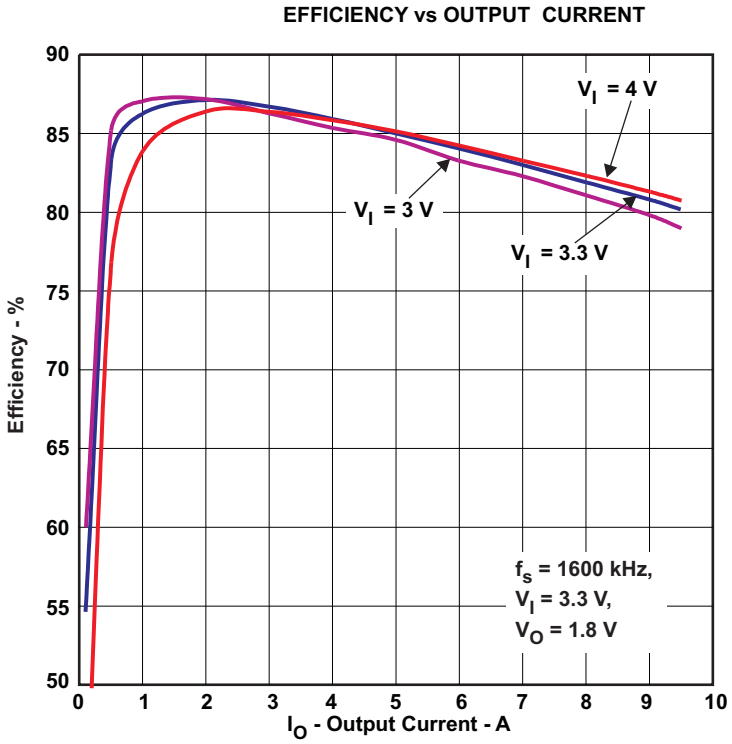


Figure 1. TPS54917EVM-367 Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

The load regulation for the TPS54917EVM-367is shown in Figure 2.

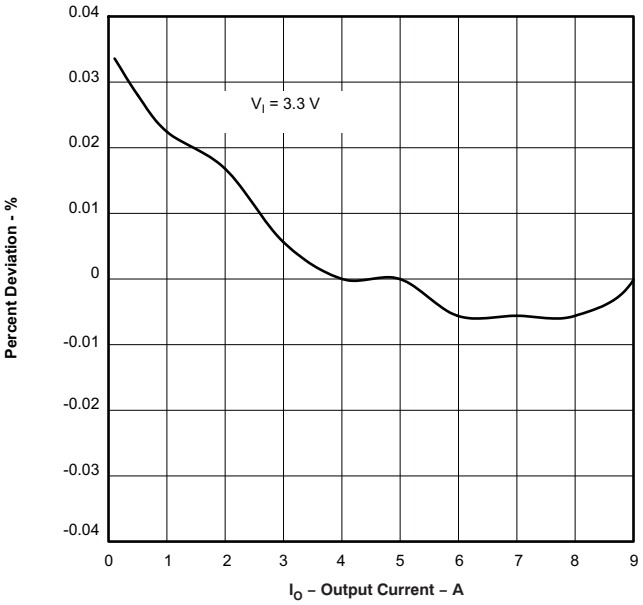


Figure 2. TPS54917EVM-367 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

The line regulation for the TPS54917EVM-367is shown in Figure 3.

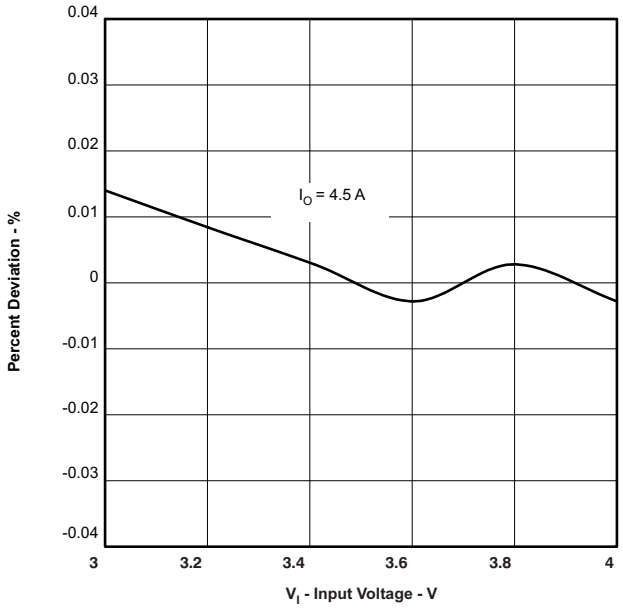


Figure 3. TPS54917EVM-367 Line Regulation

2.5 Load Transients

The TPS54917EVM-367response to load transients is shown in Figure 4. The current step is from approximately 25% to 75% of maximum rated load at 3.3 V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

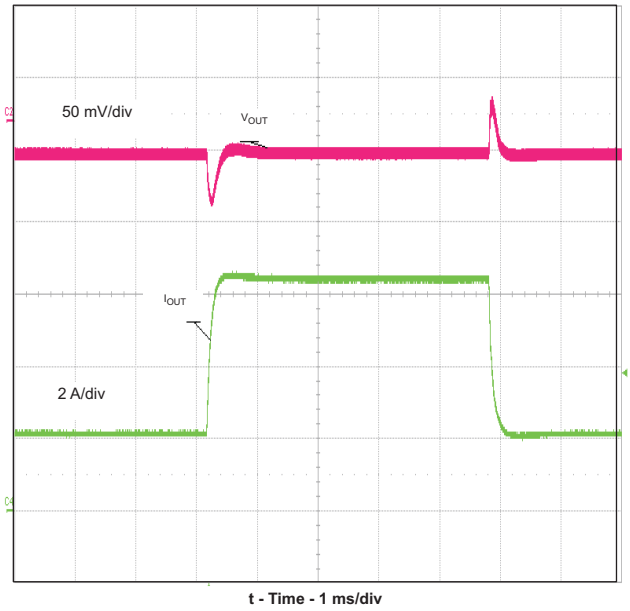


Figure 4. TPS54917EVM-367 Transient Response

2.6 Loop Characteristics

The TPS54917EVM-367loop-response characteristics are shown in Figure 5 . Gain and phase plots are shown for V_{IN} voltage of 3.3 V. Load current for the measurement is 4.5 A.

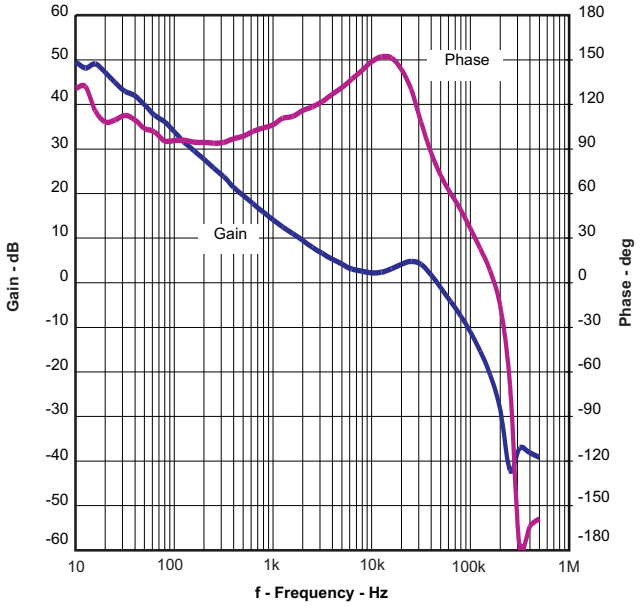


Figure 5. TPS54917EVM-367 Loop Response

2.7 Output Voltage Ripple

The TPS54917EVM-367output voltage ripple is shown in Figure 6 . The output current is the rated full load of 9 A and V_{IN} = 15 V. The ripple voltage is measured directly across the output capacitors.

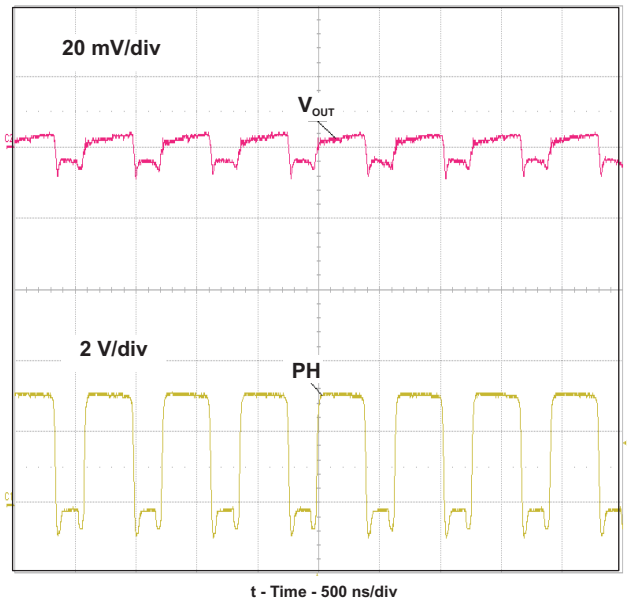


Figure 6. TPS54917EVM-367 Output Ripple

2.8 Input Voltage Ripple

The TPS54917EVM-367input voltage ripple is shown in Figure 7 . The output current is the rated full load of 9 A and V_{IN} = 3.3 V. The ripple voltage is measured directly across the input capacitors.

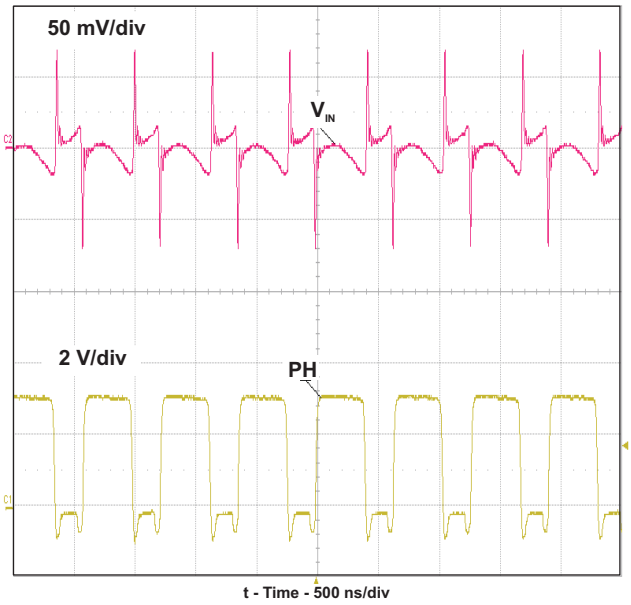


Figure 7. TPS54917EVM-367 Input Ripple

2.9 Powering Up

The start-up waveforms are shown in Figure 8 and Figure 9. In Figure 8, the top trace shows V_{IN}, and the bottom trace shows V_{OUT}. In Figure 9 , the top trace shows EN (enable) whereas the bottom trace shows V_{OUT}. In Figure 9, the input voltage is initially applied and the output is inhibited by using a jumper at J2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage of 1.25 V, the start-up sequence begins and the internal reference voltage begins to ramp up at the internally set rate toward 0.8 V and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 15 V and there is no load.

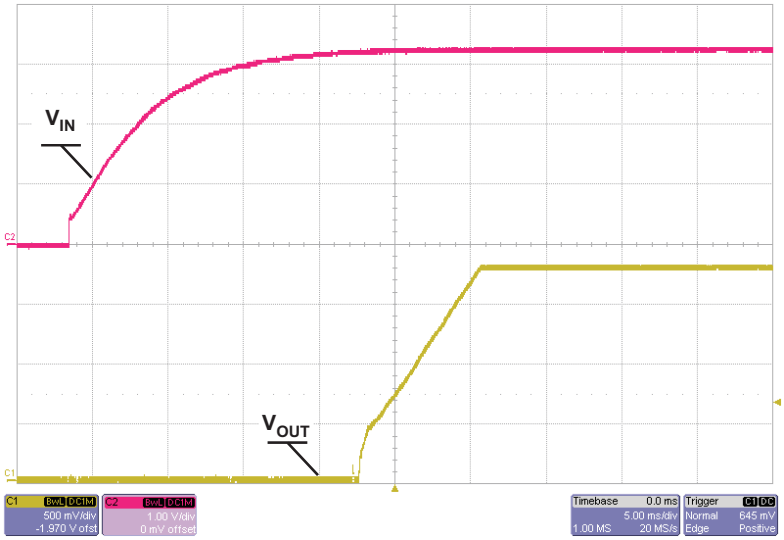


Figure 8. TPS54917EVM-367 Start-Up Relative to V_{IN}

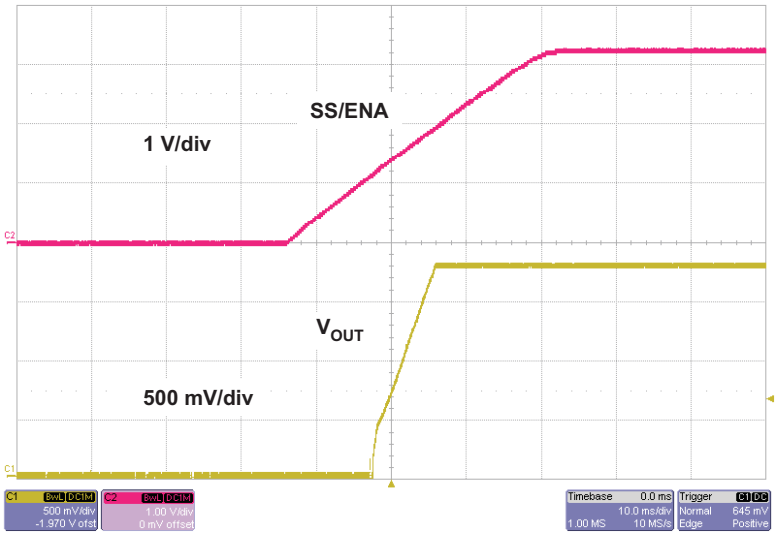


Figure 9. TPS54917EVM-367 Start-up Relative to Enable

2.10 Thermal Characteristics

This section shows a thermal image of the TPS54917EVM-367 running at 3.3 V input and 9 A load. These are the worst case conditions for maximum power loss. There is no air flow and the ambient temperature is 25°C. The peak temperature of the IC (85.8°C) is well below the maximum recommended operating condition listed in the datasheet of 150°C.

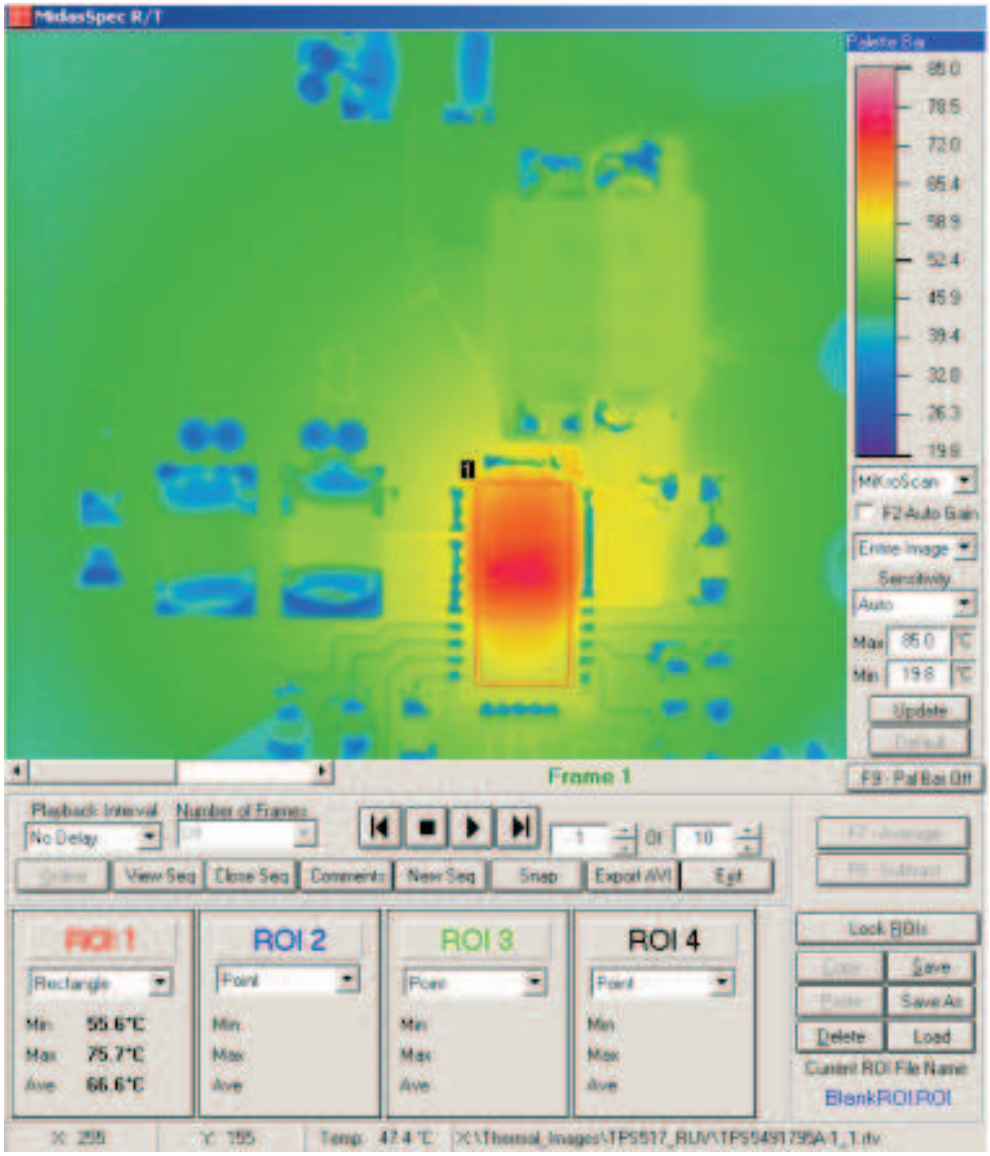


Figure 10. TPS54917EVM-367 Thermal Image

3 Board Layout

This section provides a description of the TPS54917EVM-367, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54917EVM-367is shown in Figure 11 through Figure 15. The topside layer of the EVM is laid out in a manner typical of a user application. The top, bottom and internal layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54917 and a large area filled with ground. The bottom and internal layers are dedicated ground planes. The top and bottom and internal ground areas are connected with multiple vias placed around the board including twelve vias directly under the TPS54917 device to provide a thermal path from the top-side ground plane to the bottom-side and internal ground planes.

The input decoupling capacitors (C1, C2, and C13) and bootstrap capacitor (C6) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} area fill near the output connector. For the TPS54917, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. A mounting area is provide at C13.

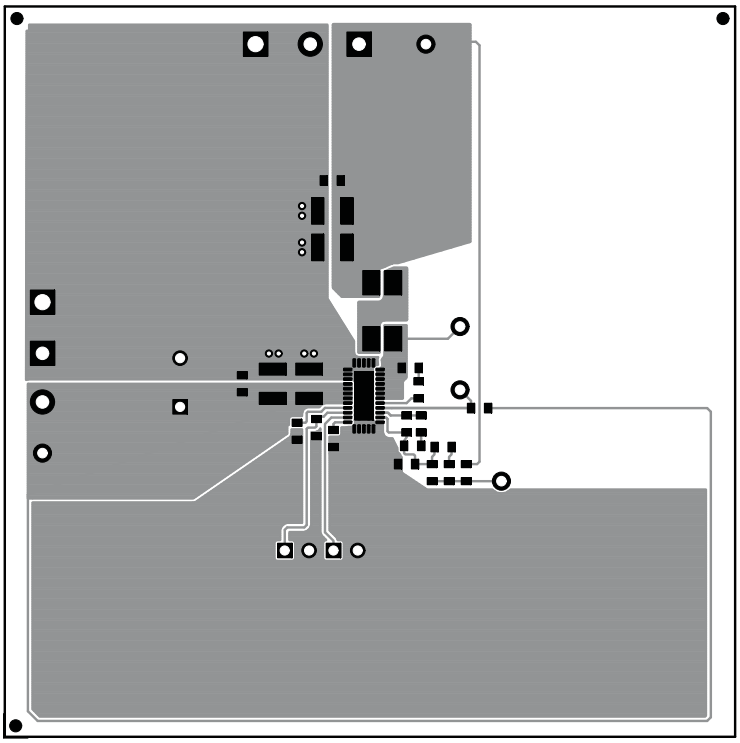


Figure 11. TPS54917EVM-367 Top-Side Layout

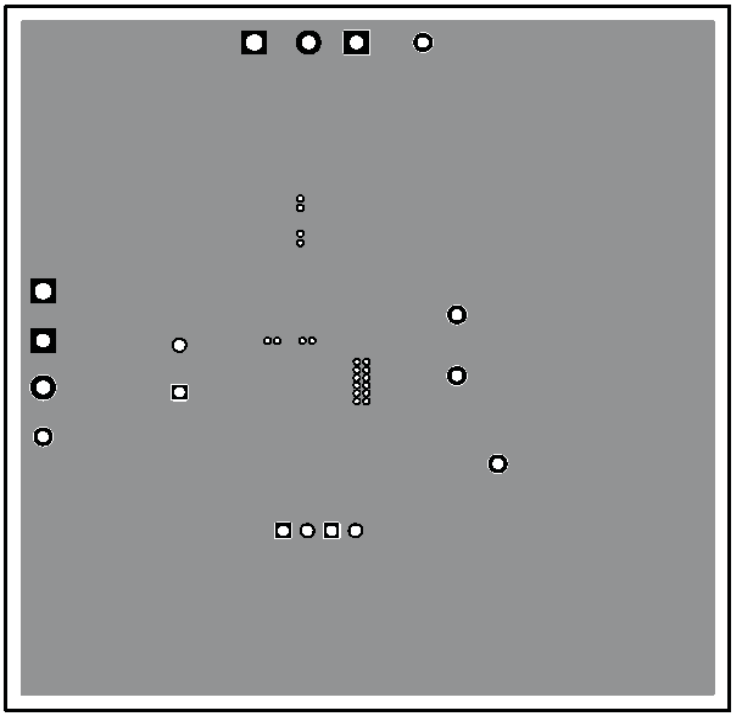


Figure 12. TPS54917EVM-367 Internal Layer 1

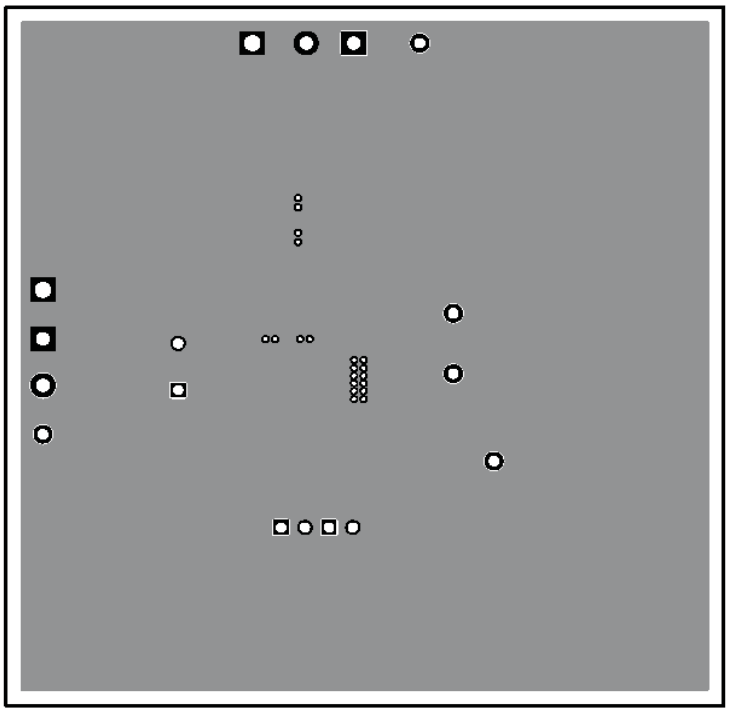


Figure 13. TPS54917EVM-367 Internal Layer 2

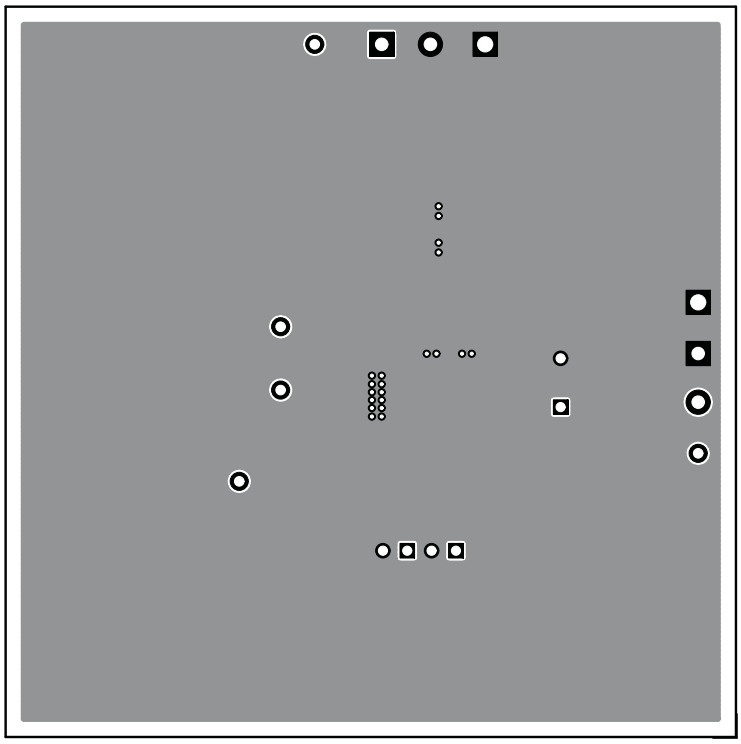


Figure 14. TPS54917EVM-367 Bottom-Side Layout

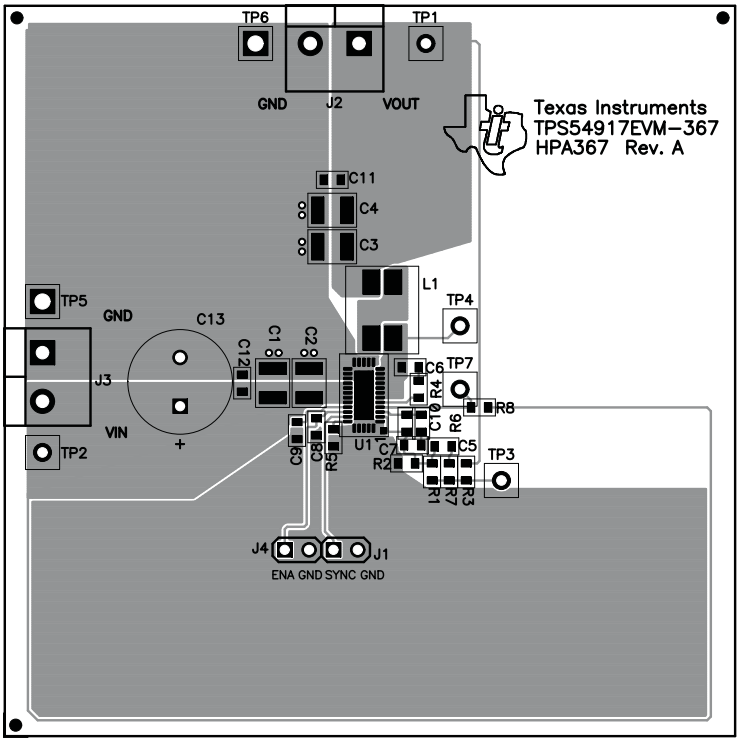


Figure 15. TPS54917EVM-367 Top-Side Assembly

3.2 Estimated Circuit Area

The estimated printed circuit board area for the components used in this design is 0.55 in^2. This area does not include test point or connectors.

4 Bill of Materials and Schematic

This section presents the TPS54917EVM-367 bill of materials and schematic.

4.1 Bill of Materials

Table 5 presents the bill of materials for the TPS54917EVM-367.

Table 5. TPS54917EVM-367 Bill of Materials

RefDes	Value	Description	Size	Part Number	MFR
C1, C2	22 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	1210	GRM32DR60J22KA01	Murata
C10	330 pF	Capacitor, Ceramic, 50V, NPO, 5%	0603	Std	Std
C3, C4	100 µF	Capacitor, Ceramic, 6.3V, X5R	1210	C3225X5R0J107M	TDK
C5	1200 pF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
C6	0.047 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
C7	5600 pF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
C8	0.047 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
C9, C11, C12	0.01 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
C13		Not installed			
J1, J4	PTC36SAAN	Header, Male 2-pin, 100mil spacing, (36-pin strip)	0.100 inch x 2	PTC36SAAN	Sullins
J2, J3	ED1609	Terminal Block, 2-pin, 15-A, 5,1mm	0.40 × 0.35"	ED1609	OST
L1 see Note 5	0.35 µH	Inductor, Dual, 11A,	0.264 × 0.295 inch	SLC7530-820ML	Coilcraft
R1, R2, R8	10.0 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R3	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R4	10	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R5	27.4 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R6	2.32 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R7	681	Resistor, Chip, 1/16W, 1%	0603	Std	Std
TP1–TP4	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 inch	5000	Keystone
TP5, TP6	5006	Test Point, Black, Thru Hole Compact Style	0.125 × 0.125 inch	5006	Keystone
TP7	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 inch	5001	Keystone
U1	TPS54917RUV	IC, 3-V TO 4-V INPUT, 9-A, Small synchronous-buck	RUV-34	TPS54917RUV	TI
–		Shunt, 100-mil, Black	0.100	929950-00	3M
		PCB, 3.0" × 3.0" × 0.062"		HPA367	Any

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFR's components.
5. L1 is used in series and the value is 0.35µH.

4.2 Schematic

Figure 16 is the schematic for the TPS54917EVM-367.

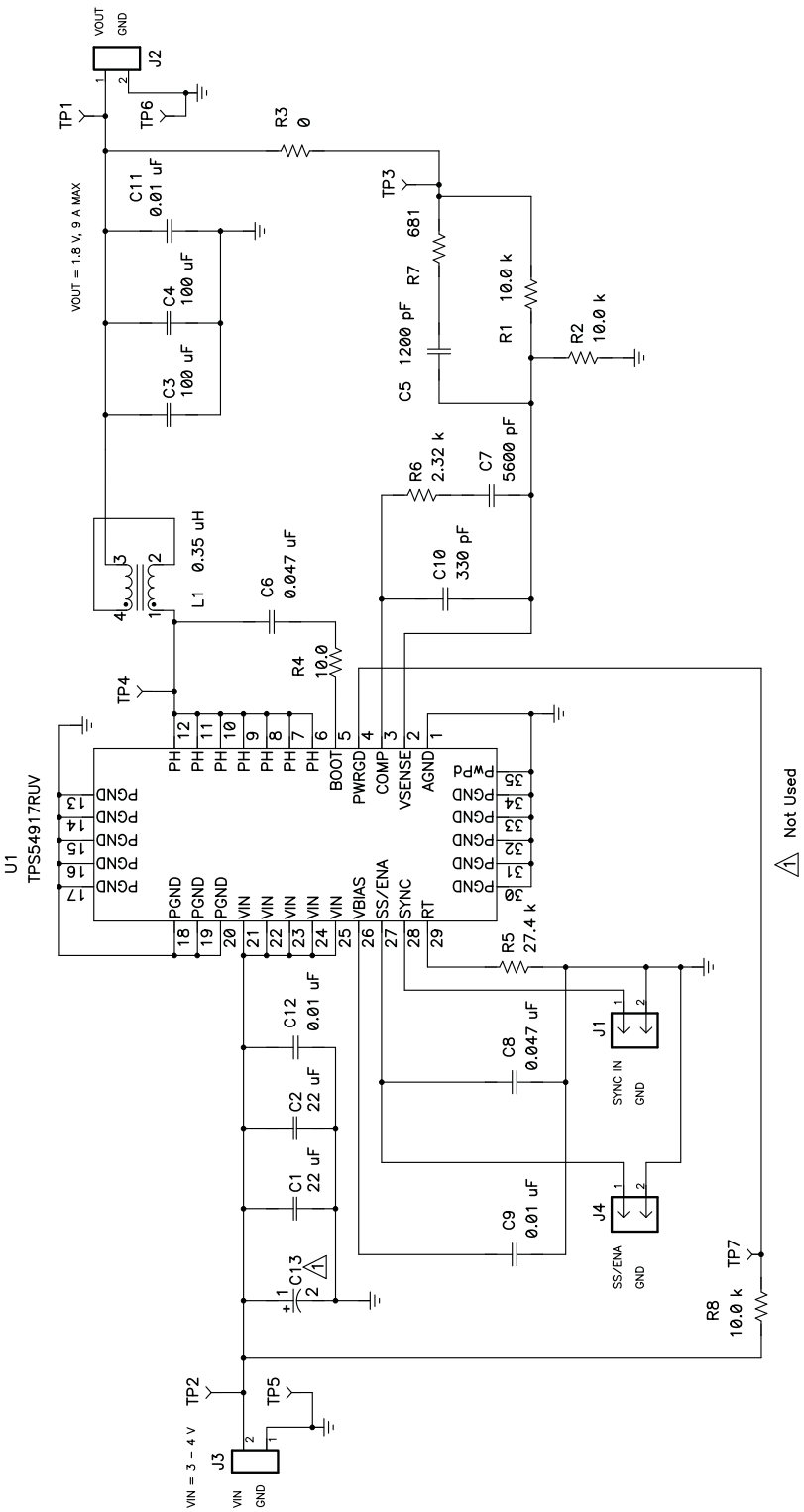


Figure 16. TPS54917EVM-367Schematic

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range and the output current range specified in Table 1.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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