TPS54824 4.5-V to 17-V (19-V Maximum) Input, 8-A Synchronous SWIFT™ Step-Down Converter

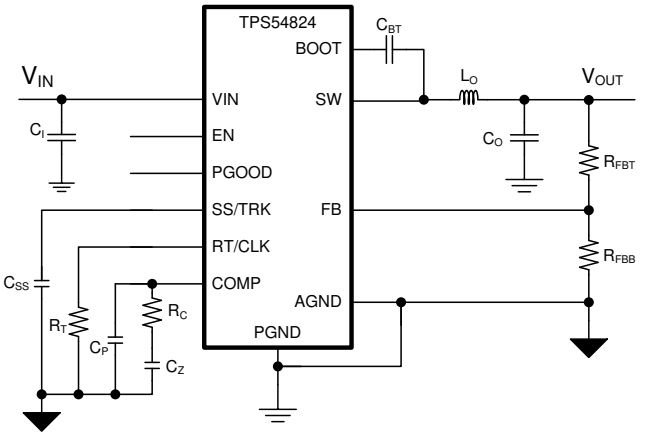
1 Features

- Small 3.5-mm × 3.5-mm HotRod™ QFN package
- Integrated 14.1-mΩ and 6.1-mΩ MOSFETs
- Peak current mode control with fast transient response
- 200-kHz to 1.6-MHz fixed switching frequency
- Synchronizes to external clock
- 0.6-V voltage reference ±0.85% over temperature
- 0.6-V to 12-V output voltage range
- Hiccup Current Limit
- Safe start-up into pre-biased output voltage
- Adjustable soft start and power sequencing
- Adjustable input undervoltage lockout
- 3-µA shutdown current
- Power good output monitor for undervoltage and overvoltage
- Output overvoltage protection
- Non-latch thermal shutdown protection
- –40°C to 150°C operating junction temperature

2 Applications

- Telecom and wireless infrastructure
- Test and measurement
- Medical imaging equipment
- Enterprise switching
- Server

Simplified Schematic



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3 Description

The TPS54824 is a full-featured 17-V (19-V maximum), 8-A synchronous step-down DC/DC converter in a 3.5 mm × 3.5 mm HotRod™ QFN package.

The device is optimized for small solution size through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are achieved through peak current mode control, which reduces component count, and by selecting a high switching frequency, reducing the inductor footprint.

The peak current mode control simplifies the loop compensation and provides fast transient response. Cycle-by-cycle peak current limiting on the high-side and low-side sourcing current limit protects the device in overload situations. Hiccup limits MOSFET power dissipation if a short circuit or over loading fault persists.

A power good supervisor circuit monitors the regulator output. The PGOOD pin is an open-drain output and goes high impedance when the output voltage is in regulation. An internal deglitch time prevents the PGOOD pin from pulling low unless a fault has occurred.

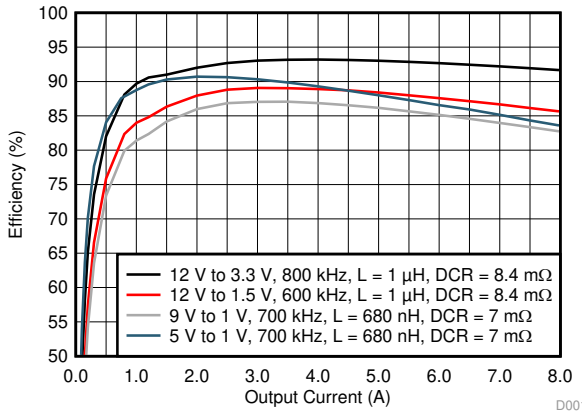
A dedicated EN pin can be used to control the regulator on/off and adjust the input undervoltage lockout. The output voltage start-up ramp is controlled by the SS/TRK pin, which allows operation as either a standalone power supply or in tracking situations.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54824	RNV (18)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (February 2017) to Revision B **Page**

- Changed Junction-to-ambient thermal resistance from 34 °C/W to to 25 °C/W. ... 5
- Added paragraph at end of Soft Start and Tracking ... 16
- Changed Equation 8 ... 18
- Added paragraph to end of Sequencing (SS/TRK) ... 19
- Changed to "The selected switching frequency must also consider the 10% tolerance" from "Considering the 10% tolerance" ... 24
- Changed to "The control loop needs to sense the change..." from "A regulator usually needs two or more clock cycles..." ... 25
- Changed Equation 18 ... 25
- Changed from R8 to R6 and from R6 to R8 ... 26
- Changed recommendations for feed forward capacitor ... 28
- Changed Equation 34 ... 28

Changes from Original (November 2016) to Revision A **Page**

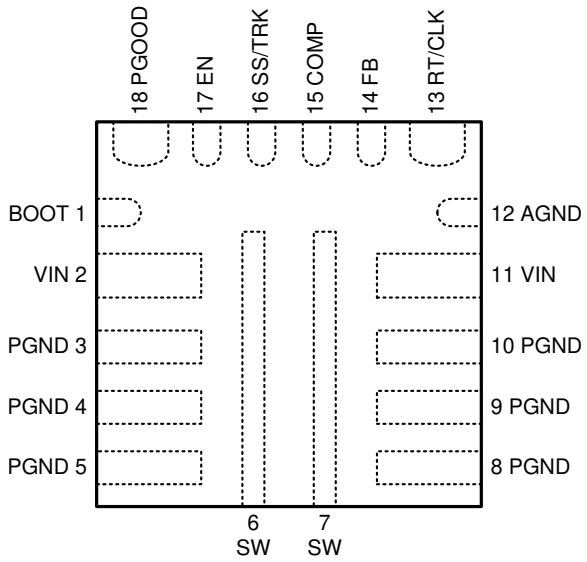
- Changed the VIN MAX value From: 18 V To: 19 V in the *Absolute Maximum Ratings* ... 4
- Changed the BOOT MAX value From: 25 V To: 27 V in the *Absolute Maximum Ratings* ... 4
- Changed the BOOT (10 ns transient) MAX value From: 27 V To: 30 V in the *Absolute Maximum Ratings* ... 4
- Changed the BOOT (vs SW) MAX value From: 6.5 V To: 7 V in the *Absolute Maximum Ratings* ... 4
- Changed the SW MAX value From: 19 V To: 20 V in the *Absolute Maximum Ratings* ... 4
- Changed the SW (10 ns transient) MAX value From: 21 V To: 23 V in the *Absolute Maximum Ratings* ... 4

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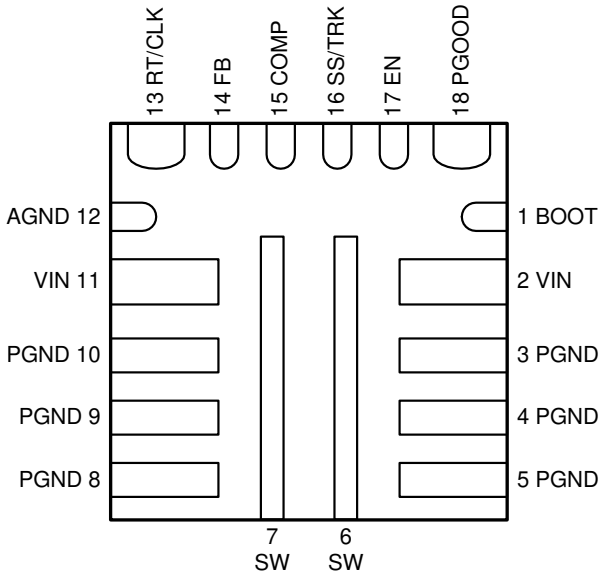
5 Pin Configuration and Functions

RNV Package
18-Pin VQFN-HR

Top View



Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	I	Floating supply voltage for high-side MOSFET gate drive circuit. Connect a 0.1-µF ceramic capacitor between BOOT and SW pins.
VIN	2, 11	I	Input voltage supply pin. Power for the internal circuit and the connection to drain of high-side MOSFET. Connect both pins to the input power source with a low impedance connection. Connect both pins and their neighboring PGND pins.
PGND	3, 4, 5, 8, 9, 10	–	Ground return for low-side power MOSFET and its drivers.
SW	6, 7	O	Switching node. Connected to the source of the high-side MOSFET and drain of the low-side MOSFET.
AGND	12	–	Ground of internal analog circuitry. AGND must be connected to the PGND plane.
RT/CLK	13	I	Switching frequency setting pin. In RT mode, an external timing resistor adjusts the switching frequency. In CLK mode, the device synchronizes to an external clock input to this pin.
FB	14	I	Converter feedback input. Connect to the output voltage with a resistor divider.
COMP	15	I	Error amplifier output and input to the PWM modulator. Connect loop compensation to this pin.
SS/TRK	16	I	Soft-start and tracking pin. Connecting an external capacitor sets the soft-start time. This pin can also be used for tracking and sequencing.
EN	17	I	Enable pin. Float or pull high to enable the device. Connect a resistor divider to this pin to implement adjustable under voltage lockout and hysteresis.
PGOOD	18	O	Open-drain power good indicator. It is asserted low if output voltage is outside if the PGOOD thresholds, VIN is low, EN is low, device is in thermal shutdown or device is in soft-start.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VIN	–0.3	19	V
	BOOT	–0.3	27	
	BOOT (10 ns transient)	–0.3	30	
	BOOT (vs SW)	–0.3	7	
	SW	–1	20	
	SW (10 ns transient)	–3	23	
	EN, SS/TRK, PGOOD, RT/CLK, FB, COMP	–0.3	6.5	
Operating Junction Temperature Range, T_J		-40	150	°C
Storage Temperature Range, T_{STG}		-55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	4.5		17	V
V_{OUT}	Output Voltage	0.6		12	V
I_{OUT}	Output current			8	A
T_J	Operating junction temperature	-40		150	°C
f_{SW}	Switching Frequency (RT mode and PLL mode)	200		1600	kHz

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6.4 Thermal Information

THERMAL METRIC(1)		TPS54824 RNV 18 PINS	UNIT
$Theta_{JA}$	Junction-to-ambient thermal resistance JEDEC	57.1	°C/W
$Theta_{JA}$	Junction-to-ambient thermal resistance EVM	25	°C/W
$Theta_{JCtop}$	Junction-to-case (top) thermal resistance	26.3	°C/W
$Theta_{JB}$	Junction-to-board thermal resistance	18.8	°C/W
Psi_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Psi_{JB}	Junction-to-board characterization parameter	18.8	°C/W
$Theta_{JCbot}$	Junction-to-case (bottom) thermal resistance	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

T_J = -40°C to 150°C, VIN = 4.5 V to 17 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
UVLO_rise	VIN under-voltage lockout	$V_{(VIN)}$ rising		4.1	4.3	V
UVLO_fall		$V_{(VIN)}$ falling	3.7	3.9		V
UVLO_hys		Hysteresis VIN voltage		0.2		V
Ivin	Operating non-switching supply current	$V_{(EN)}$ = 5 V, $V_{(FB)}$ = 1.5 V		580	800	µA
Ivin_sdn	Shutdown supply current	$V_{(EN)}$ = 0 V		3	11	µA
ENABLE						
Ven_rise	EN threshold	$V_{(EN)}$ rising		1.20	1.26	V
Ven_fall		$V_{(EN)}$ falling	1.1	1.15		V
Ven_hys	EN pin threshold voltage hysteresis			50		mV
Ip	EN pin sourcing current	$V_{(EN)}$ = 1.1V		1.2		µA
Iph	EN pin sourcing current	$V_{(EN)}$ = 1.3V		4.8		µA
Ih	EN pin hysteresis current			3.6		µA
FB						
V_{FB}	Regulated FB voltage	T_J = 25°C	596	600	604	mV
			595	600	605	mV
ERROR AMPLIFIER						
gmea	Error Amplifier Transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		1100		µA/V
	Error Amplifier DC gain			80		dB
Icomp_src	Error Amplifier source current	$V_{(FB)}$ = 0 V		100		µA
Icomp_snk	Error Amplifier sink current	$V_{(FB)}$ = 2 V		-100		µA
gmps	Power Stage Transconductance			16		A/V
SOFT-START						
Iss	Soft-start current			5		µA
	$V_{(SS/TRK)}$ to $V_{(FB)}$ matching	$V_{(SS/TRK)}$ = 0.4 V		25		mV
MOSFET						
Rds(on)_h	High-side switch resistance	T_A = 25°C, $V_{(VIN)}$ = 12 V		14.1		mΩ
		T_A = 25°C, $V_{(VIN)}$ = 4.5 V, $V_{(BOOT-SW)}$ = 4.5 V		15.9		mΩ
Rds(on)_l	Low-side switch resistance	T_A = 25°C, $V_{(VIN)}$ = 12 V		6.1		mΩ
		T_A = 25°C, $V_{(VIN)}$ = 4.5 V		6.9		mΩ
	BOOT UVLO Falling			2.2	2.6	V
CURRENT LIMIT						
Ioc_HS_pk	High-side peak current limit		10.8	12.9	15	A
Ioc_LS_snk	Low-side sinking current limit			–3.4		A
Ioc_LS_src	Low-side sourcing current limit		9.3	11.4	13.6	A

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Electrical Characteristics (continued)

T_J = -40°C to 150°C, VIN = 4.5 V to 17 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RT/CLK						
V_{IH}	Logic high input voltage		2			V
V_{IL}	Logic low input voltage				0.8	V
PGOOD						
	Power good threshold	$V_{(FB)}$ rising (fault)		108%		
		$V_{(FB)}$ falling (good)		106%		
		$V_{(FB)}$ rising (good)		91%		
		$V_{(FB)}$ falling (fault)		89%		
Ipg_lkg	Leakage current when pulled high	$V_{(PGOOD)}$ = 5 V		5		nA
Vpg_low	PGOOD voltage when pulled low	$I_{(PGOOD)}$ = 2 mA			0.3	V
	Minimum VIN for valid output	$V_{(PGOOD)}$ < 0.5 V, $I_{(PGOOD)}$ = 4 mA		0.7	1	V
Thermal protection						
T_{TRIP}	Thermal protection trip point	Temperature Rising		170		°C
T_{HYST}	Thermal protection hysteresis			15		°C

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6.6 Switching Characteristics

T_J = -40°C to 150°C, $V_{(VIN)}$ = 4.5 V to 17 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN						
	EN to start of switching			135		µs
PGOOD						
	Deglitch time PGOOD going high			272		Cycles
	Deglitch time PGOOD going low			16		Cycles
SW						
ton_min	Minimum on time	Measured at 50% to 50% of V_{IN}, L = 0.68 µH, I_{OUT} = 0.1 A		95		ns
toff_min	Minimum off time (1)	$V_{(BOOT-SW)}$ ≥ 2.6 V			0	ns
RT/CLK						
fsw_min	Minimum switching frequency (RT mode)	$R_{(RT/CLK)}$ = 250 kΩ		200		kHz
	Switching frequency (RT mode)	$R_{(RT/CLK)}$ = 100 kΩ	450	500	550	kHz
fsw_max	Maximum switching frequency (RT mode)	$R_{(RT/CLK)}$ = 30.1 kΩ		1.6		MHz
fsw_clk	Switching frequency synchronization range (PLL mode)		200		1600	kHz
	RT/CLK falling edge to SW rising edge delay (PLL mode)	Measure at 500kHz with RT resistor in series with RT/CLK		70		ns
HICCUP						
	Wait time before hiccup			512		Cycles
	Hiccup time before restart			16384		Cycles

(1) Specified by design.

6.7 Timing Requirements

T_J = -40°C to 150°C, $V_{(VIN)}$ = 4.5 V to 17 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
RT/CLK						
	Minimum synchronization signal pulse width (PLL mode)				35	ns

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6.8 Typical Characteristics

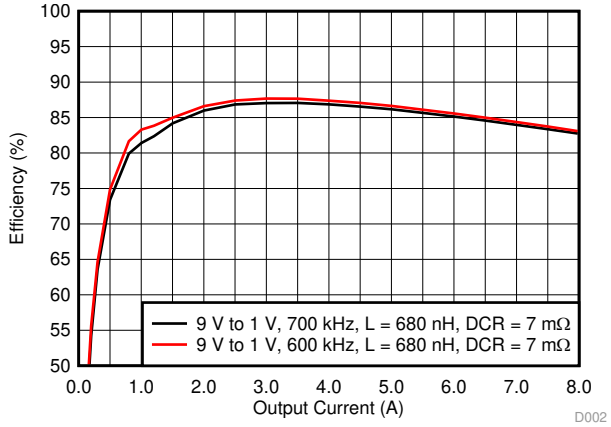


Figure 1. Efficiency for 9 V Input to 1 V Output

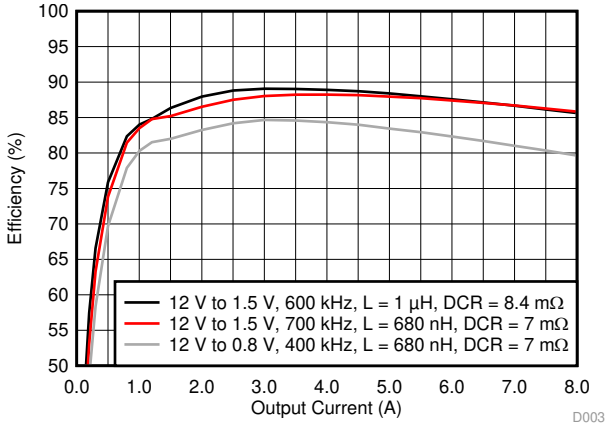


Figure 2. Efficiency for 12 V Input to 1.5 V and 0.8 V Output

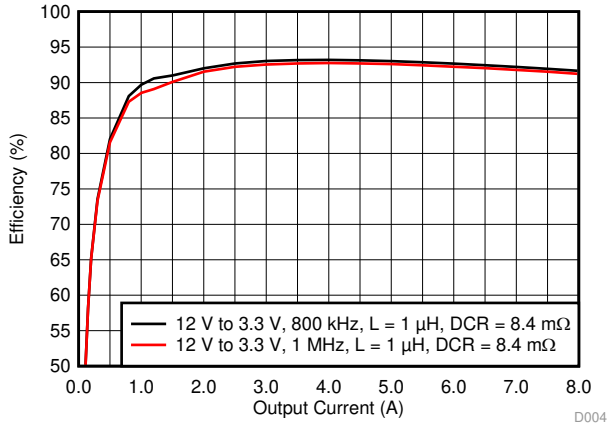


Figure 3. Efficiency for 12 V Input to 3.3 V Output

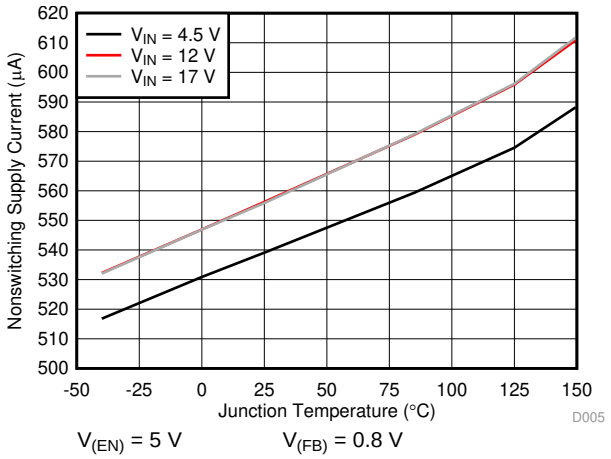


Figure 4. VIN Pin Nonswitching Supply Current vs Junction Temperature

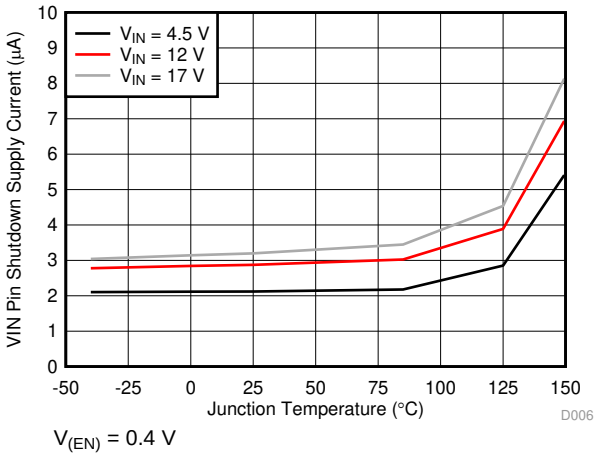


Figure 5. VIN Pin Shutdown Current vs Junction Temperature

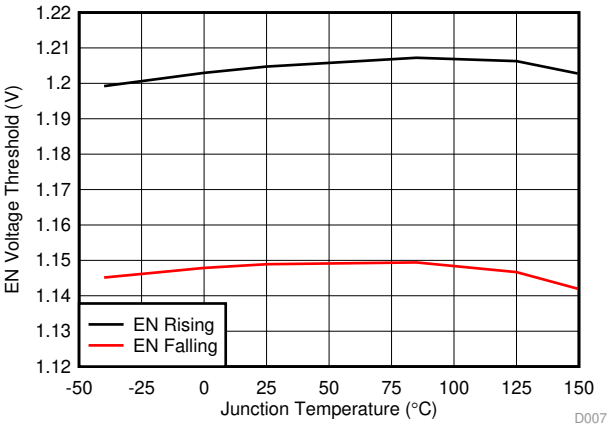


Figure 6. EN Pin Voltage Threshold vs Junction Temperature

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Typical Characteristics (continued)

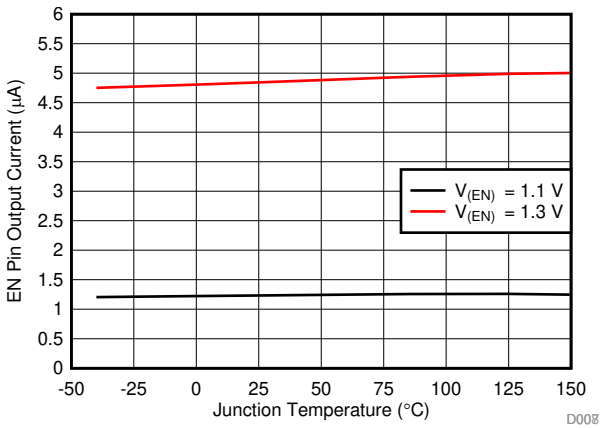


Figure 7. EN Pin Current vs Junction Temperature

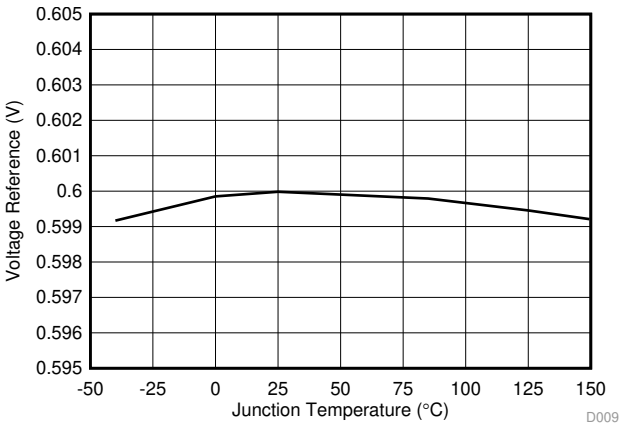


Figure 8. Regulated FB Voltage vs Junction Temperature

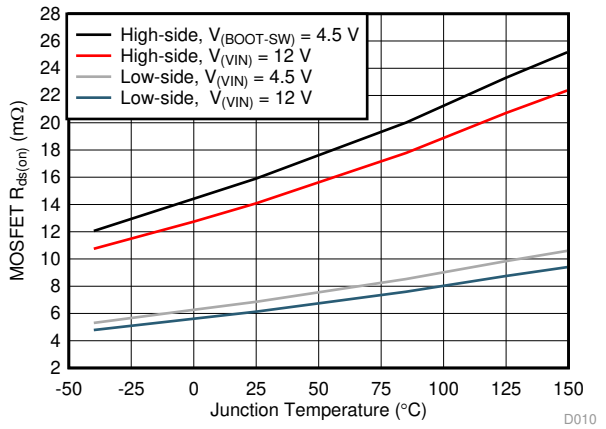


Figure 9. MOSFET Rds(on) vs Junction Temperature

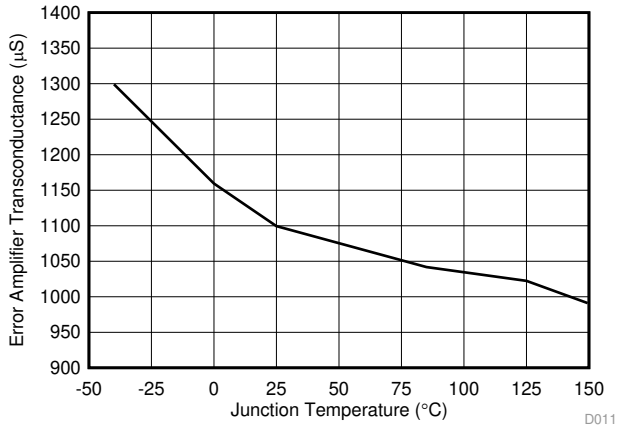


Figure 10. Error Amplifier Transconductance vs Junction Temperature

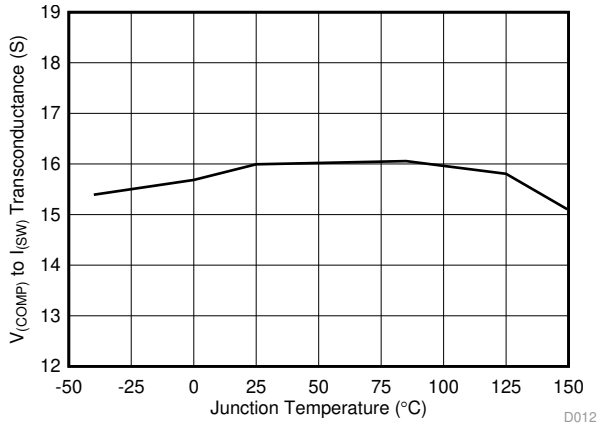


Figure 11. COMP to SW Transconductance vs Junction Temperature

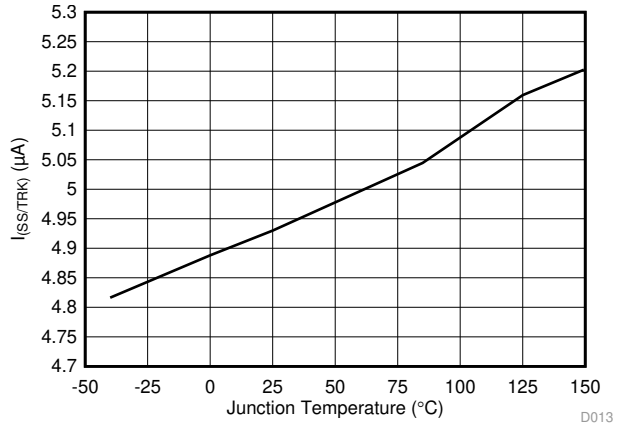
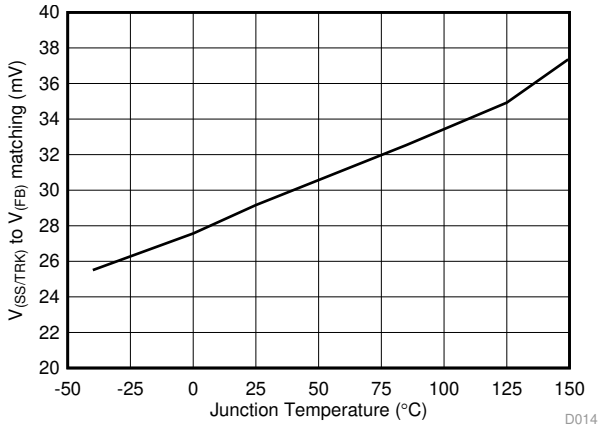


Figure 12. SS/TRK Current vs Junction Temperature

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Typical Characteristics (continued)



$V_{(SS/TRK)}$ = 0.4 V

Figure 13. SS/TRK to FB Offset vs Junction Temperature

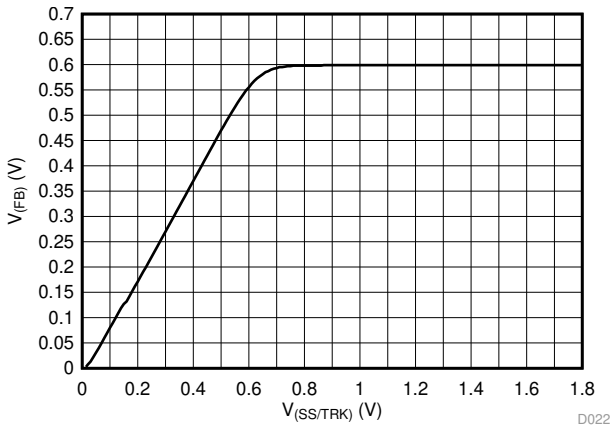


Figure 14. FB voltage vs SS/TRK Voltage

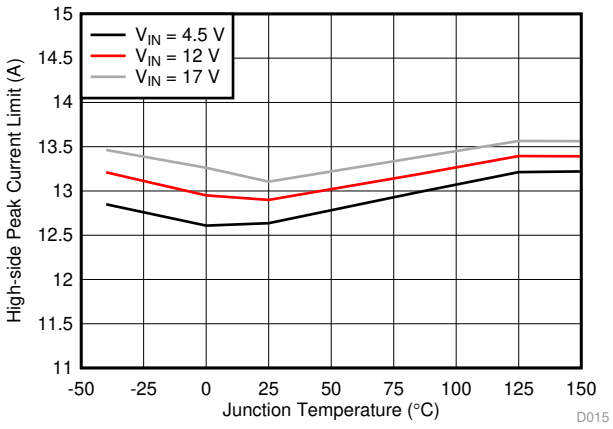


Figure 15. High-side Peak Current Limit vs Junction Temperature

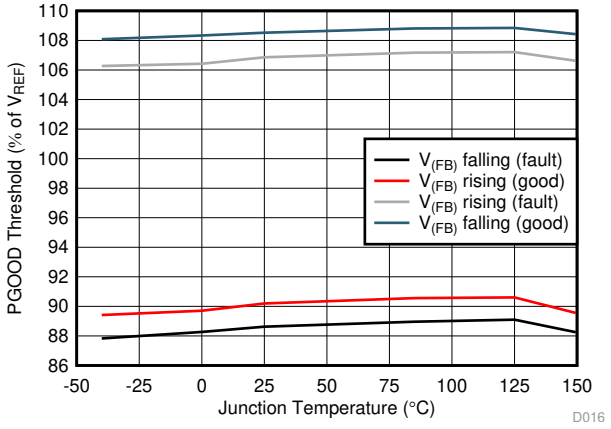
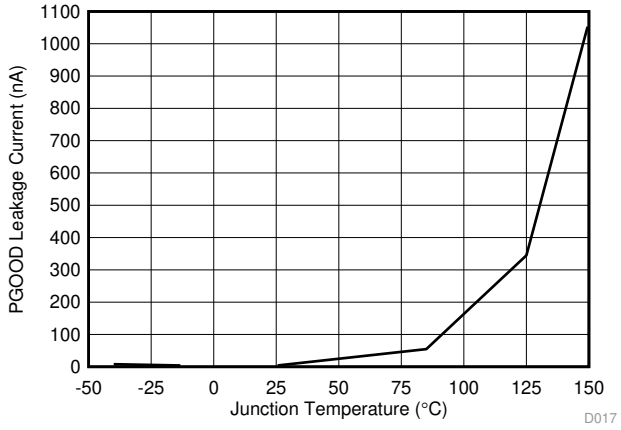
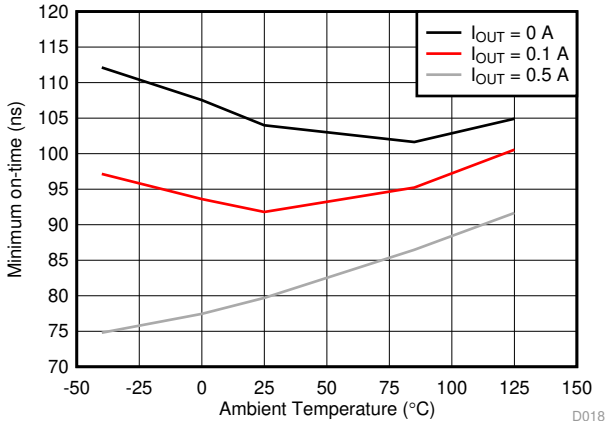


Figure 16. PGOOD Thresholds vs Junction Temperature



$V_{(FB)}$ = 0.6 V $V_{(PGOOD)}$ = 5 V

Figure 17. PGOOD Leakage Current vs Junction Temperature

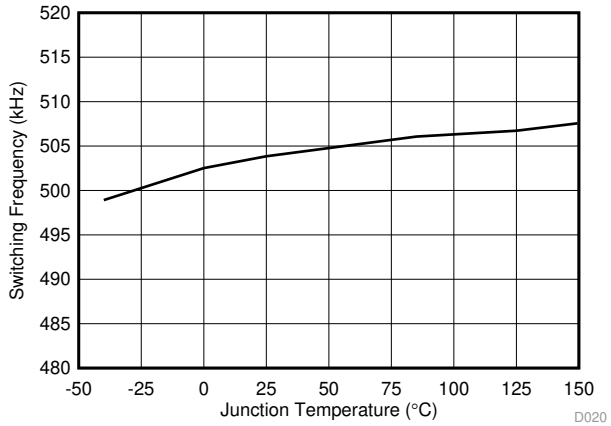


V_{IN} = 12 V L = 0.68 µH

Figure 18. Minimum on-time vs Ambient Temperature

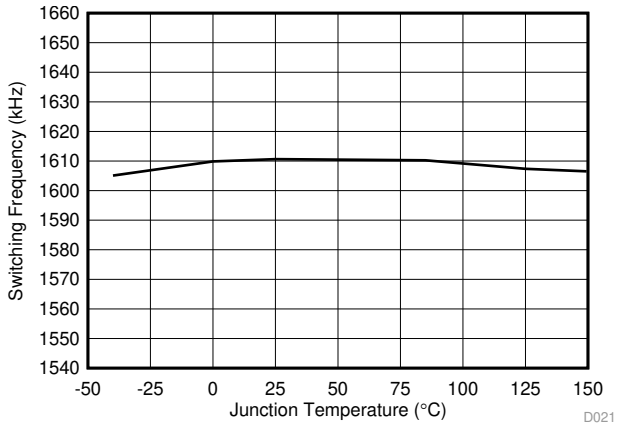
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Typical Characteristics (continued)



$R_{(RT/CLK)}$ = 100 kΩ

Figure 19. Switching Frequency vs Junction Temperature (500 kHz)



$R_{(RT/CLK)}$ = 30.1 kΩ

Figure 20. Switching Frequency vs Junction Temperature (1600 kHz)

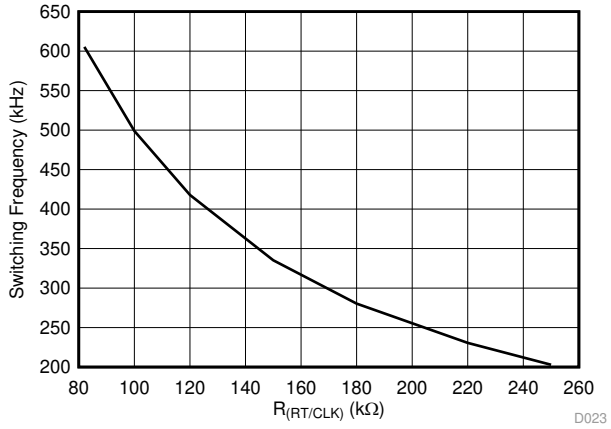


Figure 21. Switching Frequency vs RT/CLK Resistor (Low Range)

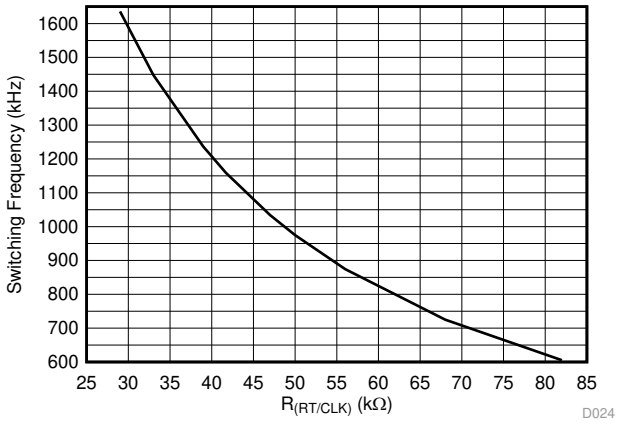


Figure 22. Switching Frequency vs RT/CLK Resistor (High Range)

7 Detailed Description

7.1 Overview

The TPS54824 is a 17-V, 8-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant frequency, peak current mode control which also simplifies external frequency compensation. The wide switching frequency of 200 kHz to 1600 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The TPS54824 also has an internal phase lock loop (PLL) connected to the RT/CLK pin that can be used to synchronize the switching cycle to the falling edge of an external system clock.

The integrated MOSFETs allow for high efficiency power supply designs with continuous output currents up to 8 amperes. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications. The device reduces the external component count by integrating a bootstrap recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and SW pins. The BOOT capacitor voltage is monitored by a BOOT to SW UVLO (BOOT-SW UVLO) circuit allowing SW pin to be pulled low to recharge the BOOT capacitor. The device can operate at 100% duty cycle as long as the BOOT capacitor voltage is higher than the preset BOOT-SW UVLO threshold which is typically 2.2 V.

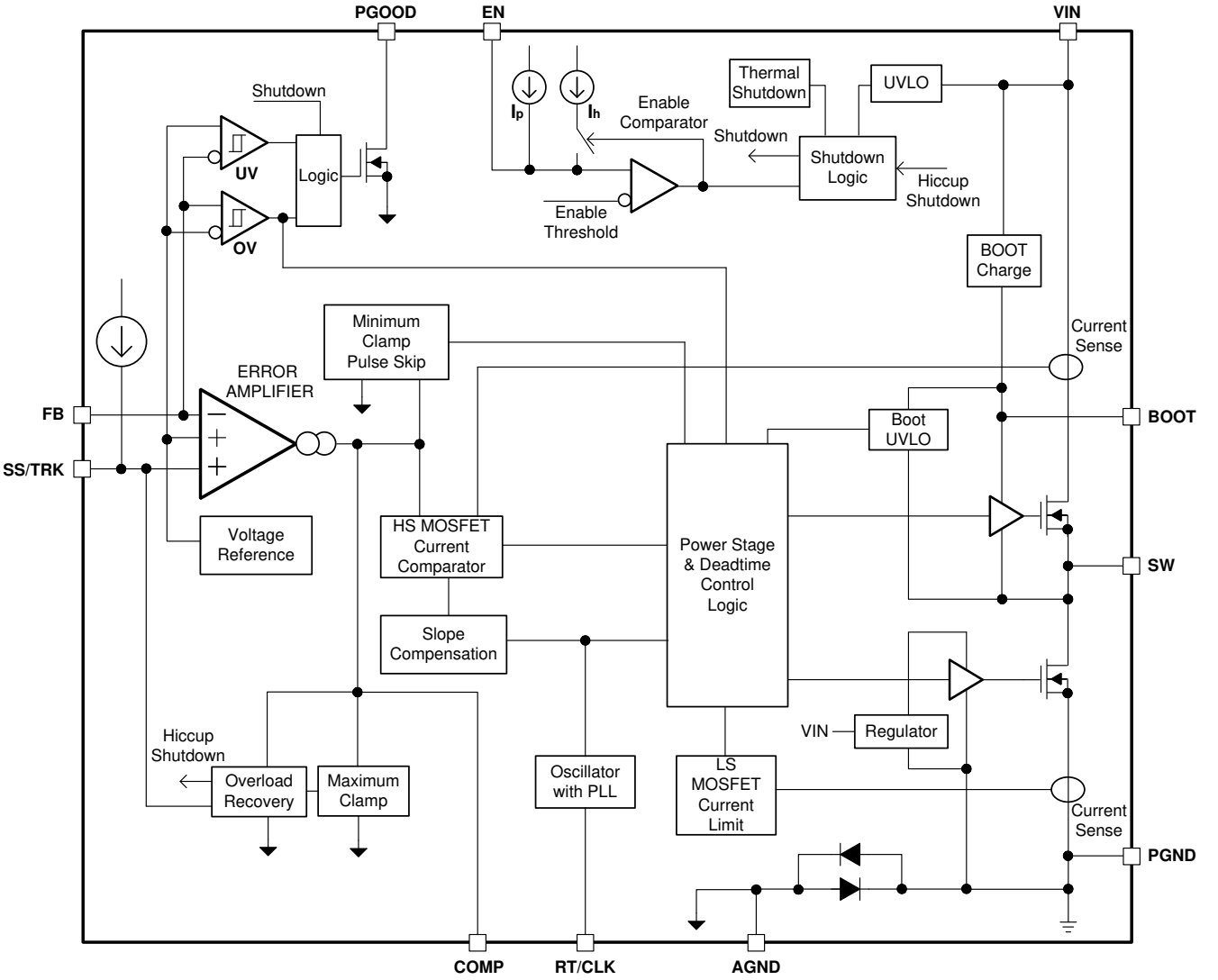
The TPS54824 has been designed for safe monotonic startup into pre-biased loads. The default start up is when VIN is typically 4.1 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the internal pull-up current of the EN pin allows the device to operate with the EN pin floating. The operating current for the TPS54824 is typically 580 μA when not switching and under no load. When the device is disabled, the supply current is typically 3 μA.

The SS/TRK (soft start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider should be coupled to the pin for soft start or critical power supply sequencing requirements. The output voltage can be stepped down to as low as the 0.6 V voltage reference (V_{REF}). The device has a power good comparator (PGOOD) with hysteresis which monitors the output voltage through the FB pin. The PGOOD pin is an open drain MOSFET which is pulled low when the FB pin voltage is less than 89% or greater than 108% of the reference voltage V_{REF} and asserts high when the FB pin voltage is 91% to 106% of V_{REF}.

The device is protected from output overvoltage, overload and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the FB pin voltage is lower than 106% of the V_{REF}. The device implements both high-side MOSFET over current protection and bidirectional low-side MOSFET over current protections which help control the inductor current and avoid current runaway. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the soft start circuit automatically when the junction temperature drops 15°C typically below the thermal shutdown trip point.

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7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The device uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches current reference generated by the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on.

The device adds an internal slope compensation ramp to prevent subharmonic oscillations. The peak inductor current limit remains constant over the full duty cycle range.

7.3.2 Continuous Conduction Mode Operation (CCM)

As a synchronous buck converter, the device works in CCM (Continuous Conduction Mode) under all load conditions.

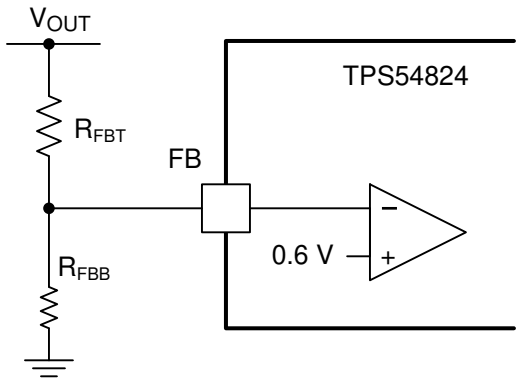
Feature Description (continued)

7.3.3 VIN Pins and VIN UVLO

The VIN pin voltage supplies the internal control circuits of the device and provides the input voltage to the power converter system. The input voltage for VIN can range from 4.5 V to 17 V. The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 200 mV. A voltage divider connected to the EN pin can adjust the input voltage UVLO appropriately. See *Enable and Adjustable UVLO* for more details.

7.3.4 Voltage Reference and Adjusting the Output Voltage

The voltage reference system produces a precise ±0.85%, 0.6 V voltage reference over temperature by scaling the output of a temperature stable band gap circuit. The output voltage is set with a resistor divider from the output (V_{OUT}) to the FB pin shown in Figure 23. It is recommended to use 1% tolerance or better divider resistors. Start with a fixed value for the bottom resistor in the divider, typically 10 kΩ, then use Equation 1 to calculate the top resistor in the divider. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable. The minimum output voltage and maximum output voltage can be limited by the minimum on time of the high side MOSFET and bootstrap voltage (BOOT-SW voltage) respectively.



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Figure 23. FB Resistor Divider

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

7.3.5 Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the FB pin voltage to the lower of the SS/TRK pin voltage or the internal 0.6-V voltage reference. The transconductance of the error amplifier is 1100 μA/V. The frequency compensation network is connected between the COMP pin and ground.

When operating at current limit the COMP pin voltage is clamped to a maximum level to improve response when the load current decreases. When FB is greater than the internal voltage reference or SS/TRK the COMP pin voltage is clamped to a minimum level and the devices enters a high-side skip mode.

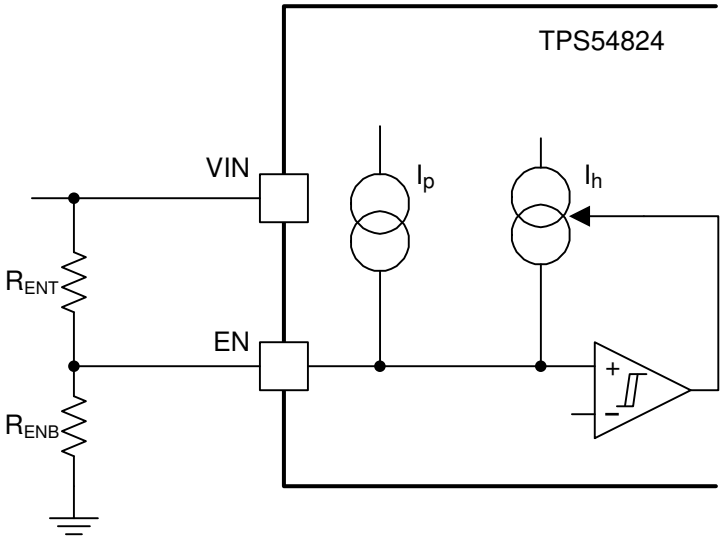
7.3.6 Enable and Adjustable UVLO

The EN pin provides on/off control of the device. Once the EN pin voltage exceeds its threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low operating current state. The EN pin has an internal pull-up current source, Ip, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, an open drain or open collector output logic can be interfaced with the pin.

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Feature Description (continued)

An external resistor divider can be added from VIN to the EN pin for adjustable UVLO and hysteresis as shown in Figure 24. The EN pin has a small pull-up current Ip which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function since it increases by Ih once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 2 and Equation 3. When using the adjustable UVLO function, 500 mV or greater hysteresis is recommended. For applications with very slow input voltage slew rate, a capacitor can be placed from the EN pin to ground to filter any glitches on the input voltage.



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Figure 24. Adjustable UVLO Using EN

$$R_{ENT} = \frac{V_{START} \times \left(\frac{V_{ENFALLING}}{V_{ENRISING}} \right) - V_{STOP}}{I_p \times \left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_h} \quad (2)$$

$$R_{ENB} = \frac{R_{ENT} \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_{ENT} \times \left(I_p + I_h \right)} \quad (3)$$

7.3.7 Soft Start and Tracking

The TPS54824 regulates to the SS/TRK pin while its voltage is lower than the internal reference to implement soft start. A capacitor on the SS/TRK pin to ground sets the soft start time. The SS/TRK pin has an internal pull-up current source of 5 μA that charges the external soft start capacitor. Equation 4 calculates the required soft start capacitor value. The FB voltage will follow the SS/TRK pin voltage with a 25 mV offset up to 90% of the internal voltage reference. When the SS/TRK voltage is greater than 90% of the internal reference voltage the offset increases as the effective system reference transitions from the SS/TRK voltage to the internal voltage reference.

$$C_{SS}\left(nF\right) = \frac{I_{SS}\left(\mu A\right) \times t_{SS}\left(ms\right)}{V_{REF}\left(V\right)} = 8.3 \times t_{SS}\left(ms\right) \quad (4)$$

If during normal operation, VIN goes below the UVLO, EN pin pulled below 1.15 V, or a thermal shutdown event occurs, the TPS54824 stops switching and the SS/TRK pin floats. When the VIN goes above UVLO, EN goes above 1.20 V, or a thermal shutdown is exited, the SS/TRK pin is discharged to near ground before reinitiating a powering up sequence.

Feature Description (continued)

When the COMP pin voltage is clamped by the maximum COMP clamp in an overload condition the SS/TRK pin is discharged to near the FB voltage. When the overload condition is removed, the soft-start circuit controls the recovery from the fault output level to the nominal output regulation voltage. At the beginning of recovery a spike in the output voltage may occur while the COMP voltage transitions from the maximum clamp to the value determined by the loop.

If a nominal SS/TRK capacitance of 22 nF or greater is used, TI recommends adding a 470-kΩ to 1-MΩ resistor in parallel with the SS/TRK capacitor. With higher SS/TRK capacitance and if the EN pin voltage goes low then high quickly, the SS/TRK capacitor may not fully discharge before switching begins. Adding this resistor helps discharge the SS/TRK capacitor. For the SS capacitor to fully discharge, disable the TPS54824 for a time period equal to 3 times the RC time constant of the SS/TRK capacitor and the added resistor.

7.3.8 Safe Start-up into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to sink current until the SS/TRK pin voltage is higher than the FB pin voltage and the high-side MOSFET begins to switch. The one exception is if the BOOT-SW voltage is below the UVLO threshold. While in BOOT-SW UVLO, the low-side MOSFET is allowed to turn on to charge the BOOT capacitor. The low-side MOSFET reverse current protection provides another layer of protection for the device after the high-side MOSFET begins to switch.

7.3.9 Power Good

The PGOOD pin is an open-drain output requiring an external pull-up resistor to output a high signal. Once the FB pin is between 91% and 106% of the internal voltage reference and SS/TRK is greater than 0.75 V, after a 272 cycle deglitch time the PGOOD pin is de-asserted and the pin floats. A pull-up resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is 6.5 V or less is recommended. PGOOD is in a defined state once the VIN input voltage is greater than 1 V but with reduced current sinking capability.

When the FB is lower than 89% or greater than 108% of the nominal internal reference voltage, after a 16 cycle deglitch time the PGOOD pin is pulled low. PGOOD is immediately pulled low if VIN falls below its UVLO, EN pin is pulled low or the TPS54824 enters thermal shutdown.

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Feature Description (continued)

7.3.10 Sequencing (SS/TRK)

Many of the common power supply sequencing methods can be implemented using the SS/TRK, EN and PGOOD pins.

The sequential method is illustrated in Figure 25 using two TPS54824 or similar devices. The power good of the first device is coupled to the EN pin of the second device which enables the second power supply once the primary supply reaches regulation.

Figure 26 shows the method implementing ratiometric sequencing by connecting the SS/TRK pins of two devices together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time the current source must be doubled in Equation 4.

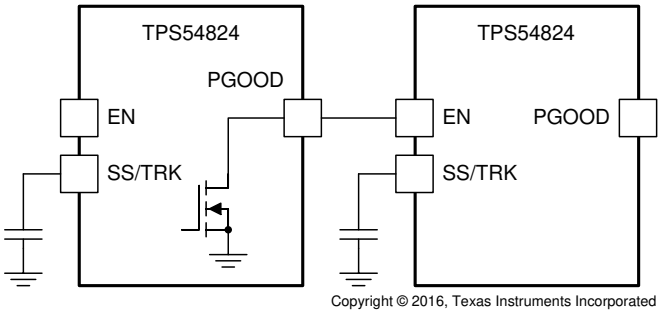


Figure 25. Sequential Start-Up Sequence

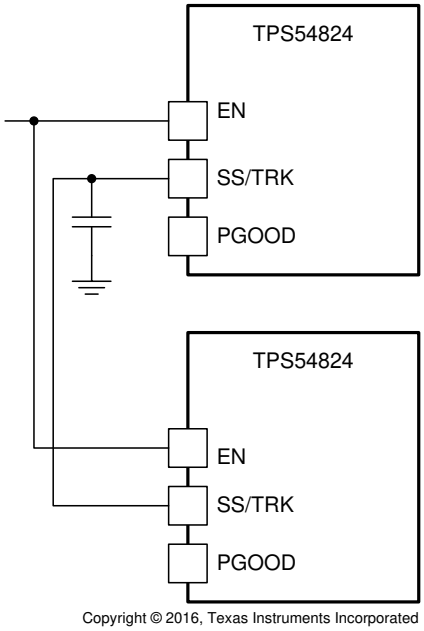


Figure 26. Ratiometric Start-Up Sequence

Feature Description (continued)

Ratiometric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R_{TRT} and R_{TRB} shown in Figure 27 to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 6 and Equation 7, the tracking resistors can be calculated to initiate the V_{OUT2} slightly before, after or at the same time as V_{OUT1}. Equation 5 is the voltage difference between V_{OUT1} and V_{OUT2}.

To design a ratiometric start-up in which the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in Equation 6 and Equation 7 for deltaV. Equation 5 results in a positive number for applications where the V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved.

The deltaV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TRK to FB offset (Vssoffset = 25 mV) in the soft-start circuit and the offset created by the pull-up current source (Iss = 5 μA) and tracking resistors, the Vssoffset and Iss are included as variables in the equations.

When the TPS54824 is enabled, an internal switch at the SS/TRK pin turns on to discharge the SS/TRK voltage to near ground as described in Soft Start and Tracking. The SS/TRK pin voltage must discharge low enough before the TPS54824 starts up. If there is voltage on V_{OUT1} and the upper resistor at the SS/TRK pin is too small, the SS/TRK pin cannot discharge low enough and V_{OUT2} does not ramp up. The upper resistor in the SS/TRK divider may need to be increased to allow the SS/TRK pin to drop close enough to ground. To ensure proper startup of V_{OUT2} , the calculated R_{TRT} value from Equation 6 must be greater than the value calculated in Equation 6. Calculate R_{TRB} using the final value of R_{TRT}.

$$\Delta V = V_{OUT1} - V_{OUT2} \tag{5}$$

$$R_{TRT} = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{Vssoffset}{Iss} \tag{6}$$

$$R_{TRB} = \frac{V_{REF} \times R_{TRT}}{V_{OUT2} + \Delta V - V_{REF}} \tag{7}$$

$$R_{TRT} > 20000 \times V_{OUT1} \tag{8}$$

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Feature Description (continued)

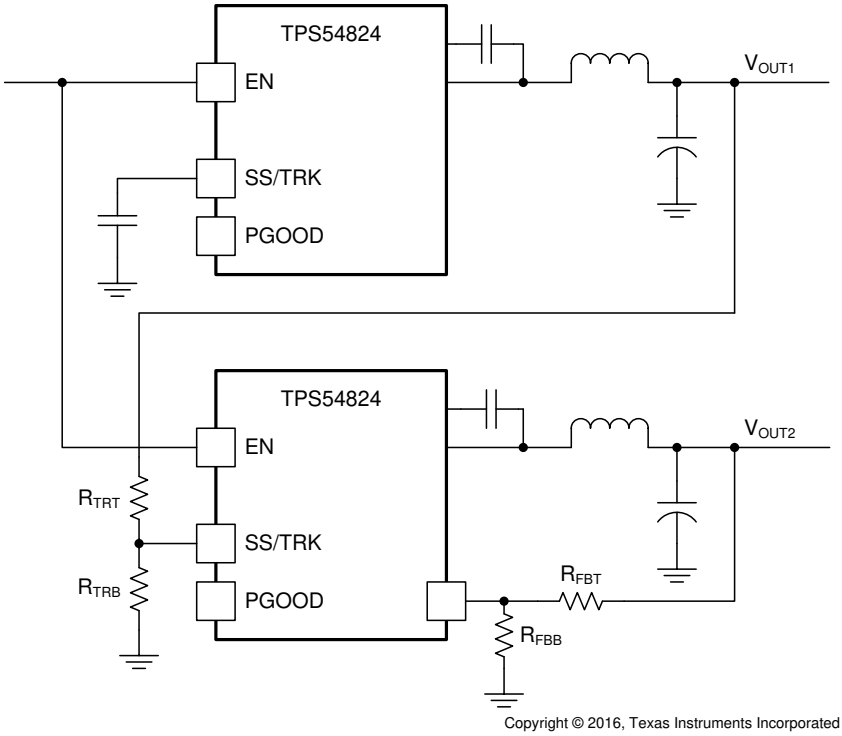


Figure 27. Ratiometric and Simultaneous Start-Up Sequence

As described in Power Good, for the PGOOD output to be active the SS/TRK voltage must be above 0.75 V. The external divider may prevent the SS/TRK voltage from charging above the threshold. For the SS/TRK pin to charge above the threshold, a switch may be needed to disconnect the resistor divider or modify the resistor divider ratio of the V_{OUT2} converter after start-up is complete. The PGOOD pin of the V_{OUT1} converter could be used for this. One solution is to add a resistor from SS/TRK of the V_{OUT2} converter to the PGOOD of the V_{OUT1} converter. While the PGOOD of V_{OUT1} pulls low, this resistor is in parallel with R_{TRB}. When V_{OUT1} is in regulation its PGOOD pin will float. If the PGOOD pin of V_{OUT1} is connected to a pullup voltage, make sure to include this in calculations. A second option is to use the PGOOD pin to turn on or turn off the external switch to change the divide ratio.

7.3.11 Adjustable Switching Frequency (RT Mode)

In RT mode, a resistor (RT resistor) is connected between the RT/CLK pin and AGND. The switching frequency of the device is adjustable from 200 kHz to 1600 kHz by placing a maximum of 250 kΩ and minimum of 30.1 kΩ respectively. To determine the RT resistance for a given switching frequency, use Equation 9. To reduce the solution size one would set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on-time should be considered. Equation 10 can be used to calculate the switching frequency for a given RT resistance.

$$RT\left(k\Omega\right) = 58650 \times f_{SW}\left(kHz\right)^{-1.028} \tag{9}$$

$$f_{SW}\left(kHz\right) = 43660 \times RT\left(k\Omega\right)^{-0.973} \tag{10}$$

Feature Description (continued)

7.3.12 Synchronization (CLK Mode)

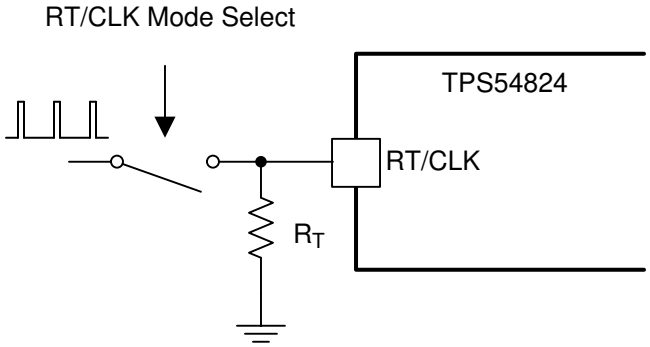
An internal Phase Locked Loop (PLL) has been implemented to allow synchronization from 200 kHz to 1600 kHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle from 20% to 80%. If the clock signals rising edge occurs near the falling edge of SW, increased SW jitter may occur. Use Equation 11 to calculate the maximum clock pulse width to minimize jitter in CLK mode. The clock signal amplitude must transition lower than 0.8 V and higher than 2 V. The start of the switching cycle is synchronized to the falling edge of the RT/CLK pin.

$$CLK_PW_{MAX} = \frac{0.75 \times \left(1 - \frac{V_{OUT}}{V_{IN(min)}}\right)}{f_{SW}} \quad (11)$$

In applications where both RT mode and CLK mode are needed, the device can be configured as shown in Figure 28. Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the SYNC pin is pulled above the RT/CLK high threshold (2 V), the device switches from the RT mode to the CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock.

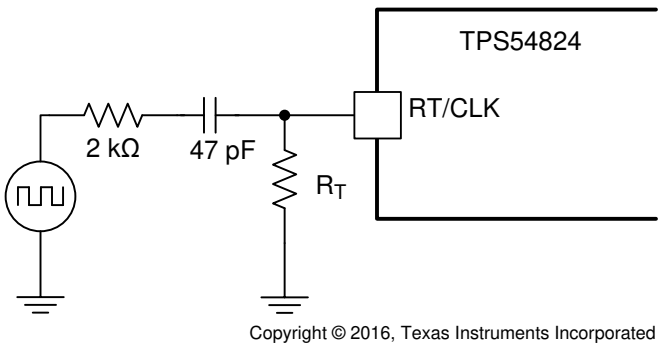
If the input clock goes away the internal clock frequency begins to drop and after 10 µs without a clock the device returns to RT mode. Output undershoot while the switching frequency drops can occur. Output overshoot can also occur when the switching frequency steps back up to the RT mode frequency. A high impedance tri-state buffer as shown in Figure 30 is recommended for best performance during the transition from CLK mode to RT mode because it minimizes the loading on the RT/CLK pin allowing faster transition back to RT mode. Figure 31 shows the typical performance for the transition from RT mode to CLK mode then back to RT mode.

A series RC circuit as shown in Figure 29 can also be used to interface the RT/CLK pin but the capacitive load slows down the transition back to RT mode. The series RC circuit is not recommended if the transition from CLK mode to RT mode is important. A capacitor in the range of 47 pF to 470 pF is recommended. When using the series RC circuit verify the amplitude of the signal at the RT/CLK pin goes above the high threshold.



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Figure 28. Simplified Circuit When Using Both RT Mode and CLK Mode

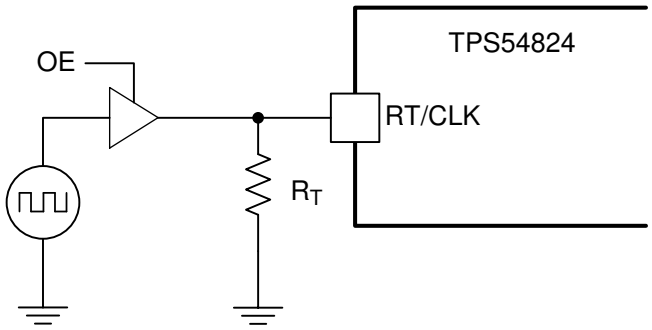


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Figure 29. Interfacing to the RT/CLK Pin with Series RC

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Feature Description (continued)



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Figure 30. Interfacing to the RT/CLK Pin with Buffer

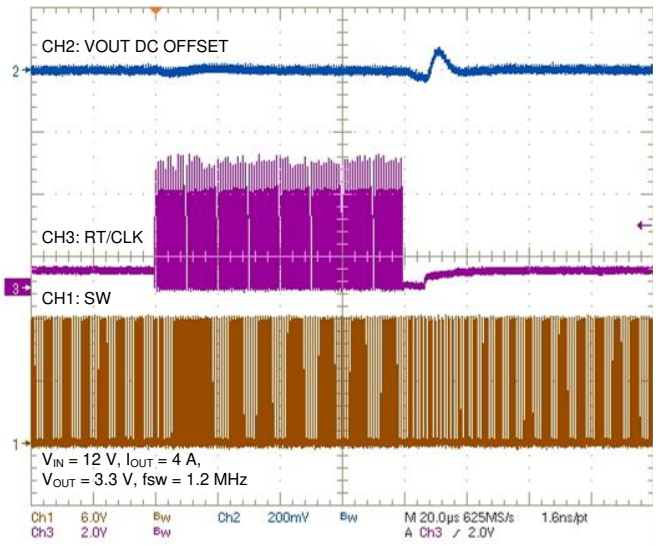


Figure 31. RT to CLK to RT Transition with Buffer

7.3.13 Bootstrap Voltage and 100% Duty Cycle Operation (BOOT)

The device provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high side MOSFET. The BOOT capacitor is refreshed when the low-side MOSFET is on. The recommended value of the BOOT capacitor is 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high side MOSFET of the device will operate at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.2 V. The device will begin to transition to 100% duty cycle operation when the high-side MOSFET off-time is less than 100 ns typical. When the voltage from BOOT to SW drops below 2.2 V, the high-side MOSFET is turned off due to BOOT UVLO and the low side MOSFET pulls SW low to recharge the BOOT capacitor. When operating at 100% duty cycle the high-side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor because the gate drive current sourced by the BOOT capacitor is small. The effective switching frequency reduced and the effective maximum duty cycle of the switching regulator is near 100%. The output voltage of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, and the printed circuit board resistance.

7.3.14 Output Overvoltage Protection (OVP)

The TPS54824 incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. The OVP feature minimizes the overshoot by comparing the FB pin voltage to the OVP threshold. The OVP threshold is the same as the 108% PGOOD threshold. If the FB pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the high-side MOSFET turns off, the low-side MOSFET turns on and the current in the inductor discharges. The output voltage can overshoot the OVP threshold as the current in the inductor discharges to 0 A. When the FB voltage drops lower than the 106% PGOOD threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

7.3.15 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET. In an extended overcurrent condition the device will enter hiccup to reduce power dissipation.

Feature Description (continued)

7.3.15.1 High-side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turnoff of the high-side MOSFET and the turnon of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off. The maximum peak switch current through the high-side MOSFET for overcurrent protection is done by limiting the current reference internally. If the peak current required to regulate the output is greater than the internal limit, the output voltage is pulled low and the error amplifier responds by driving the COMP pin high. The maximum COMP voltage is then clamped by an internal COMP clamp circuit. If the COMP voltage is clamped high for more than the hiccup wait time of 512 switching cycles, the device will shut down itself and restart after the hiccup time of 16384 cycles.

7.3.15.2 Low-side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on the current through it is monitored. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle. The low-side sourcing current limit prevents current runaway.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle. If the low-side MOSFET turns off due to sinking current limit protection, the low-side MOSFET can only turn on again after the high-side MOSFET turns on then off or if the device enters BOOT UVLO.

7.4 Device Functional Modes

The EN pin and a VIN UVLO is used to control turn on and turn off of the TPS54824. The device becomes active when $V_{(VIN)}$ exceeds the 4.1 V typical UVLO and when $V_{(EN)}$ exceeds 1.20 V typical. The EN pin has an internal current source to enable the output when the EN pin is left floating. If the EN pin is pulled low the device is put into a low quiescent current state.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54824 is a synchronous buck converter designed for 4.5 V to 17 V input and 8-A load. This procedure illustrates the design of a high-frequency switching regulator using ceramic output capacitors. Alternatively the WEBENCH® software can be used to generate a complete design. The WEBENCH® software uses an interactive design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

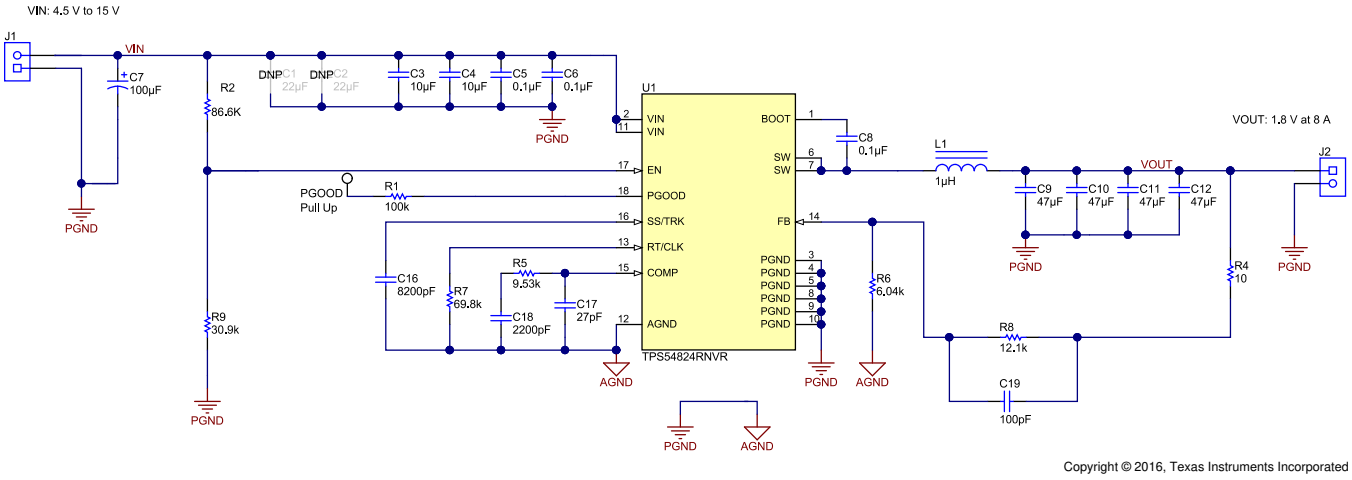


Figure 32. TPS54824 4.5-V to 15-V Input, 1.8-V Output Converter Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 1.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	4.5 to 15 V, 12 V Nominal
Output voltage (V_{OUT})	1.8 V
Transient response	+/- 4%, +/- 72 mV
Output ripple voltage	0.5%, 9 mV
Output current rating (I_{OUT})	8 A
Operating frequency (f_{SW})	700 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency

The first step is to decide on a switching frequency for the converter. It is capable of running from 200 kHz to 1.6 MHz. Typically the highest switching frequency possible is desired because it will produce the smallest solution size. A high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The main trade off made with selecting a higher switching frequency is extra switching power loss, which hurt the converter's efficiency.

The maximum switching frequency for a given application is limited by the minimum on-time of the converter and is estimated with Equation 12. Using a maximum minimum on-time of 150 ns for the TPS54824 and 15 V maximum input voltage for this application, the maximum switching frequency is 800 kHz. The selected switching frequency must also consider the 10% tolerance of the switching frequency. Considering this, a switching frequency of 700 kHz was selected. Equation 13 calculates R7 to be 69.7 kΩ. A standard 1% 69.8 kΩ value was chosen in the design.

$$f_{SW}(max) = \frac{1}{tonmin} \times \frac{V_{OUT}}{V_{IN}(max)} \tag{12}$$

$$RT(k\Omega) = 58650 \times f_{SW}(kHz)^{-1.028} \tag{13}$$

8.2.2.2 Output Inductor Selection

To calculate the value of the output inductor, use Equation 14. K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Additionally with current mode control the sensed inductor current ripple is used in the PWM modulator. Choosing small inductor ripple currents can degrade the transient response performance or introduce jitter in the high-side MOSFET on-time. The inductor ripple, K_{IND}, is normally from 0.2 to 0.4 for the majority of applications giving a peak to peak ripple current range of 1.6 A to 3.2 A. For applications requiring operation near the minimum on-time, with on-times less than 200 ns, the target Iripple must be 2.4 A or larger for best performance. For other applications the target Iripple should be 0.8 A or larger.

For this design example, K_{IND} = 0.3 is used and the inductor value is calculated to be 0.94 µH. The nearest standard value 1 µH is selected. It is important that the RMS current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from Equation 16 and Equation 17. For this design, the RMS inductor current is 8.0 A and the peak inductor current is 9.1 A. The chosen inductor is a Cyntec CMLE063T-1R0MS. It has a saturation current rating of 16.0 A (30% inductance loss) and a RMS current rating of 16.0 A (40 °C temperature rise). The DC series resistance is 5.6 mΩ typical.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated in Equation 17. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify the ratings of the inductor based on the switch current limit rather than the steady-state peak inductor current.

$$L1 = \frac{Vinmax - Vout}{Io \times Kind} \times \frac{Vout}{Vinmax \times fsw} \tag{14}$$

$$Iripple = \frac{Vinmax - Vout}{L1} \times \frac{Vout}{Vinmax \times fsw} \tag{15}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times L1 \times fsw}\right)^2} \tag{16}$$

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$$ILpeak = Iout + \frac{Iripple}{2} \quad (17)$$

8.2.2.3 Output Capacitor

There are two primary considerations for selecting the value of the output capacitor. The output voltage ripple and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these two criteria.

The desired response to a large change in the load current is the first criteria and is typically the most stringent. A regulator does not respond immediately to a large, fast increase or decrease in load current. The output capacitor supplies or absorbs charge until the regulator responds to the load step. The control loop needs to sense the change in the output voltage then adjust the peak switch current in response to the change in load. The minimum output capacitance is selected based on an estimate of the loop bandwidth. Typically the loop bandwidth is $f_{SW}/10$. Equation 18 estimates the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current and ΔV_{OUT} is the allowable change in the output voltage.

For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step of 4 A. Therefore, ΔI_{OUT} is 4 A and ΔV_{OUT} is 72 mV. Using these numbers gives a minimum capacitance of 126 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the effect of the ESR can be small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be considered for load step response.

Equation 19 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Vripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the target maximum output voltage ripple is 9 mV. Under this requirement, Equation 19 yields 46 µF.

$$C_{OUT} > \frac{\Delta I_{OUT}}{\Delta V_{OUT}} \times \frac{1}{2\pi \times \frac{f_{SW}}{10}} \quad (18)$$

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}} \quad (19)$$

Where:

- ΔI_{OUT} is the change in output current
- ΔV_{OUT} is the allowable change in the output voltage
- *f*sw is the regulators switching frequency

Equation 20 calculates the maximum combined ESR the output capacitors can have to meet the output voltage ripple specification and this shows the ESR should be less than 4 mΩ. In this case ceramic capacitors will be used and the combined ESR of the ceramic capacitors in parallel is much less than 4 mΩ. Capacitors also have limits to the amount of ripple current they can handle without producing excess heat and failing. An output capacitor that can support the inductor ripple current must be specified. Capacitor datasheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation 21 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 21 yields 660 mA and the ceramic capacitors used in this design will have a ripple current rating much higher than this.

$$Resr < \frac{Voripple}{Iripple} \quad (20)$$

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \quad (21)$$

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X5R and X7R ceramic dielectrics or similar should be selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias and AC voltage derating taken into account. The derated capacitance value of a ceramic capacitor due to DC voltage bias and AC RMS voltage is usually found on the manufacturer's website. For this application example, four 47 µF 6.3 V 1206 X5R ceramic capacitors each with 3 mΩ of ESR are used. The estimated capacitance after derating using the capacitor manufacturer's website is 29 µF each. With 4 parallel capacitors the total effective output capacitance is 116 µF and the ESR is 0.7 mΩ. The effective capacitance used is less than originally calculated above because testing the real circuit on the bench showed that less capacitance was required to achieve the desired response.

8.2.2.4 Input Capacitor

The TPS54824 requires input decoupling ceramic capacitors type X5R, X7R or similar from VIN to PGND placed as close as possible to the IC. A total of at least 4.7 µF of capacitance is required and some applications may require a bulk capacitance. At least 1 µF of bypass capacitance is recommended near both VIN pins to minimize the input voltage ripple. A 0.1 µF to 1 µF capacitor must be placed by both VIN pins 2 and 11 to provide high frequency bypass to reduce the high frequency overshoot and ringing on VIN and SW pins. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum RMS input current of the TPS54824. The RMS input current can be calculated using Equation 22.

For this example design, a ceramic capacitor with at least a 25 V voltage rating is required to support the maximum input voltage. Two 10 µF 1206 X5R 25 V and two 0.1 µF 0603 X7R 25 V capacitors in parallel has been selected to be placed on both sides of the IC near both VIN pins to PGND pins. Based on the capacitor manufacturer's website, the total ceramic input capacitance derates to 7.6 µF at the nominal input voltage of 12 V. A 100 µF bulk capacitance is also used in this circuit to bypass long leads when connected a lab bench top power supply.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 23. The maximum input ripple occurs when operating nearest to 50% duty cycle. Using the nominal design example values of Ioutmax = 8 A, Cin = 7.6 µF, and f_{SW} = 700 kHz, the input voltage ripple with the 12 V nominal input is 200 mV and the RMS input ripple current with the 4.5 V minimum input is 3.0 A.

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{\text{Vout}}{\text{Vinmin}} \times \frac{(\text{Vinmin} - \text{Vout})}{\text{Vinmin}}} \tag{22}$$

$$\Delta\text{Vin} = \frac{\text{Ioutmax} \times \left(1 - \frac{\text{Vout}}{\text{Vin}}\right) \times \frac{\text{Vout}}{\text{Vin}}}{\text{Cin} \times f_{SW}} \tag{23}$$

8.2.2.5 Output Voltage Resistors Selection

The output voltage is set with a resistor divider created by R8 (R_{FBT}) and R6 (R_{FBB}) from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. For this example design, 6.04 kΩ was selected for R6. Using Equation 24, R8 is calculated as 12.08 kΩ. The nearest standard 1% resistor is 12.1 kΩ.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \tag{24}$$

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8.2.2.6 Soft-start Capacitor Selection

The soft-start capacitor determines the amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54824 reach its current limit or cause the input voltage rail to sag due excessive current draw from the input power supply. Limiting the output voltage slew rate solves both of these problems. The soft-start capacitor value can be calculated using Equation 25. For the example circuit, the soft-start time is not critical because the output capacitor value of 4 x 47 µF does not require much current to charge to 1.8 V. The example circuit has the soft-start time set to an arbitrary value of 1 ms which requires a 8.2-nF capacitor.

$$C_{SS}(nF) = \frac{I_{SS}(\mu A) \times t_{SS}(ms)}{V_{REF}(V)} = 8.3 \times t_{SS}(ms) \tag{25}$$

8.2.2.7 Undervoltage Lockout Set Point

The Undervoltage Lockout (UVLO) is adjusted using the external voltage divider network of R2 (R_{ENT}) and R9 (R_{ENB}). The UVLO has two thresholds; one for power up when the input voltage is rising and one for power-down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 4.5 V (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.0 V (UVLO stop or disable). Equation 2 and Equation 3 can be used to calculate the values for the upper and lower resistor values. For the voltages specified, the standard resistor value used for R2 is 86.6 kΩ and for R4 is 30.9 kΩ.

8.2.2.8 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to SW pin for proper operation. A 1 Ω to 5.6 Ω resistor can be added in series with the BOOT capacitor to slow down the turn on of the high-side MOSFET. This can reduce voltage spikes on the SW node with the trade off of more power loss and lower efficiency.

8.2.2.9 PGOOD Pull-up Resistor

A 100 kΩ resistor is used to pull-up the power good signal when FB conditions are met. The pull-up voltage source must be less than the 6.5 V absolute maximum of the PGOOD pin.

8.2.2.10 Compensation

There are several methods used to compensate DC - DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation internal to the device. Because the slope compensation is ignored, the actual cross-over frequency will usually be lower than the cross-over frequency used in the calculations. This method assumes the cross-over frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater the modulator pole. This is the case when using low ESR output capacitors. Use the WEBENCH® software for more accurate loop compensation. These tools include a more comprehensive model of the control loop.

To get started, the modulator pole, fpmod, and the ESR zero, fz1 must be calculated using Equation 26 and Equation 27. For Cout, use a derated value of 116 µF and an ESR of 1 mΩ. Use equations Equation 28 and Equation 29, to estimate a starting point for the crossover frequency, fco, to design the compensation. For the example design, fpmod is 6.1 kHz and fzmod is 1370 kHz. Equation 28 is the geometric mean of the modulator pole and the ESR zero. Equation 29 is the mean of modulator pole and one half the switching frequency. Equation 28 yields 92 kHz and Equation 29 gives 46 kHz. Use the lower value of Equation 28 or Equation 29 for an initial crossover frequency. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

$$fp\,mod = \frac{Ioutmax}{2 \times \pi \times Vout \times Cout} \tag{26}$$

$$fz\,mod = \frac{1}{2 \times \pi \times Resr \times Cout} \tag{27}$$

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$$f_{co} = \sqrt{f_p \text{mod} \times f_z \text{mod}} \quad (28)$$

$$f_{co} = \sqrt{f_p \text{mod} \times \frac{f_{sw}}{2}} \quad (29)$$

To determine the compensation resistor, R5, use Equation 30. R5 is calculated to be 5.71 kΩ and the closest standard value 5.76 kΩ. Use Equation 31 to set the compensation zero to the modulator pole frequency. Equation 31 yields 4500 pF for compensating capacitor C18 and the closest standard value is 4700 pF.

$$R_{COMP} = \left(\frac{2 \times \pi \times f_{CO} \times C_{OUT}}{gm_{PS}} \right) \times \left(\frac{V_{OUT}}{V_{REF} \times gm_{EA}} \right) \quad (30)$$

Where:

- Power stage transconductance, gm_{PS} = 16 A/V
- V_{OUT} = 1.8 V
- V_{REF} = 0.6 V
- Error amplifier transconductance, gm_{EA} = 1100 µA/V

$$C_{COMP} = \frac{1}{2 \times \pi \times R_{COMP} \times f_{PMOD}} \quad (31)$$

A compensation pole is implemented using an additional capacitor C17 in parallel with the series combination of R5 and C18. This capacitor is recommended to help filter any noise that may couple to the COMP voltage signal. Use the larger value of Equation 32 and Equation 33 to calculate the C17 and to set the compensation pole. C17 is calculated to be the largest of 20 pF and 79 pF. The closest standard value is 82 pF.

$$C_{HF} = \frac{C_{OUT} \times R_{ESR}}{R_{COMP}} \quad (32)$$

$$C_{HF} = \frac{1}{\pi \times R_{COMP} \times f_{SW}} \quad (33)$$

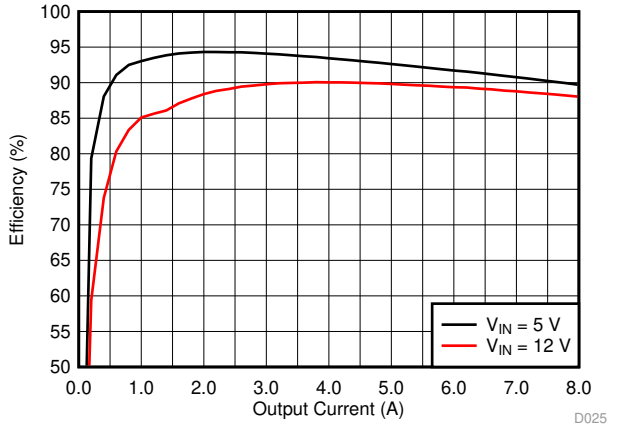
Type III compensation can be used by adding the feed forward capacitor C19 in parallel with the upper feedback resistor. Type III compensation adds phase boost above what is possible from type II compensation because it places an additional zero/pole pair. The zero/pole pair is not independent. As a result once the zero location is chosen, the pole is fixed as well. The zero is placed at 1/2 the f_{SW} by calculating the value of C19 with Equation 34. The calculated value is 37 pF and the closest standard value is 39 pF. It is possible to use larger feed forward capacitors to further improve the transient response but care should be taken to ensure there is a minimum of -10 dB gain margin at 1/2 the f_{SW} in all operating conditions. The feed forward capacitor injects noise on the output into the FB pin and this added noise can result in more jitter at the switching node. To little gain margin can cause a repeated wide and narrow pulse behavior. This example design does not use the optional feedforward capacitor.

$$C_{FF} = \frac{1}{\pi \times R_{FBT} \times f_{SW}} \quad (34)$$

The initial compensation based on these calculations is R5 = 5.76 kΩ, C18 = 4700 pF, C17 = 82 pF and C19 = 39 pF. These values yield a stable design but after testing the real circuit these values were changed to target a higher crossover frequency to improve transient response performance. The crossover frequency is increased by increasing the value of R5 and decreasing the value of the compensation capacitors. The final values used in this example are R5 = 9.53 kΩ, C18 = 2200 pF, C17 = 27 pF and C19 = 100 pF.

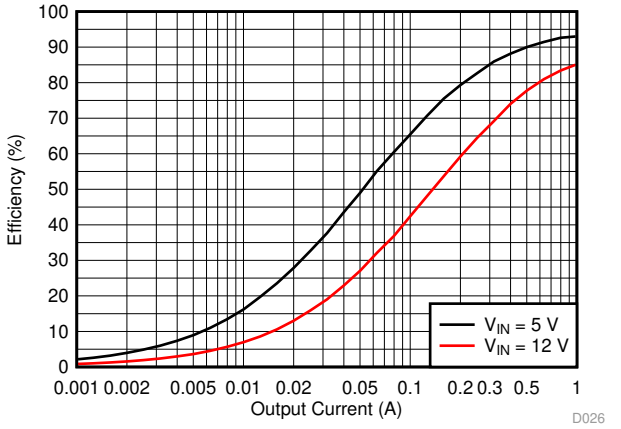
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8.2.3 Application Curves



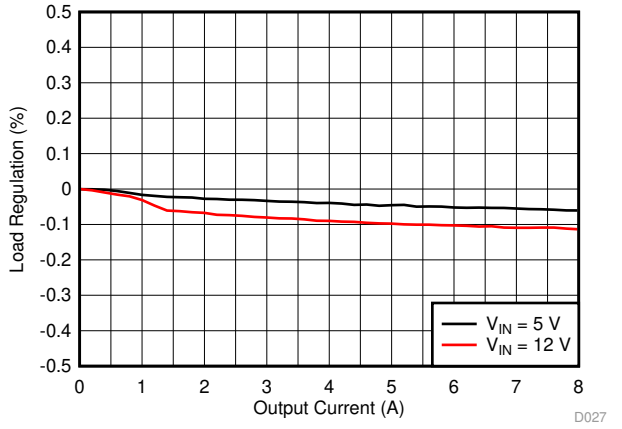
T_J = 25°C V_{OUT} = 1.8 V f_{SW} = 700 kHz

Figure 33. Efficiency



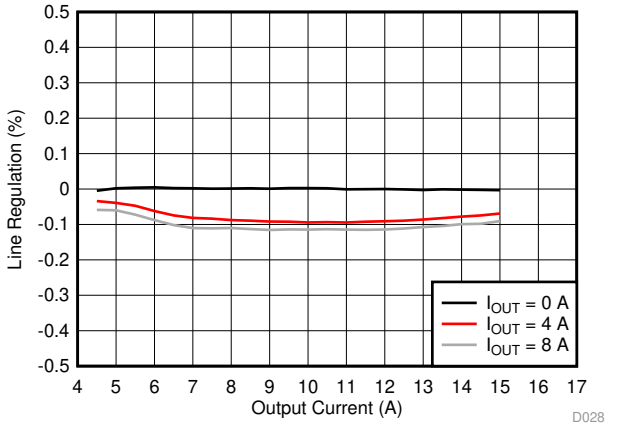
T_J = 25°C V_{OUT} = 1.8 V f_{SW} = 700 kHz

Figure 34. Efficiency (Log Scale)



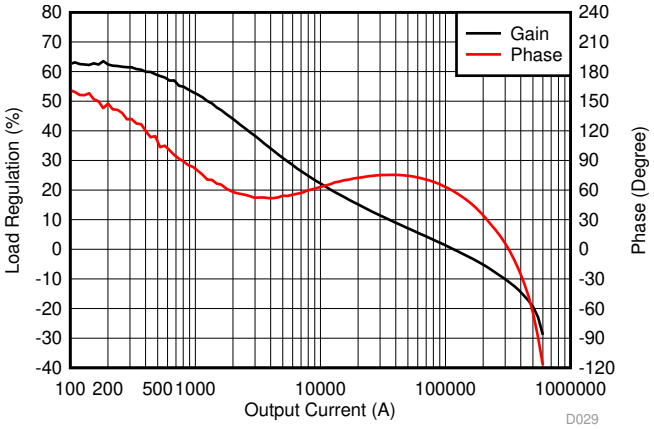
T_J = 25°C V_{OUT} = 1.8 V f_{SW} = 700 kHz

Figure 35. Load Regulation



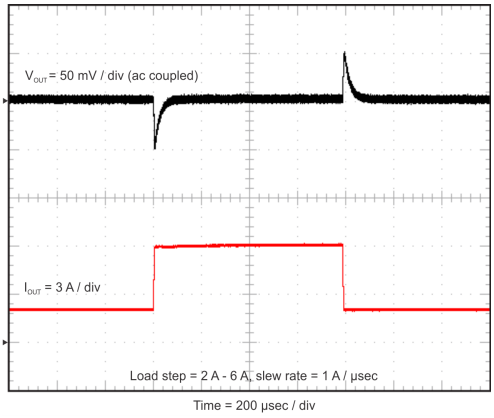
T_J = 25°C V_{OUT} = 1.8 V f_{SW} = 700 kHz

Figure 36. Line Regulation



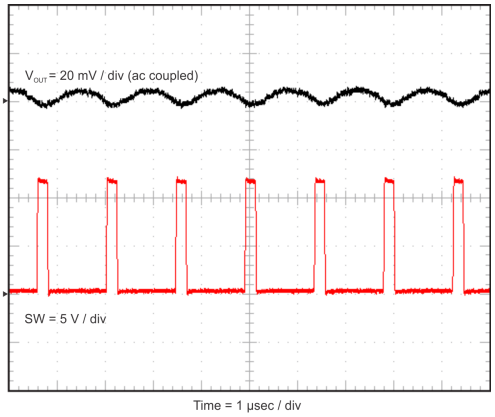
V_{IN} = 12 V V_{OUT} = 1.8 V I_{OUT} = 4 A

Figure 37. Loop Response



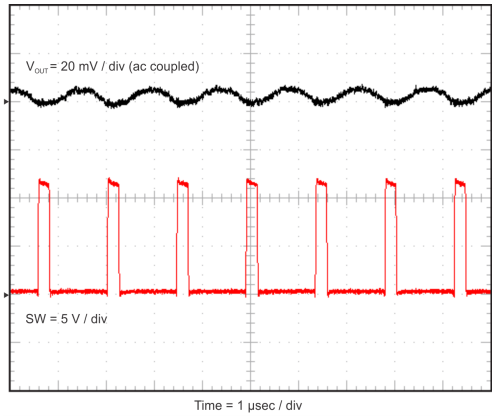
V_{IN} = 12 V V_{OUT} = 1.8 V

Figure 38. Transient Response



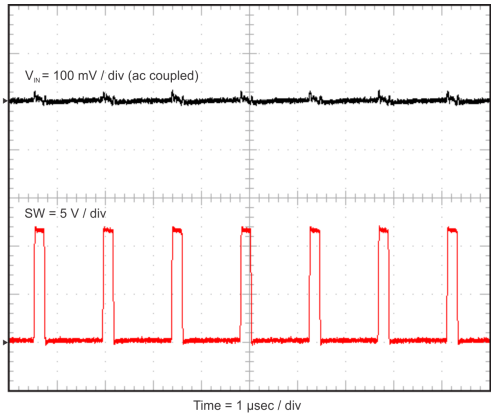
V_{IN} = 12 V V_{OUT} = 1.8 V I_{OUT} = 0 A

Figure 39. Output Ripple, No Load



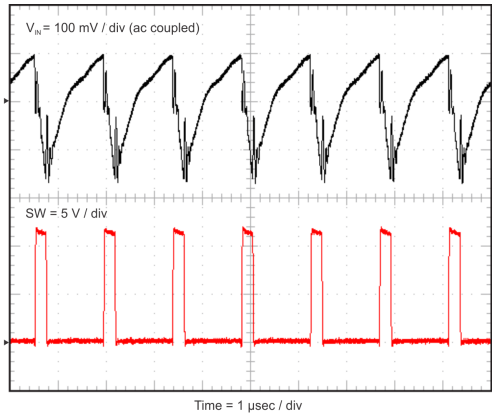
V_{IN} = 12 V V_{OUT} = 1.8 V I_{OUT} = 8 A

Figure 40. Output Ripple, Full Load



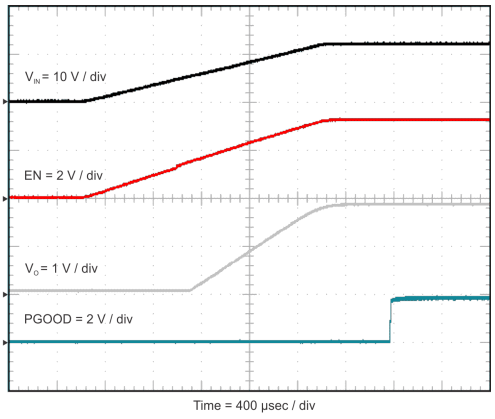
V_{IN} = 12 V V_{OUT} = 1.8 V I_{OUT} = 0 A

Figure 41. Input Voltage Ripple, No Load



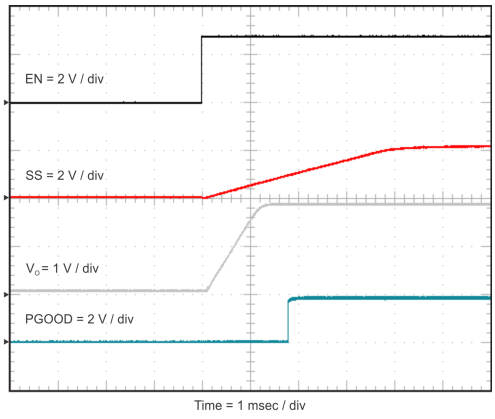
V_{IN} = 12 V V_{OUT} = 1.8 V I_{OUT} = 8 A

Figure 42. Input Voltage Ripple, Full Load



R_{LOAD} = 1 Ω

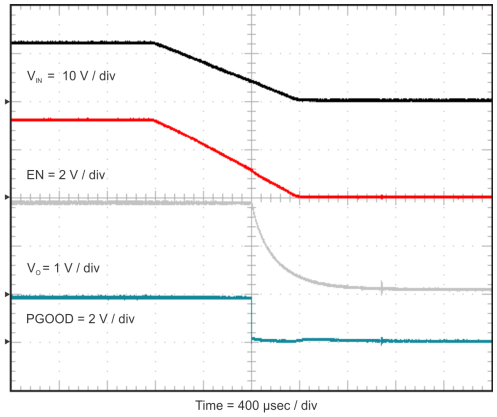
Figure 43. V_{IN} Startup



R_{LOAD} = 1 Ω

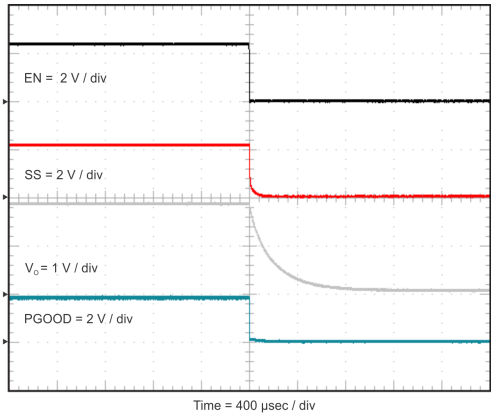
Figure 44. EN Startup

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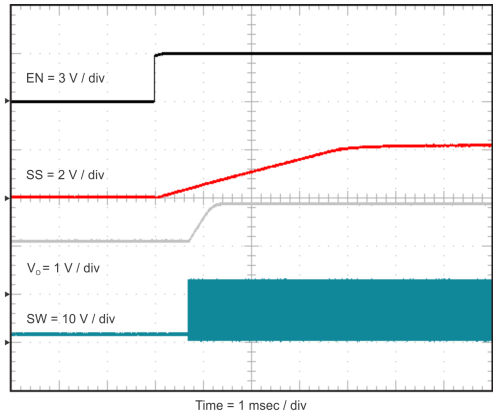
R_{LOAD} = 1 Ω V_{IN} = 12 V

Figure 45. V_{IN} Shutdown



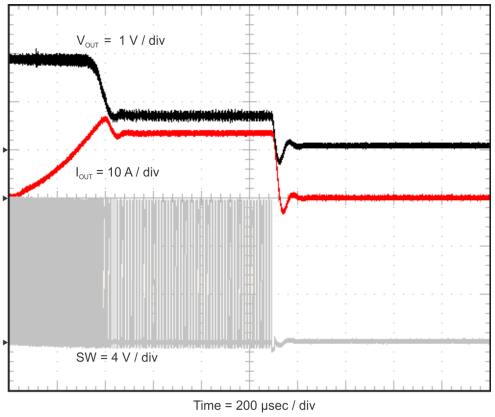
R_{LOAD} = 1 Ω

Figure 46. EN Shutdown



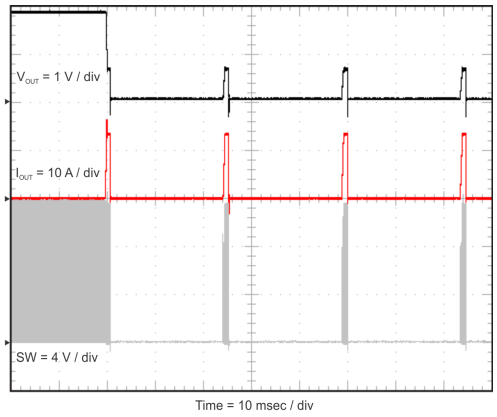
V_{IN} = 12 V

Figure 47. EN Startup with Pre-biased Output



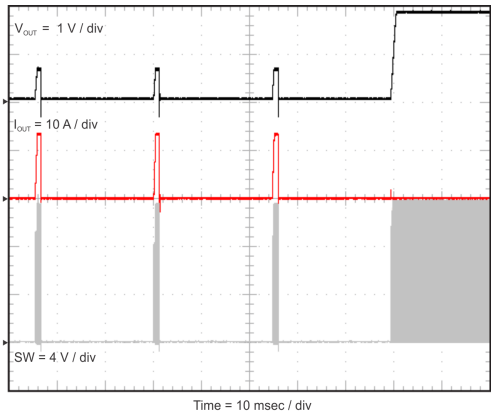
V_{IN} = 12 V I_{OUT} = short

Figure 48. Output Short Circuit Response



V_{IN} = 12 V I_{OUT} = short

Figure 49. Hiccup Mode Current Limit



V_{IN} = 12 V I_{OUT} = short removed

Figure 50. Hiccup Mode Recovery

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9 Power Supply Recommendations

The TPS54824 is designed to be powered by a well regulated dc voltage between 4.5 and 17 V. The TPS54824 is a buck converter so the input supply voltage must be greater than the desired output voltage to regulate the output voltage to the desired value. If the input supply voltage is not high enough the output voltage will begin to drop. Input supply current must be appropriate for the desired output current.

10 Layout

10.1 Layout Guidelines

- VIN and PGND traces should be as wide as possible to reduce trace impedance and improve heat dissipation.
- At least 1 µF of input capacitance is required on both VIN pins of the IC and must be placed as close as possible to the IC. The input capacitors must connect directly to the adjacent PGND pins.
- It is recommended to use a ground plane directly below the IC to connect the PGND pins on both sides of the IC together.
- The PGND trace between the output capacitor and the PGND pin should be as wide as possible to minimize its trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- A separate VOUT path should be connected to the upper feedback resistor.
- Voltage feedback loop should be placed away from the high-voltage switching trace. It is preferable to use ground copper near it as a shield.
- The trace connected to the FB node should be as small as possible to avoid noise coupling.
- Place components connected to the RT/CLK, FB, COMP and SS/TRK pins as close to the IC as possible and minimize traces connected to these pins to avoid noise coupling.
- AGND must be connected to PGND on the PCB. Connect AGND to PGND in a region away from switching currents.

10.2 Layout Example

Figure 51 through Figure 54 shows an example PCB layout and the following list provides a description of each layer.

- The top layer has all components and the main traces for VIN, SW, VOUT and PGND. Both VIN pins are bypassed with two input capacitors placed as close as possible to the IC and are connected directly to the adjacent PGND pins. Multiple vias are placed near the input and output capacitors. The AGND trace is connected to PGND with a wide trace away from the input capacitors to minimize switching noise.
- Midlayer 1 has a solid PGND plane to connect the PGND pins on both sides of the IC together with the shortest path possible and to aid with thermal performance.
- Midlayer 2 has a wide trace connecting both VIN pins of the IC. It is also used to route the BOOT pin to the BOOT-SW capacitor (CBT). It also has a parallel trace for VOUT to minimize trace resistance. The rest of this layer is covered with PGND.
- The bottom layer has the trace connecting the FB resistor divider to VOUT at the point of regulation. PGND is filled into the rest of this layer to aid with thermal performance.

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Layout Example (continued)

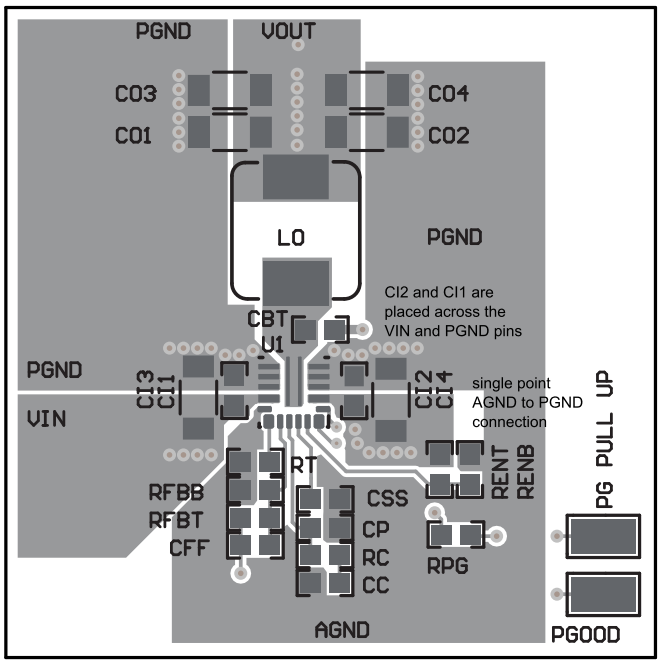


Figure 51. TPS54824 Layout Top

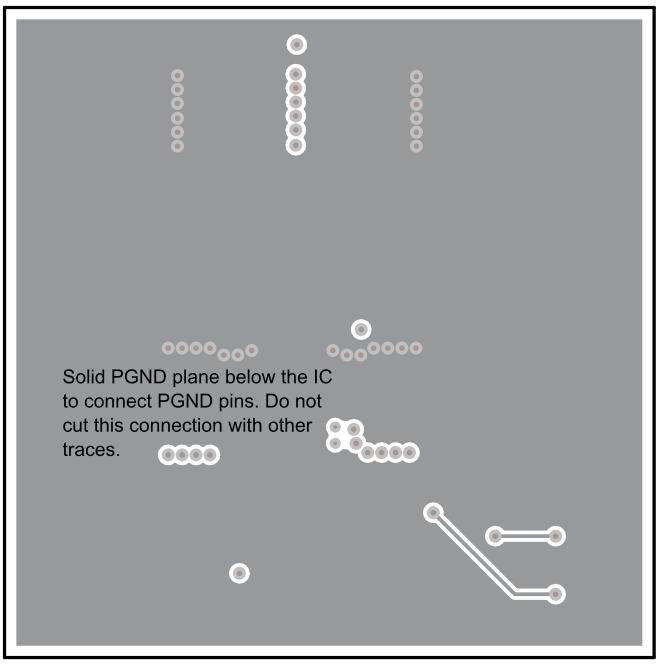


Figure 52. TPS54824 Layout Midlayer 1

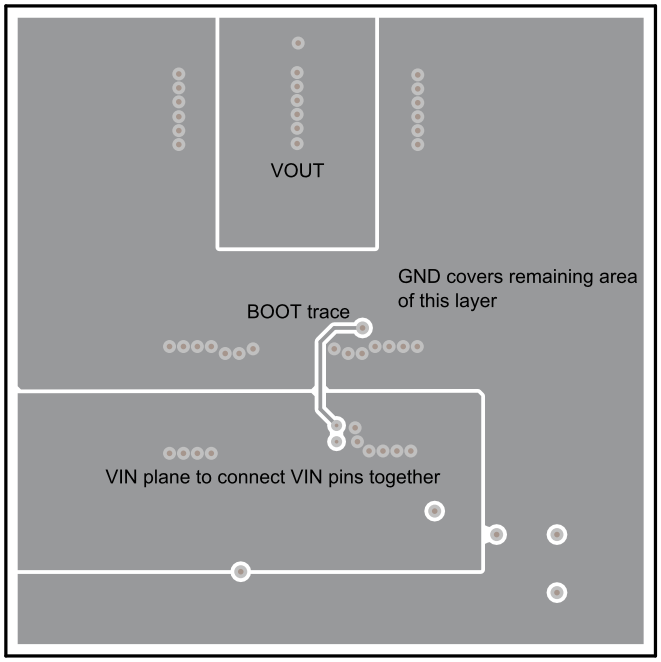


Figure 53. TPS54824 Layout Midlayer 2

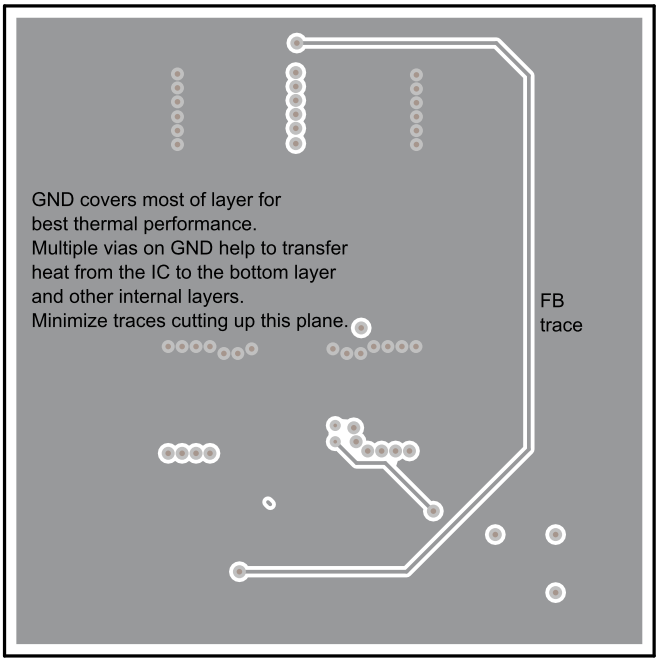


Figure 54. TPS54824 Layout Bottom

10.3 Alternate Layout Example

Figure 55 through Figure 58 shows an alternate example PCB layout with unsymmetrical placement of the input capacitors and output capacitors. Both VIN pins are still bypassed to their adjacent PGND pins with an input capacitor placed as close as possible to the IC. When using this alternate layout, CI2 should be increased to 1 µF.

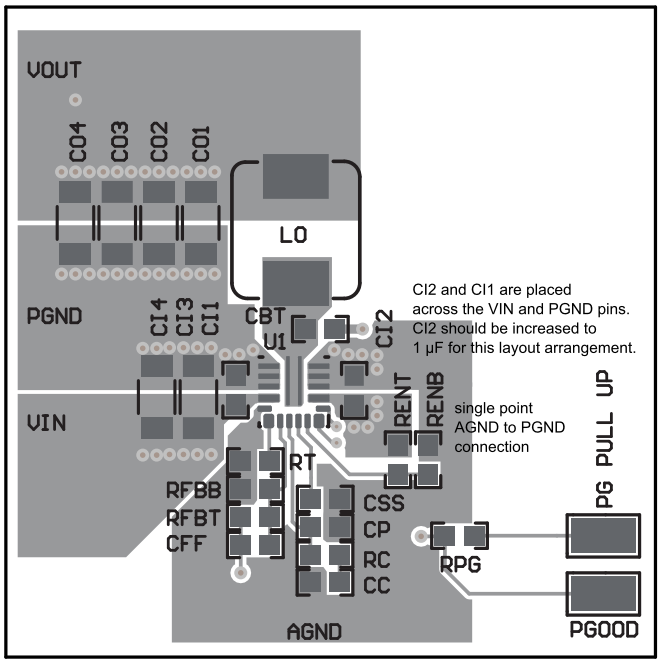


Figure 55. TPS54824 Alternate Layout Top



Figure 56. TPS54824 Alternate Layout Midlayer 1

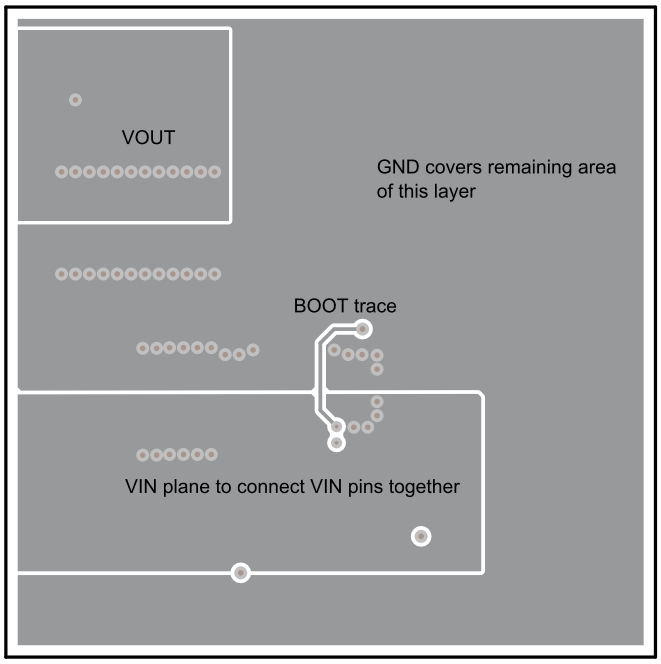


Figure 57. TPS54824 Alternate Layout Midlayer 2

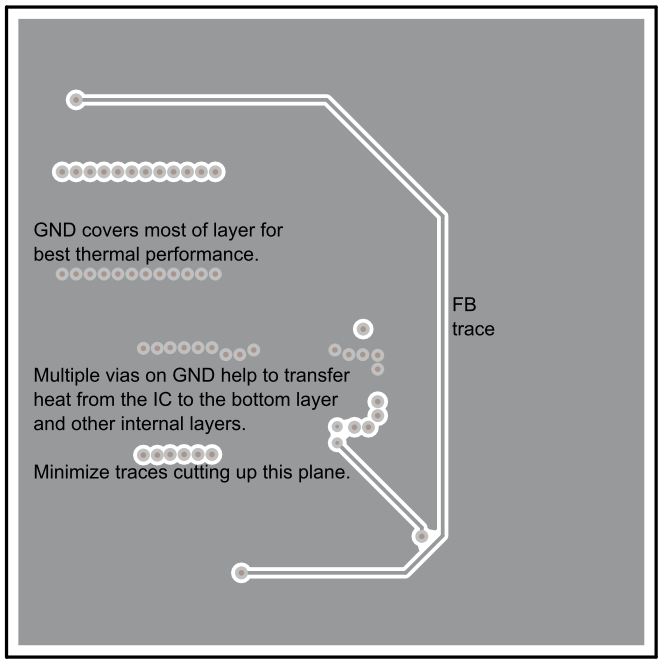


Figure 58. TPS54824 Alternate Layout Bottom

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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

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WEBENCH is a registered trademark of Texas Instruments.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54824RNVR	ACTIVE	VQFN-HR	RNV	18	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54824	Samples
TPS54824RNVT	ACTIVE	VQFN-HR	RNV	18	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54824	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

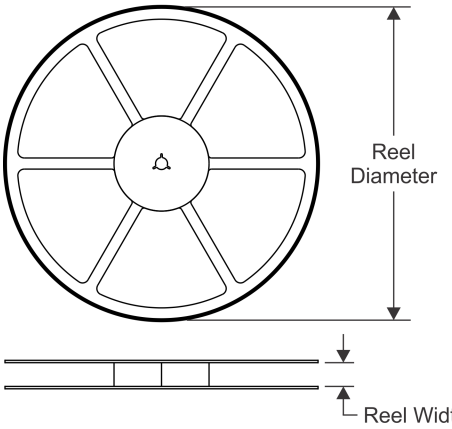
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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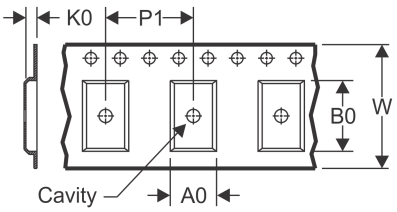
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

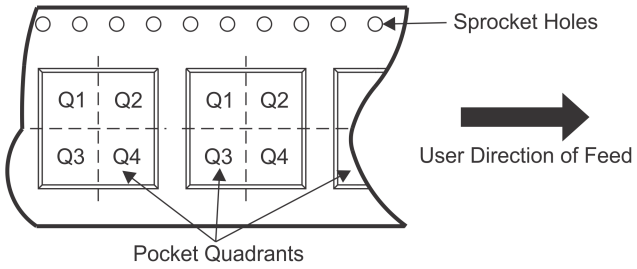


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

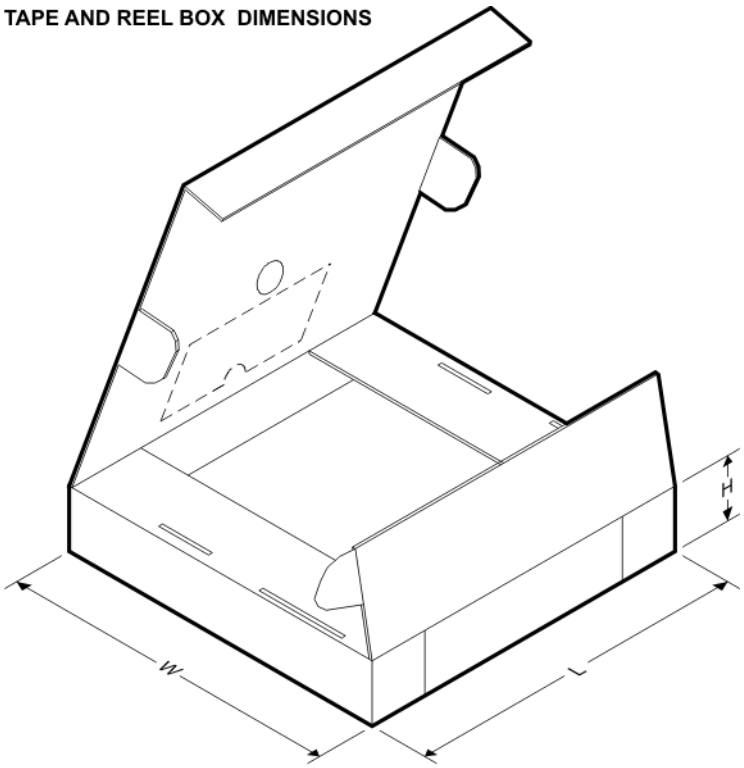
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54824RNVR	VQFN-HR	RNV	18	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS54824RNVT	VQFN-HR	RNV	18	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



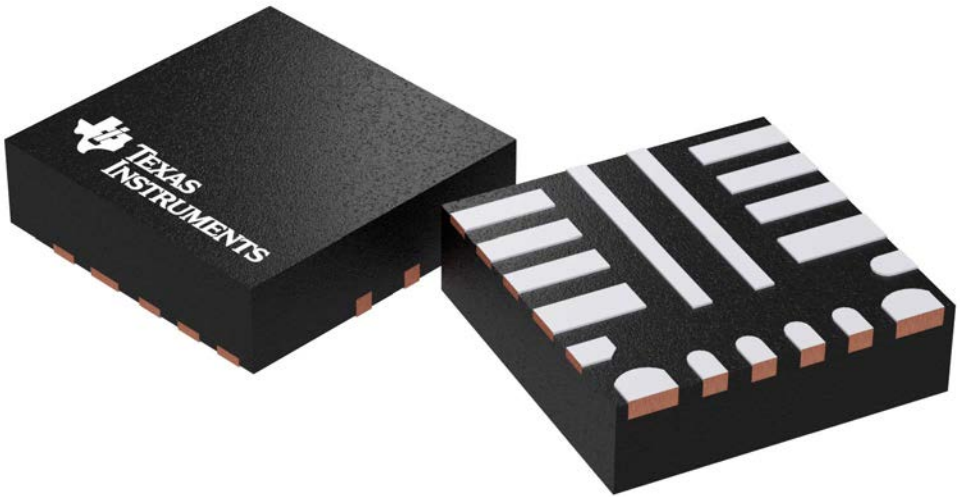
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54824RNVR	VQFN-HR	RNV	18	3000	367.0	367.0	35.0
TPS54824RNVT	VQFN-HR	RNV	18	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RNV 18 VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

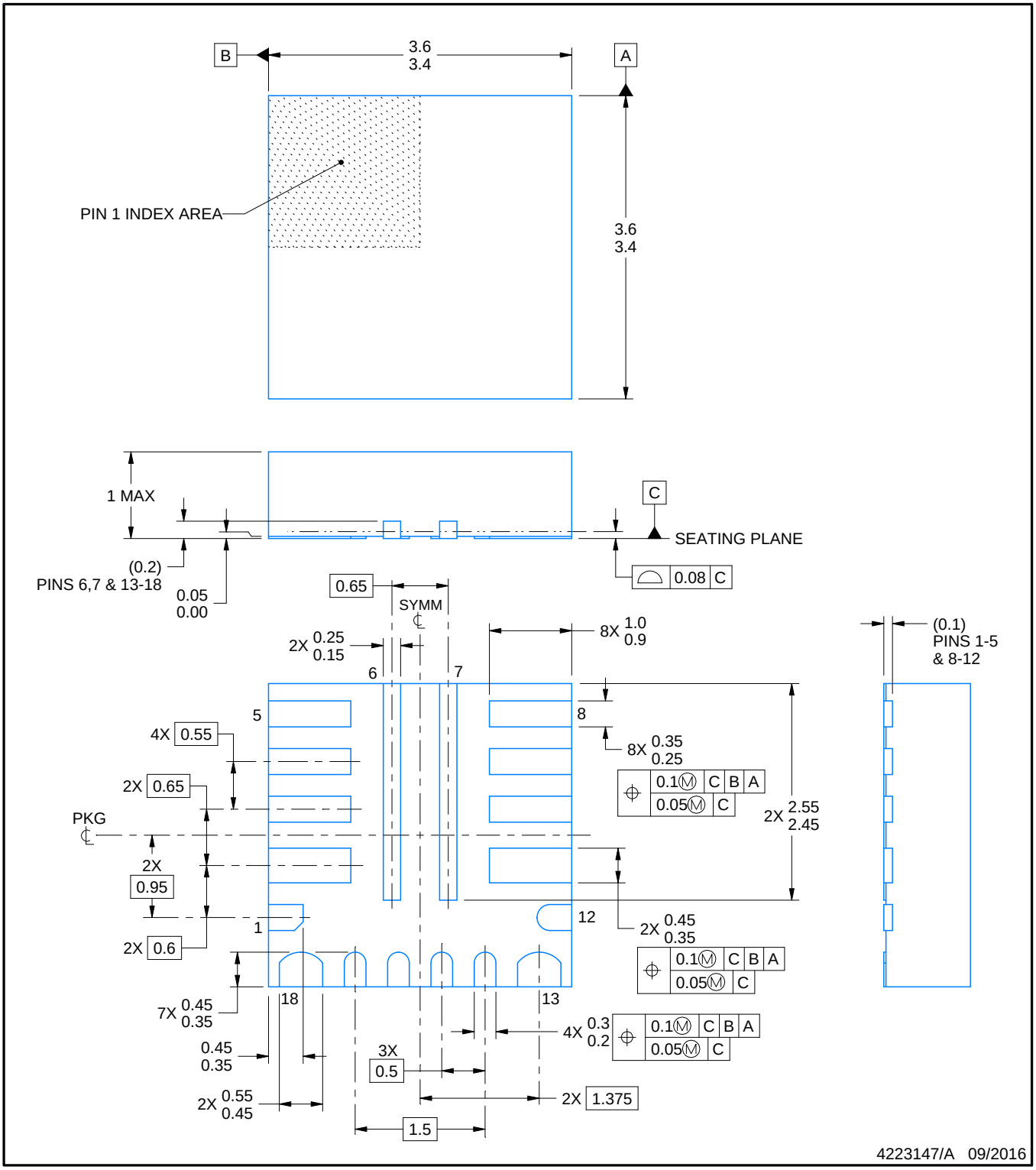
4223696-3/A

PACKAGE OUTLINE

RNV0018B

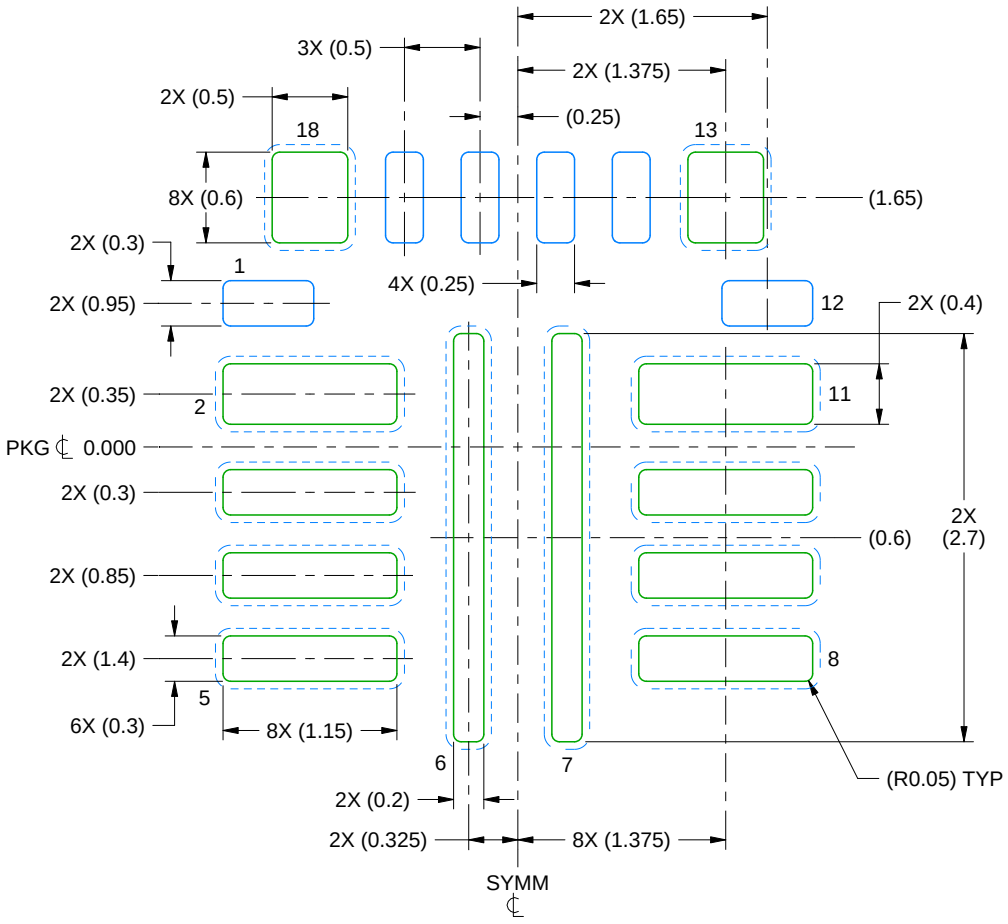
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

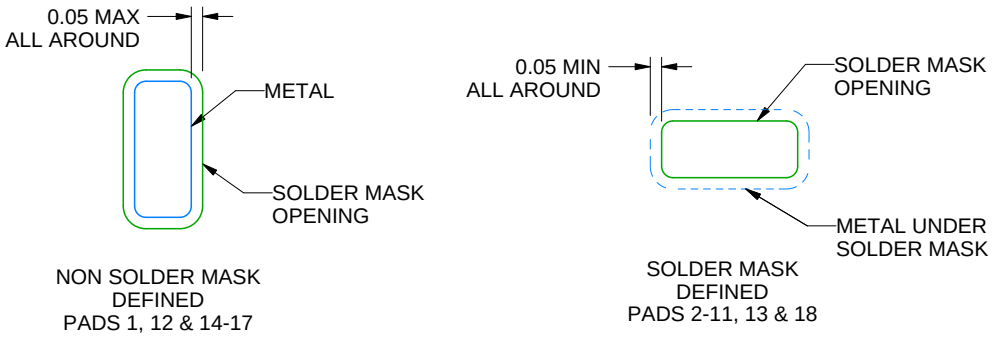


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

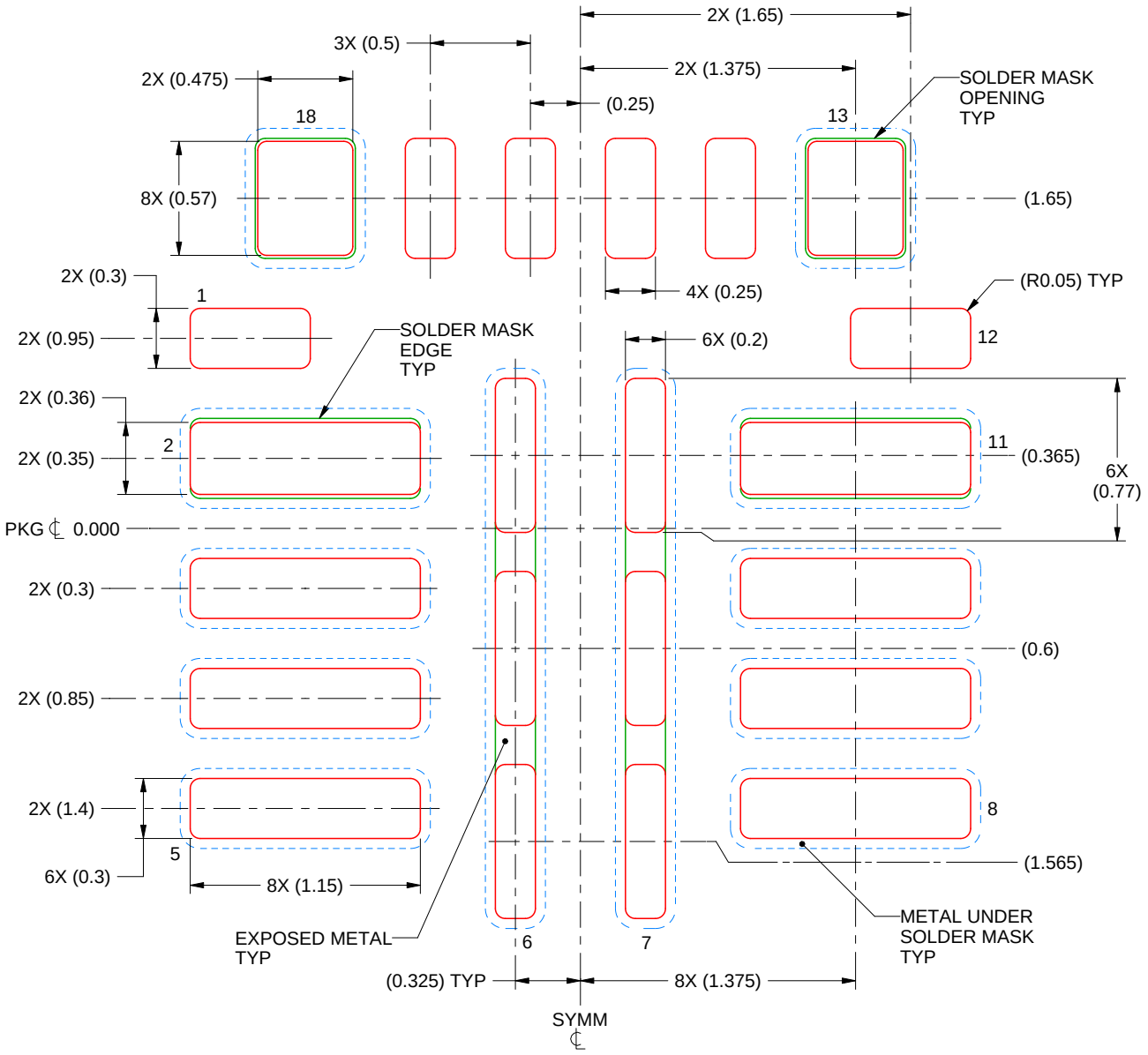
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. If any vias are implemented, it is recommended that vias under paste to be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RNV0018B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 7: 85.6% - PADS 2, 11, 13 & 18: 90%
SCALE:30X

4223147/A 09/2016

NOTES: (continued)

6. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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