3-V TO 6-V INPUT, 6-A, SMALL SYNCHRONOUS-BUCK SWITCHER WITH INTEGRATED FETs (SWIFT™)

FEATURES

- **30-mΩ MOSFET Switches for High Efficiency at 6-A Continuous Output**
- **Adjustable Output Voltage Down to 0.9 V With 1% Accuracy**
- **Externally Compensated for Design Flexibility**
- **Wide PWM Frequency: Fixed 350 kHz, 550 kHz, or Adjustable 280 kHz to 1.6 MHz**
- **Synchronizable to 1.6MHz**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Small 3.5mm x 7mm Package and Similar Layout to TPS54610 Reduces Board Area and Total Cost**
- **SWIFT Documentation Application Notes, and SwitcherPro™ Software: www.ti.com/swift**

APPLICATIONS

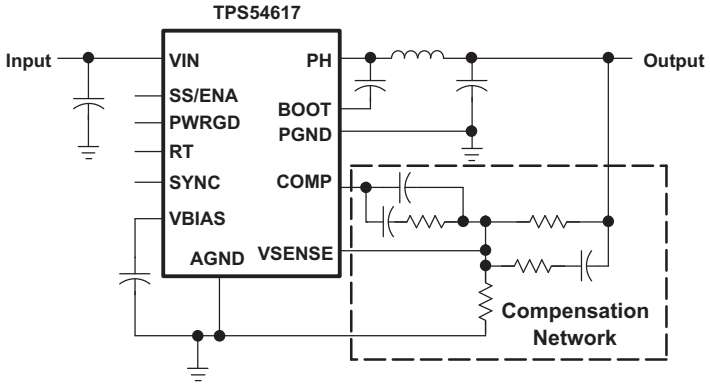
- **Low-Voltage, High-Density Systems With Power Distributed at 3.3 V or 5 V**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs, and Microprocessors**
- **Broadband, Networking and Optical Communications Infrastructure**

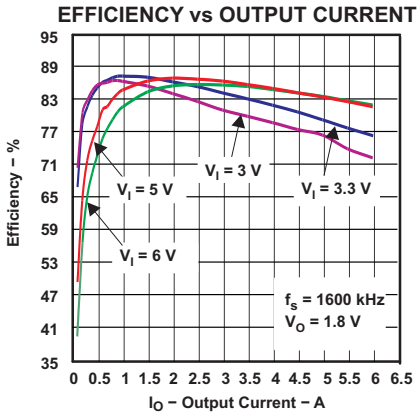
DESCRIPTION

As a member of the SWIFT™ family of dc/dc regulators, the TPS54617 low-input voltage high-output current synchronous buck PWM converter offers the same features as the TPS54610 in a small package and higher switching frequency. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance under transient conditions and flexibility in choosing the output filter L and C components; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

The TPS54617 is available in a thermally enhanced 34 pin QFN (RUV) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SwitcherPro™ design software tool to aid in achieving high-performance power supply designs to meet aggressive equipment development cycles.

SIMPLIFIED SCHEMATIC





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_J	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
–40°C to 125°C	Adjustable down to 0.9 V	QFN (RUV)(2)	TPS54617RUV

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The RUV package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54617RUVR). See the application section of this data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE / UNIT
V_I	Input voltage range	SS/ENA, SYNC	–0.3 V to 7 V
		RT	–0.3 V to 6 V
		VSENSE	–0.3 V to 4 V
		VIN	–0.3 V to 7 V
		BOOT	–0.3 V to 17 V
V_O	Output voltage range	VBIAS, PWRGD, COMP	–0.6 V to 7 V
		PH	–0.6 V to 10 V
		PH (transient < 10 nsec)	-2.0 V
I_O	Source current	PH	Internally Limited
		COMP, VBIAS	6 mA
I_S	Sink current	PH	12 A
		COMP	6 mA
		SS/ENA, PWRGD	10 mA
	Voltage differential	AGND to PGND	±0.3 V
T_J	Operating virtual junction temperature range		–40°C to 125°C
T_{stg}	Storage temperature		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	3		6	V
T_J	Operating junction temperature	–40		125	°C

PACKAGE DISSIPATION RATINGS (1)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	THERMAL IMPEDANCE JUNCTION-TO-CASE
34-Pin RUV with solder	14.5°C/W	0.5 °C/W(2)

(1) Test board conditions:
a. 3 inch × 3 inch, 4 layers, Thickness: 0.062 inch
b. 2.0 oz copper traces located on the top of the PCB
c. 2.0 oz copper ground plane on the bottom of the PCB
d. 2.0 oz copper ground planes on the 2 internal layers
e. 12 thermal vias
(2) Maximum power dissipation may be limited by overcurrent protection.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN						
	VIN input voltage range		3		6	V
	Quiescent current	f_s = 350 kHz, SYNC ≤ 0.8 V, RT open, PH pin open		9.2	15.8	mA
		f_s = 550 kHz, SYNC ≥ 2.5 V, RT open, PH pin open		13.9	23.5	
		Shutdown, SS/ENA = 0 V		1	1.4	
UNDER VOLTAGE LOCK OUT						
	Start threshold voltage, UVLO			2.95	3.0	V
	Stop threshold voltage, UVLO		2.70	2.80		
	Hysteresis voltage, UVLO			0.16		V
	Rising and falling edge deglitch, UVLO(1)			2.5		µs
BIAS VOLTAGE						
V_O	Output voltage, VBIAS	$I_{(VBIAS)}$ = 0	2.70	2.80	2.90	V
	Output current, VBIAS(2)				100	µA
CUMULATIVE REFERENCE						
V_{ref}	Accuracy		0.882	0.891	0.900	V
REGULATION						
	Line regulation(1)	I_L = 3 A, f_s = 350 kHz, T_J = 85°C			0.04	%/V
		I_L = 3 A, f_s = 550 kHz, T_J = 85°C			0.04	
	Load regulation(1)	I_L = 0 A to 6 A, f_s = 350 kHz, T_J = 85°C			0.03	%/A
		I_L = 0 A to 6 A, f_s = 550 kHz, T_J = 85°C			0.03	
OSCILLATOR						
	Internally set free-running frequency range	SYNC ≤ 0.8 V, RT open	280	350	420	kHz
		SYNC ≥ 2.5 V, RT open	440	550	660	
	Externally set free-running frequency range	RT = 100 kΩ (1% resistor to AGND)	460	500	540	kHz
		RT = 27 kΩ (1% resistor to AGND)	1480	1600	1720	
	High-level threshold voltage, SYNC		2.5			V
	Low-level threshold voltage, SYNC				0.8	V
	Pulse duration, SYNC(1)		50			
	Frequency range, SYNC		330		1600	kHz
	Ramp valley(1)			0.75		V
	Ramp amplitude (peak-to-peak)(1)			1		V
	Minimum controllable on time				160	ns
	Maximum duty cycle		90%			

(1) Specified by design
(2) Static resistive loads only

ELECTRICAL CHARACTERISTICS (continued)

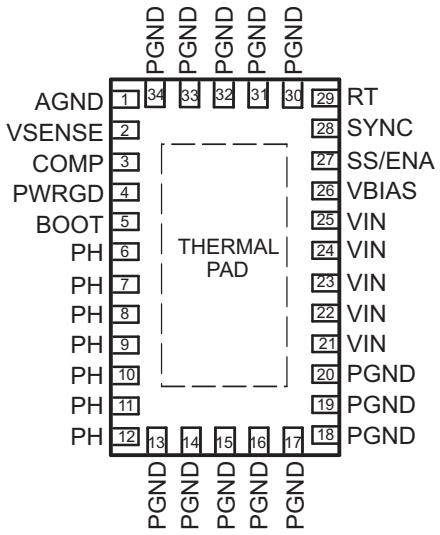
T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
	Error amplifier open loop voltage gain	1 kΩ COMP to AGND(3)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(3)	3	5		MHz
	Error amplifier common-mode input voltage range	Powered by internal LDO(3)	0		VBIAS	V
I_{IB}	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
V_O	Output voltage slew rate (symmetric), COMP(3)		1	1.4		V/µs
PWM COMPARATOR						
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding dead time)	10 mV overdrive(3)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, SS/ENA		0.82	1.20	1.40	V
	Enable hysteresis voltage, SS/ENA(1)			0.03		V
	Falling edge deglitch, SS/ENA(1)			2.5		µs
	Internal slow-start time		2.6	3.35	4.1	ms
	Charge current, SS/ENA	SS/ENA = 0 V	3	5	8	µA
	Discharge current, SS/ENA	SS/ENA = 1.3 V, V_I = 1.5 V	1.5	2.3	4	mA
POWER GOOD						
	Power good threshold voltage	VSENSE falling		90		%V_{ref}
	Power good hysteresis voltage(1)			3		%V_{ref}
	Power good falling edge deglitch(1)			35		µs
	Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
	Leakage current, PWRGD	V_I = 5.5 V			1	µA
CURRENT LIMIT						
	Current limit trip point	V_I = 3 V(1), Output shorted	7.2	10		A
		V_I = 6 V(1), Output shorted	10	12		
	Current limit leading edge blanking time(3)			100		ns
	Current limit total response time(3)			200		ns
THERMAL SHUTDOWN						
	Thermal shutdown trip point(1)		135	150	165	°C
	Thermal shutdown hysteresis(1)			10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$	Power MOSFET switches	V_I = 3 V		26	47	mΩ
		V_I = 3.6 V		36	65	

(3) Specified by design

PIN ASSIGNMENTS

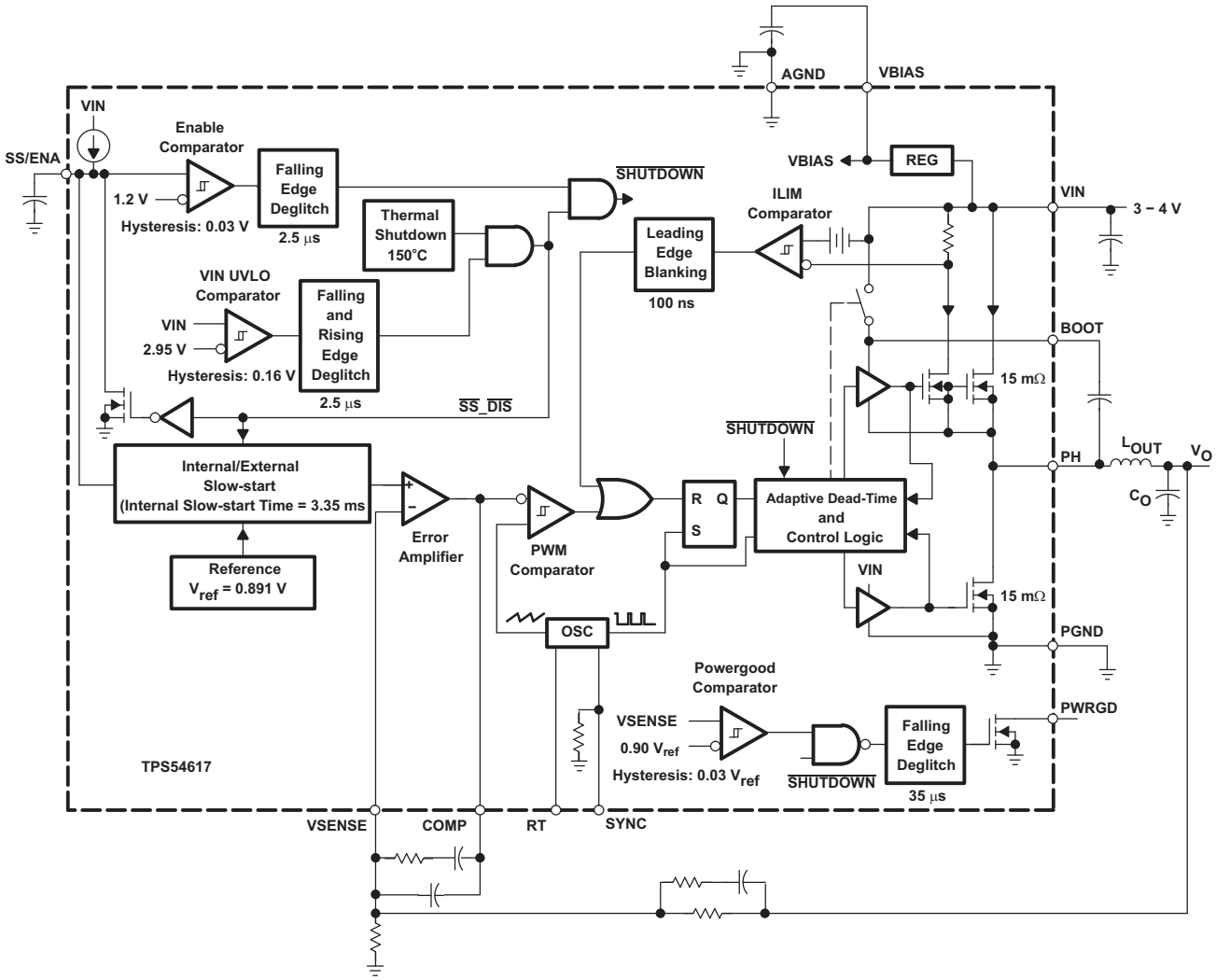
RUV PACKAGE
(Top VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor and SYNC pin. Connect PowerPAD to AGND.
BOOT	5	Bootstrap input. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE.
PGND	13–20 30–34	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6–12	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PWRGD	4	Power good open drain output. High when VSENSE ≥ 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or internal shutdown signal active.
RT	29	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s.
SS/ENA	27	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	28	Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
VBIAS	26	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low ESR 0.1-µF to 1-µF ceramic capacitor.
VIN	21–25	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high-quality, low-ESR 10-µF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

INTERNAL BLOCK DIAGRAM



RELATED DC/DC PRODUCTS

- TPS40000 – dc/dc controller
- TPS56300 – dc/dc controller
- TPS54610 - SWIFT 6A converter
- TPS54917 and TPS54910 - SWIFT 9A converters

TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

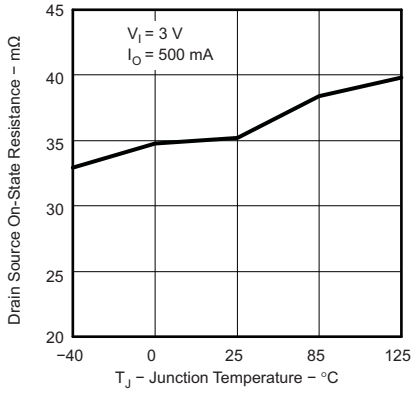


Figure 1.

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

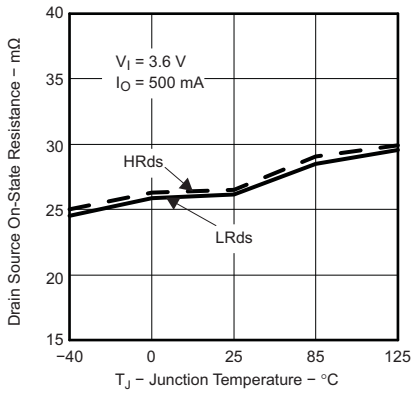


Figure 2.

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

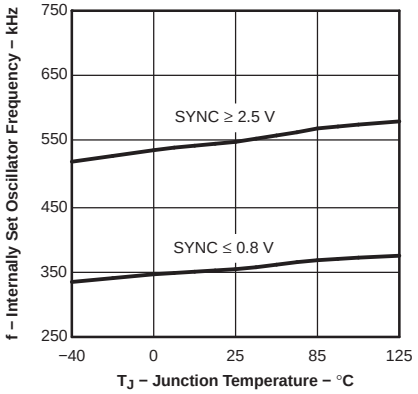


Figure 3.

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

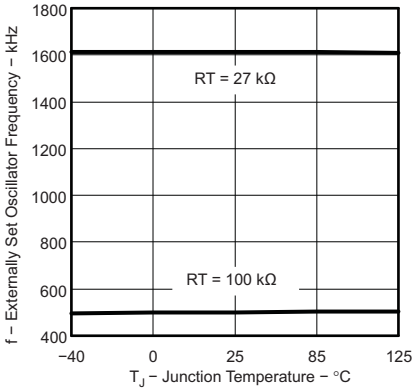


Figure 4.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

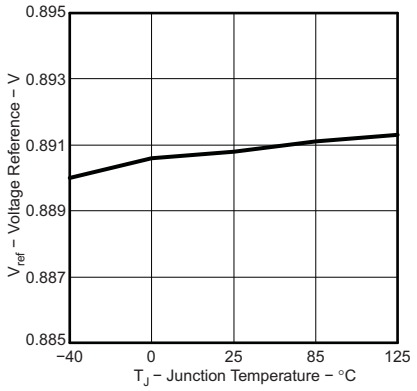


Figure 5.

DEVICE POWER LOSSES vs LOAD CURRENT

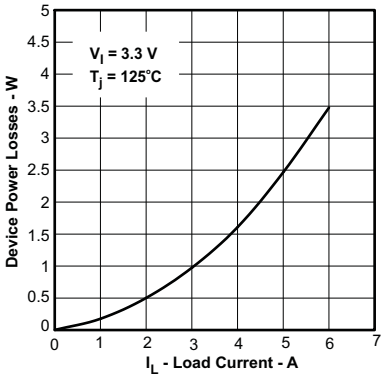


Figure 6.

OUTPUT VOLTAGE REGULATION INPUT VOLTAGE

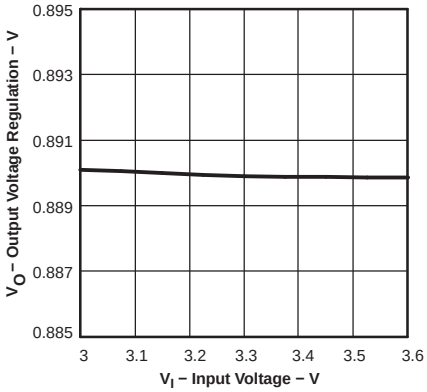


Figure 7.

ERROR AMPLIFIER vs OPEN LOOP RESPONSE

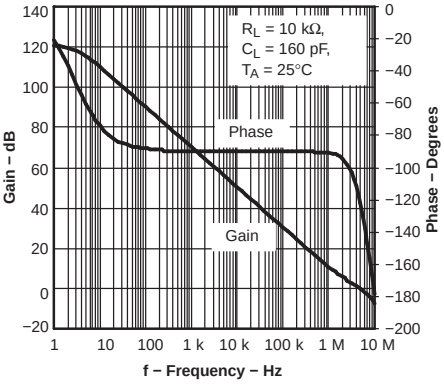


Figure 8.

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

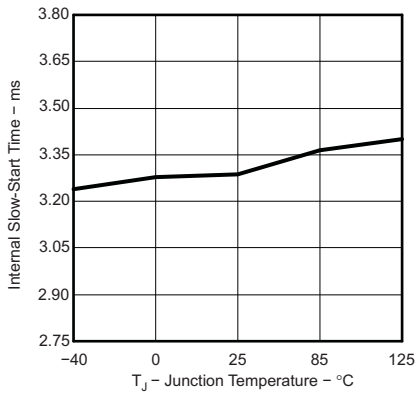
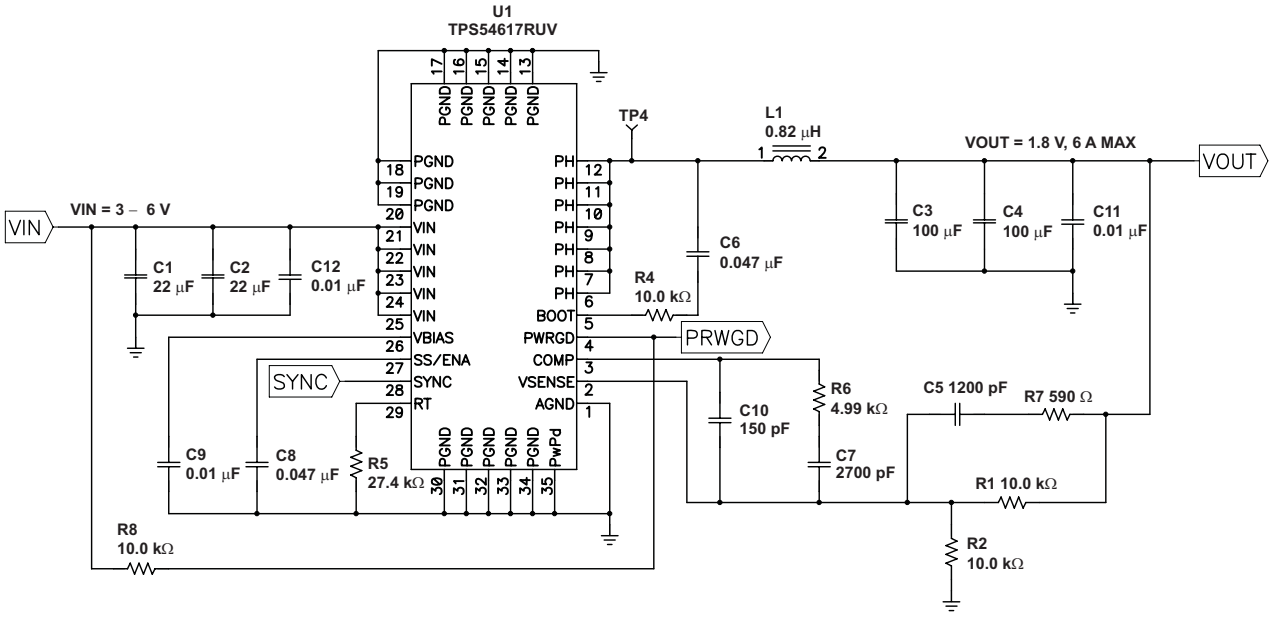


Figure 9.

APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54617 application. The TPS54617 (U1) can provide up to 6A of output current at a nominal output voltage of 1.8 V. For proper thermal performance, the exposed thermal PowerPAD underneath the integrated circuit, TPS54617, package must be soldered to the printed-circuit board.



Analog and power grounds are ties at the pad under the package of the IC

Figure 10. Application Circuit

COMPONENT SELECTION

The values for the components used in this design example were selected for best load transient response and small PCB area. Additional design information is available at www.ti.com.

INPUT FILTER

The input voltage is a nominal 3.3 or 5 VDC. The input filter capacitors (C1 and C2) are 10-µF ceramic capacitors (MuRata). C12 is a 0.01-µF ceramic capacitor that provides high-frequency decoupling of the TPS54617 from the input supply. C1, C2 and C12 must be located as close as possible to the device. Input ripple current is shared among C1, C2 and C12.

FEEDBACK CIRCUIT

The values for these components are selected to provide fast transient response times.

The resistor divider network of R1 and R2 sets the output voltage for the circuit at 1.8 V. R1 along with R6, R7, C5, C7, and C10 forms the loop compensation network for the circuit. For this design, a Type-3 topology is used. The feedback loop is compensated so that the closed loop crossover frequency is approximately 45 kHz at 5 V input.

OPERATING FREQUENCY

In the application circuit, RT is grounded through a 27.4-kΩ resistor to select the operating frequency of 1.6 MHz. To set a different frequency, place a 27-kΩ to 180-kΩ resistor between RT (pin 29) and analog ground or leave RT floating to select the default of 350 kHz. The switching frequency in MHz can be approximated using the following equation:

$$F_{SW} = \frac{51000}{(R_T + 4400)} \quad (1)$$

OUTPUT FILTER

The output filter is composed of a 0.82-µH inductor and 2 × 100-µF capacitors. The inductor is a Vishay IHLM-2525CZ-01 type. The capacitors used are 100-µF, 6.3-V ceramic types with X5R dielectric.

PCB LAYOUT

Figure 11 shows a generalized PCB layout guide for the TPS54617. The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54617 ground pins. The minimum recommended bypass capacitance is 10 µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the PGND pins.

The TPS54617 has two internal grounds (analog and power). The analog ground ties to all of the noise-sensitive signals, while the power ground ties to the noisier power signals. Noise injected between the two grounds can degrade the performance of the TPS54617, particularly at higher output currents. Ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground traces are recommended. There should be an area of ground on the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The AGND and PGND pins should be tied to the PCB ground by connecting them to the ground area under the device as shown. Use a separate wide traces for the analog ground signal path. This analog ground should be used for the voltage set point divider, timing resistor RT, slow start capacitor, and bias capacitor grounds. Connect this trace the topside groud area near AGND (Pin 1).

The PH pins should be tied together and routed to the output inductor. Since the PH connection is the switching node, the inductor should be located very close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths.

Connect the output filter capacitor(s) as shown between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, Lout, Cout and PGND as small as practical.

Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pinout, the components will have to be routed somewhat close, but maintain as much separation as possible while still keeping the layout compact.

Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If a slow-start capacitor or RT resistor is used, or if the SYNC pin is used to select 350 kHz operating frequency, connect them to this trace as well.

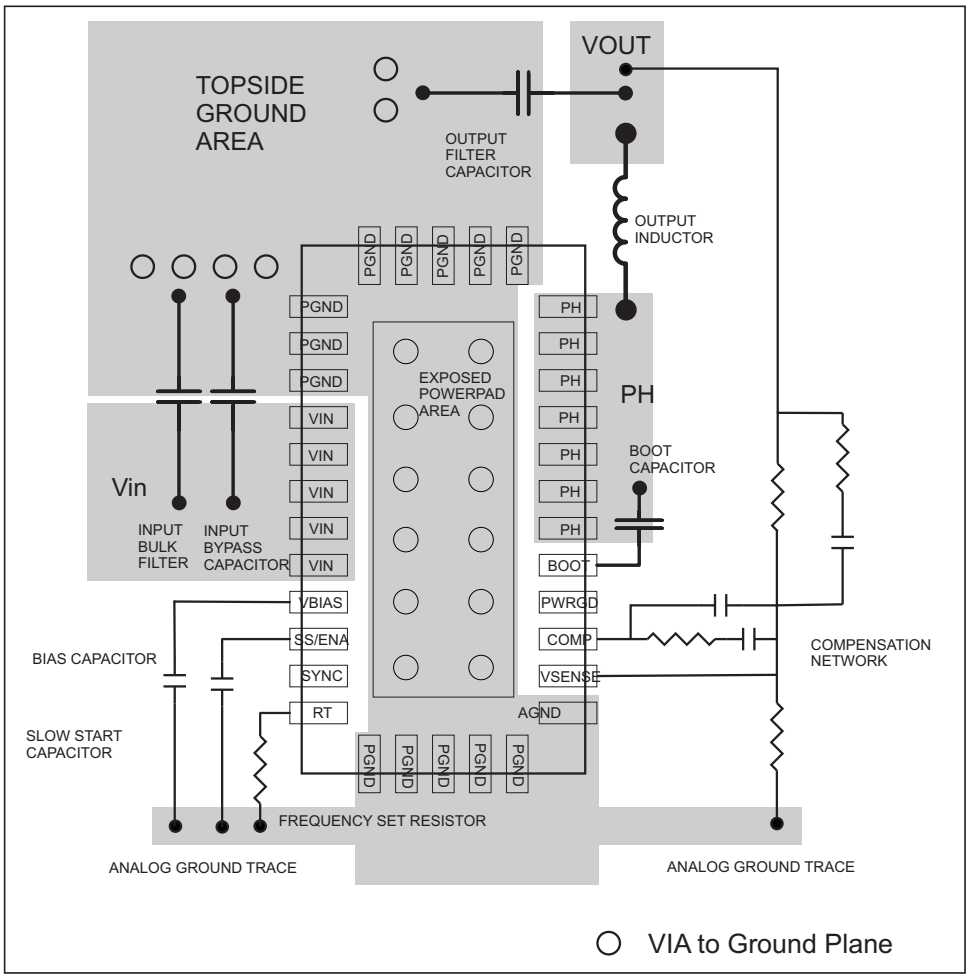


Figure 11. TPS54617 PCB Layout

Estimated Circuit Area

The estimated printed circuit board area for the components used in the design of Figure 11 is 0.55 in^2. This area does not include test points or connectors.

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

The RUV package has been chosen to enable a thermal management scheme, allowing a ground plane to extend beyond both ends of the package.

For operation at full rated load current, the analog ground plane must provide an adequate heat dissipating area. A 3-inch by 3-inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD must be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available must be used when 6 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer must be made using 0.013-inch diameter vias to avoid solder wicking through the vias.

12 vias must be in the PowerPAD area located under the device package. Additional vias beyond the twelve recommended may be added in the ground area outside the package footprint to enhance thermal performance. The size of the vias outside of the package, not in the exposed thermal pad area, can be increased to 0.018.

PERFORMANCE GRAPHS

EFFICIENCY VS OUTPUT CURRENT

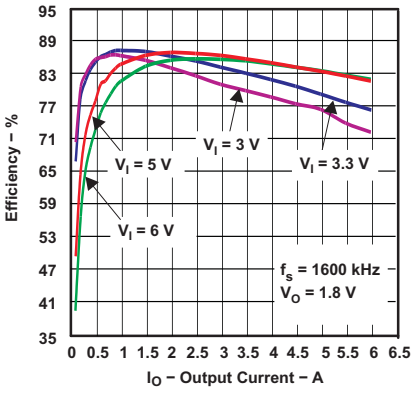


Figure 12.

LOAD REGULATION VS OUTPUT CURRENT

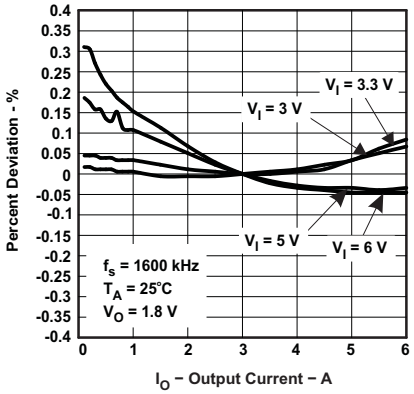


Figure 13.

LINE REGULATION VS INPUT VOLTAGE

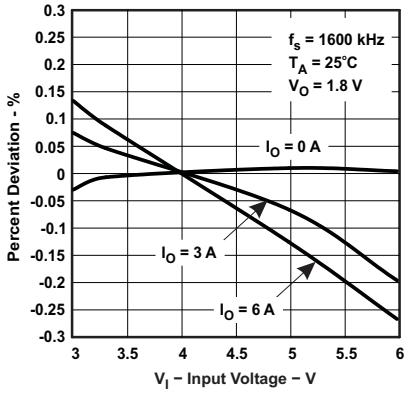


Figure 14.

AMBIENT TEMPERATURE VS LOAD CURRENT(1)

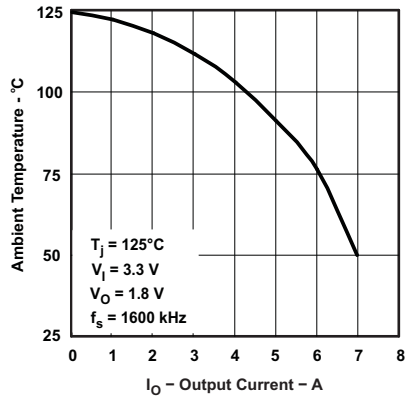


Figure 15.

OUTPUT RIPPLE VOLTAGE

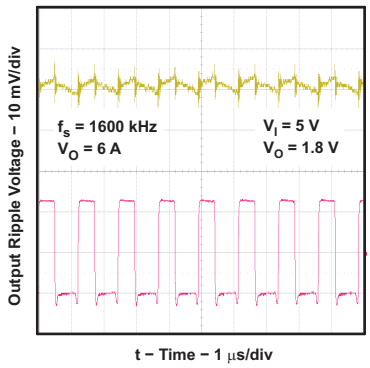


Figure 16.

TRANSIENT RESPONSE

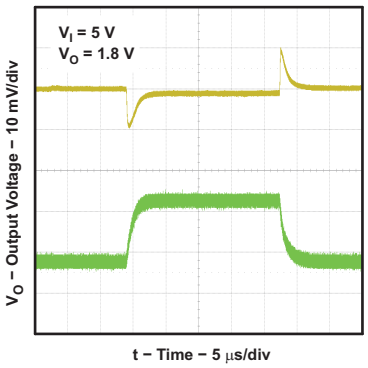


Figure 17.

SLOW-START TIMING

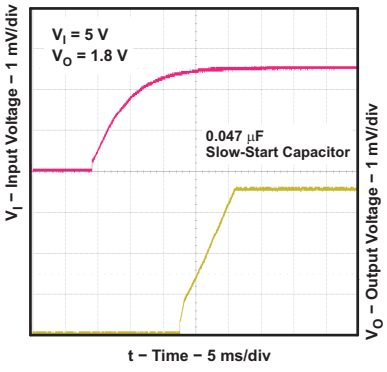


Figure 18.

INPUT RIPPLE VOLTAGE

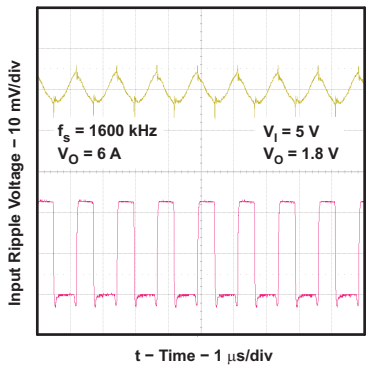


Figure 19.

CLOSED LOOP RESPONSE

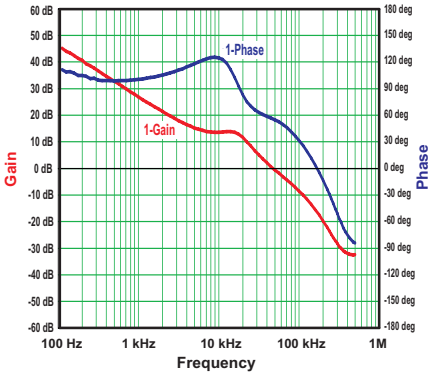


Figure 20.

(1)Safe operating area is applicable to the test board conditions listed in the dissipation rating table section of this data sheet.

DETAILED DESCRIPTION

Under Voltage Lock Out (UVLO)

The TPS54617 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

Slow-Start/Enable (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \quad (2)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \quad (3)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

VBIAS Regulator (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

Voltage Reference

The voltage reference system produces a precise Vref signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54617, since it cancels offset errors in the scale and error amplifier circuits.

Oscillator and PWM Ramp

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the SYNC pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 to 1600 kHz by connecting a resistor between the RT pin to ground and floating the SYNC pin. The switching frequency in MHz is approximated by the following equation, where R is the resistance in Ohms from RT to AGND:

$$F_{SW} = \frac{51000}{(R_T + 4400)} \quad (4)$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 1600 kHz by driving a synchronization signal into SYNC and connecting a resistor from RT to AGND. Choose a RT resistor that sets the free running frequency to 80% of the synchronization signal. Table 1 summarizes the frequency selection configurations:

Table 1. Summary of the Frequency Selection Configurations

SWITCHING FREQUENCY	SYNC PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	≥ 2.5 V	Float
Externally set 280 kHz to 1.6MHz	Float	R = 27 k to 180 k
Externally synchronized frequency	Synchronization signal	R = RT value for 80% of external synchronization frequency

Error Amplifier

The high performance, wide bandwidth, voltage error amplifier sets the TPS54617 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type-2 or Type-3 compensation can be employed using external compensation components.

PWM Control

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control-logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54617 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

Dead-Time Control and MOSFET Drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

Overcurrent Protection

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

Thermal Shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault condition, and then shutting down upon reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

Power Good (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low. When VIN ≥ UVLO threshold, SS/ENA ≥ enable threshold, and VSENSE > 90% of V_{ref}, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35 µs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54617RUVR	ACTIVE	VQFN	RUV	34	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	54617	Samples
TPS54617RUVR/2801	ACTIVE	VQFN	RUV	34	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	54617	Samples
TPS54617RUVT	ACTIVE	VQFN	RUV	34	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	54617	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

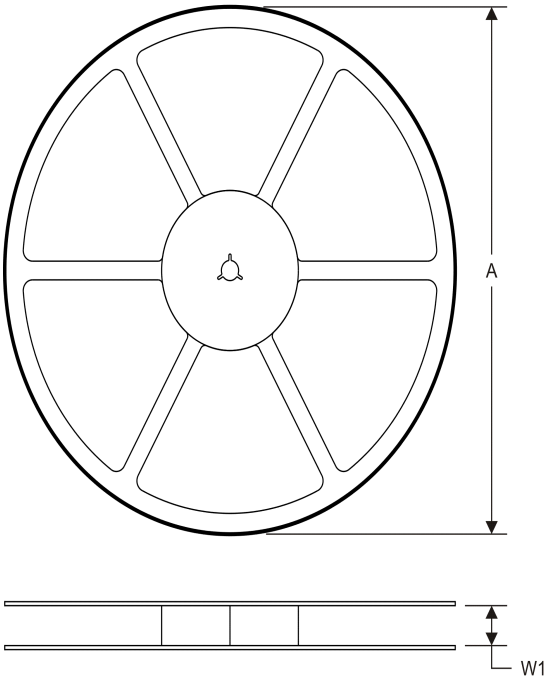
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

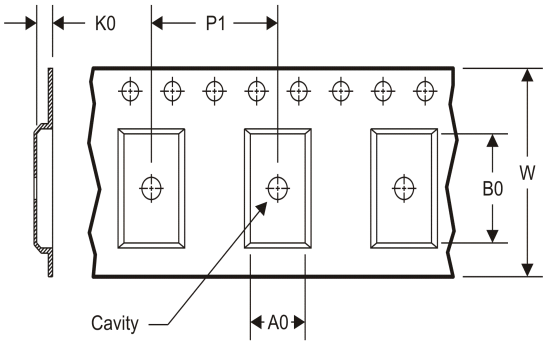
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



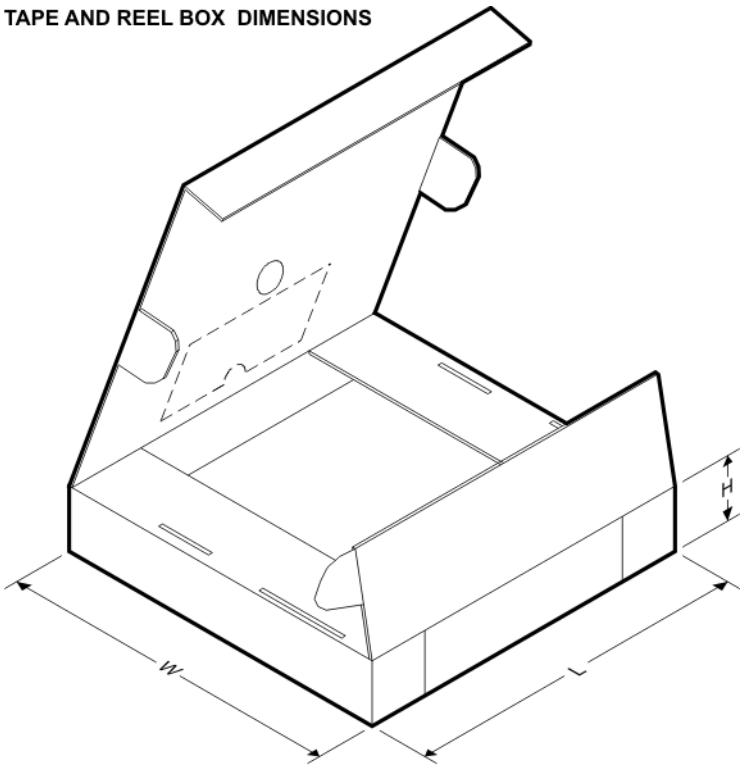
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54617RUVR	VQFN	RUV	34	3000	330.0	16.4	3.85	7.35	1.2	8.0	16.0	Q1
TPS54617RUVT	VQFN	RUV	34	250	180.0	16.4	3.85	7.35	1.2	8.0	16.0	Q1

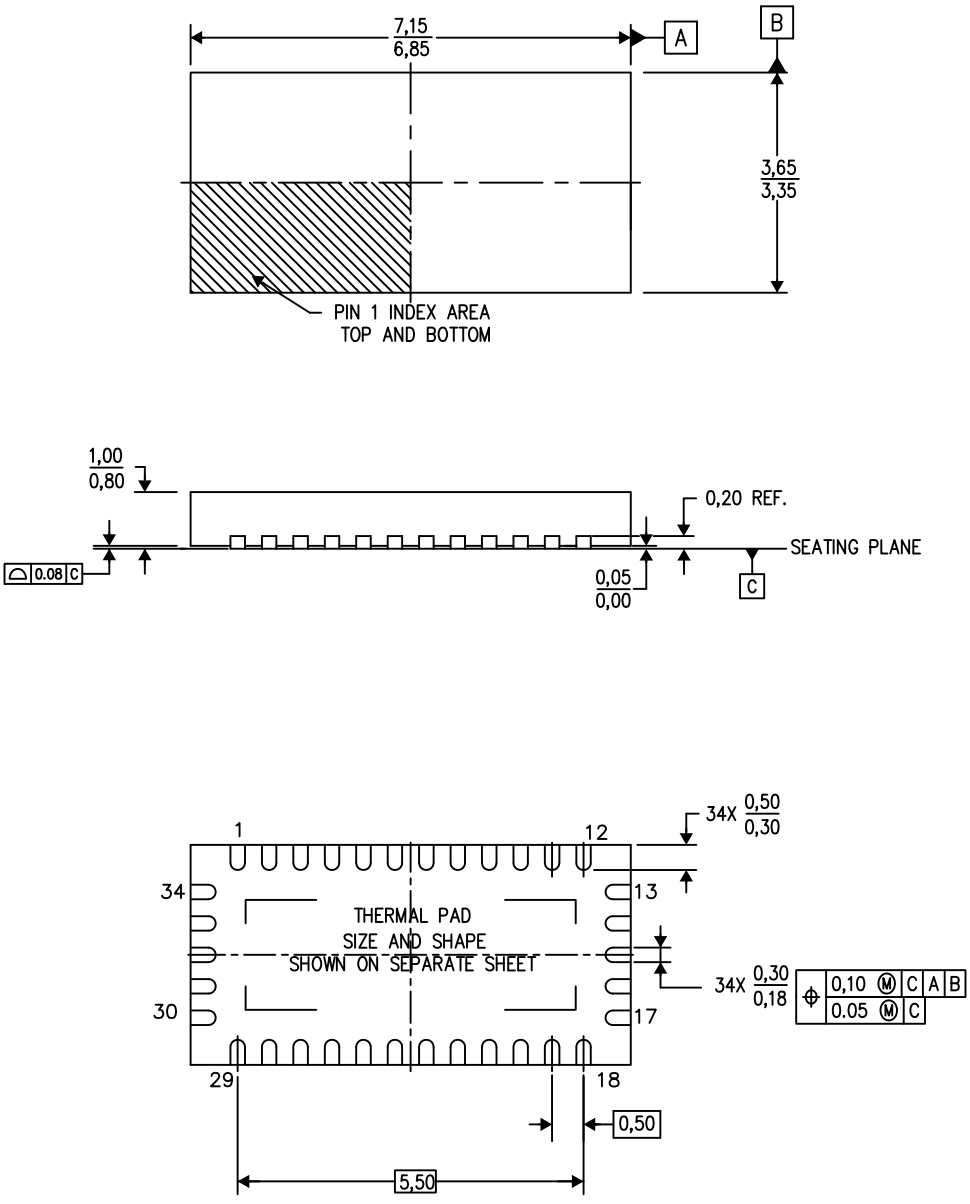
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54617RUVR	VQFN	RUV	34	3000	367.0	367.0	38.0
TPS54617RUVT	VQFN	RUV	34	250	210.0	185.0	35.0

RUV (R–PVQFN–N34) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

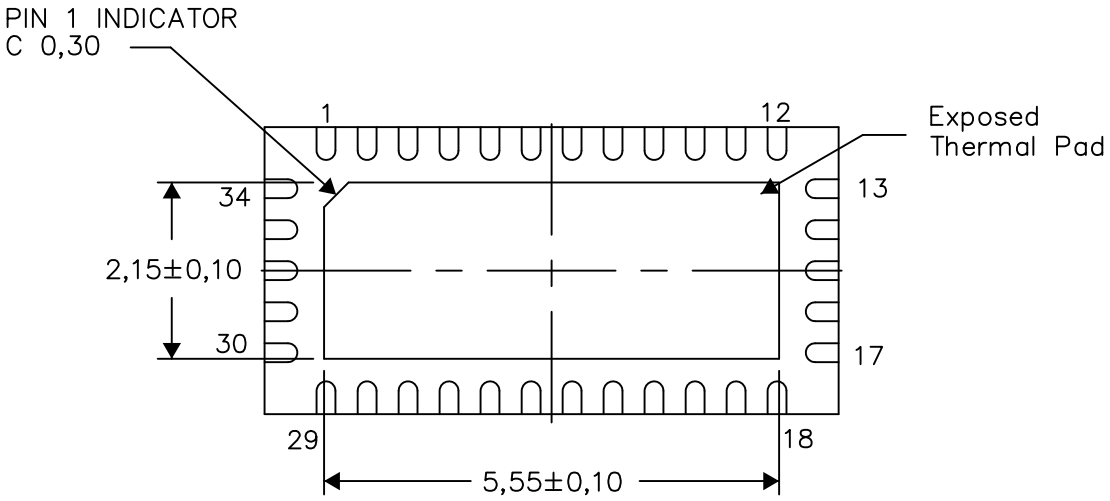
RUV (S–PVQFN–N34) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



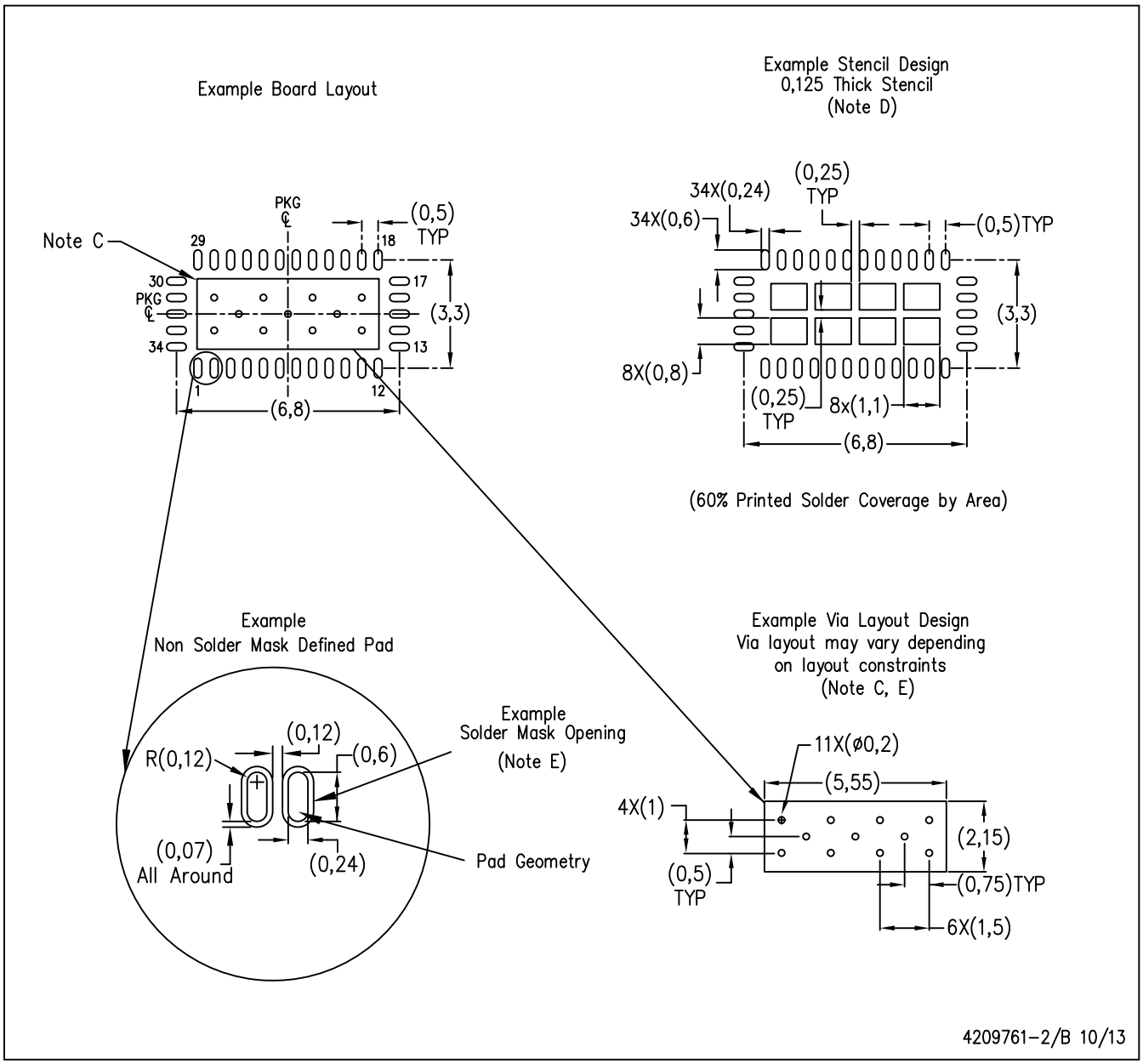
Bottom View

Exposed Thermal Pad Dimensions

4209552–2/E 06/13

NOTE: All linear dimensions are in millimeters

RUV (R–PVQFN–N34) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265