TEXAS INSTRUMENTS

TPS54356EVM-058 3-Amp

SWIFT™ Regulator Evaluation Module

User's Guide

May 2004

PMP Systems Power

SLVU110

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and the use of the TPS54356EVM−058 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and bill of materials are included.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Test Setup and Results
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials

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Chapter 1

Introduction

This chapter contains background information for the TPS54356 as well as support documentation for the TPS54356EVM-058 evaluation module (HPA058). The TPS54356EVM-058 performance specifications are given, along with a schematic and bill of material for the TPS54356EVM-058.

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1.1 Background

The TPS54356 dc/dc converter is designed to provide up to 3-A output from an input voltage source of 4.5 to 20 V. Rated input voltage and output current range is given in Table 1−1. This evaluation module is designed to demonstrate the small PCB areas that may be achieved when designing with the TPS54356 regulator, and does not reflect the high efficiencies that may be achieved when designing with this part. The switching frequency is set at a nominal 500 kHz, allowing the use of a relatively small footprint 22-µH output inductor. The high-side MOSFET is incorporated inside the TPS54356 package along with gate drive circuitry for an external synchronous FET. The low drain-to-source on resistance of the MOSFET allows the TPS54356 to achieve high efficiencies and helps to keep the junction temperature low at high output currents. The compensation components are provided internal to the IC. The TPS54356 is a full featured device including programmable under-voltage lockout, bidirectional sychronization, adjustable switching frequency, enable and power good functions

Table 1−1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54356EVM−058	4.5 V to 20 V† max 6.0 to 18 V nom	0 to 3 A

† Operation specified to 4.0 V, after initial start up.

1.2 Performance Specification Summary

A summary of the TPS54356EVM−058 performance specifications is provided in Table 1−2. Specifications are given for an input voltage of 12 V and an output voltage of 3.3 V, unless otherwise specified. The ambient temperature is 25°C for all measurements, unless otherwise noted. The maximum input voltage for the TPS54356 is 4.5 to 20 V. The EVM operates over this range, but is designed and tested for 6-V to 18-V input range (12 V nominal).

Table 1−2. TPS54356EVM-058 Performance Specification Summary

Specification		Test Conditions	Min	Typ	Max	Units
Input voltage range			6.0	12.0	18	V
Output voltage set point				3.3		V
Output current range		V_I = 6 V to 18 V	0		3	A
Line regulation		IO = 0−3 A, V_I = 6 V to 18 V		±0.1%		
Load regulation		V_I = 6 to 18 V, I_O = 0 A to 3 A		±0.2%		
Load transient response	Voltage change	I_O = 0.75 A to 2.25 A		−80		mV_{PK}
	Recovery time			320		µs
	Voltage change	I_O = 2.25 A to 0.75 A		80		mV_{PK}
	Recovery time			320		µs
Loop bandwidth		V_I = 6 V		21.5		kHz
Phase margin		V_I = 6 V		80		°
Loop bandwidth		V_I = 18 V		25.0		kHz
Phase margin		V_I = 18 V		71		°
Input ripple voltage				160	200	mV_{PP}
Output ripple voltage				5	10	mV_{PP}
Output rise time				3.5		ms
Operating frequency				500		kHz
Maximum efficiency		V_I = 6.0 V, V_O = 3.3 V, I_O = 0.5 A		92%		

1.3 Modifications

While the TPS54356EVM−058 is designed to demonstrate the small size that can be attained when designing with the TPS54356, features which allow for extensive modifications have been included in this EVM.

1.3.1 Output Voltage Setpoint

To change the output voltage of the EVM, it is necessary to change the SWIFT device (U1). Table 1−3 list the part numbers for the available output voltages.

Table 1−3. Output Voltages Available

Output Voltage (V)	Part Number
1.2	TPS54352
1.5	TPS54353
1.8	TPS54354
2.5	TPS54355
3.3	TPS54356
5.0	TPS54357

1.3.2 Switching Frequency

The switching frequency of the EVM is set to 500 kHz by leaving R4 open. Shorting R4 sets the operating frequency to 250 kHz. The switching frequency may also be trimmed to any value between 250 kHz and 700 kHz by changing the value of R4 using Equation 1−1. Decreasing the switching frequency results in increased output ripple unless the value of L1 is increased.

Equation 1−1.

$$\mathrm{RT(k\Omega)} = \frac{46000}{f_S\mathrm{(kHz)} - 35.9}$$

If using a programmable switching frequency, be sure to populate R11 with a 10-kΩ resistor to decrease susceptibility to noise at the SYNC pin.

1.3.3 Input Filter

An onboard electrolytic input capacitor is included at C1. Depending on the application this capacitor may be removed.

1.3.4 UVLO Programming

The TPS54356 is provided with an internal voltage divider from V_{IN} to AGND. The start and stop thresholds are given in Table 1−4.

Table 1−4. Internal UVLO Setting

		Start Voltage Threshold	Stop Voltage Threshold
VIN	TPS54352-6	4.49 V	3.69 V
	TPS54357	6.65 V	5.45 V
UVLO		1.24 V	1.02 V

To set a different set of thresholds, R6 and R7 can be selected using the following equations.

Equation 1−2.

$$R6 = \frac{V_{I(start)} \times R7}{UVLO(start)} - R7$$

Equation 1−3.

$$V_{I(stop)} = \frac{(R6 + R7) \times 1.02}{R7}$$

1 kΩ is a good value for R7.

1.3.5 Synchronization

The TPS54356EVM-058 provides the capability for synchronous operation with other devices of the TPS5435X family. When the EVM is configured so that the switching frequency is set to 250 or 500 kHz operation by grounding or floating the RT pin, the SYNC pin functions as an output. If the RT pin is terminated with a resistor to ground, setting a programmable operating frequency, then the SYNC pin functions as an input. When operated as an input, the SYNC pin is falling-edge triggered. When operating as an output, the falling edge of the SYNC signal is approximately 180 degrees out of phase with the rising edge oh the PH signal. This allows two TPS5435X devices to share an input capacitor with reduced input ripple due to cancellation. The SYNC signal is accessed on the EVM by the J3 header. R11 should be terminated with a 10-kΩ resistor if the SYNC signal is configured as an input.

1.3.6 Extending Slow Start Time

The slow start time may be extended by populating the R12 and C6 positions on the EVM. R12 must be 2 kΩ and C6 must less than 0.47 μF. A desired slow start time determines the value for C6, and is given by Equation 1−4.

Equation 1−4.

$$C6\ (\mu F) = 5.5 \times 10^{-3} \times 0.818 \times T_{SS}\ (ms)$$

Note that this equation is only valid for the TPS54356. If the EVM is modified for a different output voltage, see the product data sheet (SLVS519) for additional information on setting the slow start time.

1.3.7 Operation Without the Low-Side FET

It is possible to operate the TPS54356EVM−058 with a catch diode instead of the external low-side FET. Pads for the catch diode D1 are provided on the back of the PCB. The Motorola MBRS340T3 works well for this application.

Chapter 2

Test Setup and Results

This chapter describes how to properly connect, setup, and use the TPS54356EVM-058 evaluation module. The chapter also includes test results typical for the TPS54356EVM-058 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

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2.1 Input/Output Connections

The TPS54356EVM-058 is provided with input/output connectors and testpoints as shown in Table 2−1. A power supply capable of supplying 4 A should be connected to J1 through a pair of 20-AWG wires. The load should be connected to J2 through a pair of 20-AWG wires. The maximum load current capability should be 3 A. Wire lengths should be minimized to reduce losses in the wires. Testpoints TP4 and TP5 provide a place to monitor the input voltage, while TP3 and TP6 are used to monitor the output voltage.

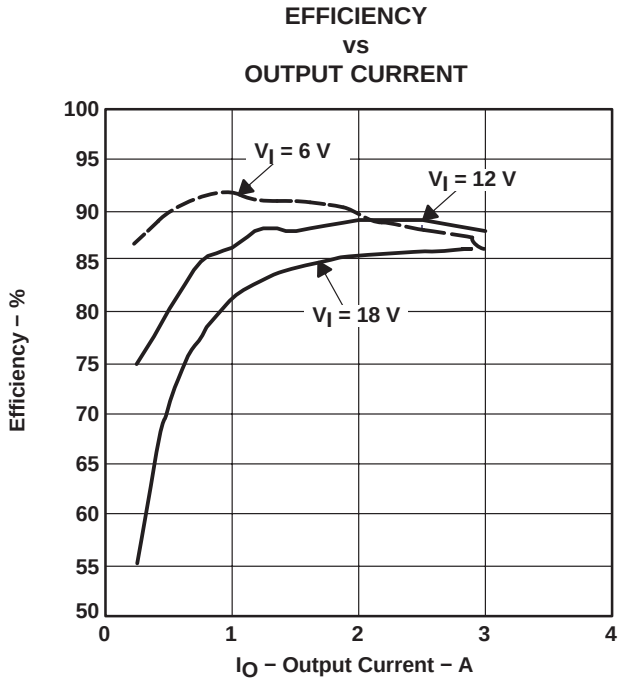
Table 2−1. EVM Connectors and Testpoints

Reference Designator	Function
J1	Vin, 6 to 18 V nominal, 4.5 to 20 V maximum
J2	Vout, 3.3 V at 0 to 3 A
J3	2-pin header for SYNC signal input or output
J4	2-pin header for ENA, ground to disable , open to enable
TP1	Connection for external 3.3-V or 5-V PWRGD pullup
TP2	PWRGD signal monitor testpoint
TP3	Output voltage testpoint at V_{OUT} connector
TP4	Input voltage testpoint at V_{IN} connector
TP5	GND testpoint at V_{IN} connector
TP6	GND testpoint at V_{OUT} connector
TP7	V_{SENSE} testpoint
TP8	PH testpoint
TP9	UVLO testpoint
TP10	RT testpoint

2.2 Efficiency

The TPS54356EVM-058 efficiency peaks at load current of about 1 to 2 A, and then decreases as the load current increases towards full load. Figure 2−1 shows the efficiency for theTPS54356 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 700 kHz than efficiency at lower switching frequencies due to the gate and switching losses in the MOSFETs.

Figure 2−1. Measured Efficiency, TPS54356



2.3 Output Voltage Regulation

The output voltage load regulation of the TPS54356EVM−058 is shown in Figure 2−2, while the output voltage line regulation is shown in Figure 2−3. Measurements are given for an ambient temperature of 25°C.

Figure 2−2. Load Regulation

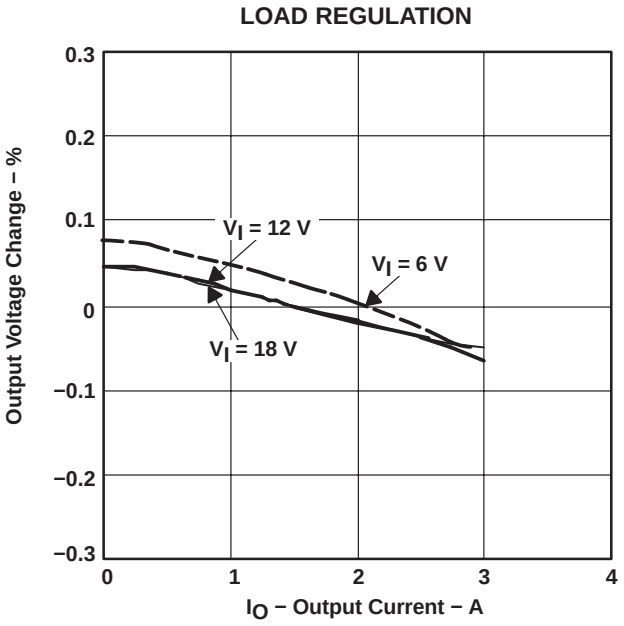
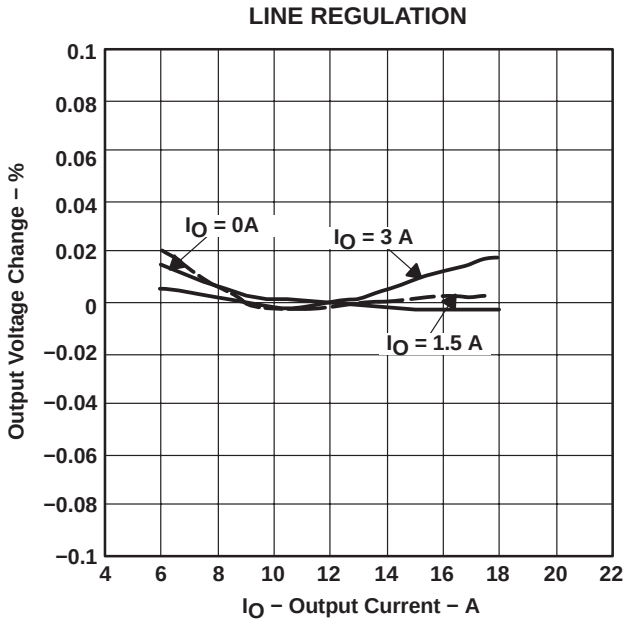


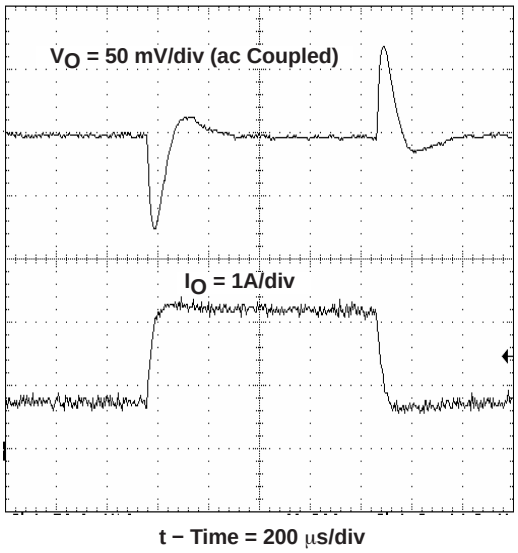
Figure 2−3. Line Regulation



2.4 Load Transients

The TPS54356EVM−058 response to load transients is shown in Figure 2−4. The current step is from 25 to 75 percent of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2−4. Load Transient Response, TPS54350



2.5 Loop Characteristic

The TPS54356EVM-058 loop response characteristics are shown in Figure 2−5 and Figure 2−6. Gain and phase plots are shown for each device at minimum and maximum operating voltage.

Figure 2−5. Measured Loop Response, TPS54356, V_I = 6 V

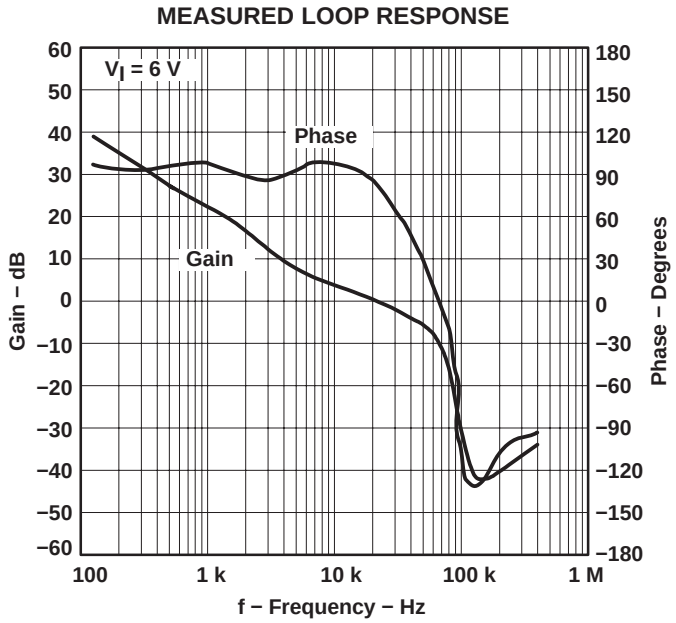
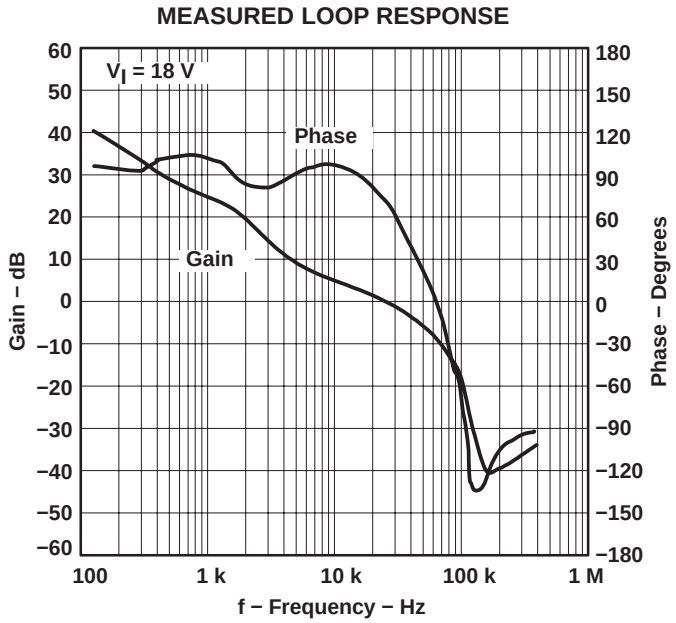


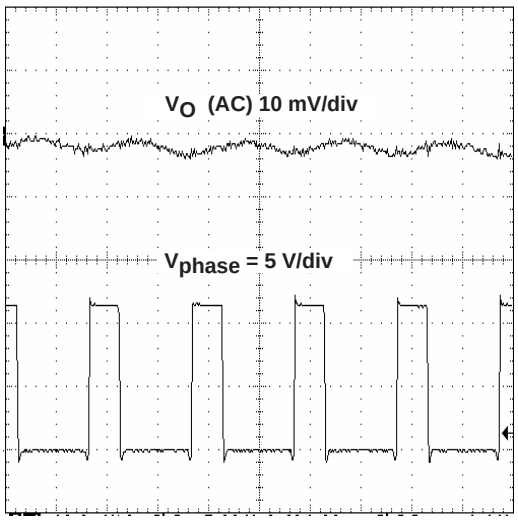
Figure 2−6. Measured Loop Response, TPS54356, V_I = 18 V



2.6 Output Voltage Ripple

The TPS54356EVM−058 output voltage ripple is shown in Figure 2−7. The input voltage is 12 V for the TPS54356. Output current is the rated full load of 3 A. Voltage is measured directly across output capacitors.

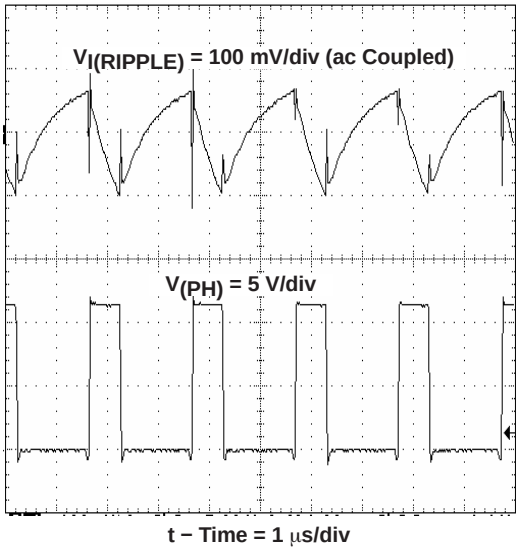
Figure 2−7. Measured Output Voltage Ripple, TPS54356



2.7 Input Voltage Ripple

The TPS5456EVM-058 output voltage ripple is shown in Figure 2−8. The input voltage is 12 V for the TPS54356. Output current for each device is rated full load of 3 A.

Figure 2−8. Input Voltage Ripple, TPS54350



2.8 Powering Up and Down

The TPS54356EVM−058 start up waveforms are shown in Figure 2−9. In the figure, the top trace shows Vi charging up from 0-V to 12-V. When the input voltage reaches the internally set UVLO threshold voltage of 4.49 V, V_O begins to ramp up linearly at the internally-set slow start rate towards 3.3 V. As soon as the output reaches 97 percent of its preset final value, the PWRGD signal is asserted high. In this case, the PWRGD output has been pulled up to 3.3V.

The power-down sequence is shown in Figure 2−10. When the input decays to the stop voltage threshold of 3.69 V, the regulator tuns off and the output starts to decay toward 0 V. The shape of the discharge curve is dependent on the load. As soon as the output falls out of regulation, the PWRGD signal is asserted low. When the input voltage decays below about 2.8 V, the internal control circuitry state is undefined and the PWRGD signal *floats*.

Figure 2−9. Power Up With Tracking

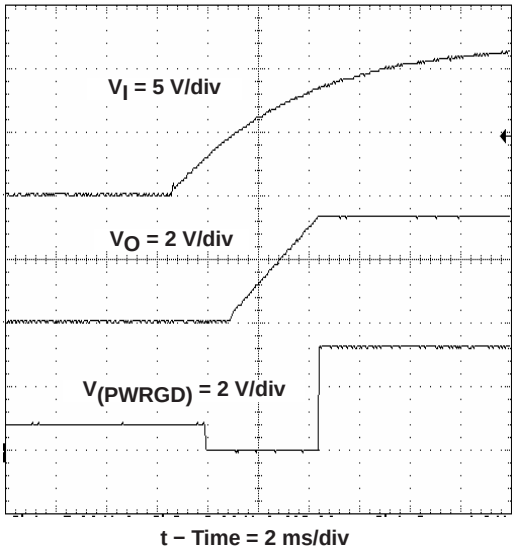
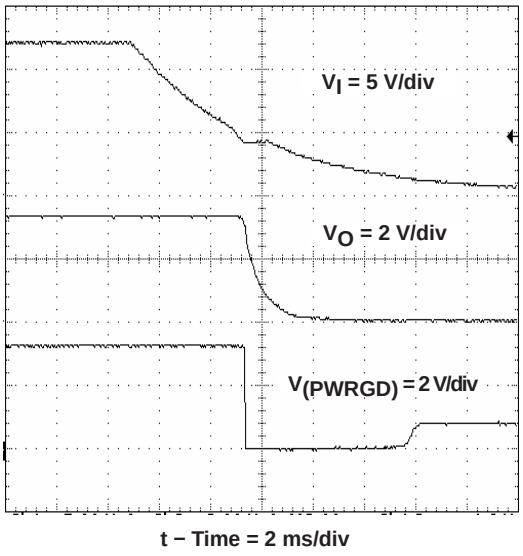


Figure 2−10. Powering Down With Tracking



Chapter 3

Board Layout

This chapter provides a description of the TPS54356EVM−058 board layout and layer illustrations.

Topic **Page**

3.1 Layout 3-2

3.1 Layout

The board layout for the TPS54356EVM−058 is shown in Figure 3−1 through Figure 3−4. The topside layer of the TPS54356EVM−058 is laid out in a manner typical of a user application. The top and bottom layers are 1.5 oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and V_{PHASE}. Also on the top layer are connections for the remaining pins of the TPS54356, and a large ground area. The bottom layer contains ground and V_{OUT} copper areas, and some signal routing. The top and bottom ground traces are connected with multiple vias placed around the board including 10 directly under the TPS54356 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitors (C5 and C9), bias decoupling capacitor (C4), and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, adjacent to the high frequency bypass output capacitor.

Figure 3−1. Top-Side Layout

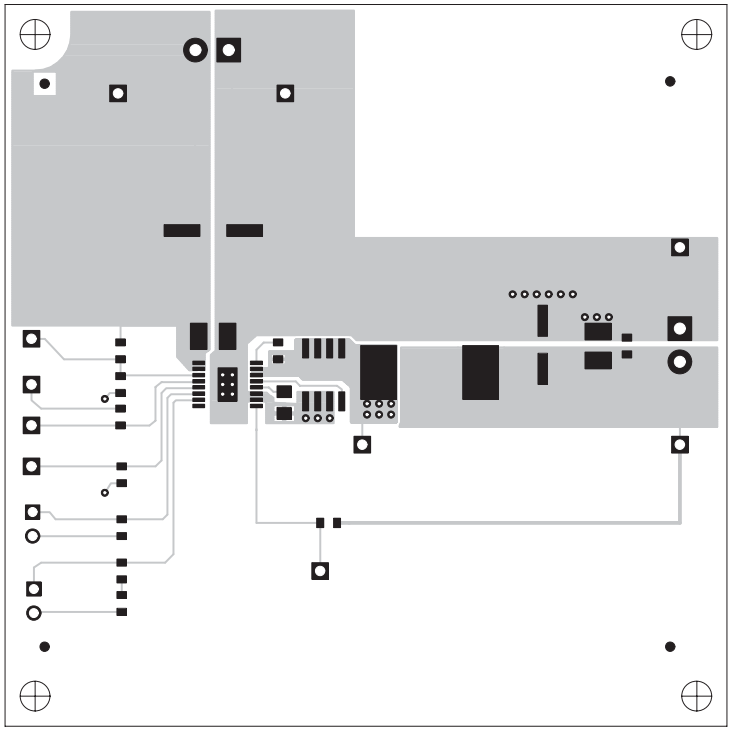


Figure 3−2. Bottom Side Layout (looking from top side)

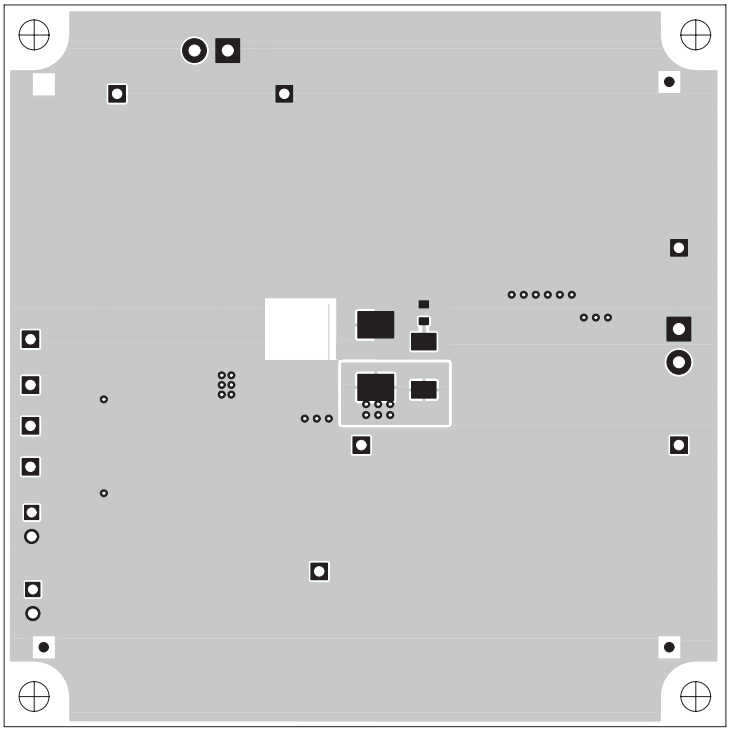


Figure 3−3. Top Side Assembly

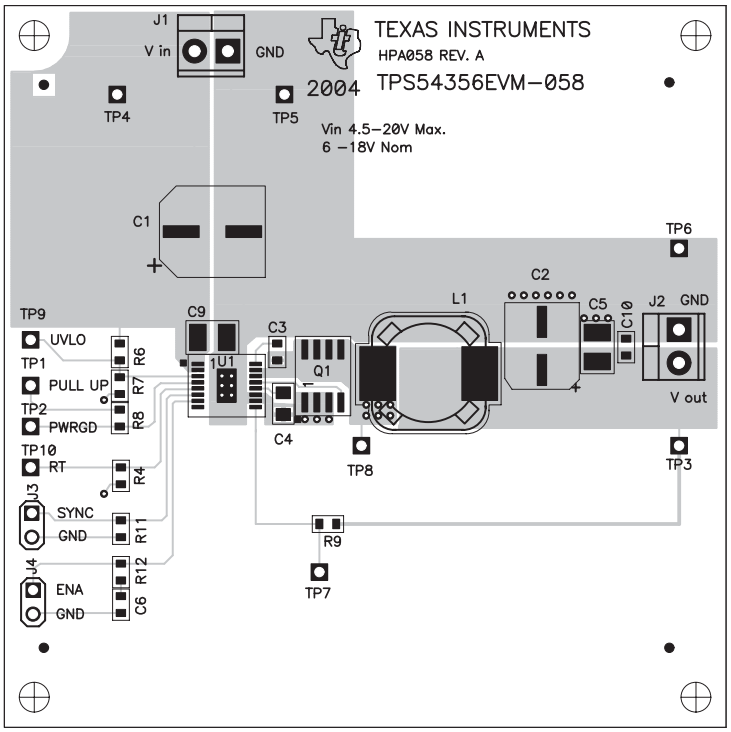
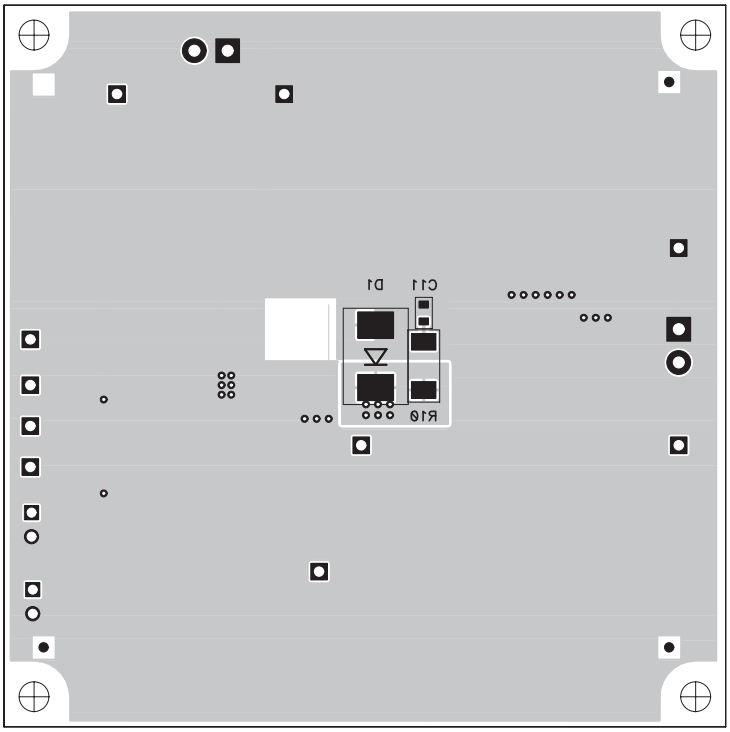


Figure 3−4. Bottom Side Assembly (looking from top side)



Chapter 4

Schematic and Bill of Materials

The TPS54356EVM−058 schematic and bill of materials are presented in this chapter.

Topic **Page**

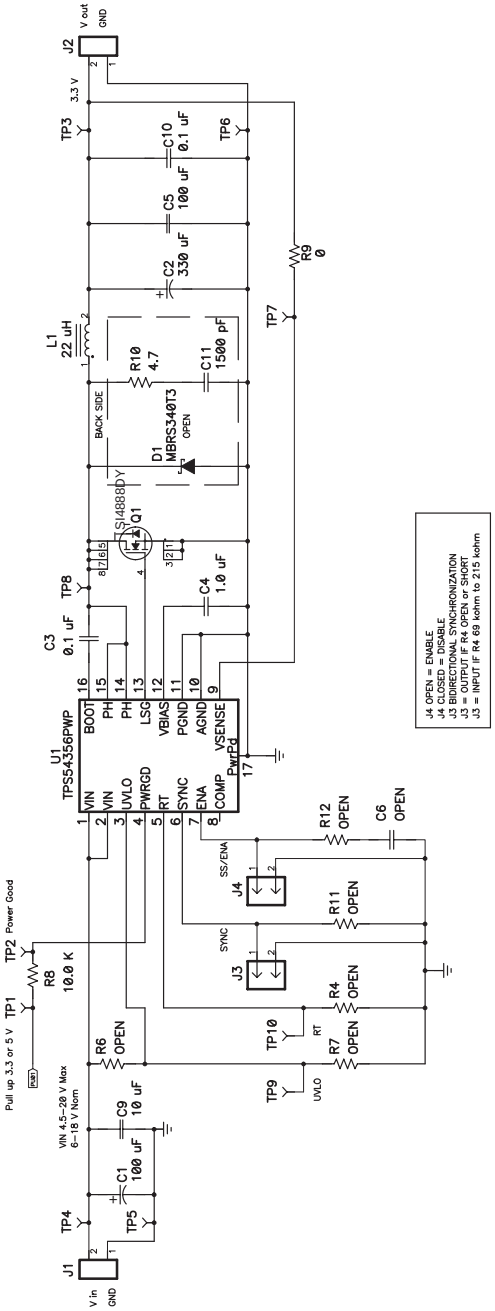
4.1 Schematic 4-2

4.2 Bill of Materials 4-3

4.1 Schematic

The schematic for the TPS54356EVM−058 is shown in Figure 4−1.

Figure 4−1. TPS54356EVM-058 Schematic



4.2 Bill of Materials

The bill of materials for the TPS54356EVM−058 is given by Table 4−1.

Table 4−1. TPS54356EVM-058 Bill of Materials

COUNT	RefDes	DESCRIPTION	SIZE	MFR	PART NUMBER
1	C1	Capacitor, aluminum, SM, 100 µF, 35−V, 160−mΩ (FK series)	8x10mm	Panasonic	EEV−FK1V101P
1	C11	Capacitor, ceramic, 1500−pF, 50−V, X7R, 10%	603	std	std
1	C2	Capacitor, aluminum, 330 µF, 6.3−V, 20%, FK Series	0.268 × 0.307	Panasonic	EEVFK0J331XP
2	C3, C10	Capacitor, Ceramic, 0.1 µF, 16−V, X7R, 10%	603	std	std
1	C4	Capacitor, Ceramic, 1.0 µF, 16−V, X7R 10%	805	std	std
1	C5	Capacitor, Ceramic, 100 µF, 6.3−V, X5R, 20%	1210	TDK	C3225X5R0J107M
—	C6	Capacitor, Ceramic, xxx µF, 50−V, X7R, 10%	603	std	std
1	C9	Capacitor, Ceramic, 10 µF, 25−V, X5R, 20%	1210	Taiyo Yuden	TMK325BJ106MN
−	D1	Diode, Schottky, 3−A, 40−V	SMC	Motorola	MBRS340T3
2	J1, J2	Terminal Block, 2−pin, 6−A, 3.5mm	75525	OST	ED1514
2	J3, J4	Header, 2−pin, 100 mil spacing, (36-pin strip)	0.100 × 2	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 22 µH, 7.57−A, 39−mΩ	250000	Coiltronics	DR127−220
1	Q1	MOSFET, N−ch, 30−V, 16−A, 7−mΩ	SO8	Siliconix	Si4888DY
1	R10	Resistor, Chip, 4.7 Ω, ½ W, 5%	2010	std	std
—	R4, R6, R7, R11, R12	Resistor, Chip, xxx Ω, 1/16−W, 1%	603	std	std
1	R8	Resistor, Chip, 10.0 KΩ, 1/16−W, 1%	603	std	std
1	R9	Resistor, Chip, 0 Ω, 1/16−W, 1%	603	std	std
1	—	Shunt, 100−mil, Black	0.100	3M	929950−00
6	TP1, TP3, TP4, TP8, TP9, TP10	Test Point, Red, 1 mm	0.038	Farnell	240−345
4	TP2, TP5, TP6, TP7	Test Point, Black, 1 mm	0.038	Farnell	240−333
1	U1	IC, dc/dc converter	PWP16	TI	TPS54356PWP
1	—	PCB, 3 In × 3 In × 0.062 In		Any	HPA058