User's Guide
SLVU377–May 2010

TPS54319EVM-626 3-A, SWIFT™ Regulator Evaluation Module

This user's guide contains information for the TPS54319EVM-626 evaluation module (HPA597). Included are the performance specifications, the schematic, and the bill of materials for the TPS54319EVM-626.

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1 Introduction

This user's guide contains background information for the TPS54319 as well as support documentation for the TPS54319EVM-626 evaluation module (HPA597). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54319EVM-626.

1.1 Background

The TPS54319 dc/dc converter is designed to provide up to a 3-A output from an input voltage source of 2.95 V to 6 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small, printed-circuit-board areas that may be achieved when designing with the TPS54319 regulator. The switching frequency is externally set at a nominal 1000 kHz. The both high-side and low-side MOSFETs are incorporated inside the TPS54319 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFETs allows the TPS54319 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54319 provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 7 V for the TPS54319EVM-626.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54319EVM-626	VI_N = 3 V to 6 V	0 A to 2.5 A

1.2 Performance Specification Summary

A summary of the TPS54319EVM-626 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 5 V and an output voltage of 1.8 V, unless otherwise specified. The TPS54319EVM-626 is designed and tested for V_{IN} = 3 V to 6 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54319EVM-626 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			3	5	6	V
Output voltage set point				1.8		V
Output current range	V_{IN} = 3 V to 6 V		0		3	A
Line regulation	I_O = 1.5 A, V_{IN} = 3 V to 6 V			±0.06%		
Load regulation	V_{IN} = 5 V, I_O = 0.001 A to 3 A			±0.15%		
Load transient response	I_O = 0 A to12.5 A	Voltage change		–100		mV
		Recovery time		0.1		ms
	I_O = 1.5 A to 0 A	Voltage change		100		mV
		Recovery time		0.1		ms
Loop bandwidth	V_{IN} = 5 V, I_O = 3 A			50		kHz
Phase margin	V_{IN} = 5 V , I_O =3 A			49		°
Input ripple voltage	I_O = 3 A			100		mV_{PP}
Output ripple voltage	I_O = 3 A			10		mV_{PP}
Output rise time				6		ms
Operating frequency				1000		kHz
Maximum efficiency	TPS54319EVM-626, V_{IN} = 3.3 V, I_O = 0.5 A			93.8 %		

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1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54319. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

The voltage divider of R6 and R7 is used to set the output voltage of the EVM. The 51.1 Ω resistor R8 is provided as an aid to check the loop response of the circuit. To change the output voltage of the EVM, it is necessary to change the value of resistor R6. Changing the value of R6 can change the output voltage above 0.8 V. The value of R6 for a specific output voltage can be calculated using Equation 1.

$$R6 = 10\ k\Omega \times \frac{(V_{OUT} - 0.827\ V)}{0.827\ V} \quad (1)$$

Table 3 lists the R6 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 130 ns, and the maximum duty cycle is less than 94%. Higher duty cycles are possible, but may result in uneven switching behavior. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Common Output Voltages

Output Voltage (V)	R6 Value (kΩ)
1.2	4.53
1.5	8.06
1.8	11.8
2.5	20.0
3.3	30.1

Be aware that changing the output voltage can affect the loop response. It may be necessary to modify the compensation components. See the data sheet (SLVSA83) for details.

1.3.2 Operating Frequency, Slow-Start and UVLO

The operating frequency, slow-start time and UVLO voltage may also be adjusted. R5 sets the operating frequency, C7 sets the slow-start time and the resistor divider of R1 and R2 sets the UVLO start and stop voltages. See the TPS54319 (SLVSA83) data sheet for details on adjusting these parameters.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54319EVM-626 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS54319EVM-626 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 1.5 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J2 through a pair of 20 AWG wires. The maximum load current capability must be 2.5 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP9 is used to monitor the output voltage with TP10 as the ground reference.

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Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range).
J2	V_{OUT}, 1.8 V at 3 A maximum.
JP1	Jumper for ENABLE function. Install jumper for disable. Open for enable.
JP2	Jumper for PWRGD pull up. Install jumper to pull PWRGD to V_{IN} through 100 kΩ.
TP1	V_{IN} test point at V_{IN} connector.
TP2	GND test point at V_{IN}.
TP3	PH test point EN test point. Connect EN to ground to disable, open to enable.
TP4	Slow start monitor test point.
TP5	Test point between R8 and R6. Used for loop response measurements.
TP6	Output voltage test point at OUT connector.
TP7	GND test point at OUT connector.
TP8	PWRGD test point.

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.5 A with V_{IN} = 3.3 V, and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPS54319EVM-626 at an ambient temperature of 25°C.

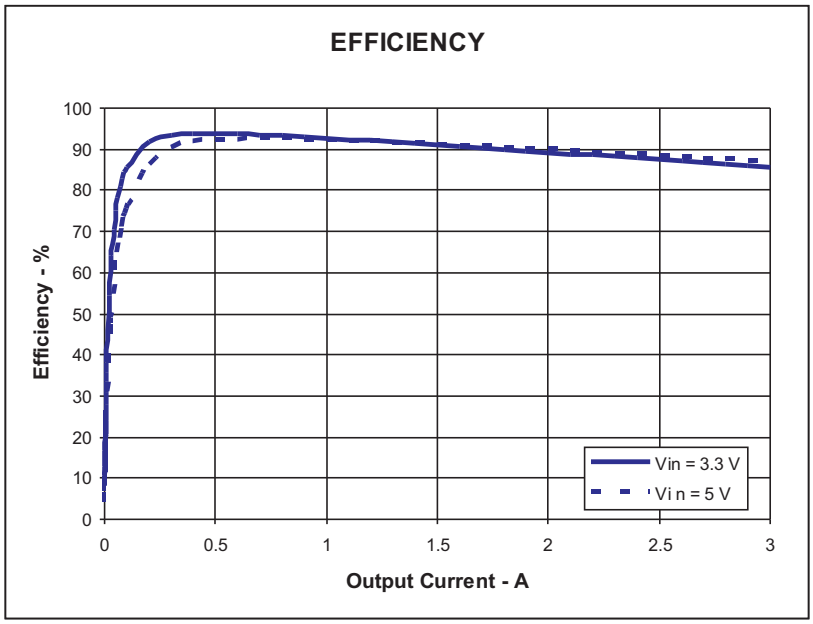


Figure 1. TPS54319EVM-626 Efficiency

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Figure 2 shows the efficiency for the TPS54319EVM-626 at lower output currents between 0.001 A and 3 A at an ambient temperature of 25°C.

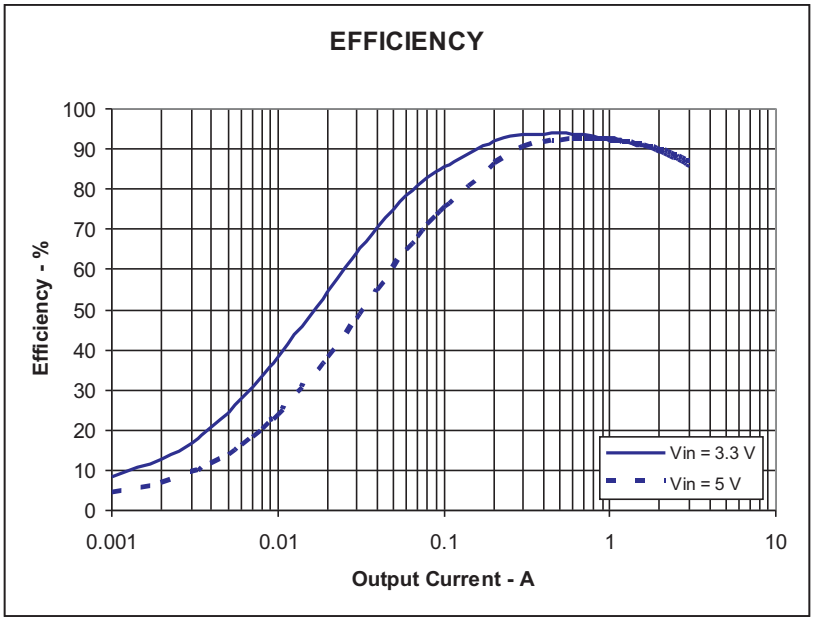


Figure 2. TPS54319EVM-626 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

The load regulation for the TPS54319EVM-626 is shown in Figure 3.

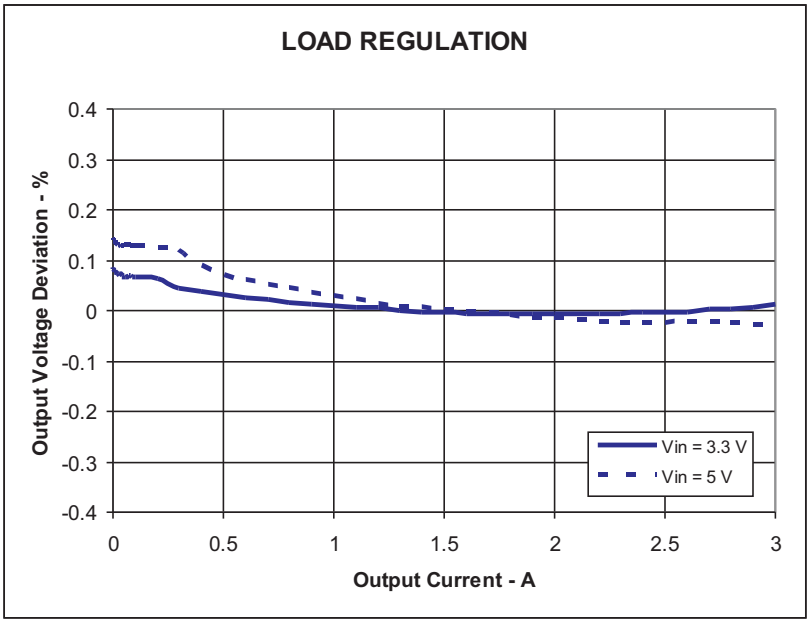


Figure 3. TPS54319EVM-626 Load Regulation

Measurements are given for an ambient temperature of 25°C.

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2.4 Output Voltage Line Regulation

The line regulation for the TPS54319EVM-626 is shown in Figure 4.

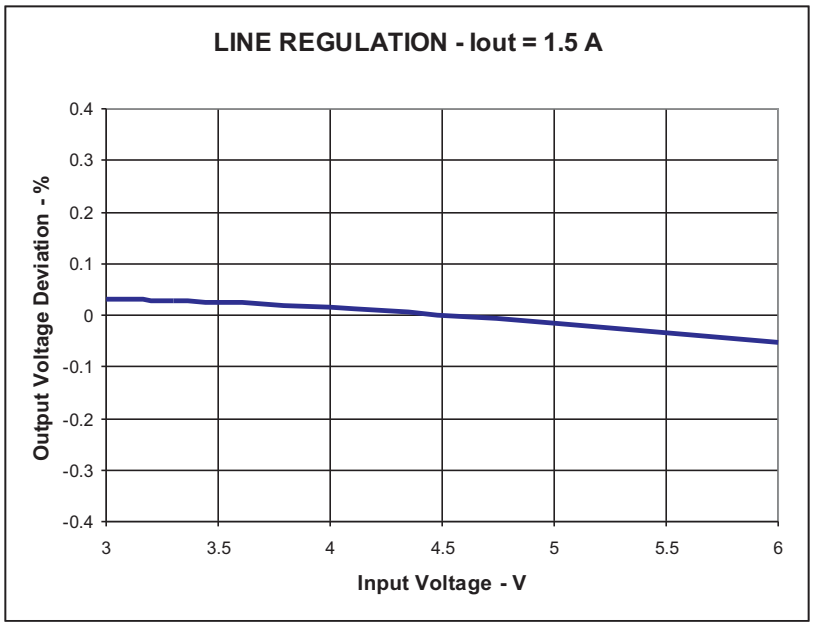


Figure 4. TPS54319EVM-626 Line Regulation

2.5 Load Transients

The TPS54319EVM-626 response to load transients is shown in Figure 5. The current step is from 0 A to 1.5 A . The input voltage is 5 V. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

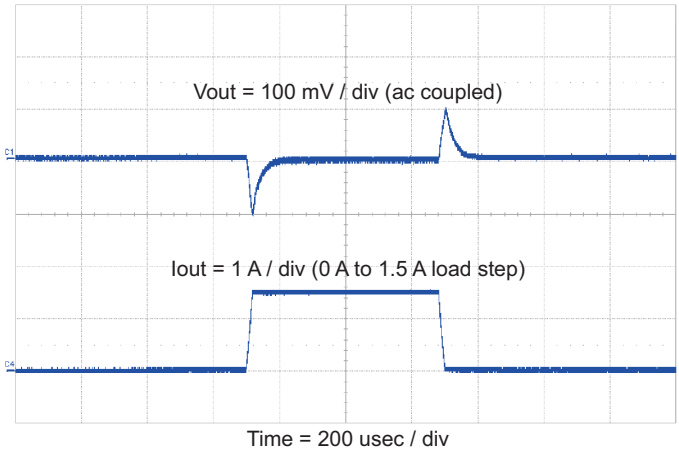


Figure 5. TPS54319EVM-626 Transient Response

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2.6 Loop Characteristics

The TPS54319EVM-626 loop-response characteristics are shown in Figure 6 . Gain and phase plots are shown for V_{IN} voltage of 5 V. Load current for the measurement is 3 A.

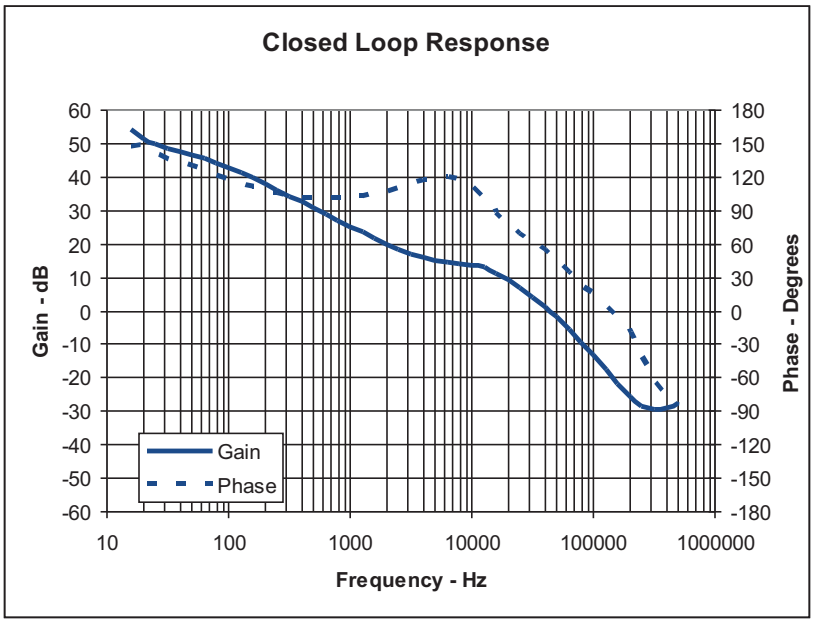


Figure 6. TPS54319EVM-626 Loop Response

2.7 Output Voltage Ripple

The TPS54319EVM-626 output voltage ripple is shown in Figure 7 . The output current is the rated full load of 3 A and V_{IN} = 5 V. The ripple voltage is measured directly across the output capacitors.

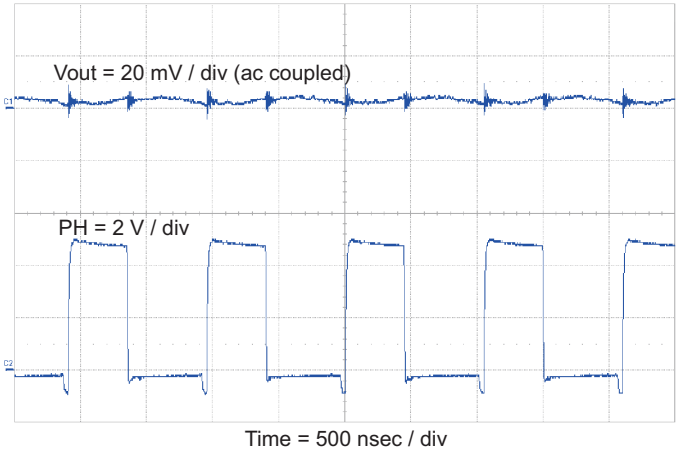


Figure 7. TPS54319EVM-626 Output Ripple

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2.8 Input Voltage Ripple

The TPS54319EVM-626 input voltage ripple is shown in Figure 8 . The output current is the rated full load of 3 A and V_{IN} = 5 V. The ripple voltage is measured directly across the input capacitors.

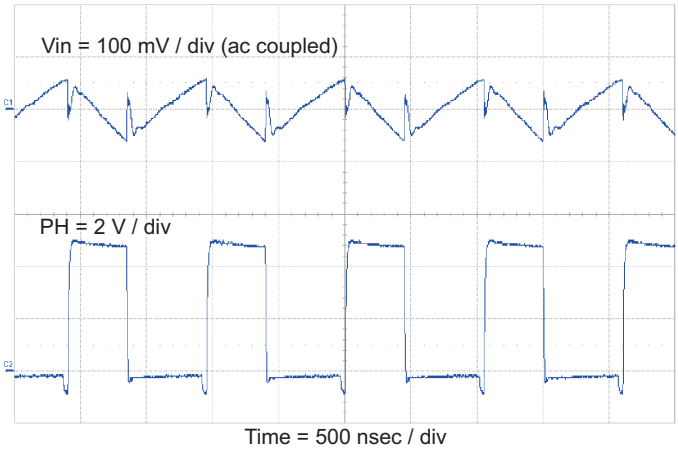


Figure 8. TPS54319EVM-626 Input Ripple

2.9 Powering Up

2.9.1 Power Up Relative to V_{IN}

The start-up waveform shown in Figure 9 shows start-up is relative to VIN rising. The input voltage is initially applied, and when the input reaches the undervoltage lockout threshold, the start-up sequence begins and the output ramps up at the externally set rate toward the set value of 1.8 V. The input voltage for this plot is 5 V with a 2 Ω load.

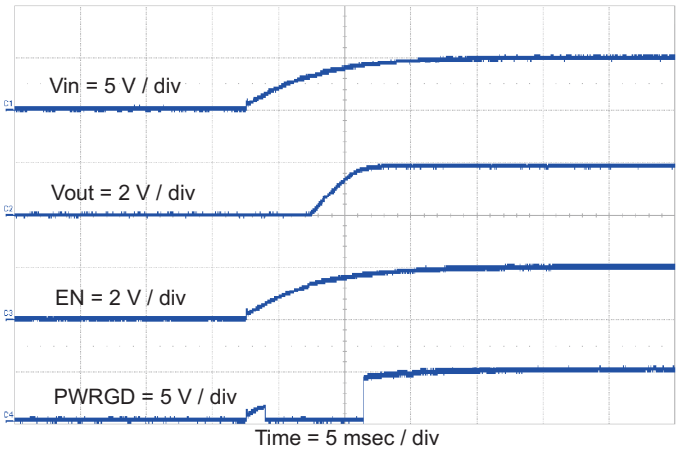


Figure 9. TPS54319EVM-626 Start-Up Relative to V_{IN}

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2.9.2 Power Up Relative to EN

The start-up waveform shown in Figure 10shows start-up is relative to EN rising. The input voltage is initially applied and allowed to reach 5V while EN is held low by installing a jumper across JP1. When the jumper is removed, the device is enabled and the start-up sequence begins. The output ramps up at the externally set rate toward the set value of 1.8 V. The input voltage for this plot is 5 V with a 2 Ω load.

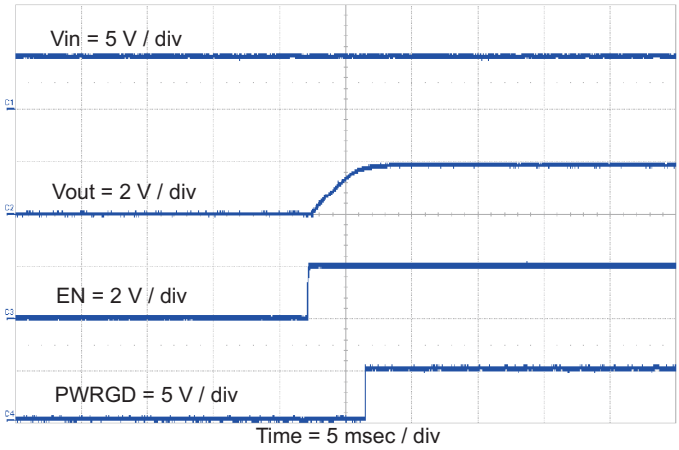


Figure 10. TPS54319EVM-626 Start-Up Relative to EN

3 Board Layout

This section provides a description of the TPS54319EVM-626, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54319EVM-626 is shown in Figure 11 through Figure 15. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and VPHASE. The top layer also has connections for the remaining pins of the TPS54319, and a large area filled with ground. The two internal layers and bottom layer contain ground planes. The top and bottom and internal ground traces are connected with multiple vias placed around the board including four vias directly under the TPS54319 device to provide a thermal path from the top-side ground area to the bottom-side ground plane.

The input decoupling capacitors (C2 and C3) and bootstrap capacitor (C6) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the output connector (J2). For the TPS54319, an additional input bulk capacitor may be required (C1), depending on the EVM connection to the input supply.

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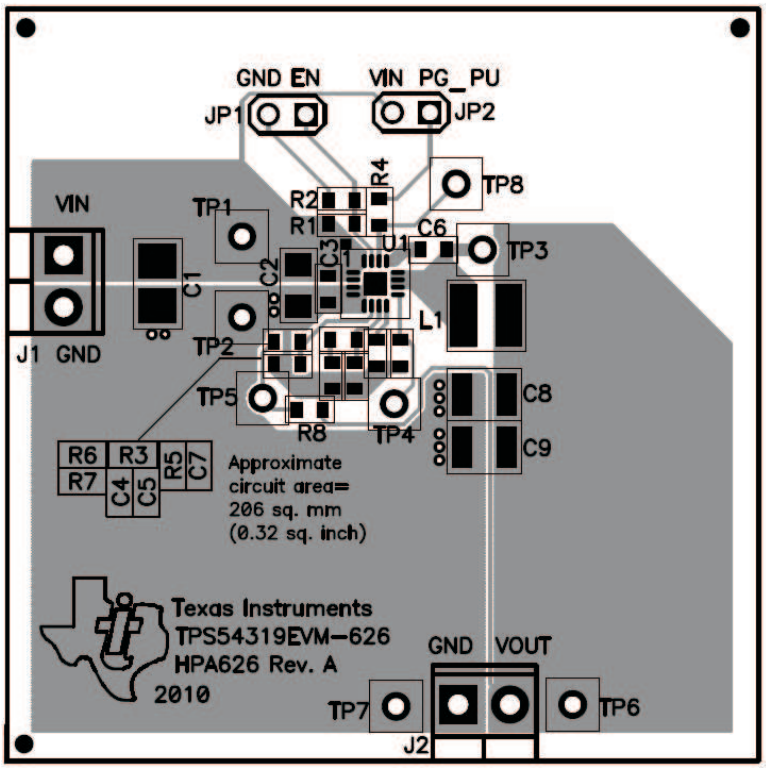


Figure 11. TPS54319EVM-626 Top-Side Assembly

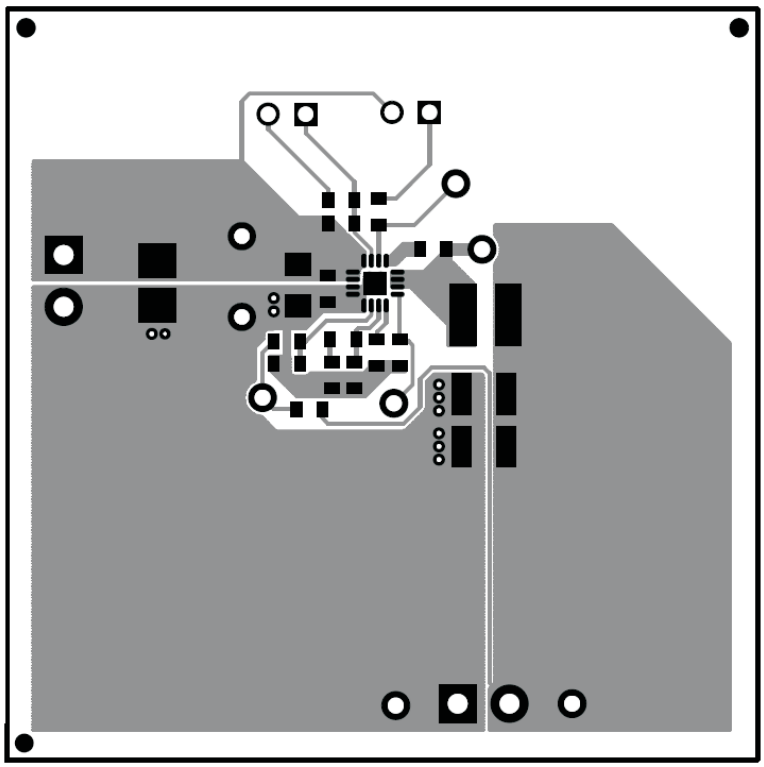


Figure 12. TPS54319EVM-626 Top-Side Layout

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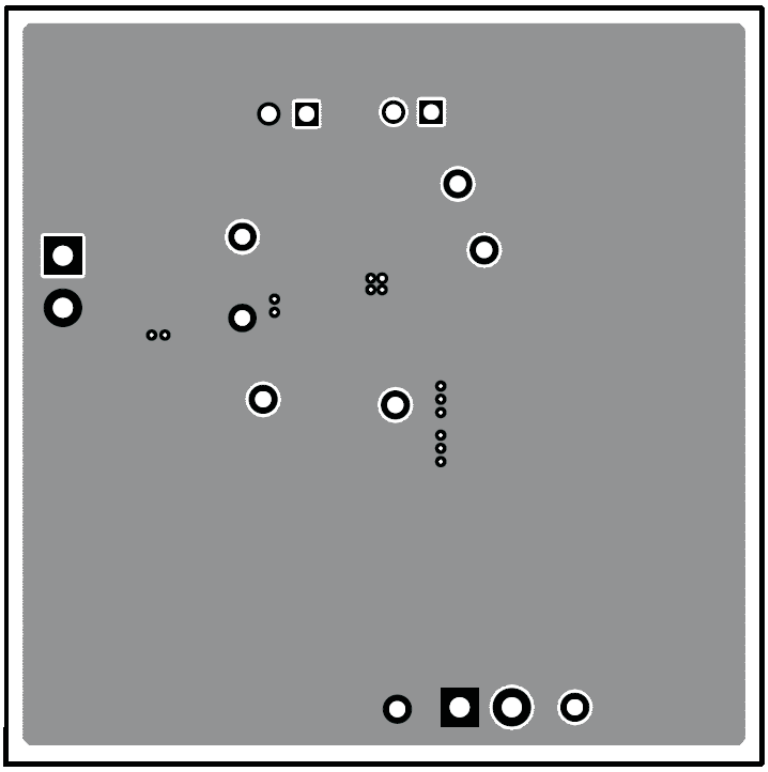


Figure 13. Internal Layer 1

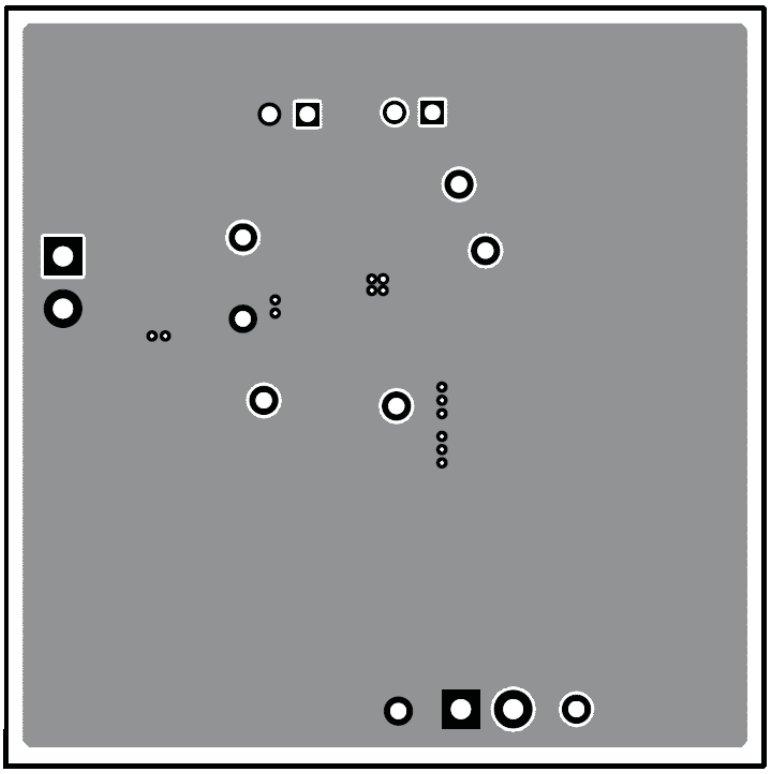


Figure 14. Internal Layer 2

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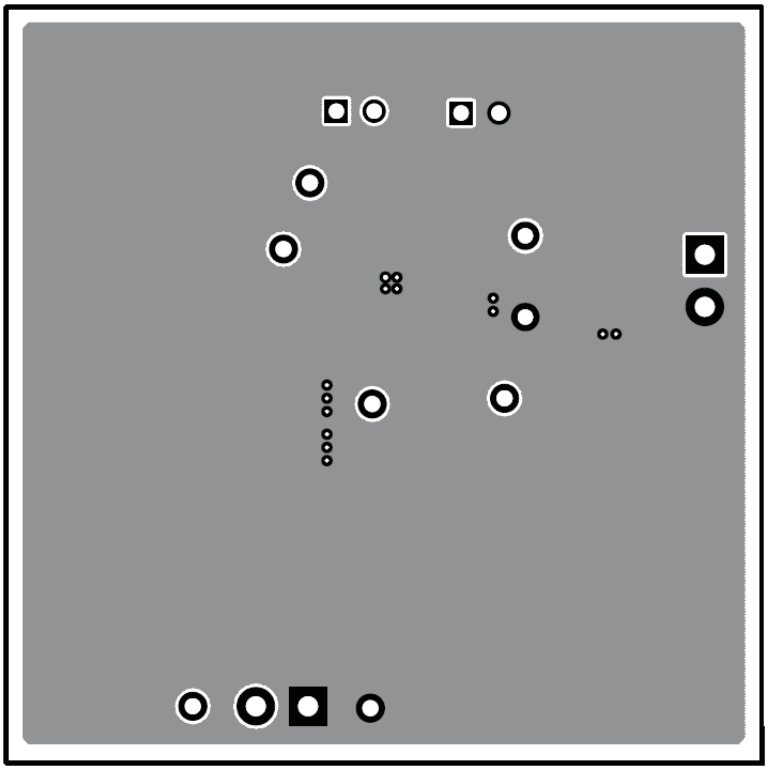


Figure 15. TPS54319EVM-626 Bottom-Side Layout

3.2 Estimated Circuit Area

The estimated printed-circuit board area for the components used in this design is 0.32 in^2. This area does not include test points or connectors.

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4 Schematic and Bill of Materials

This section presents the TPS54319EVM-626 schematic and bill of materials.

4.1 Schematic

Figure 16 is the schematic for the TPS54319EVM-626.

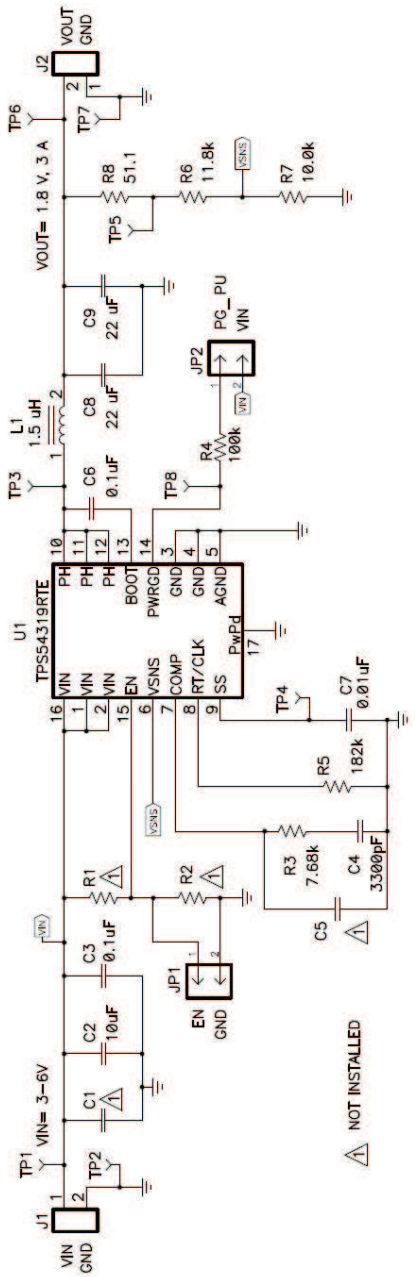


Figure 16. TPS54319EVM-626 Schematic

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4.2 Bill of Materials

Table 5 presents the bill of materials for the TPS54319EVM-626.

Table 5. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1	open	Capacitor, multi pattern, SM 1210 to E case + F THole	Multi sizes	Engineering Only	Std
1	C2	10uF	Capacitor, Ceramic, 10V, X5R, 20%	1206	Std	Std
1	C3, C6	0.1uF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
1	C4	3300pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C5	open	Capacitor, Ceramic	0603	Std	Std
0	C7	0.01uF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
2	C8, C9	22uF	Capacitor, Ceramic, 10V, X5R, 20%	1210	GRM32ER61A226KE20	Murata
2	J1, J2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25""	ED555/2DS	OST
2	JP1, JP2	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	1.5uH	Inductor, Power, 21.45mOhm, 4.6A, ±20%	0.157 x 0.157 inch	XAL4020-152ME	Coilcraft
1	R1, R2	open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	7.68k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	182k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	11.8k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	51.1	Resistor, Chip, 1/16W, 1%	0603	Std	Std
5	TP1, TP3, TP4, TP5, TP6, TP8	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
3	TP2, TP7	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	TPS54319RTE	IC, DC-DC Converter, 3-6 V, 3 A	QFN-16	TPS54319RTE	TI
2	–		Shunt, 100-mil, Black	0.100	929950-00	3M
1			PCB, 2.5" x 2.5" x 0.062"	2.5" x 2.5" x 0.062"	HPA526	Any

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 3.5 V to 60 V and the output voltage range of 1.8 V to 5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 55°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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