User's Guide
SLVU263–August 2008

TPS54231EVM-372 2-A, SWIFT™ Regulator Evaluation Module

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1 Introduction

This user's guide contains background information for the TPS54231 as well as support documentation for the TPS54231EVM-372 evaluation module (HPA372). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54231EVM-372.

1.1 Background

The TPS54231 dc/dc converter is designed to provide up to a 2 A output from an input voltage source of 3.5 V to 28 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54231 regulator. The switching frequency is internally set at a nominal 570 kHz. The high-side MOSFET is incorporated inside the TPS54231 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS54231 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54231 provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 30 V for the TPS54231EVM-372.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54231EVM-372	VIN = 7 V to 28 V	0 A to 2 A

1.2 Performance Specification Summary

A summary of the TPS54231EVM-372 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 15 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54231EVM-372 is designed and tested for V_{IN} = 7 V to 28 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54231EVM-372 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			7	15	28	V
Output voltage set point				3.3		V
Output current range	V_{IN} = 7 V to 28 V		0		2	A
Line regulation	I_O = 1 A, V_{IN} = 7 V to 28 V			±0.15%		
Load regulation	V_{IN} = 15 V, I_O = 0 A to 2 A			±0.15%		
Load transient response	I_O = 0.5 A to 1.5 A	Voltage change		–100		mV
		Recovery time		150		µs
	I_O = 1.5 A to 0.5 A	Voltage change		100		mV
		Recovery time		150		µs
Loop bandwidth	V_{IN} = 15 V, I_O = 1 A			27		kHz
Phase margin	V_{IN} = 15 V , I_O = 1 A			55		°
Input ripple voltage	I_O = 2 A			125		mVpp
Output ripple voltage	I_O = 2 A			5		mVpp
Output rise time				6		ms
Operating frequency				570		kHz
Maximum efficiency	TPS54231EVM-372, V_{IN} = 7 V, I_O = 0.5 A			92.7%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54231. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R_6. Changing the value of R_6 can change the output voltage above 0.8 V. The value of R_6 for a specific output voltage can be calculated using Equation 1.

$$R_6 = 10.2\ k\Omega \times \frac{0.8\ V}{V_{OUT} - 0.8\ V} \quad (1)$$

Table 3 lists the R_6 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 130 ns, and the maximum duty cycle is less than 91%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Output Voltages Available

Output Voltage (V)	R_6 Value (kΩ)
1.8	8.25
2.5	4.75
3.3	3.24
5	1.96

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54231EVM-372 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The TPS54231EVM-372 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 2 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J4 through a pair of 20 AWG wires. The maximum load current capability must be 2 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP5 is used to monitor the output voltage with TP6 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range)
J2	2-pin header for enable. Connect EN to ground to disable, open to enable.
J3	2-pin header for slow start monitor and GND.
J4	V_{OUT}, 3.3 V at 2 A maximum
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	PH test point
TP4	Test point between voltage divider network and output. Used for loop response measurements.
TP5	Output voltage test point at OUT connector
TP6	GND test point at OUT connector

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.5 A - 1 A and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPS54231EVM-372 at an ambient temperature of 25°C.

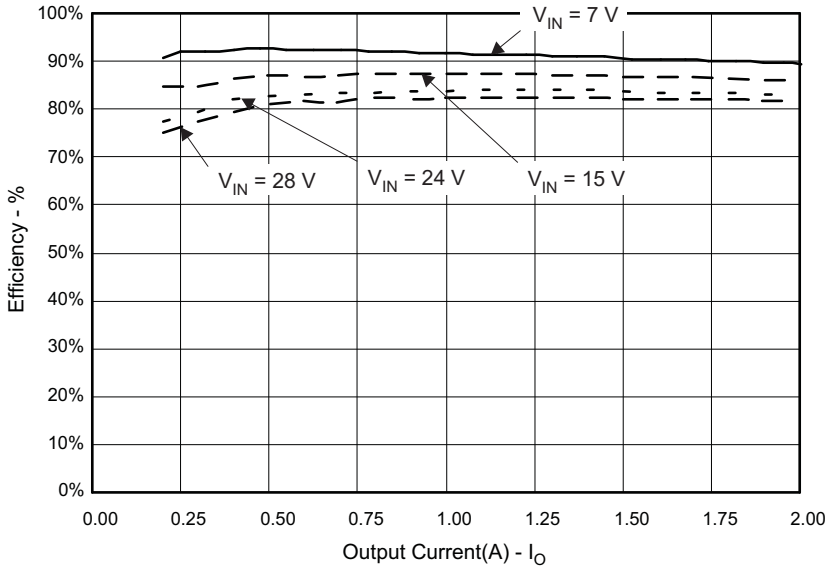


Figure 1. TPS54231EVM-372 Efficiency

Figure 2 shows the efficiency for the TPS54231EVM-372 at lower output currents between 0.02 A and 0.20 A at an ambient temperature of 25°C.

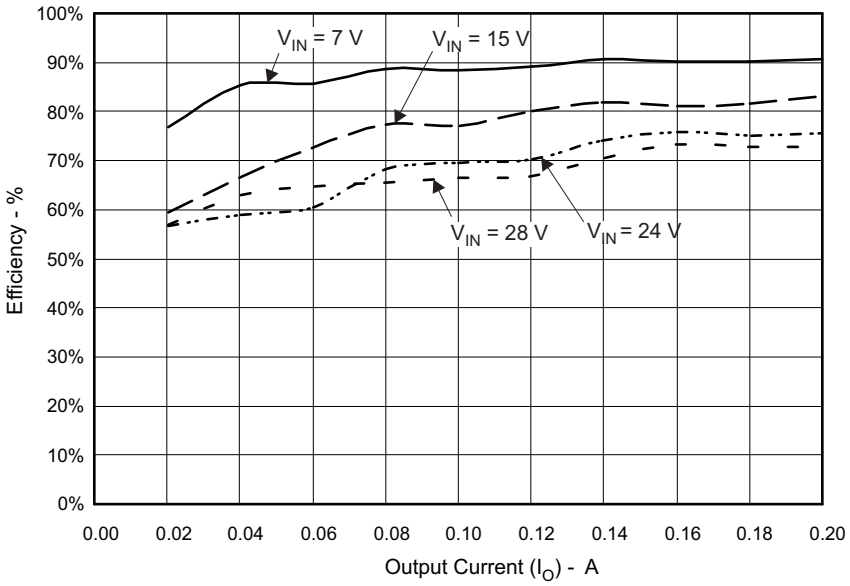


Figure 2. TPS54231EVM-372 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

The load regulation for the TPS54231EVM-372 is shown in Figure 3.

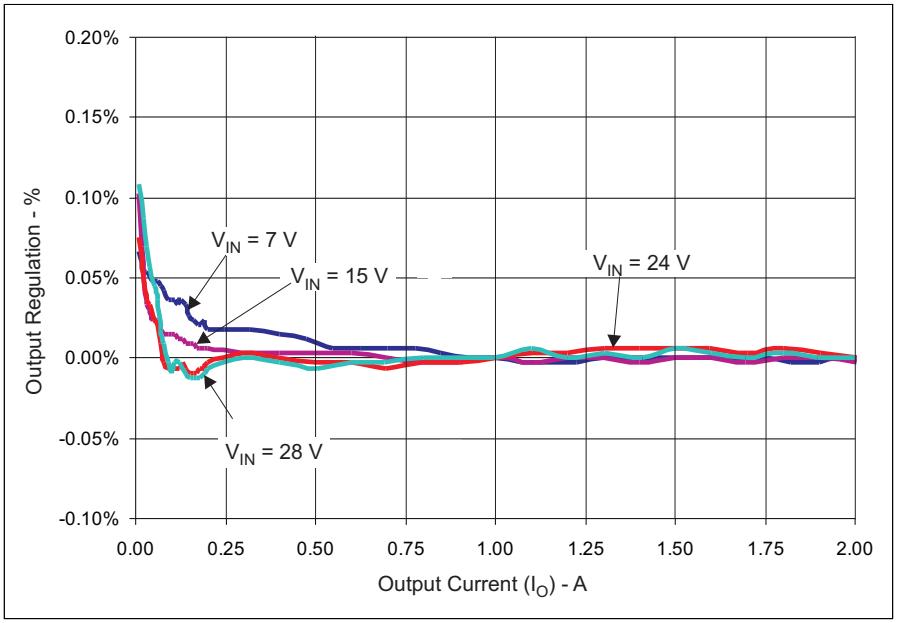


Figure 3. TPS54231EVM-372 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

The line regulation for the TPS54231EVM-372 is shown in Figure 4.

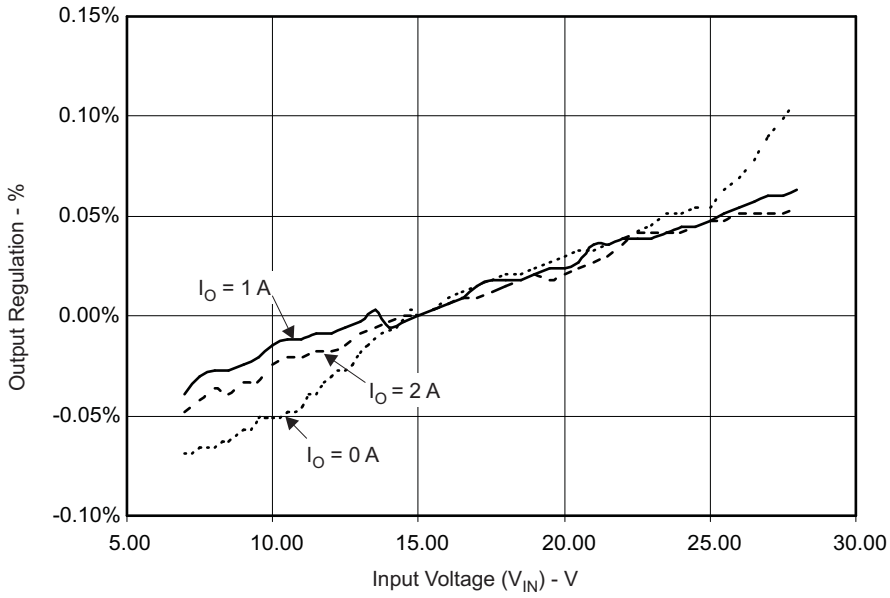


Figure 4. TPS54231EVM-372 Line Regulation

2.5 Load Transients

The TPS54231EVM-372 response to load transients is shown in Figure 5. The current step is from 25% to 75% of maximum rated load at 15V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

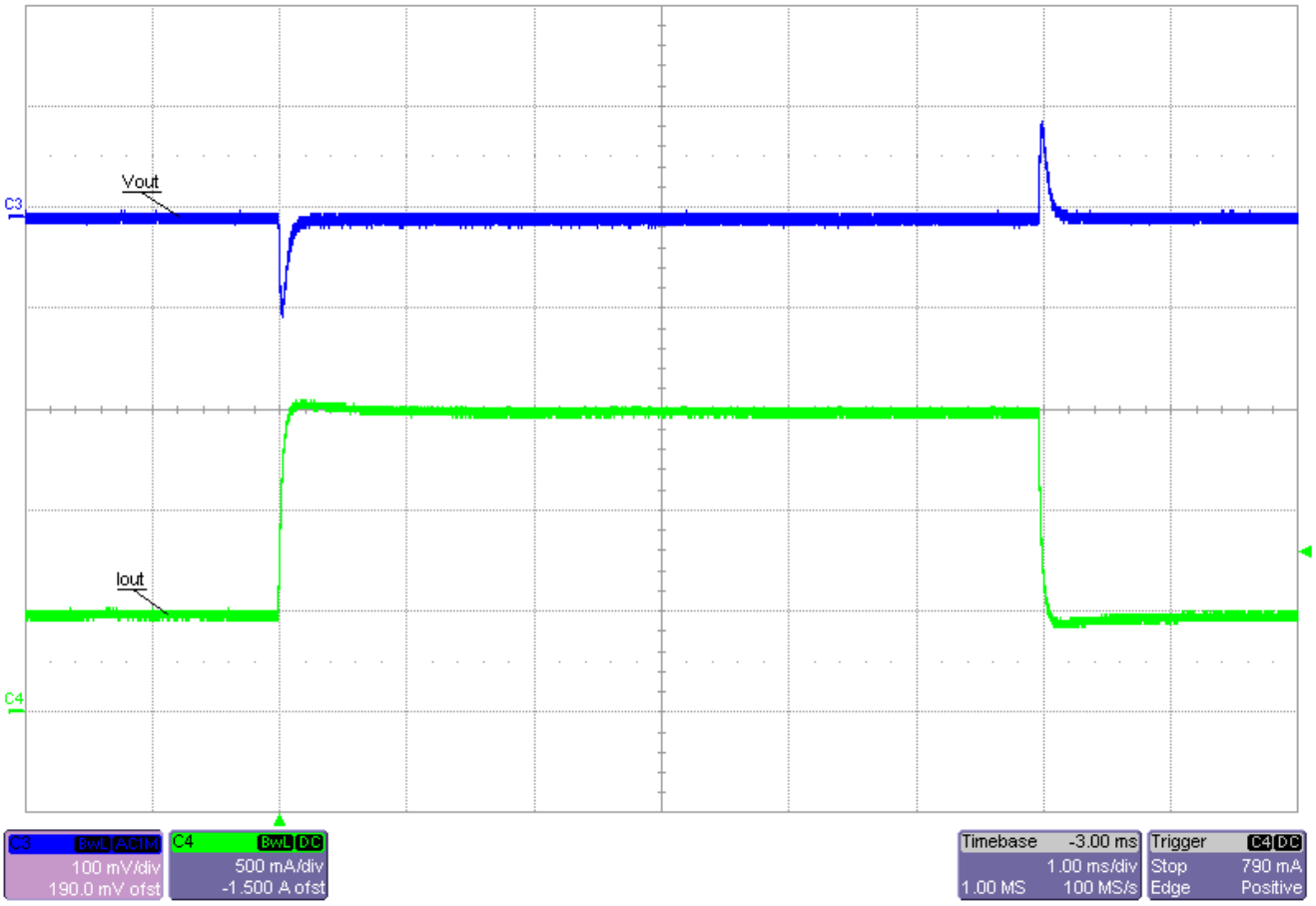


Figure 5. TPS54231EVM-372 Transient Response

2.6 Loop Characteristics

The TPS54231EVM-372 loop-response characteristics are shown in Figure 6 . Gain and phase plots are shown for V_{IN} voltage of 15 V. Load current for the measurement is 1 A.

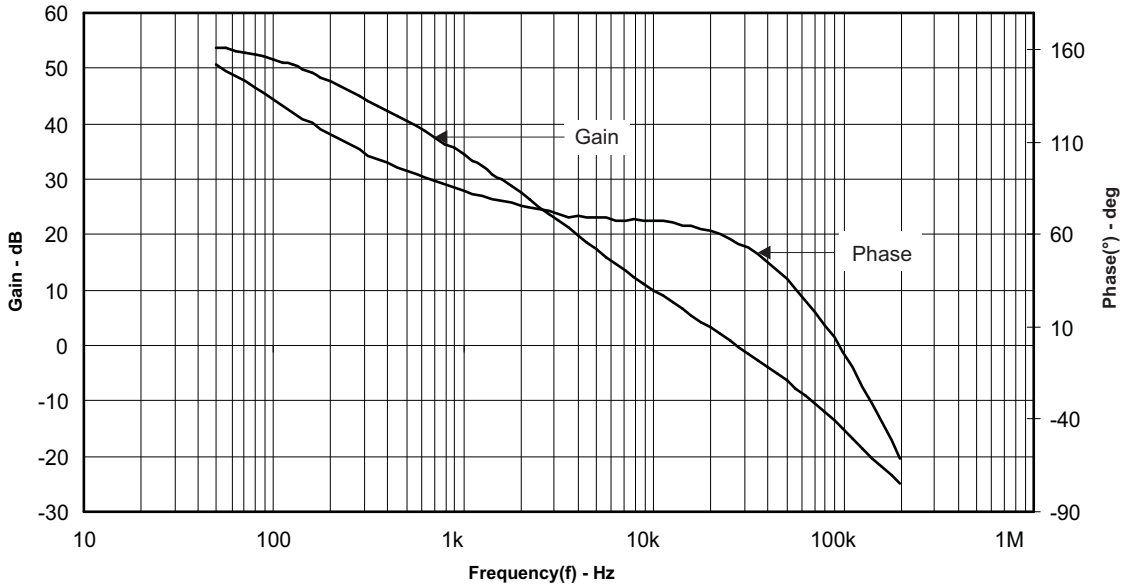


Figure 6. TPS54231EVM-372 Loop Response

2.7 Output Voltage Ripple

The TPS54231EVM-372 output voltage ripple is shown in Figure 7 . The output current is the rated full load of 2 A and V_{IN} = 15 V. The ripple voltage is measured directly across the output capacitors.

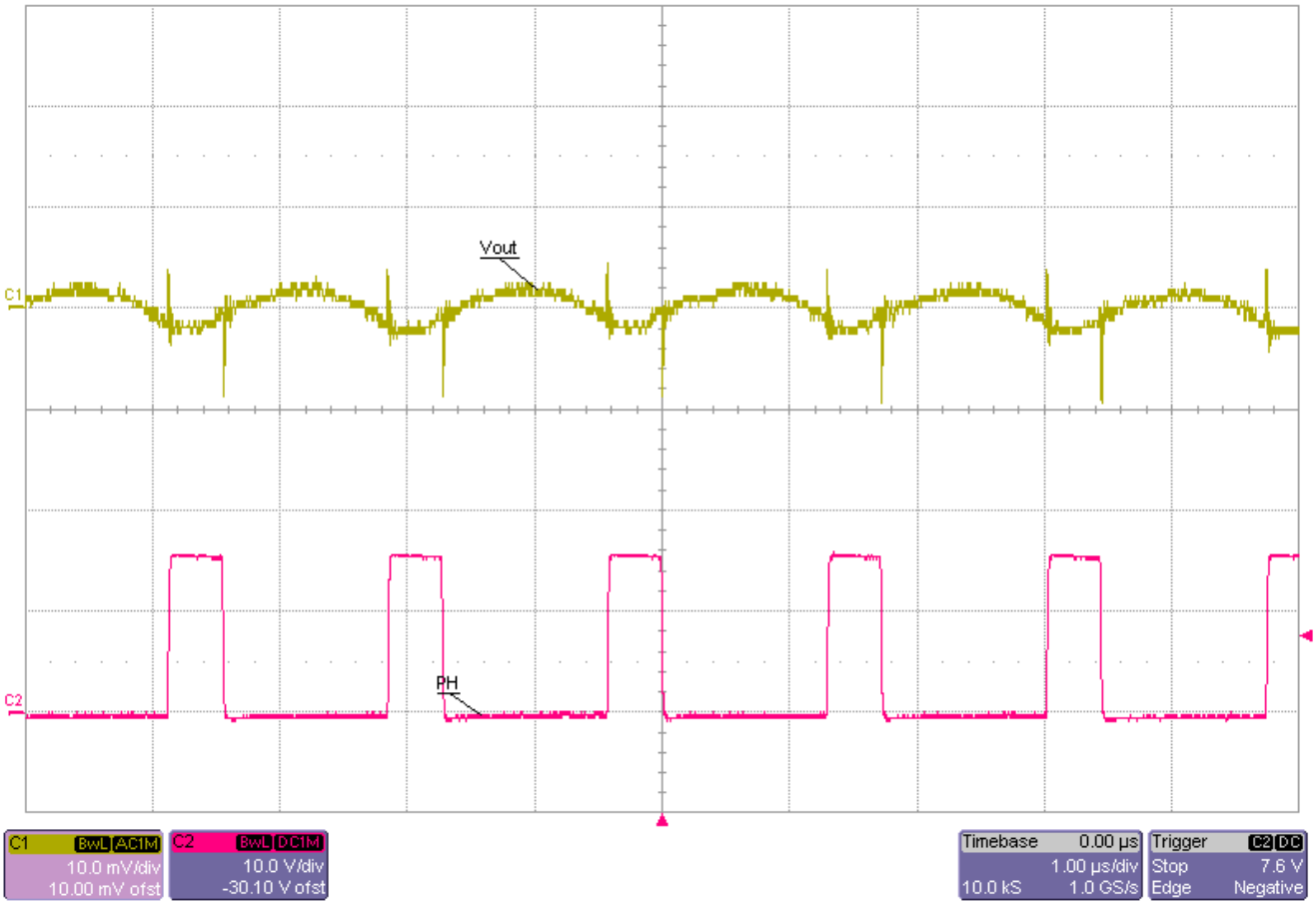


Figure 7. TPS54231EVM-372 Output Ripple

2.8 Input Voltage Ripple

The TPS54231EVM-372 input voltage ripple is shown in Figure 8 . The output current is the rated full load of 2 A and V_{IN} = 15 V. The ripple voltage is measured directly across the input capacitors.

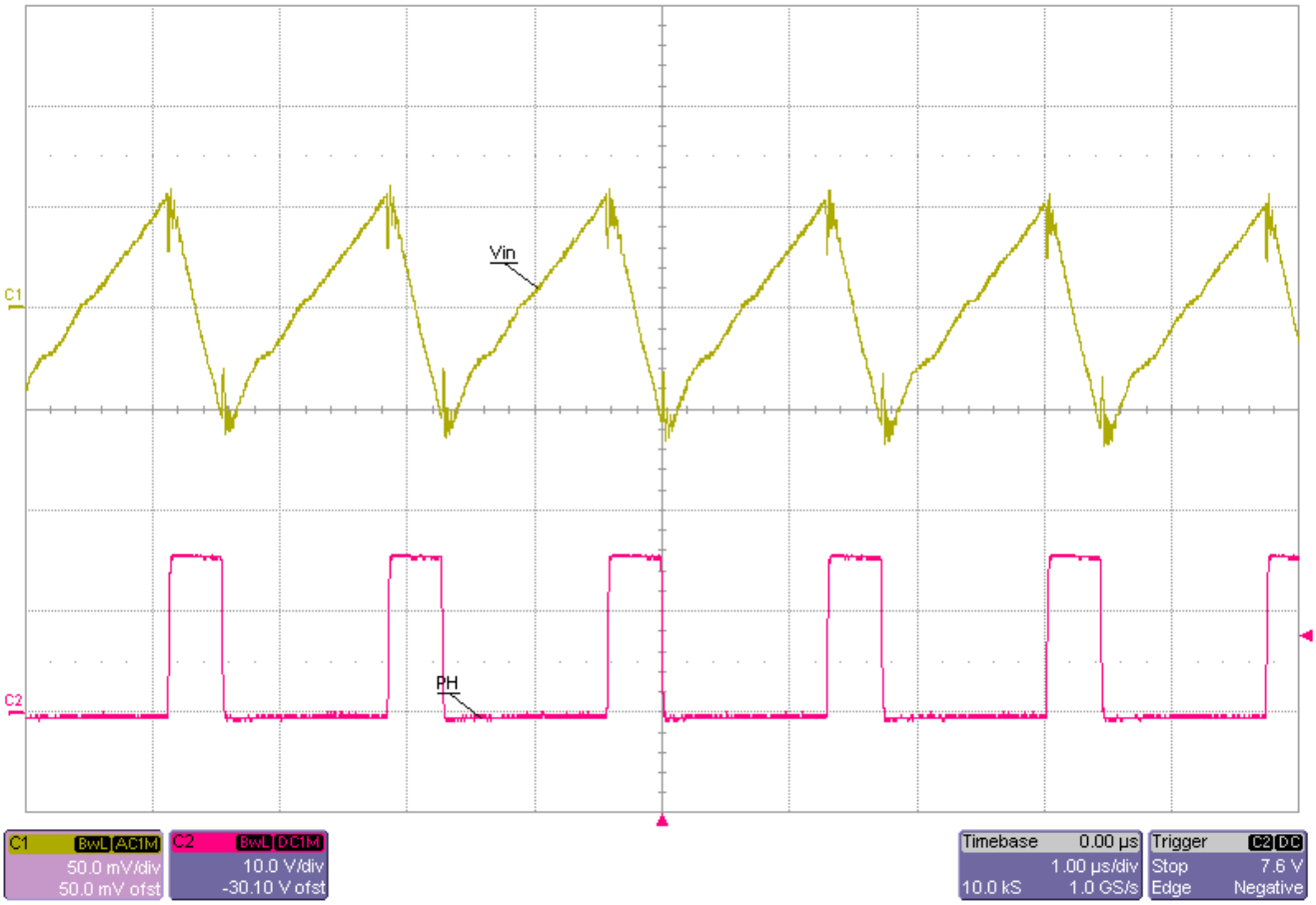


Figure 8. TPS54231EVM-372 Input Ripple

2.9 Powering Up

The start-up waveforms are shown in Figure 9 and Figure 10. In Figure 9, the top trace shows V_{IN}, and the bottom trace shows V_{OUT}. In Figure 10 , the top trace shows EN (enable) whereas the bottom trace shows V_{OUT}. In Figure 10, the input voltage is initially applied and the output is inhibited by using a jumper at J2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage of 1.25 V, the start-up sequence begins and the internal reference voltage begins to ramp up at the internally set rate toward 0.8 V and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 15 V and there is no load.

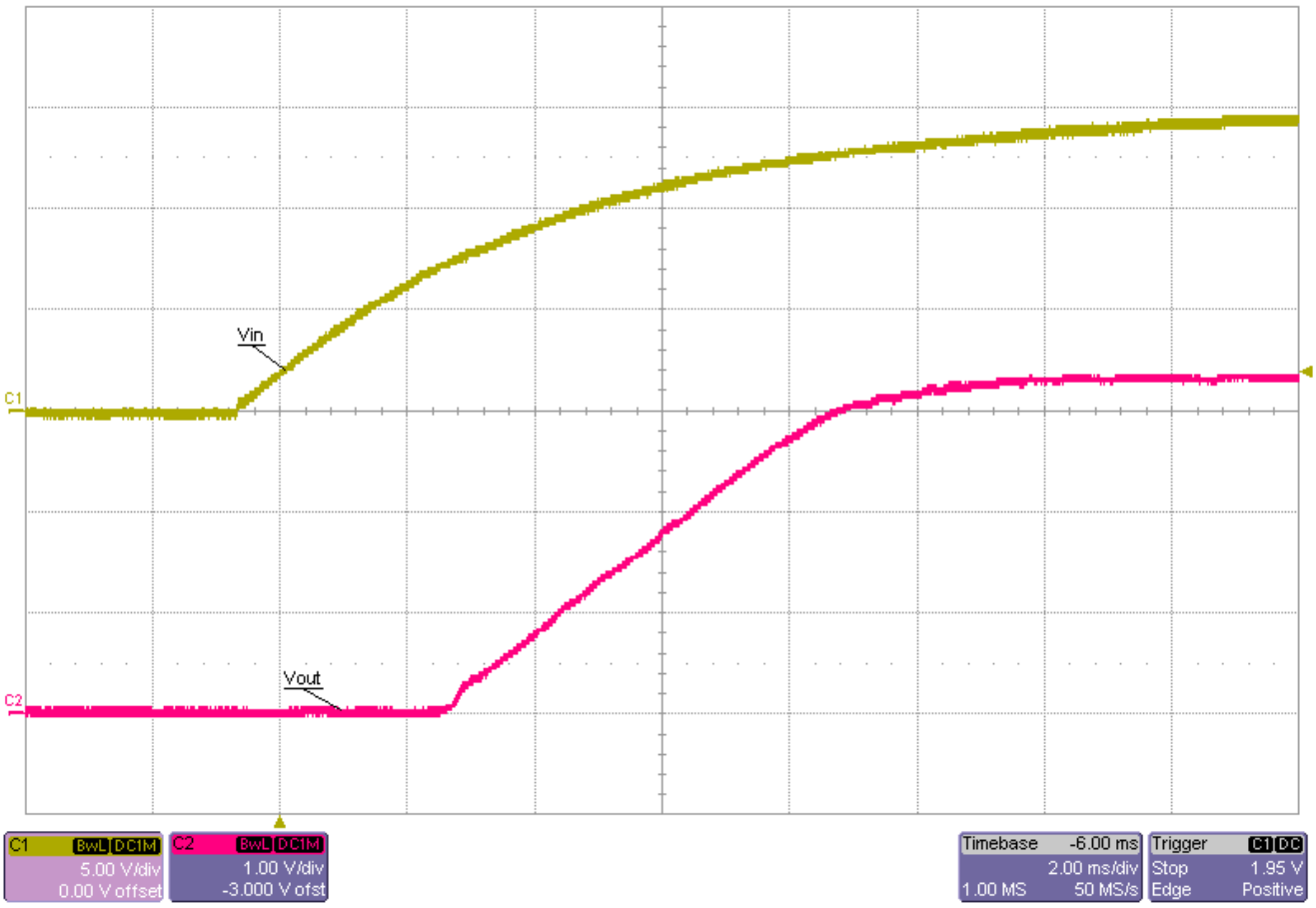


Figure 9. TPS54231EVM-372 Start-Up Relative to V_{IN}

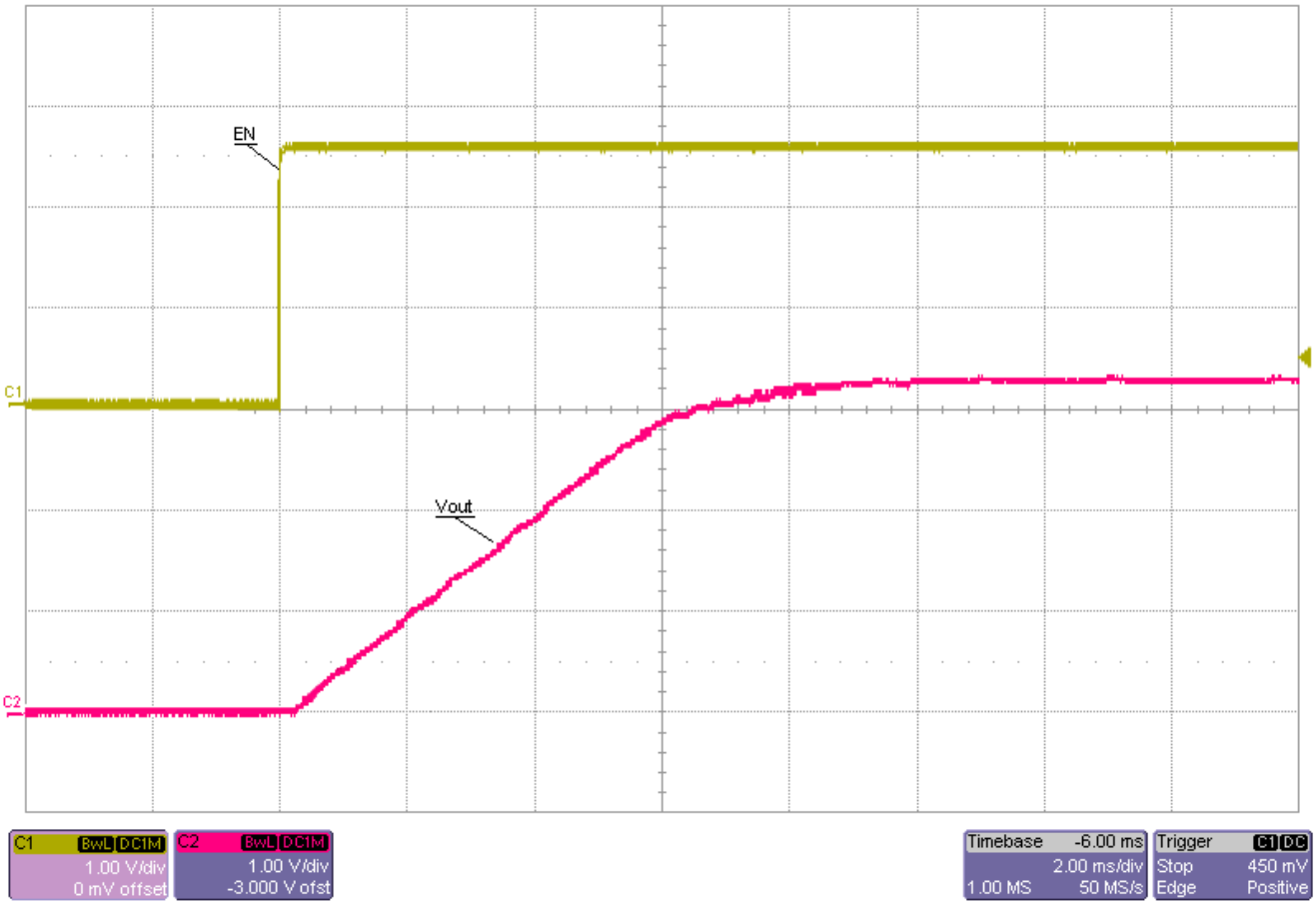


Figure 10. TPS54231EVM-372 Start-up Relative to Enable

2.10 Eco-mode™ Operation

At light load currents, the TPS54231 is designed to operate in pulse skipping Eco-mode™. When the peak inductor current is lower than 100 mA typical, the device enters Eco-mode™.

Figure 11 shows Eco-mode operation, channel 1(C1) shows the output voltage while channel 2(C2) shows the switching node (PH).

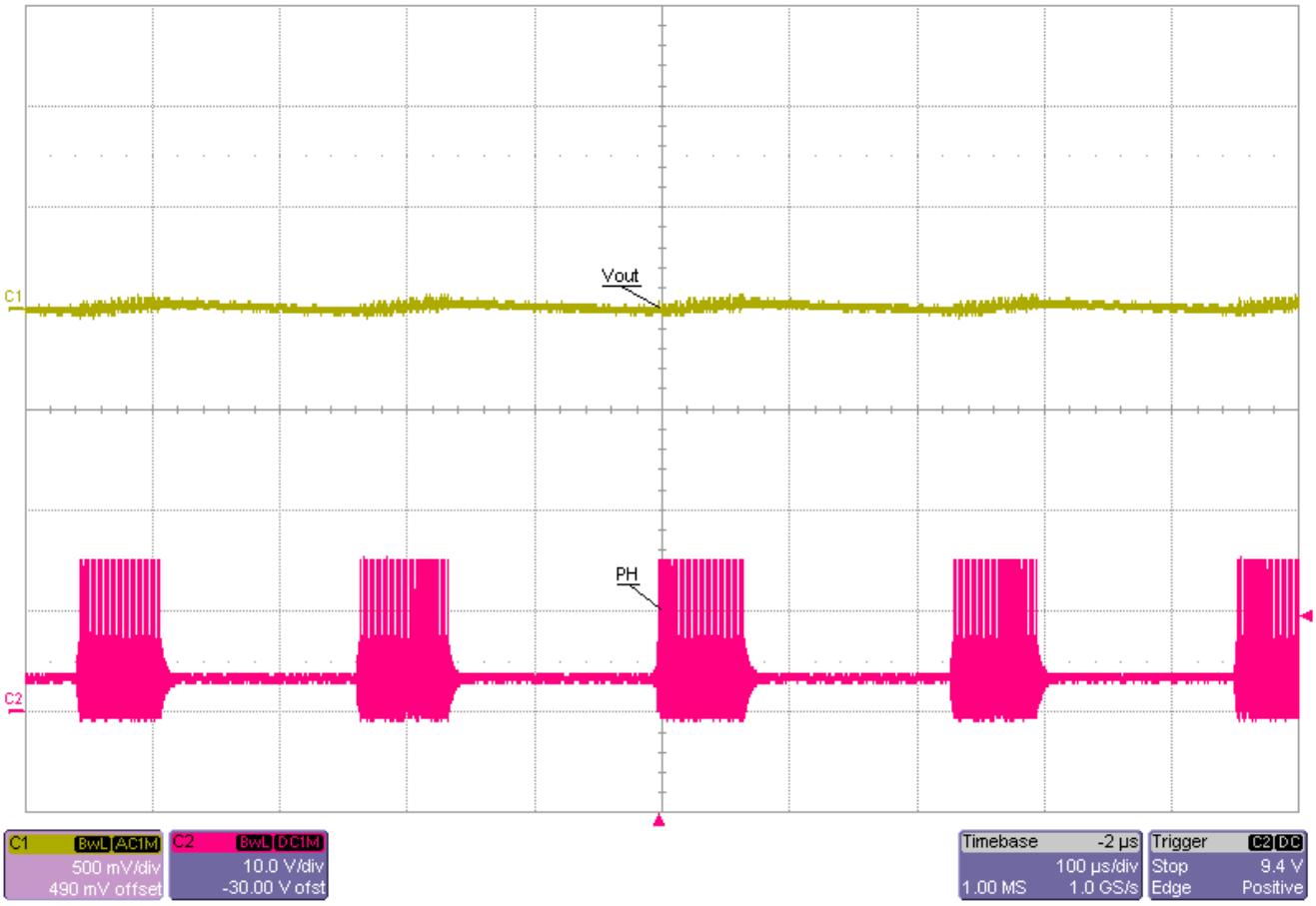


Figure 11. TPS54231EVM–372 Eco–mode™ Operation

2.11 Thermal Characteristics

This section shows a thermal image of the TPS54231EVM-372 running at 28 V input and 2 A load. These are the worst case conditions for maximum power loss. There is no air flow and the ambient temperature is 25°C. The peak temperature of the IC (85.8°C) is well below the maximum recommended operating condition listed in the datasheet of 150°C.

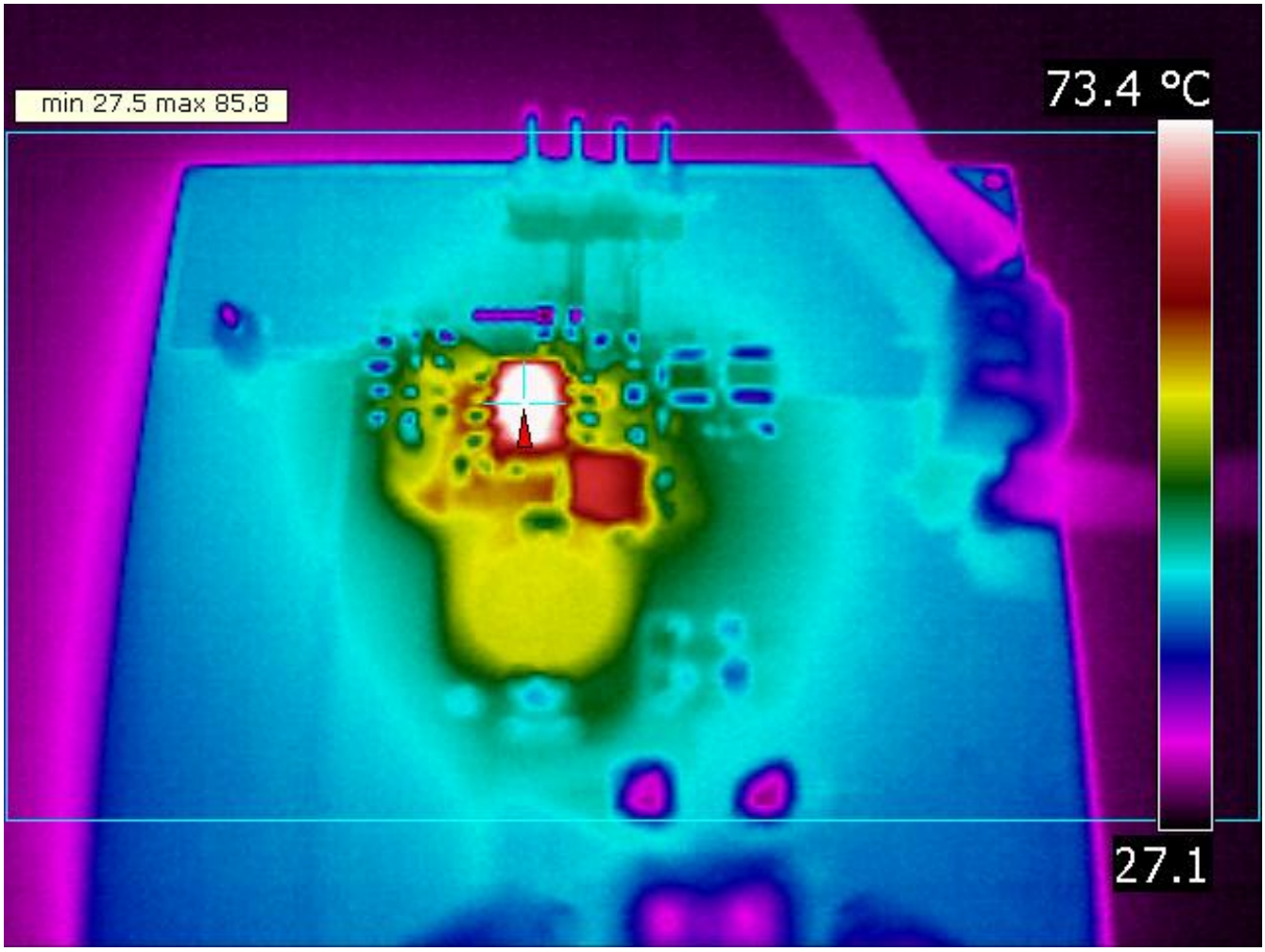


Figure 12. TPS54231EVM-372 Thermal Image

3 Board Layout

This section provides a description of the TPS54231EVM-372, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54231EVM-372 is shown in Figure 13 through Figure 15. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54231 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including ten vias directly under the TPS54231 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C1, C2, and C3) and bootstrap capacitor (C4) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace past the output capacitor C10. For the TPS54231, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply.

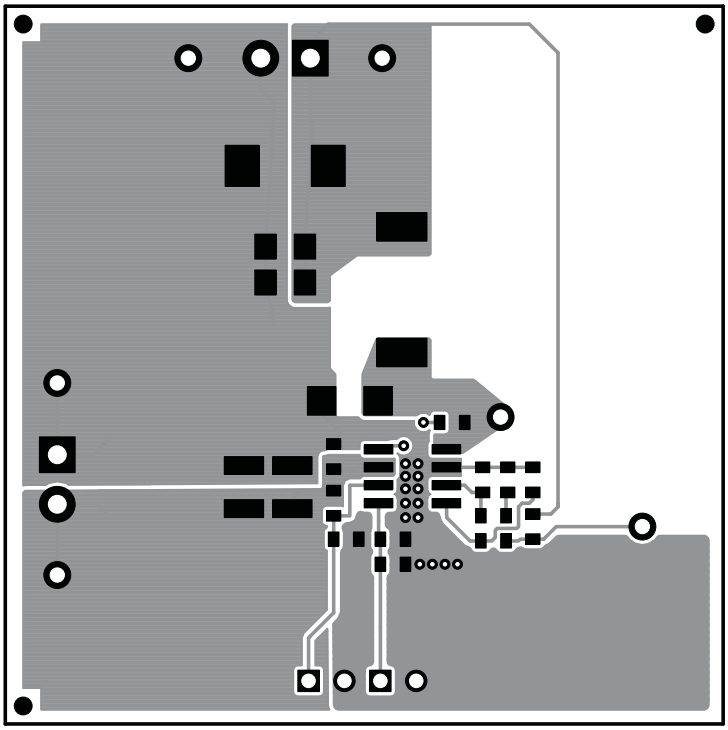


Figure 13. TPS54231EVM-372 Top-Side Layout

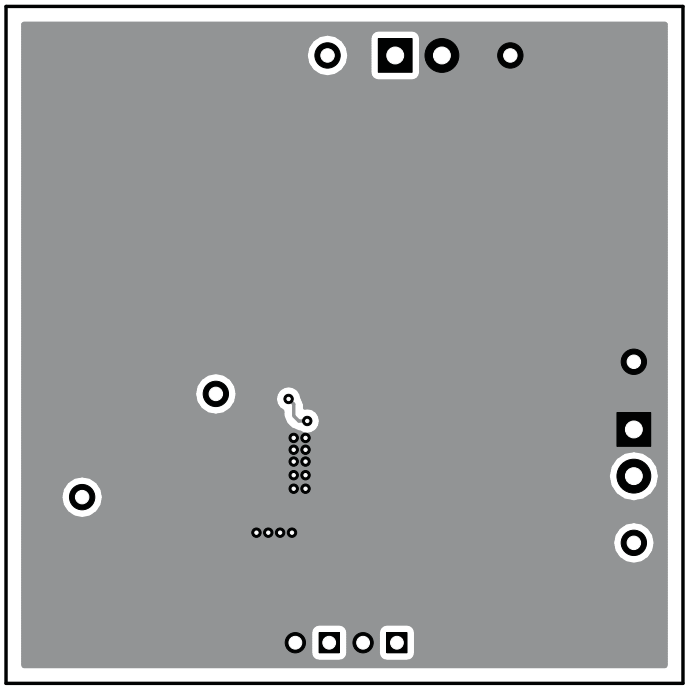


Figure 14. TPS54231EVM-372 Bottom-Side Layout

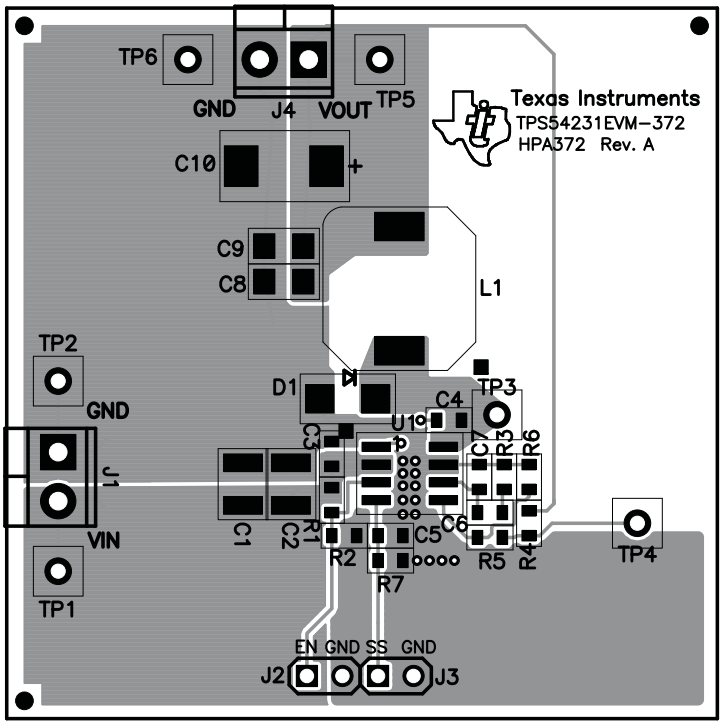


Figure 15. TPS54231EVM-372 Top-Side Assembly

3.2 Estimated Circuit Area

The estimated printed circuit board area for the components used in this design is 0.68 in^2. This area does not include test point or connectors.

4 Schematic and Bill of Materials

This section presents the TPS54231EVM-372 schematic and bill of materials.

4.1 Schematic

Figure 16 is the schematic for the TPS54231EVM-372.

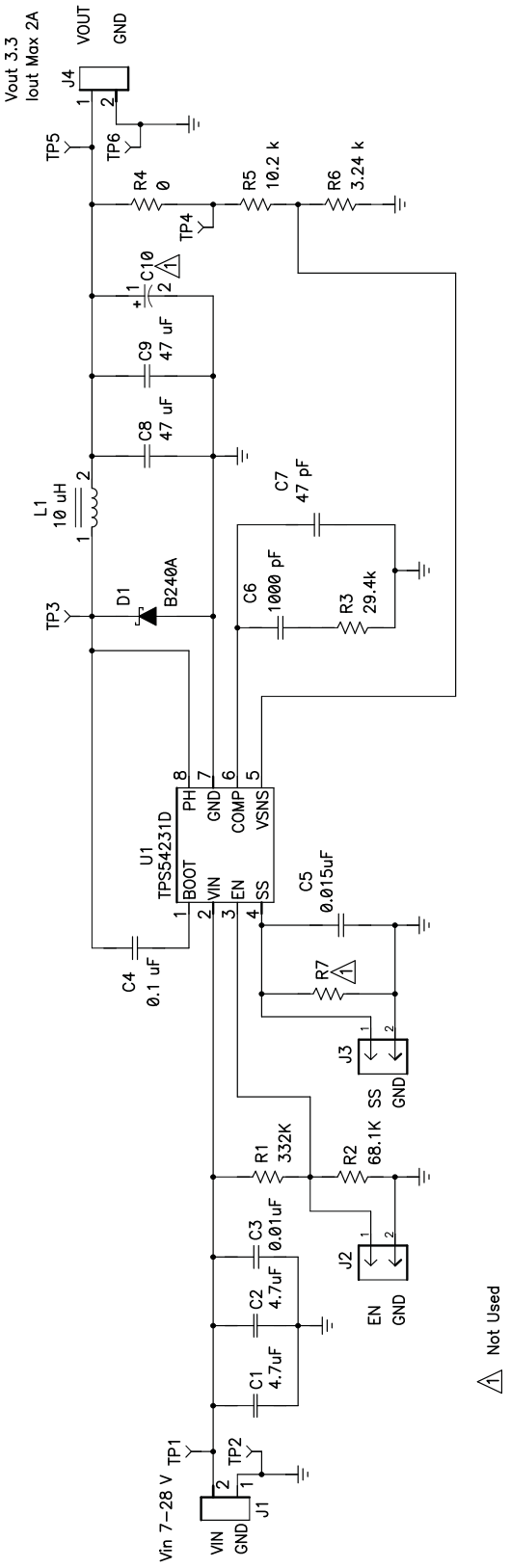


Figure 16. TPS54231EVM-372 Schematic

4.2 Bill of Materials

Table 5 presents the bill of materials for the TPS54231EVM-372.

Table 5. TPS54231EVM-372 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C2	4.7 µF	Capacitor, Ceramic, 50V, X7R, 20%	1210	Std	Std
0	C10	Open		7343(D)	Std	Std
1	C3	0.01 µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C4	0.1 µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C5	0.015 µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C6	1000 pF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C7	47 pF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
2	C8, C9	47 µF	Capacitor, Ceramic, 6.3, X5R, 20%	1206	C3216X5R0J476MT	TDK
1	D1	B240A	Diode, Schottky, 2A, 40V	SMA	B240A	Diodes Inc
2	J1, J4	ED1514	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 × 0.25 inch	ED1514	OST
2	J2, J3	PTC36SAAN	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
1	L1	10 µH	Inductor, SMT, 3.9A, 35 mΩ	0.402 × 0.394 inch	MSS1038-103NL	Coilcraft
1	R1	332k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	68.1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	29.4k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	10.2k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	3.24k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R7	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	TP1, TP3, TP5	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 inch	5000	Keystone
3	TP2, TP4, TP6	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 inch	5001	Keystone
1	U1	TPS54231D	IC, DC-DC Converter, 28V, 2A	SO-8	TPS54231D	TI
1	—		PCB	2.0" x 2.0" x 0.062"	HPA372	Any
1	—		Shunt, 100-mil, Black	0.100	929950-00	3M

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range and the output current range specified in Table 1.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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