

# **TPS54116-Q1EVM-830 4-A, 1-A, SWIFT™ Regulator Evaluation Module**

This user's guide contains information for the TPS54116-Q1EVM-830 evaluation module (PWR830) as well as for the TPS54116-Q1 dc/dc converter. Also included are the performance specifications, the schematic, and the bill of materials for the TPS54116-Q1EVM-830.

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## 1 Introduction

### 1.1 Background

The TPS54116-Q1 dc/dc converter is a synchronous buck converter designed to provide up to a 4-A output along with an integrated 1-A source/sink LDO for DDR memory termination. The input ( $V_{IN}$ ) is rated for 2.95 V to 6 V. The TPS54116-Q1 uses a fixed frequency current mode control for the 4-A buck regulator. Rated input voltage and output current range for the evaluation module are given in [Table 1](#). This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54116-Q1 regulator. An external divider allows for an adjustable output voltage. Additionally, the TPS54116-Q1 provides adjustable slow start and undervoltage lockout inputs and a power good output.

**Table 1. Input Voltage and Output Current Summary**

| EVM                | Input Voltage Range                       | $V_{DD}$ Output Current Range | $V_{TT}$ Output Current Range |
|--------------------|-------------------------------------------|-------------------------------|-------------------------------|
| TPS54116-Q1EVM-830 | $V_{IN} = 2.95 \text{ V to } 6 \text{ V}$ | 0 A to 4 A                    | -1 A to 1 A                   |

### 1.2 Performance Specification Summary

A summary of the TPS54116-Q1EVM-830 performance specifications is provided in [Table 2](#). Specifications are given for an input voltage of  $V_{IN} = 5 \text{ V}$ , a  $V_{DD}$  output voltage of 1.5 V and a  $V_{TT}$  output voltage of 0.75 V, unless otherwise specified. The TPS54116-Q1EVM-830 is designed and tested for  $V_{IN} = 2.95 \text{ V to } 6 \text{ V}$ . The ambient temperature is 25°C for all measurements, unless otherwise noted.

**Table 2. TPS54116-Q1EVM-830 Performance Specification Summary**

| Specification                     | Test Conditions                                                                                          | MIN            | TYP    | MAX | Unit   |
|-----------------------------------|----------------------------------------------------------------------------------------------------------|----------------|--------|-----|--------|
| $V_{IN}$ voltage range            |                                                                                                          | 2.95           | 5      | 6   | V      |
| $V_{IN}$ start voltage            |                                                                                                          |                |        |     | V      |
| $V_{IN}$ stop voltage             |                                                                                                          |                |        |     | V      |
| $V_{DD}$ output voltage set point |                                                                                                          |                | 1.5    |     | V      |
| $V_{TT}$ output voltage set point |                                                                                                          |                | 0.75   |     | V      |
| $V_{DD}$ output current range     | $V_{IN} = 2.95 \text{ V to } 6 \text{ V}$                                                                | 0              |        | 4   | A      |
| $V_{TT}$ output current range     | $V_{LDOIN} = V_{DD} = 1.5 \text{ V}$                                                                     | -1             |        | 1   | A      |
| $V_{DD}$ line regulation          | $I_O = 2 \text{ A}$ , $V_{IN} = 2.95 \text{ V to } 6 \text{ V}$                                          |                | ±0.05% |     |        |
| $V_{TT}$ line regulation          | $I_O = 0.5 \text{ A}$ , $V_{IN} = 2.95 \text{ V to } 6 \text{ V}$ , $V_{LDOIN} = V_{DD} = 1.5 \text{ V}$ |                | ±0.2%  |     |        |
| $V_{DD}$ load regulation          | $V_{IN} = 5 \text{ V}$ , $I_O = 0 \text{ A to } 4 \text{ A}$                                             |                | ±0.05% |     |        |
| $V_{TT}$ load regulation          | $V_{LDOIN} = V_{DD} = 1.5 \text{ V}$ , $V_{IN} = 5 \text{ V}$ , $I_O = 0 \text{ A to } 1 \text{ A}$      |                | ±1.3%  |     |        |
| $V_{DD}$ load transient response  | $I_O = 1 \text{ A to } 3 \text{ A}$                                                                      | Voltage change |        | -50 | mV     |
|                                   |                                                                                                          | Recovery time  |        | 100 | µs     |
|                                   | $I_O = 3 \text{ A to } 1 \text{ A}$                                                                      | Voltage change |        | 50  | mV     |
|                                   |                                                                                                          | Recovery time  |        | 100 | µs     |
| Loop bandwidth                    | $V_{IN} = 12 \text{ V}$ , $I_O = 6 \text{ A}$                                                            |                | 55     |     | kHz    |
| Phase margin                      | $V_{IN} = 12 \text{ V}$ , $I_O = 6 \text{ A}$                                                            |                | 64     |     | degree |
| Input ripple voltage              | $V_{DD}$ output current= 3 A, $V_{TT}$ output current= 1 A,                                              |                | 80     |     | mVPP   |
| $V_{DD}$ output ripple voltage    | $I_O = 4 \text{ A}$                                                                                      |                | 10     |     | mVPP   |
| Operating frequency               |                                                                                                          |                | 2000   |     | kHz    |
| $V_{DD}$ maximum efficiency       | TPS54116-Q1EVM-830, $V_{IN} = 5 \text{ V}$ , $I_O = 0.7 \text{ A}$                                       |                | 89.8%  |     |        |

## 1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54116-Q1. Some modifications can be made to this module.

### 1.3.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R14 ( $R_{(TOP)}$ ) and R15 ( $R_{(BOT)}$ ). R15 is fixed at 10.0 k $\Omega$ . To change the output voltage of the EVM, it is necessary to change the value of resistor R14. Changing the value of R14 can change the output voltage above the 0.6 V reference voltage  $V_{REF}$ . The value of R14 for a specific output voltage can be calculated using [Equation 1](#).

$$R_{(BOT)} = \frac{R_{(TOP)} \times V_{REF}}{(V_{OUT} - V_{REF})} \quad (1)$$

## 2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54116-Q1EVM-830 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

### 2.1 Input/Output Connections

The TPS54116-Q1EVM-830 is provided with input/output connectors and test points as shown in [Table 3](#). A power supply capable of supplying greater than 3 A must be connected to J1 through a pair of 20-AWG wires or better. The load must be connected to J2 through a pair of 20-AWG wires or better. The maximum load current capability is 12 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the  $V_{IN}$  input voltages with TP2 providing a convenient ground reference. TP9 is used to monitor the output voltage with TP10 as the ground reference.

**Table 3. EVM Connectors and Test Points**

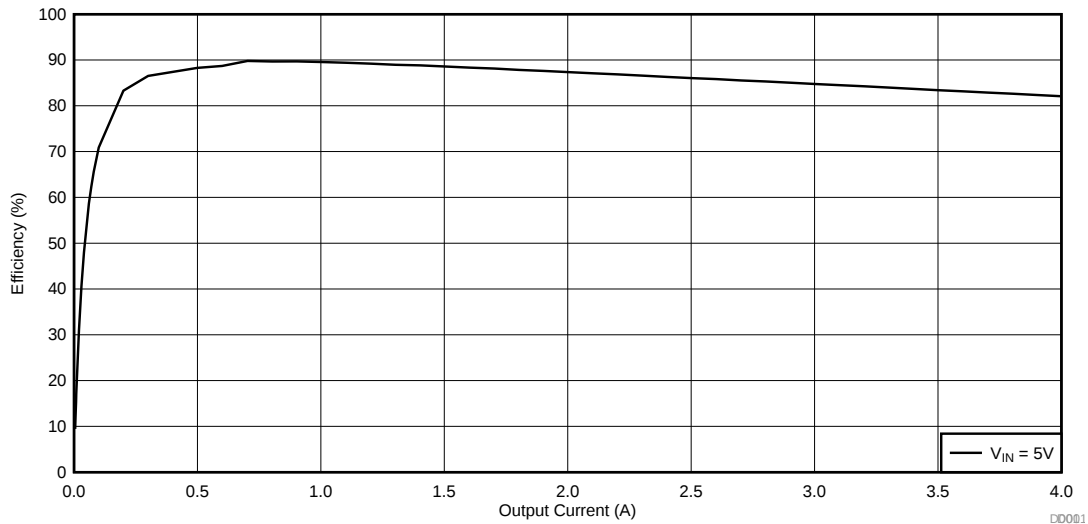
| Reference Designator | Function                                                                                                        |
|----------------------|-----------------------------------------------------------------------------------------------------------------|
| J1                   | $V_{IN}$ input voltage connector. $V_{IN}$ and PGND.                                                            |
| J2                   | $V_{DD}$ output voltage connector. $V_{DD}$ and PGND.                                                           |
| J3                   | $V_{TT}$ output voltage connector. $V_{TT}$ and PGND.                                                           |
| J4                   | 2-pin header, ENSW and PGND. Connect ENSW to ground to disable, open to enable $V_{DD}$                         |
| J5                   | 2-pin header, ENSW and ENLDO. Connect ENSW to ENLDO to have a common enable.                                    |
| J6                   | 2-pin header, ENLDO and PGND. Connect ENLDO to ground to disable, open to enable $V_{TT}$                       |
| J7                   | 2-pin header, VTTREF and PGND.                                                                                  |
| J8                   | 3-pin header, $V_{IN}$ , U2–6 input voltage and PGND. Use to select input supply for source/sink built in load. |
| J9                   | 2-pin header, CLK and PGND. Use to input clock signal for source/sink built in load.                            |
| TP1                  | $V_{IN}$ test point.                                                                                            |
| TP2                  | PGND test point at VIN connector.                                                                               |
| TP3                  | Slow Start (SS/TRK) test point.                                                                                 |
| TP4                  | PGOOD test point.                                                                                               |
| TP5                  | External sync clock input.                                                                                      |
| TP6                  | SW node test point.                                                                                             |
| TP7                  | VTTSENSE test point.                                                                                            |
| TP8                  | $V_{DD}$ output test point.                                                                                     |
| TP9                  | PGND test point.                                                                                                |
| TP10                 | Test point between voltage divider network and output. Used for loop response measurements.                     |
| TP11                 | $V_{DD}$ output test point.                                                                                     |
| TP12                 | PGND test point.                                                                                                |
| TP13                 | OUTA test point.                                                                                                |
| TP14                 | OUTB test point.                                                                                                |

**Table 3. EVM Connectors and Test Points (continued)**

| Reference Designator | Function         |
|----------------------|------------------|
| TP15                 | AGND test point. |

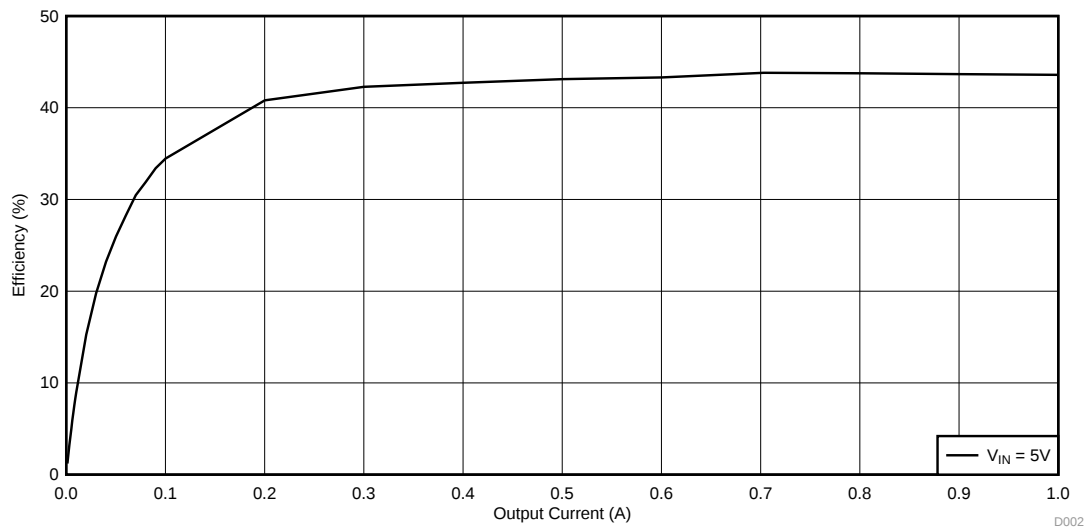
## 2.2 Efficiency

The efficiency of the  $V_{DD}$  output peaks at a load current of about 0.7 A and then decreases as the load current increases toward full load. Figure 1 shows the efficiency for the TPS54116-Q1EVM-830  $V_{DD}$  output at an ambient temperature of 25°C.



**Figure 1. TPS54116-Q1EVM-830  $V_{DD}$  Output Efficiency**

Figure 2 shows the efficiency for the TPS54116-Q1EVM-830  $V_{TT}$  output. The ambient temperature is 25°C.



**Figure 2. TPS54116-Q1EVM-830  $V_{TT}$  Output Efficiency**

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

## 2.3 Output Voltage Load Regulation

Figure 3 and Figure 4 show the load regulation for the TPS54116-Q1EVM-830  $V_{DD}$  and  $V_{TT}$  outputs.

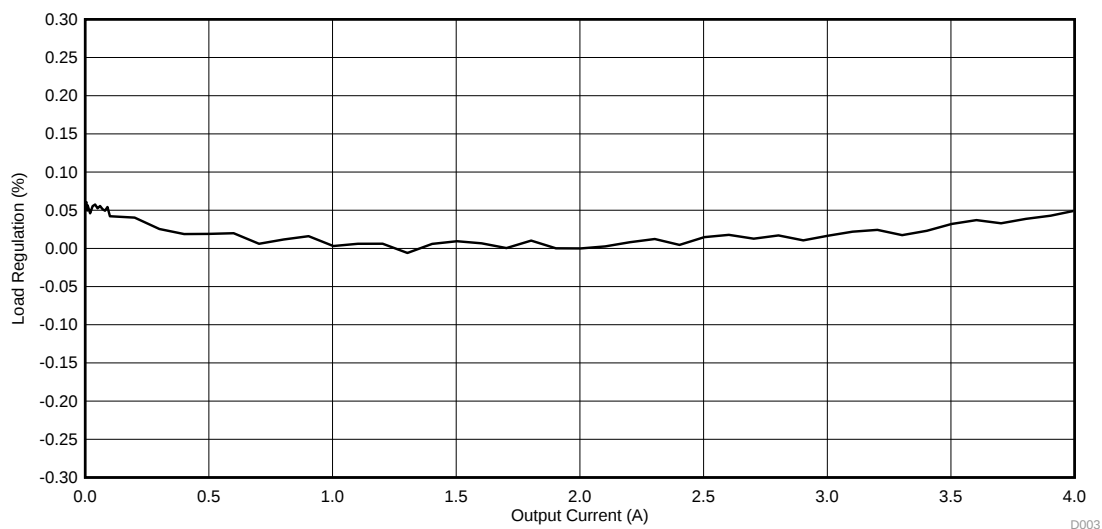


Figure 3. TPS54116-Q1EVM-830  $V_{DD}$  Output Load Regulation,  $V_{IN} = 5\text{ V}$

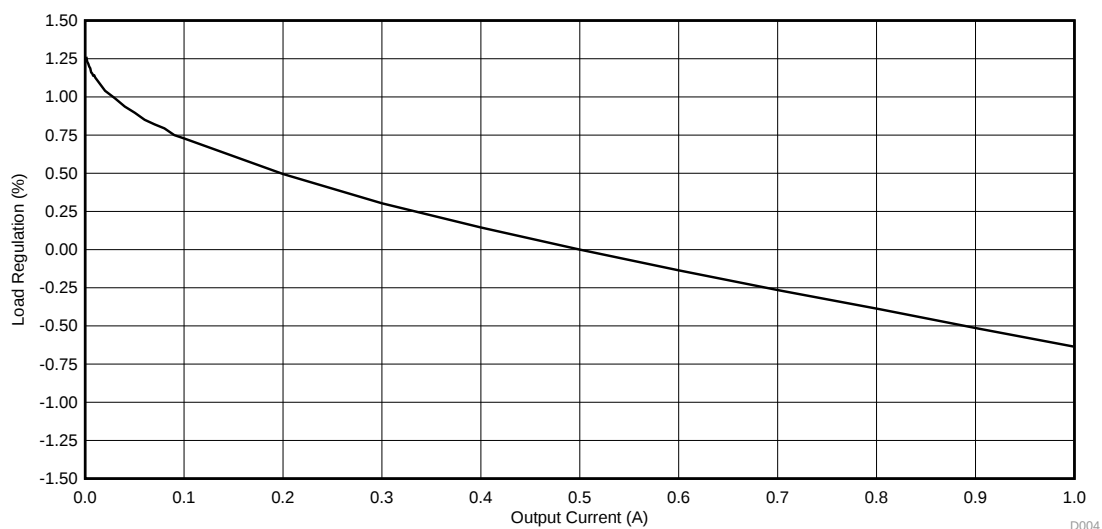


Figure 4. TPS54116-Q1EVM-830  $V_{TT}$  Output Load Regulation,  $V_{IN} = 5\text{ V}$ ,  $V_{LDOIN} = V_{DD} = 1.5\text{ V}$

Measurements are given for an ambient temperature of 25°C.

## 2.4 Output Voltage Line Regulation

Figure 5 shows the line regulation for the TPS54116-Q1EVM-830.

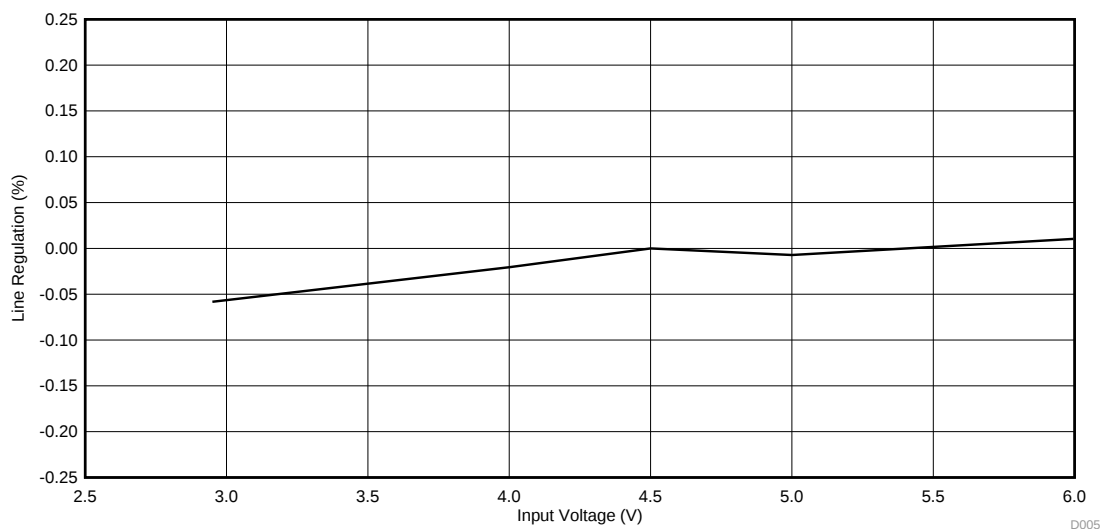


Figure 5. TPS54116-Q1EVM-830  $V_{DD}$  Output Line Regulation,  $I_{OUT} = 2\text{ A}$

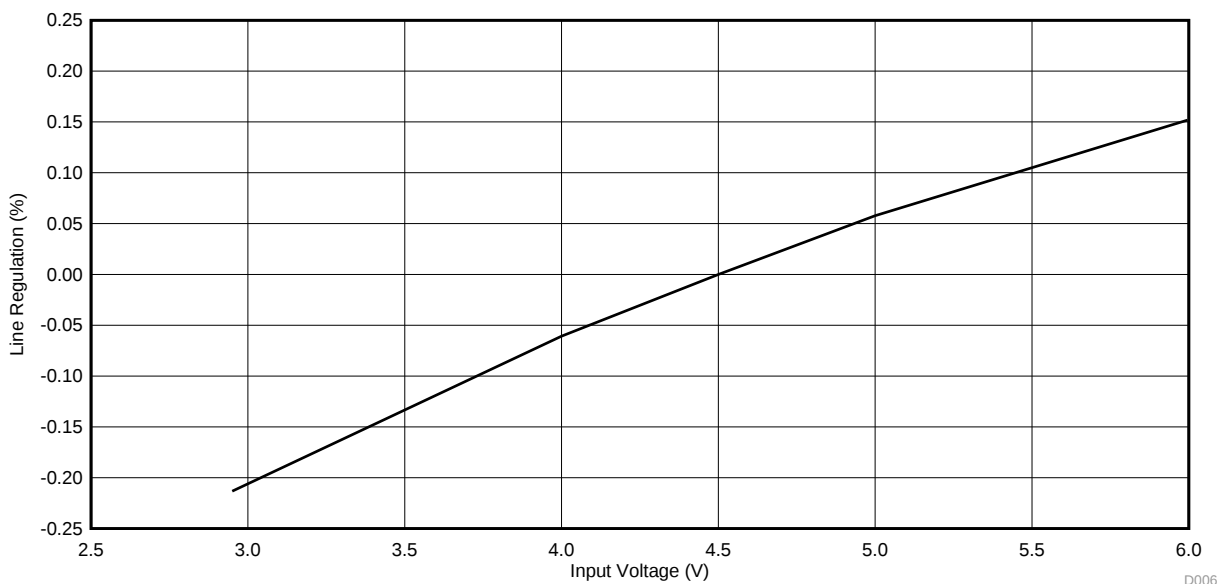
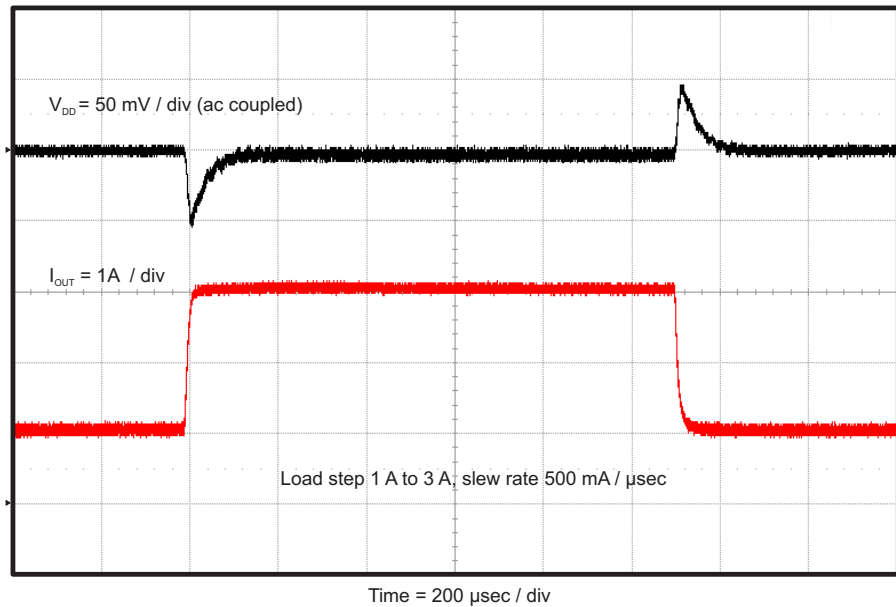


Figure 6. TPS54116-Q1EVM-830  $V_{TT}$  Output Line Regulation,  $I_{OUT} = 0.5\text{ A}$

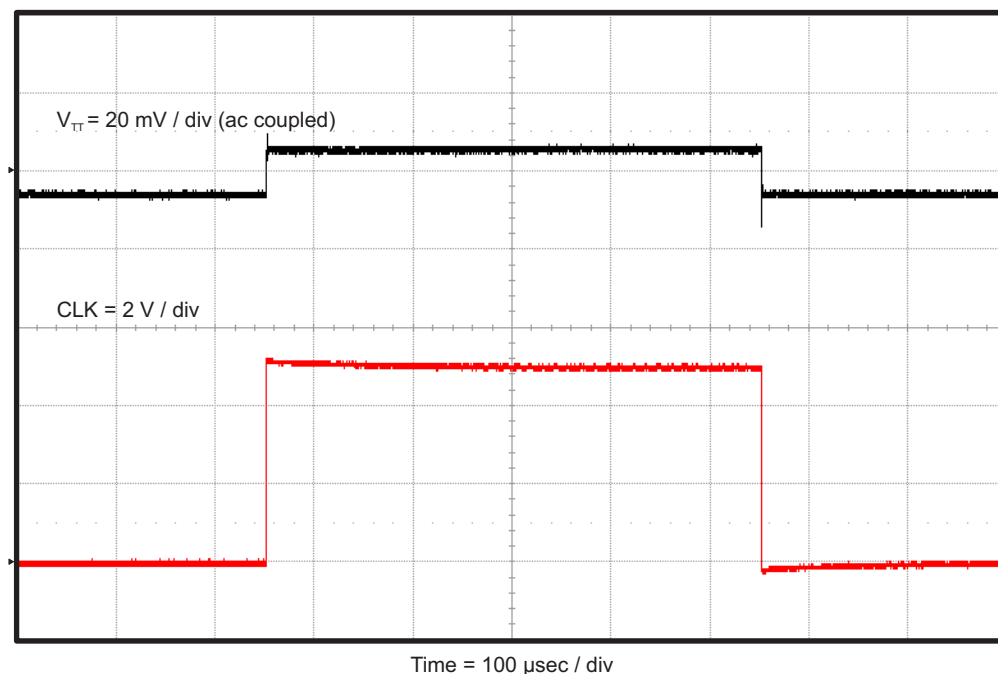
## 2.5 Load Transients

Figure 7 shows the TPS54116-Q1EVM-830  $V_{DD}$  output response to load transients. The current step is from 1 A to 3 A. The current step slew rate is 500 mA/ $\mu$ s. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.



**Figure 7. TPS54116-Q1EVM-830  $V_{DD}$  Output Transient Response**

Figure 8 shows the TPS54116-Q1EVM-830  $V_{TT}$  output response to source and sink load transients. The current step is from  $-1 \text{ A}$  to  $1 \text{ A}$ . Total peak-to-peak voltage variation is as shown, including ripple and noise on the output. The transient waveform is measured using the on-board source and sink transient circuit.



**Figure 8. TPS54116-Q1EVM-830  $V_{TT}$  Output Transient Response**

## 2.6 Loop Characteristics

Figure 9 shows the TPS54116-Q1EVM-830  $V_{DD}$  output loop-response characteristics. Gain and phase plots are shown for  $V_{IN}$  voltage of 5 V. Load current for the measurement is 2 A.

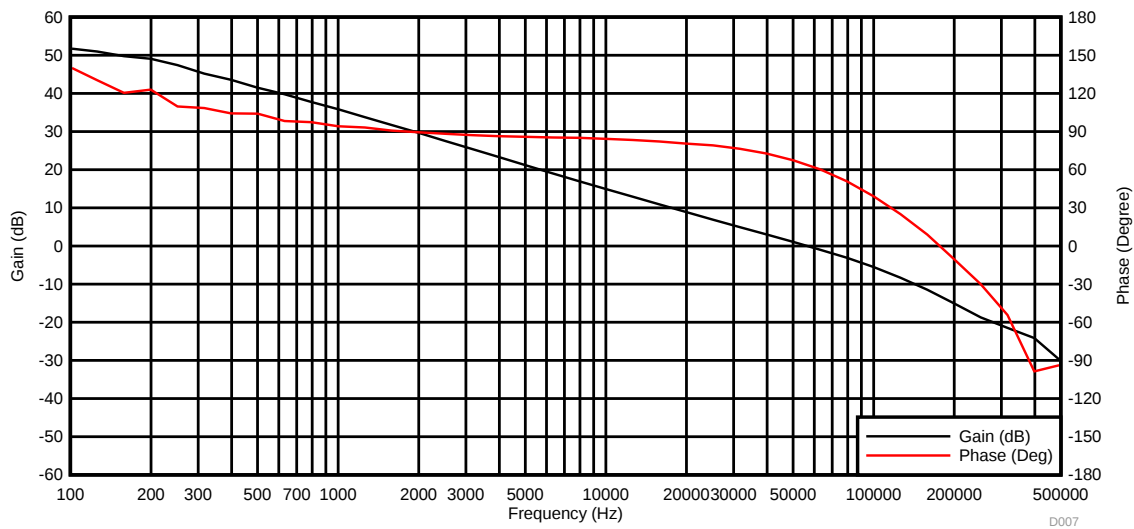


Figure 9. TPS54116-Q1EVM-830  $V_{DD}$  Output Loop Response

## 2.7 Output Voltage Ripple

Figure 10 and Figure 11 show the TPS54116-Q1EVM-830  $V_{DD}$  and  $V_{TT}$  output voltage ripple. The load currents are 3 A and 1 A, respectively.  $V_{IN} = 5$  V for  $V_{DD}$  and  $V_{DD}$  for  $V_{TT}$ .

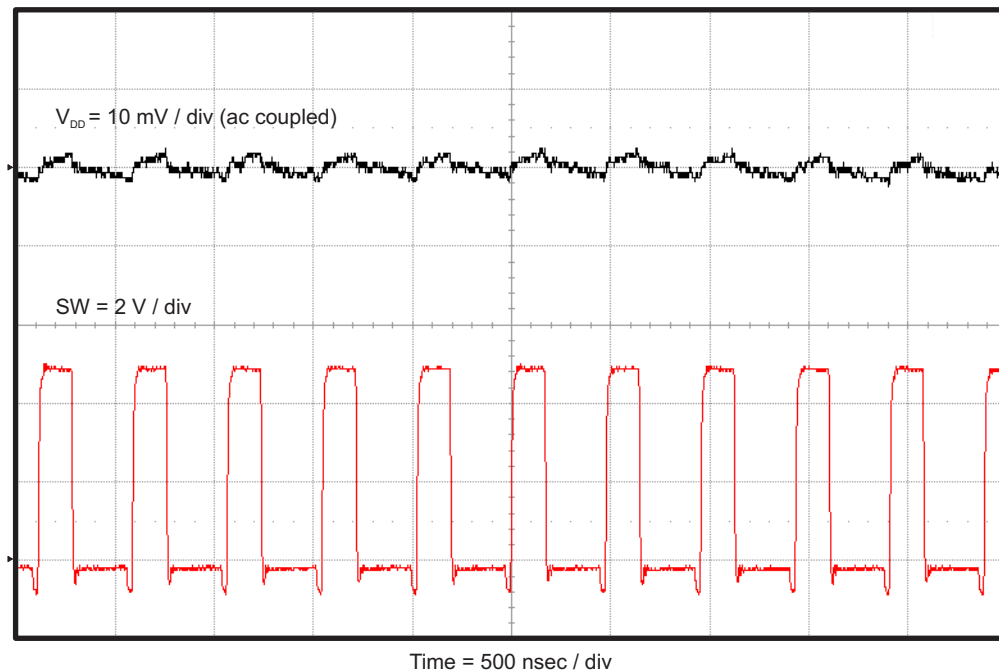
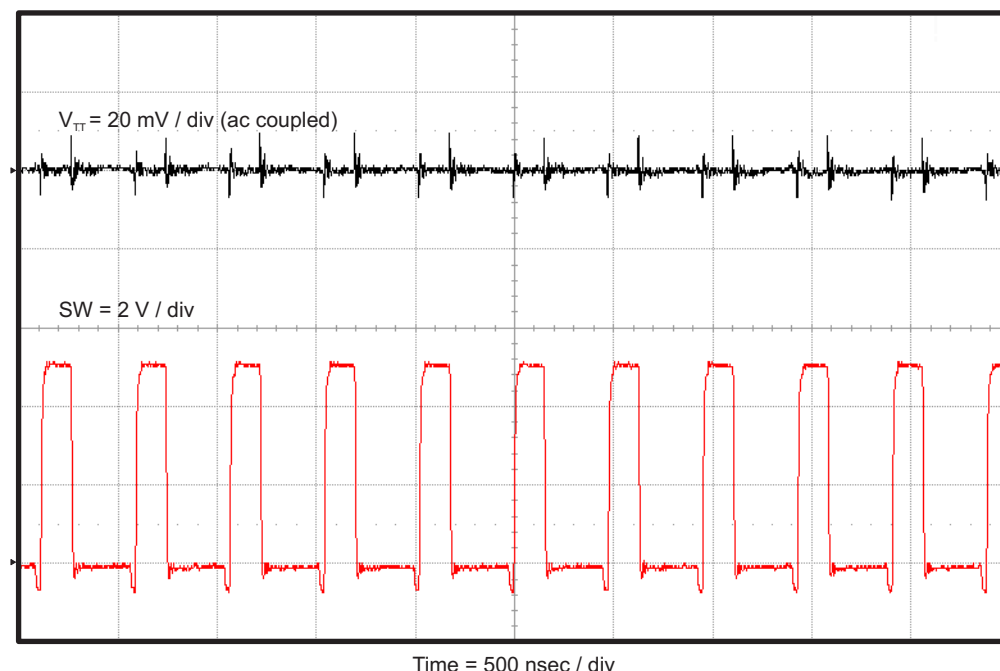


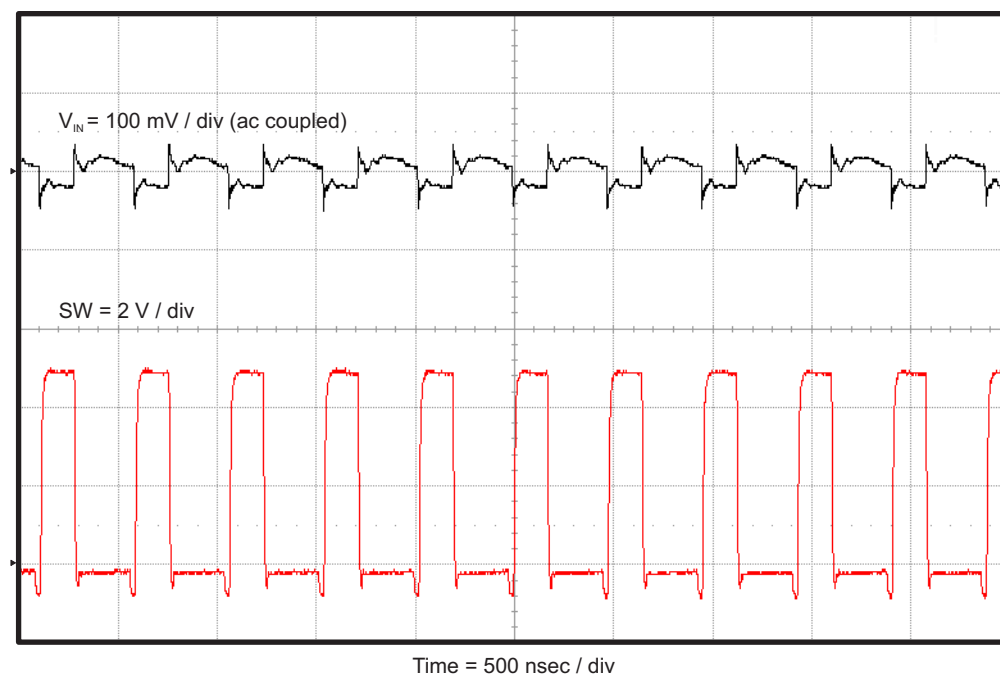
Figure 10. TPS54116-Q1EVM-830  $V_{DD}$  Output Ripple



**Figure 11. TPS54116-Q1EVM-830  $V_{TT}$  Output Ripple**

## 2.8 Input Voltage Ripple

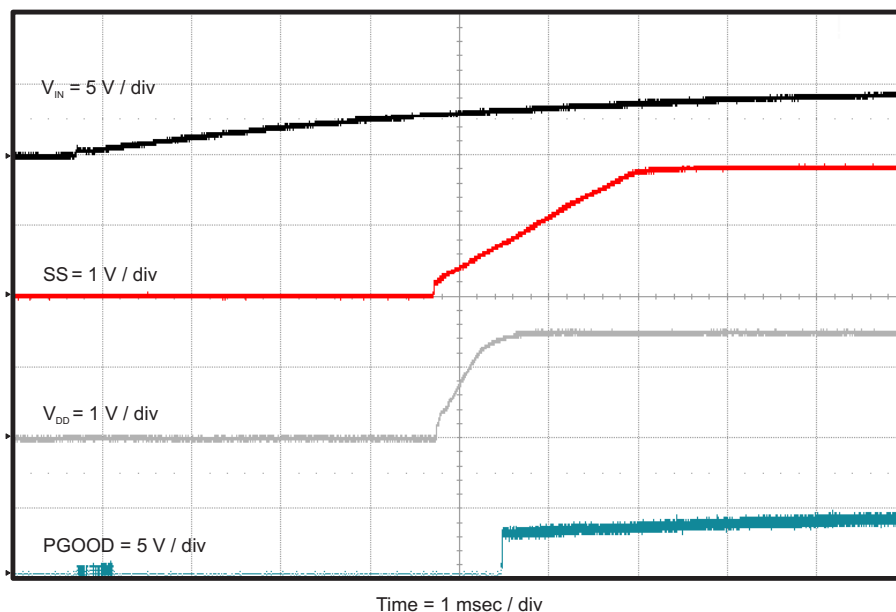
**Figure 12** shows the TPS54116-Q1EVM-830 input voltage ripple. The load currents are 3 A for  $V_{DD}$  and 1 A for  $V_{TT}$ .  $V_{IN} = 5 \text{ V}$  for  $V_{DD}$  and  $V_{DD}$  for  $V_{TT}$ . The ripple voltage is measured directly across TP1 and TP2.



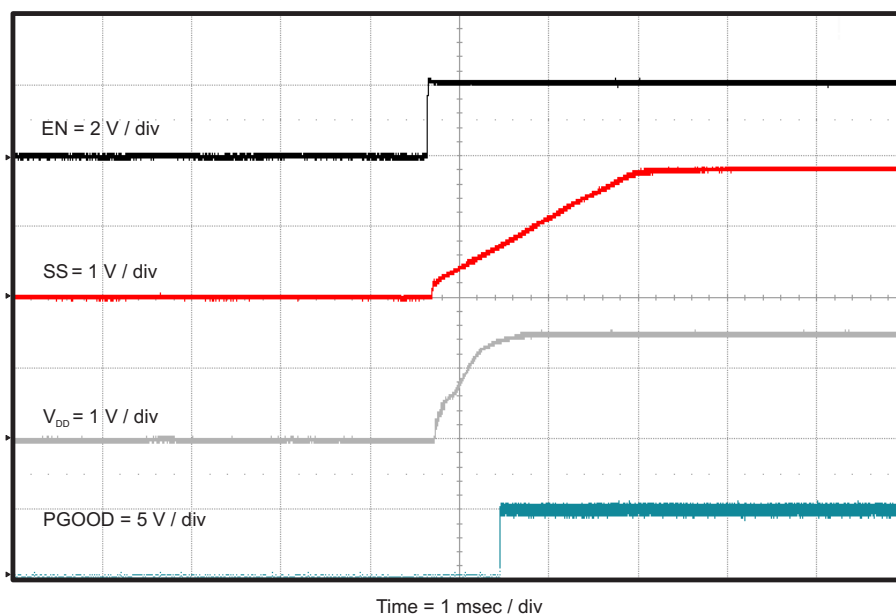
**Figure 12. TPS54116-Q1EVM-830 Input Ripple**

## 2.9 Powering Up

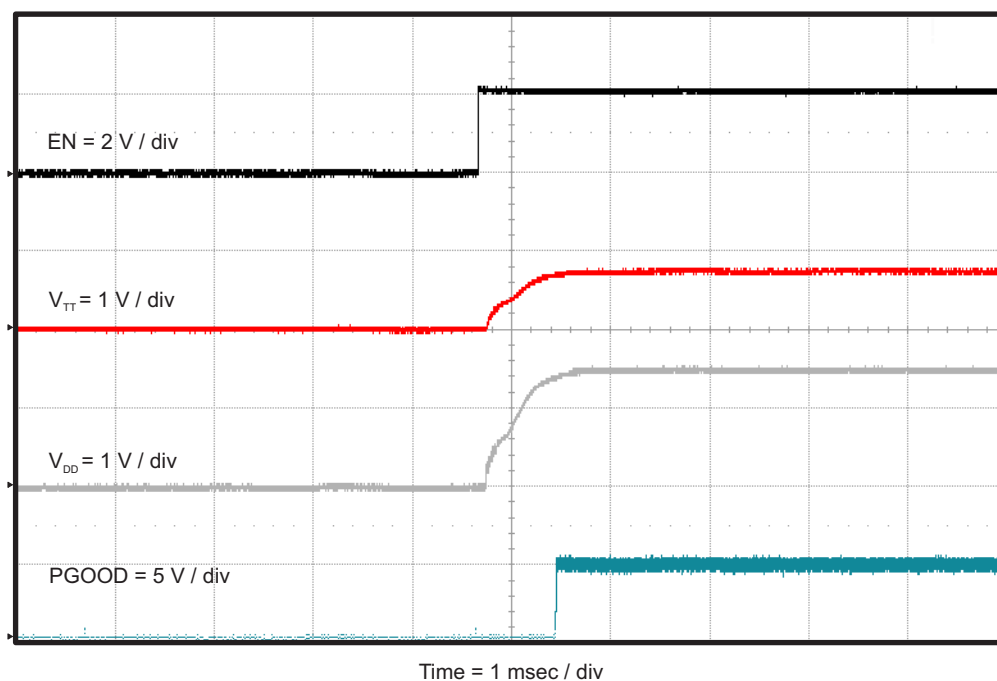
Figure 13, Figure 14, and Figure 15 show the start-up waveforms for the TPS54116-Q1EVM-830. In Figure 13, the  $V_{DD}$  output voltage ramps up as soon as the input voltage reaches the UVLO threshold. In Figure 14, the input voltage is initially applied and the  $V_{DD}$  output is inhibited by using a jumper at J4 to tie ENSW to GND. When the jumper is removed, ENSW is released. When the ENSW voltage reaches the enable-threshold voltage, the start-up sequence begins and the output  $V_{DD}$  voltage ramps up to the externally set value of 1.5 V. Figure 15 shows the  $V_{DD}$  output start up relative to enable. The input voltage for these plots is 5 V. The  $V_{DD}$  and  $V_{TT}$  loads are each 1  $\Omega$ .



**Figure 13. TPS54116-Q1EVM-830  $V_{DD}$  Start-Up Relative to  $V_{IN}$**



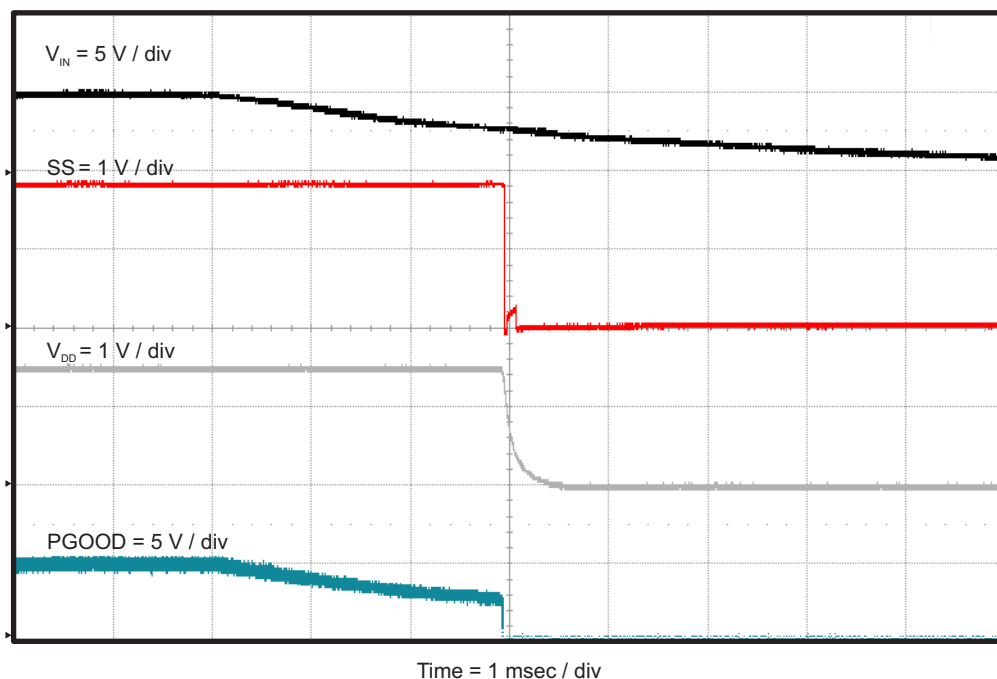
**Figure 14. TPS54116-Q1EVM-830  $V_{DD}$  Start-Up Relative to Enable**



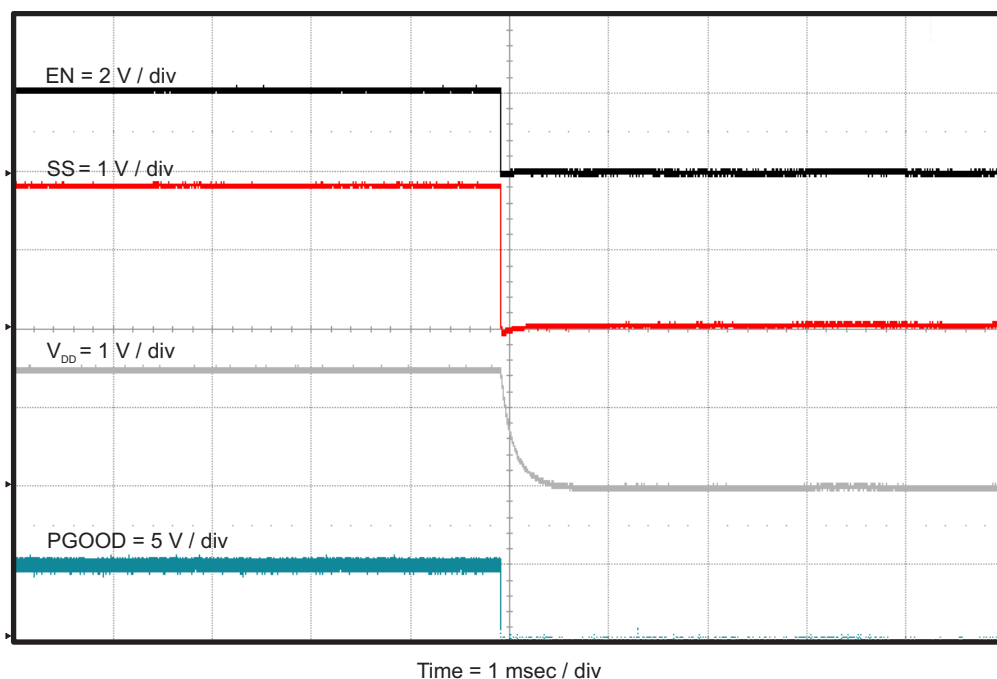
**Figure 15. TPS54116-Q1EVM-830  $V_{TT}$  and  $V_{DD}$  Start-Up Relative to Enable**

## 2.10 Powering Down

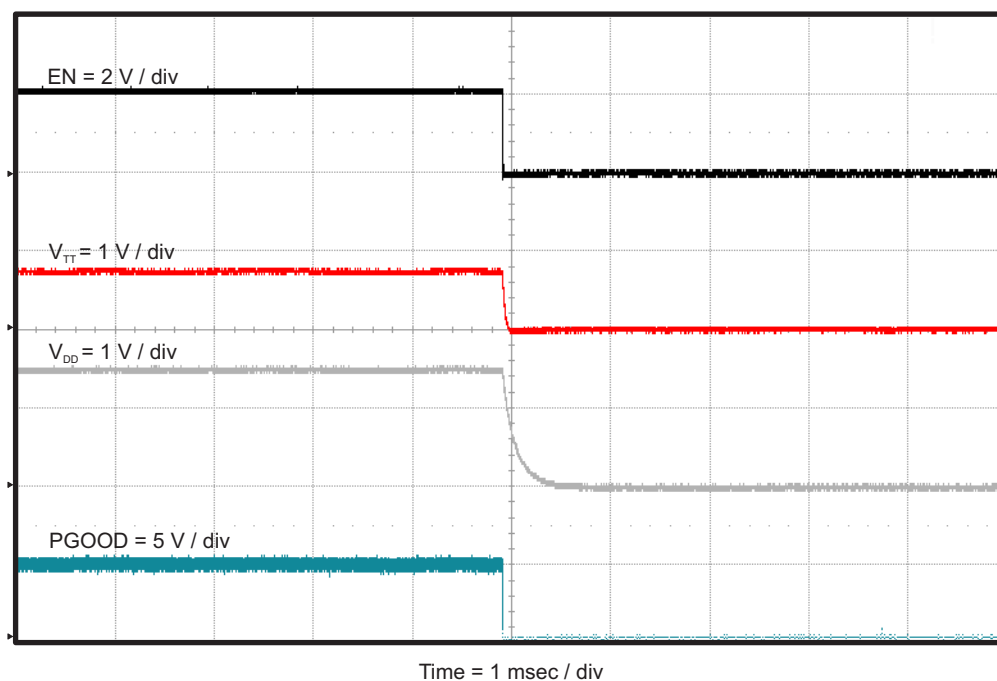
Figure 16, Figure 17, and Figure 18 show the shutdown waveforms for the TPS54116-Q1EVM-830. The input voltage for these plots is 5 V.



**Figure 16. V<sub>DD</sub> Shutdown Relative to V<sub>IN</sub>**



**Figure 17. V<sub>DD</sub> Shutdown Relative to Enable**



**Figure 18. V<sub>TT</sub> and V<sub>DD</sub> Shutdown Relative to Enable**

### 3 Board Layout

This section provides a description of the TPS54116-Q1EVM-830 board layout and layer illustrations.

#### 3.1 Layout

The board layout for the TPS54116-Q1EVM-830 is shown in [Figure 19](#) through [Figure 23](#). The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for  $V_{IN}$ ,  $V_{DD}$ ,  $V_{TT}$ , and SW. Also on the top layer are connections for the remaining pins of the TPS54116-Q1 and the majority of the signal traces. There are three large areas filled with power ground. The internal layer-1 is dedicated ground plane. The internal layer-2 contains an additional large ground copper area with an island for quiet analog ground that is connected to the main power ground plane at a single point. There are also additional  $V_{IN}$ ,  $V_{DD}$ , and  $V_{TT}$  copper fills to connect to the built-in source/sink load circuit. The bottom layer is another ground plane with additional traces to connect the remaining signals. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board.

The input decoupling capacitors and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage setpoint resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the  $V_{DD}$  output connector J2. For the TPS54116-Q1, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage set point divider, EN resistor, SS capacitor, MODE resistor, and AGND pin are terminated to quiet analog ground island on the internal layer-2.

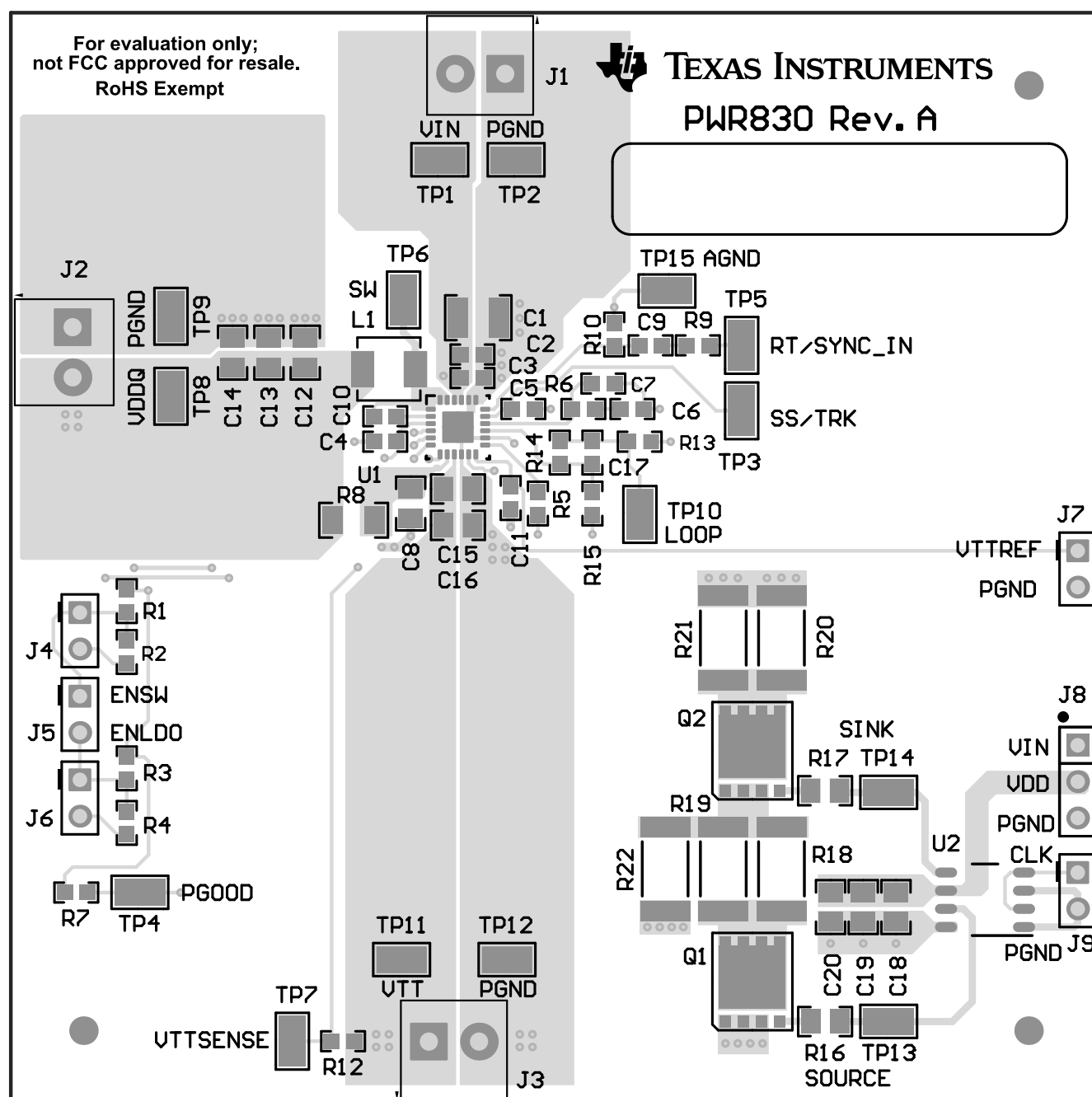


Figure 19. TPS54116-Q1EVM-830 Top-Side Assembly

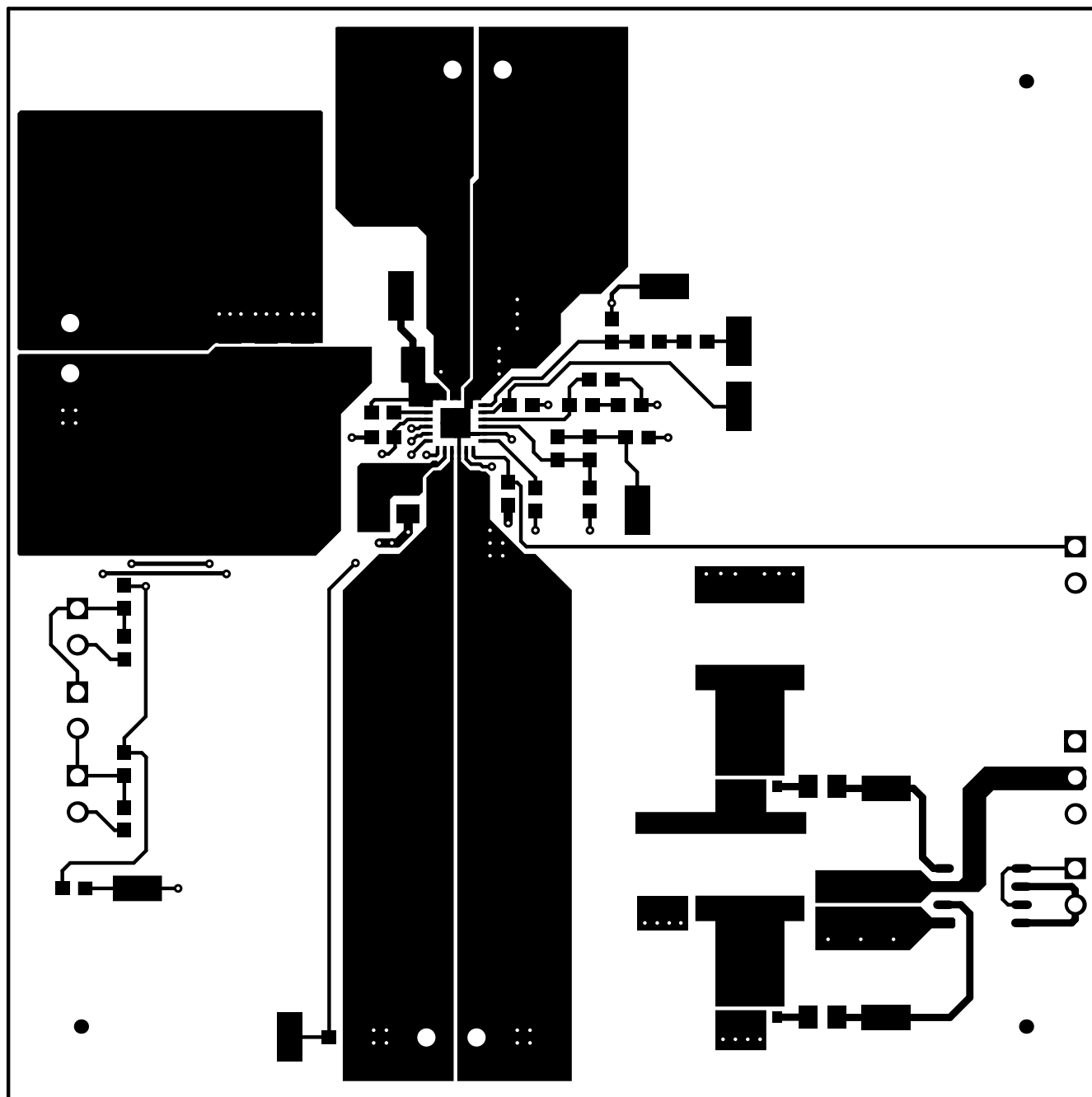


Figure 20. TPS54116-Q1EVM-830 Top-Side Layout

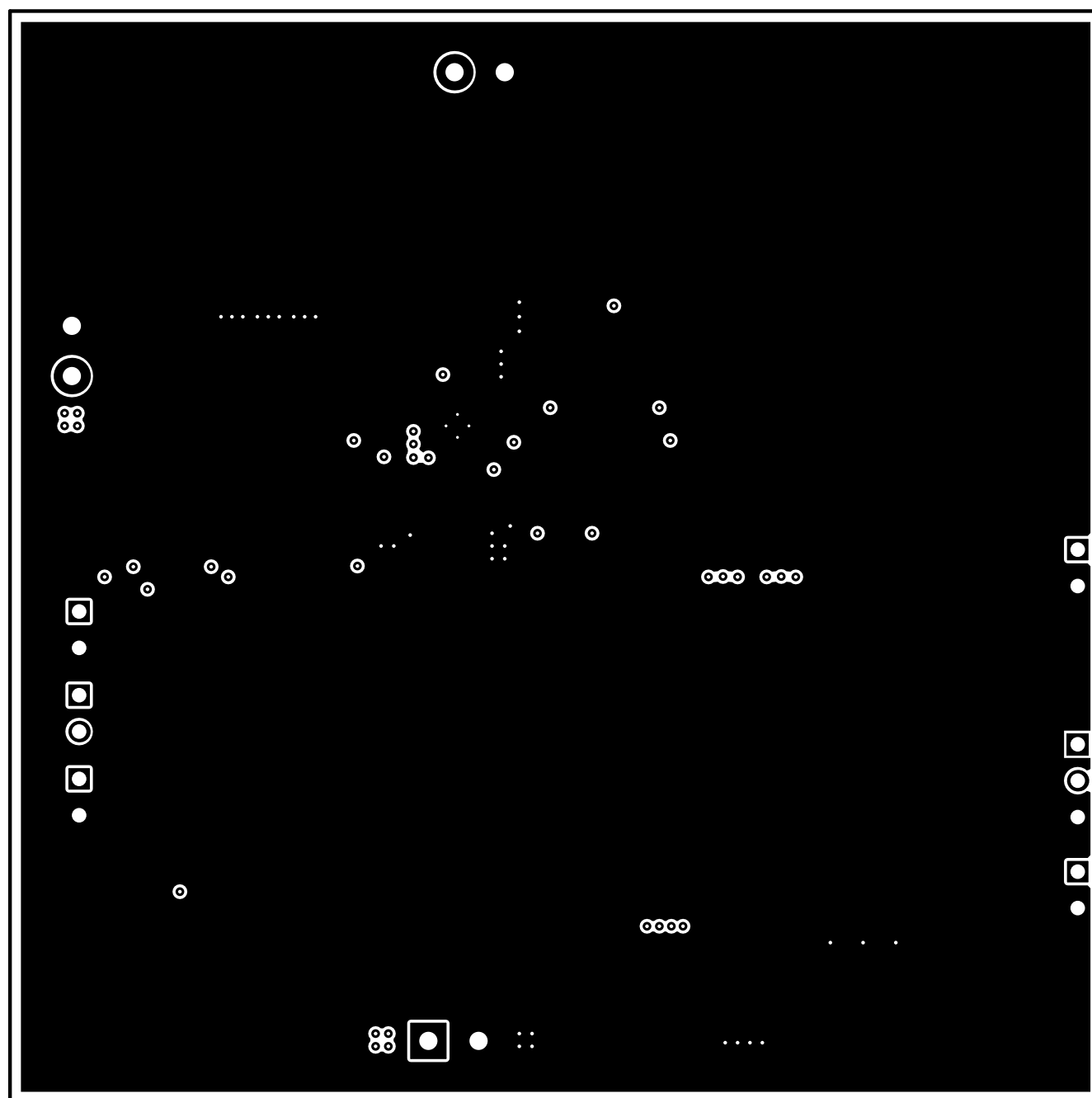
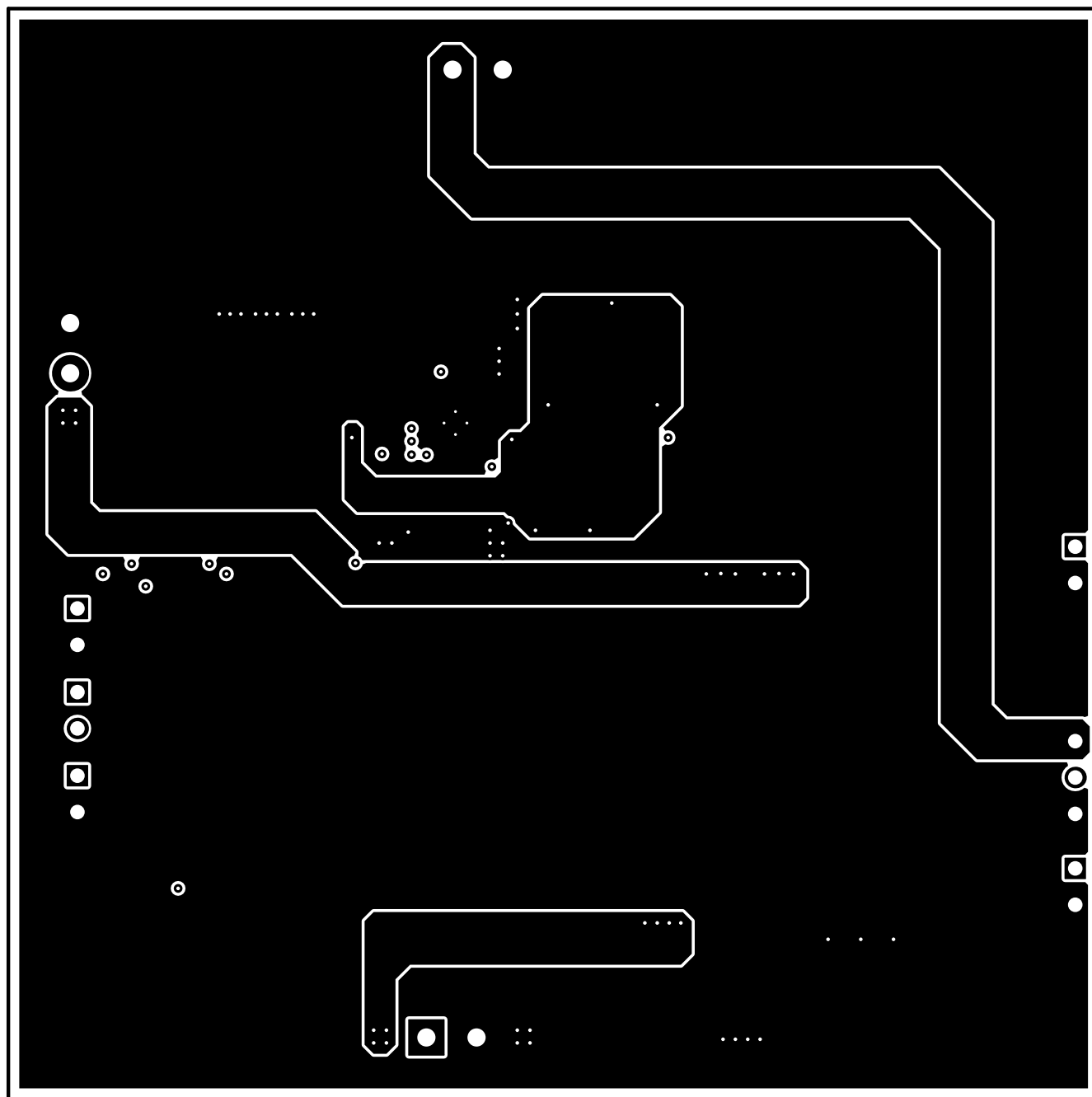


Figure 21. TPS54116-Q1EVM-830 Internal Layer-1 Layout



**Figure 22. TPS54116-Q1EVM-830 Internal Layer-2 Layout**

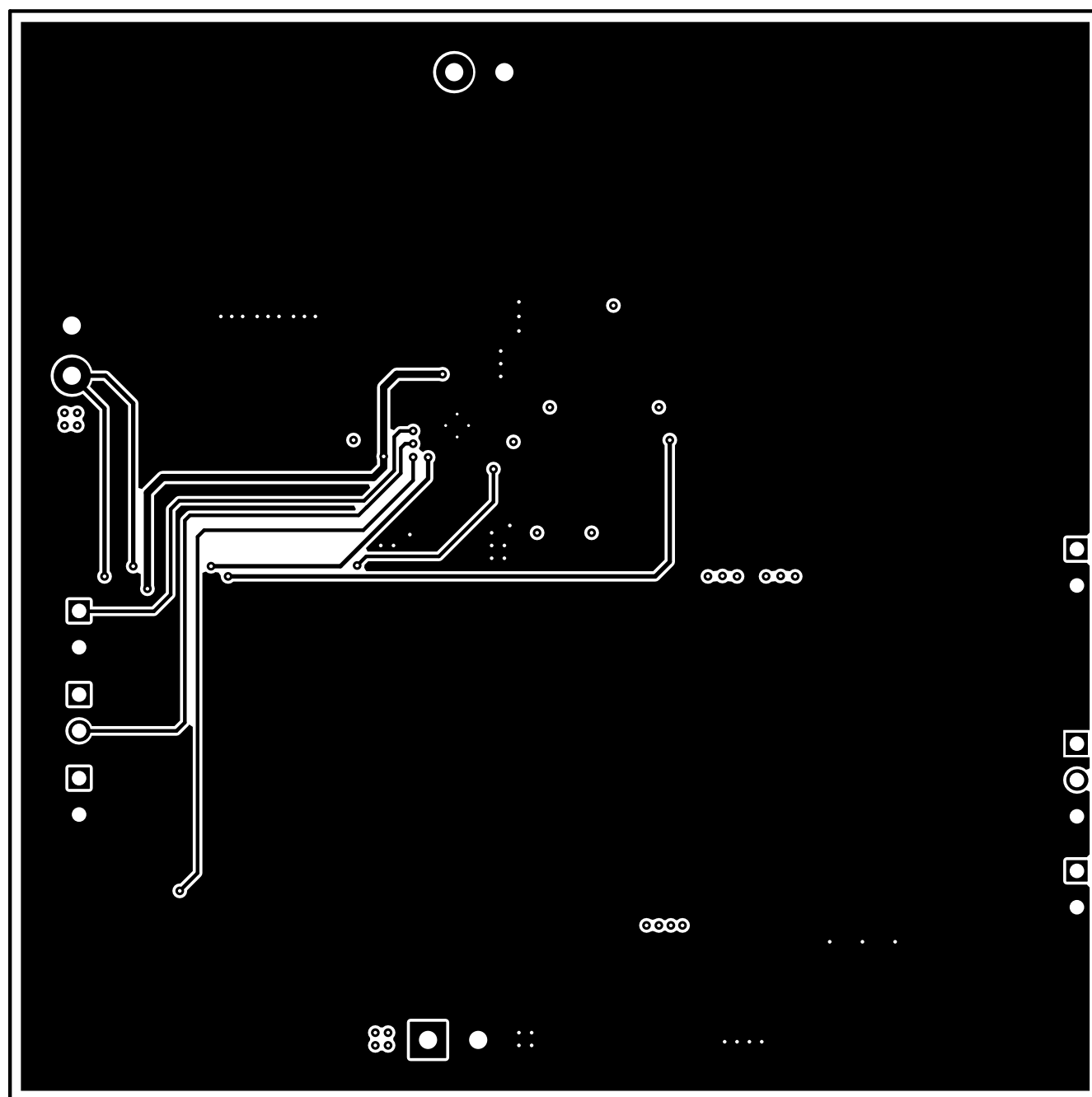


Figure 23. TPS54116-Q1EVM-830 Bottom-Side Layout

## 4 Schematic and Bill of Materials

This section presents the TPS54116-Q1EVM-830 schematic and bill of materials.

### 4.1 Schematic

Figure 24 is the schematic for the TPS54116-Q1EVM-830.

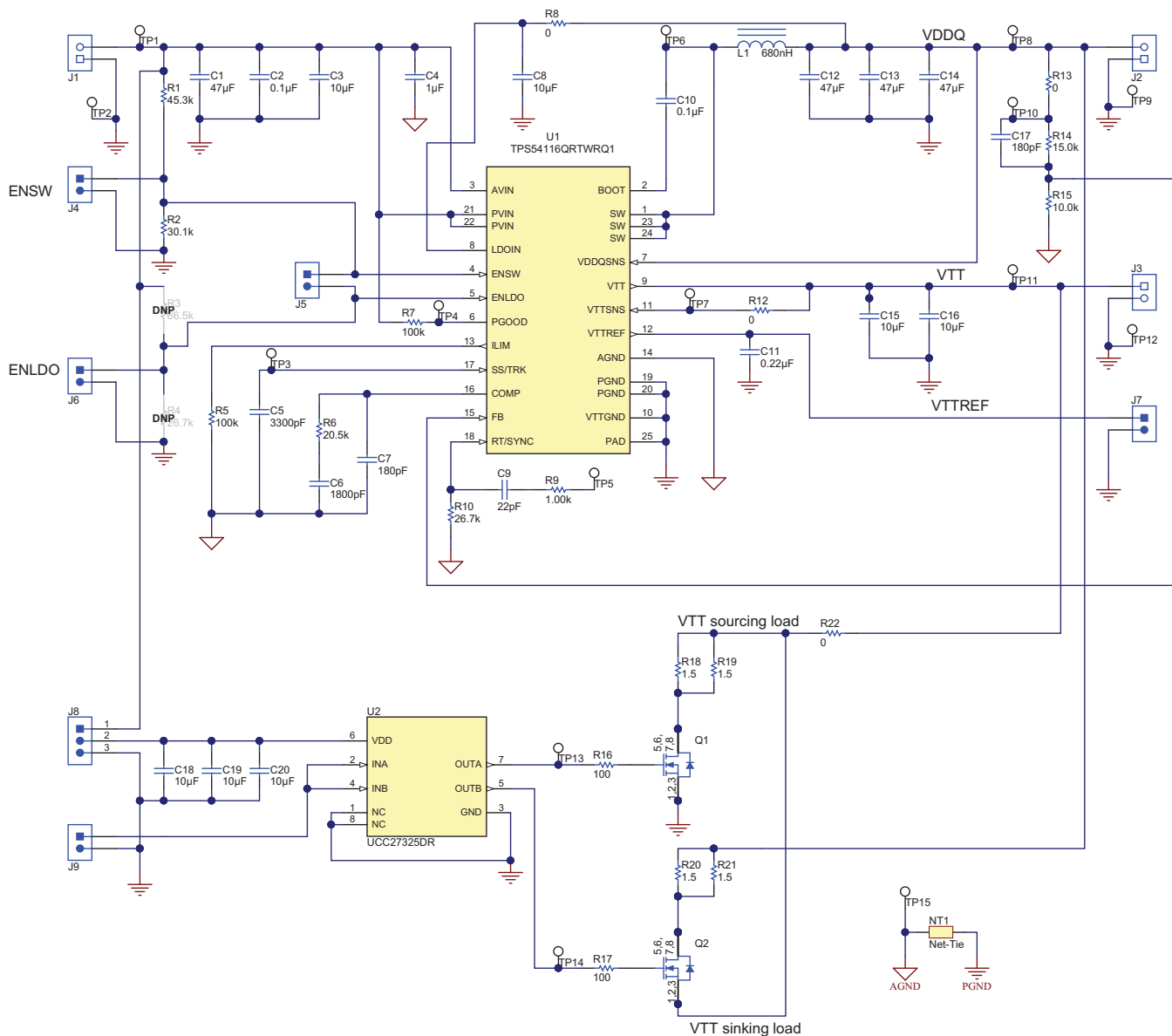


Figure 24. TPS54116-Q1EVM-830 Schematic

## 4.2 Bill of Materials

Table 4 presents the TPS54116-Q1EVM-830 bill of materials.

**Table 4. TPS54116-Q1EVM-830 Bill of Materials**

| Designator         | Qty | Value  | Description                                                                | Package Reference           | Part Number        | Manufacturer                |
|--------------------|-----|--------|----------------------------------------------------------------------------|-----------------------------|--------------------|-----------------------------|
| !PCB1              | 1   |        | Printed Circuit Board                                                      |                             | PWR830             | Any                         |
| C1, C12, C13, C14  | 4   | 47uF   | CAP, CERM, 47 $\mu$ F, 10 V, +/- 10%, X7R, 1210                            | 1210                        | GRM32ER71A476KE15L | Murata                      |
| C2, C10            | 2   | 0.1uF  | CAP, CERM, 0.1 $\mu$ F, 16 V, +/- 10%, X7R, 0603                           | 0603                        | GRM188R71C104KA01D | Murata                      |
| C3                 | 1   | 10uF   | CAP, CERM, 10 $\mu$ F, 10 V, +/- 20%, X7R, 0603                            | 0603                        | GRM188Z71A106MA73D | Murata                      |
| C4                 | 1   | 1uF    | CAP, CERM, 1 $\mu$ F, 10 V, +/- 10%, X7R, 0603                             | 0603                        | GRM188R71A105KA61D | Murata                      |
| C5                 | 1   | 3300pF | CAP, CERM, 3300 pF, 50 V, +/- 10%, X7R, 0603                               | 0603                        | GRM188R71H332KA01D | Murata                      |
| C6                 | 1   | 1800pF | CAP, CERM, 1800 pF, 25 V, +/- 10%, X7R, 0603                               | 0603                        | GRM188R71E182KA01D | Murata                      |
| C7, C17            | 2   | 180pF  | CAP, CERM, 180 pF, 50 V, +/- 5%, C0G/NP0, 0603                             | 0603                        | GRM1885C1H181JA01D | Murata                      |
| C8, C15, C16       | 3   | 10uF   | CAP, CERM, 10 $\mu$ F, 10 V, +/- 10%, X7R, 0805                            | 0805                        | GRM21BR71A106KE51L | Murata                      |
| C9                 | 1   | 22pF   | CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0603                              | 0603                        | GRM1885C1H220JA01D | Murata                      |
| C11                | 1   | 0.22uF | CAP, CERM, 0.22uF, 10V, +/-10%, X7R, 0603                                  | 0603                        | GRM188R71A224KA01D | Murata                      |
| C18, C19, C20      | 3   | 10uF   | CAP, CERM, 10 $\mu$ F, 10 V, +/- 10%, X5R, 0805                            | 0805                        | GRM21BR61A106KE19L | Murata                      |
| J1, J2, J3         | 3   |        | Terminal Block, 3.5mm Pitch, 2x1, TH                                       | 7.0x8.2x6.5mm               | ED555/2DS          | On-Shore Technology         |
| J4, J5, J6, J7, J9 | 5   |        | Header, 100mil, 2x1, Tin, TH                                               | Header, 2 PIN, 100mil, Tin  | PEC02SAAN          | Sullins Connector Solutions |
| J8                 | 1   |        | Header, 100mil, 3x1, Tin, TH                                               | Header, 3 PIN, 100mil, Tin  | PEC03SAAN          | Sullins Connector Solutions |
| L1                 | 1   | 680nH  | Inductor, Shielded Drum Core, Powdered Iron, 680 nH, 5.5 A, 0.016 ohm, SMD | 4.45x1.8x4.06mm             | 744373240068       | Würth Elektronik            |
| LBL?               | 1   |        | Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll   | PCB Label 1.25 x 0.250 inch | THT-13-457-10      | Brady                       |
| Q1, Q2             | 2   | 25V    | MOSFET, N-CH, 25 V, 100 A, SON 5x6mm                                       | SON 5x6mm                   | CSD16407Q5         | Texas Instruments           |
| R1                 | 1   | 45.3k  | RES, 45.3 k, 1%, 0.1 W, 0603                                               | 0603                        | CRCW060345K3FKEA   | Vishay-Dale                 |
| R2                 | 1   | 30.1k  | RES, 30.1 k, 1%, 0.1 W, 0603                                               | 0603                        | CRCW060330K1FKEA   | Vishay-Dale                 |
| R5, R7             | 2   | 100k   | RES, 100 k, 1%, 0.1 W, 0603                                                | 0603                        | CRCW0603100KFKEA   | Vishay-Dale                 |
| R6                 | 1   | 20.5k  | RES, 20.5 k, 1%, 0.1 W, 0603                                               | 0603                        | CRCW060320K5FKEA   | Vishay-Dale                 |
| R8                 | 1   | 0      | RES, 0, 5%, 0.25 W, 1206                                                   | 1206                        | CRCW12060000Z0EA   | Vishay-Dale                 |
| R9                 | 1   | 1.00k  | RES, 1.00 k, 1%, 0.1 W, 0603                                               | 0603                        | CRCW06031K00FKEA   | Vishay-Dale                 |
| R10                | 1   | 26.7k  | RES, 121k ohm, 1%, 0.1W, 0603                                              | 0603                        | CRCW060326K7KFKEA  | Vishay-Dale                 |
| R12, R13           | 2   | 0      | RES, 0, 5%, 0.1 W, 0603                                                    | 0603                        | CRCW06030000Z0EA   | Vishay-Dale                 |
| R14                | 1   | 15.0k  | RES, 15.0k ohm, 1%, 0.1W, 0603                                             | 0603                        | CRCW060315K0FKEA   | Vishay-Dale                 |
| R15                | 1   | 10.0k  | RES, 10.0k ohm, 1%, 0.1W, 0603                                             | 0603                        | CRCW060310K0FKEA   | Vishay-Dale                 |
| R16, R17           | 2   | 100    | RES, 100 ohm, 1%, 0.125W, 0805                                             | 0805                        | CRCW0805100RFKEA   | Vishay-Dale                 |
| R18, R19, R20, R21 | 4   | 1.5    | RES, 1.5, 5%, 1 W, 2512                                                    | 2512                        | CRCW25121R50JNEG   | Vishay-Dale                 |
| R22                | 1   | 0      | RES, 0, 5%, 1 W, 2512                                                      | 2512                        | CRCW25120000Z0EG   | Vishay-Dale                 |

**Table 4. TPS54116-Q1EVM-830 Bill of Materials (continued)**

| Designator                                                                      | Qty | Value | Description                                                                                                     | Package Reference            | Part Number      | Manufacturer      |
|---------------------------------------------------------------------------------|-----|-------|-----------------------------------------------------------------------------------------------------------------|------------------------------|------------------|-------------------|
| SH-J4, SH-J5, SH-J6, SH-J8                                                      | 4   | 1x2   | Shunt, 100mil, Gold plated, Black                                                                               | Shunt                        | 969102-0000-DA   | 3M                |
| TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15 | 15  |       | Test Point, Miniature, SMT                                                                                      | Testpoint_Keystone_Miniature | 5015             | Keystone          |
| U1                                                                              | 1   |       | Fixed Frequency Step-Down Converter and Sink/Source DDR Termination Regulator with Buffered Reference, RTW0024C | RTW0024C                     | TPS54116QRTWRQ1  | Texas Instruments |
| U2                                                                              | 1   |       | Dual 4-A Peak High-Speed Low-Side Power-MOSFET Driver, D0008A                                                   | D0008A                       | UCC27325DR       | Texas Instruments |
| FID1, FID2, FID3                                                                | 0   |       | Fiducial mark. There is nothing to buy or mount.                                                                | Fiducial                     | N/A              | N/A               |
| R3                                                                              | 0   | 66.5k | RES, 66.5k ohm, 1%, 0.1W, 0603                                                                                  | 0603                         | CRCW060366K5FKEA | Vishay-Dale       |
| R4                                                                              | 0   | 26.7k | RES, 26.7k ohm, 1%, 0.1W, 0603                                                                                  | 0603                         | CRCW060326K7FKEA | Vishay-Dale       |

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- 3 *Regulatory Notices:*

- 3.1 *United States*

### 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

### 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

## CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

## FCC Interference Statement for Class A EVM devices

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

## FCC Interference Statement for Class B EVM devices

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

## 3.2 Canada

### 3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

#### Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

#### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

## 3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see [http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page) 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。  
[http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page)

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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