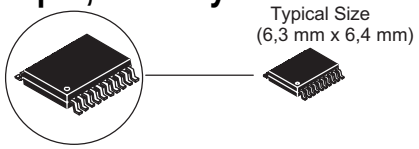
TPS54110 3-V to 6-V Input, 1.5-A Synchronous Step-Down Converter



1 Features

- Integrated MOSFET Switches for High Efficiency at 1.5-A Continuous Output Source or Sink Current
- 0.9-V to 3.3-V Adjustable Output Voltage With 1% Accuracy
- Externally Compensated for Design Flexibility
- Fast Transient Response
- Wide PWM Frequency: Fixed 350 kHz, 550 kHz, or Adjustable 280 kHz to 700 kHz
- Load Protected by Peak Current Limit and Thermal Shutdown
- Integrated Solution Reduces Board Area and Total Cost

2 Applications

- Low-Voltage, High-Density Systems With Power Distributed at 5 V or 3.3 V
- Point-of-Load Regulation for High Performance DSPs, FPGAs, ASICs, and Microprocessors
- Broadband, Networking, and Optical Communications Infrastructure
- Portable Computing/Notebook PCs

3 Description

The TPS54110 is a low-input-voltage high-output-current synchronous-buck PWM converter that integrates all required active components. Included on the substrate with the listed features are a true, high- performance, voltage error amplifier that provides high performance under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power-good output useful for processor/logic reset, fault signaling, and supply sequencing.

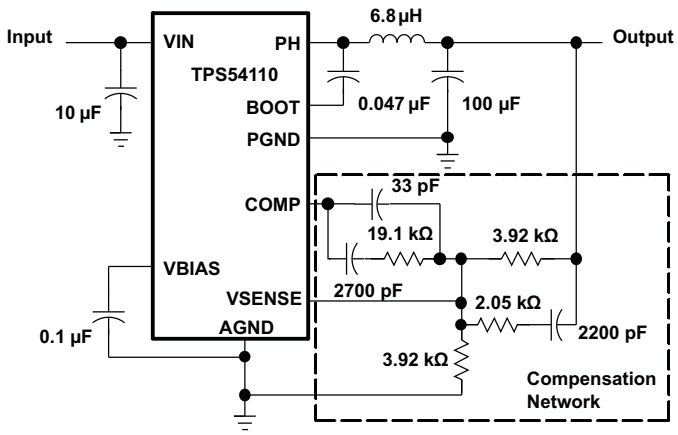
The TPS54110 device is available in a thermally enhanced 20-pin HTSSOP (PWP) PowerPAD™ package, which eliminates bulky heat sinks. TI provides evaluation modules and other technical support to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

Device Information[1]

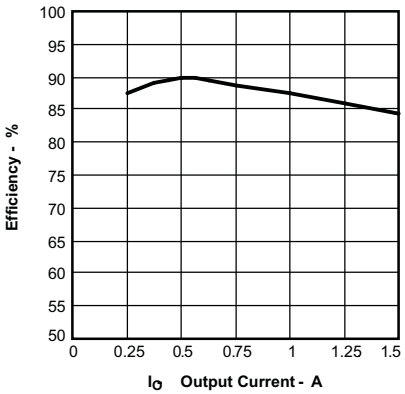
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54110	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



EFFICIENCY vs OUTPUT CURRENT



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2011) to Revision D — **Page**

- Editorial updates; no change to technical content ... 1

Changes from Revision B (xx) to Revision C — **Page**

- Added *Thermal Information* table; deleted Dissipation Ratings table ... 4

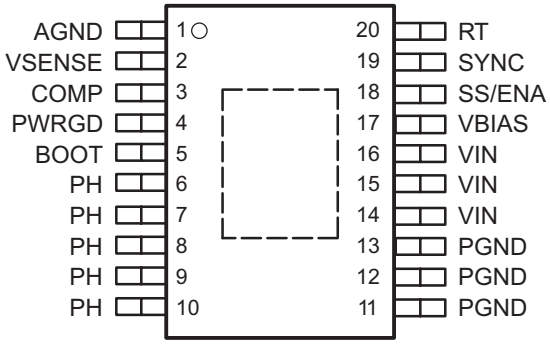
5 Device Information

T_J	OUTPUT VOLTAGE	PACKAGED DEVICES PLASTIC HTSSOP (PWP)(1)
–40°C to 125°C	Adjustable to 0.891 V	TPS54110PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54110PWPR). See application section of data sheet for PowerPAD drawing and layout information.

6 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP With PowerPAD
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	1	Analog ground—internally connected to the sensitive analog-ground circuitry. Connect to PGND and PowerPAD.
BOOT	5	Bootstrap input. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect compensation network from COMP to VSENSE.
PGND	11–13	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. Connect to AGND and PowerPAD.
PH	6–10	Phase input/output. Junction of the internal high and low-side power MOSFETs, and output inductor.
PWRGD	4	Power-good open drain output. High when VSENSE ≥ 93% Vref, otherwise PWRGD is low. Note that output is low when SS/ENA is low or internal shutdown signal active.
RT	20	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s.
SS/ENA	18	Slow-start/enable input/output. Dual-function pin that provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	19	Synchronization input. Dual-function pin that provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
VBIAS	17	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low ESR 0.1-µF to 1-µF ceramic capacitor.
VIN	14–16	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low ESR 1-µF to 10-µF ceramic capacitor.
VSENSE	2	Error amplifier inverting input.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

		VALUE	UNIT
Input voltage range, V_I	VIN, SS/ENA, SYNC	–0.3 to 7	V
	RT	–0.3 to 6	V
	VSENSE	–0.3 to 4	V
	BOOT	–0.3 to 17	V
Output voltage range, V_O	VBIAS, PWRGD, COMP	–0.3 to 7	V
	PH	–0.6 to 10	V
Source current, I_O	PH	Internally Limited	
	COMP, VBIAS	6	mA
Sink current	PH	3.5	A
	COMP	6	mA
	SS/ENA,PWRGD	10	mA
Voltage differential	AGND to PGND	±0.3	V
Continuous power dissipation		See *Thermal Information*	
Operating virtual junction temperature range, T_J		–40 to 150	°C
Storage temperature, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Input voltage range, V_I	3		6	V
Operating junction temperature, T_J	–40		125	°C

7.3 Thermal Information

THERMAL METRIC(1)		TPS54110 PWP (HTTSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

7.4 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN						
	VIN input voltage range		3		6	V
	Quiescent current	f_s = 350 kHz, SYNC ≤ 0.8 V, RT open		4.5	8.5	mA
		f_s = 550 kHz, Phase pin open, SYNC ≥ 2.5 V, RT open,		5.8	9.6	
		Shutdown, SS/ENA = 0 V		1	1.4	
UNDER VOLTAGE LOCK OUT						
	Start threshold voltage, UVLO			2.95	3	V
	Stop threshold voltage, UVLO		2.70	2.80		
	Hysteresis voltage, UVLO			0.12		V
	Rising and falling edge deglitch, UVLO(1)			2.5		µs
BIAS VOLTAGE						
V_O	Output voltage, VBIAS	$I_{(VBIAS)}$ = 0	2.70	2.80	2.90	V
	Output current, VBIAS(2)				100	µA
CUMULATIVE REFERENCE						
V_{ref}	Accuracy		0.882	0.891	0.900	V
REGULATION						
	Line regulation(1)(3)	I_L = 0.75 A, f_s = 350 kHz, T_J = 85°C		0.05		%/V
		I_L = 0.75 A, f_s = 550 kHz, T_J = 85°C		0.05		
	Load regulation(1)(3)	I_L = 0 A to 1.5 A, f_s = 350 kHz, T_J = 85°C		0.01		%/A
		I_L = 0 A to 1.5 A f_s = 550 kHz, T_J = 85°C		0.01		
OSCILLATOR						
	Internally set free-running frequency range	SYNC ≤ 0.8 V, RT open	280	350	420	kHz
		SYNC ≥ 2.5 V, RT open	440	550	660	
	Externally set free-running frequency range	RT = 180 kΩ (1% resistor to AGND)(1)	252	280	308	kHz
		RT = 100 kΩ (1% resistor to AGND)	460	500	540	
		RT = 68 kΩ (1% resistor to AGND)(1)	663	700	762	
	High-level threshold voltage, SYNC		2.5			V
	Low-level threshold voltage, SYNC				0.8	V
	Pulse duration, SYNC(1)		50			ns
	Frequency range, SYNC(1)		330		700	kHz
	Ramp valley(1)			0.75		V
	Ramp amplitude (peak-to-peak)(1)			1		V
	Minimum controllable on time(1)				200	ns
	Maximum duty cycle		90			%

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 9.

Electrical Characteristics (continued)

T_J = –40°C to +125°C, V_{IN} = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
	Error-amplifier open loop voltage gain	1 kΩ COMP to AGND(1)	90	110		dB
	Error-amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(1)	3	5		MHz
	Error-amplifier common-mode input voltage range	Powered by internal LDO(1)	0		VBIAS	V
I_{IB}	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
V_O	Output voltage slew rate (symmetric), COMP(1)			1.2		V/µs
PWM COMPARATOR						
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding dead time)	10 mV overdrive(1)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, SS/ENA		0.82	1.20	1.40	V
	Enable hysteresis voltage, SS/ENA(1)			0.03		V
	Falling-edge deglitch, SS/ENA(1)			2.5		µs
	Internal slow-start time		2.6	3.35	4.1	ms
	Charge current, SS/ENA	SS/ENA = 0 V	3	5	8	µA
	Discharge current, SS/ENA	SS/ENA = 1.3 V, V_I = 1.5 V	1.5	2.3	4	mA
POWER GOOD						
	Power-good threshold voltage	VSENSE falling		93		%V_{ref}
	Power-good hysteresis voltage(1)			3		%V_{ref}
	Power-good falling-edge deglitch(1)			35		µs
	Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.30	V
	Leakage current, PWRGD	V_I = 5.5 V			1	µA
CURRENT LIMIT						
	Current limit trip point	V_I = 3 V, output shorted(1)		3.0		A
		V_I = 6 V, output shorted(1)		3.5		
	Current-limit leading edge blanking time			100		ns
	Current-limit total response time			200		ns
THERMAL SHUTDOWN						
	Thermal-shutdown trip point(1)		135	150	165	°C
	Thermal-shutdown hysteresis(1)			10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$	Power MOSFET switches(4)	I_O = 1.5 A, V_I = 6 V(5)		240	480	mΩ
		I_O = 1.5 A, V_I = 3 V(5)		345	690	

(4) Includes package and bondwire resistance
(5) Matched MOSFETs, low side $r_{DS(on)}$ production tested, high side $r_{DS(on)}$ specified by design

7.5 Typical Characteristics

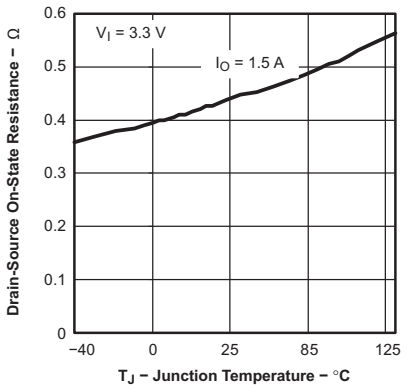


Figure 1. Drain-Source On-State Resistance vs Junction Temperature

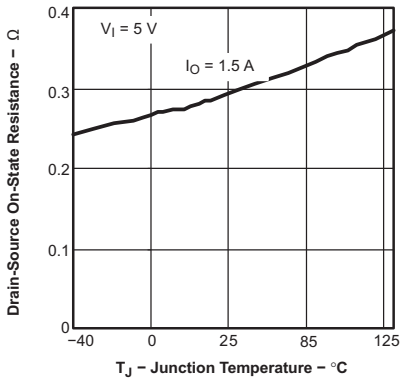


Figure 2. Drain-Source On-State Resistance vs Junction Temperature

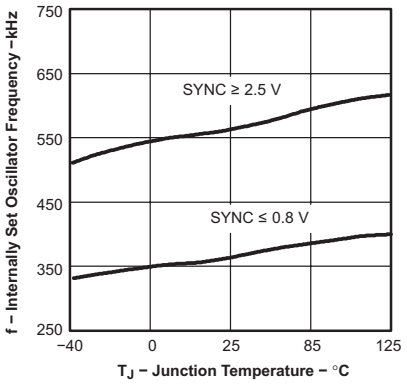


Figure 3. Internally Set Oscillatorfrequency vs Junction Temperature

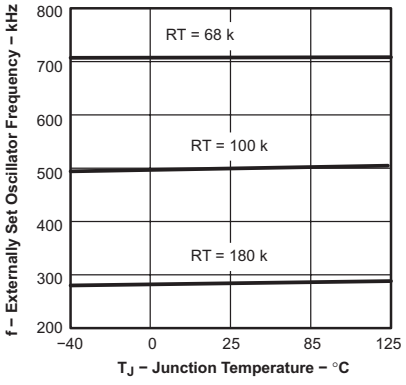


Figure 4. Externally Set Oscillatorfrequency vs Junction Temperature

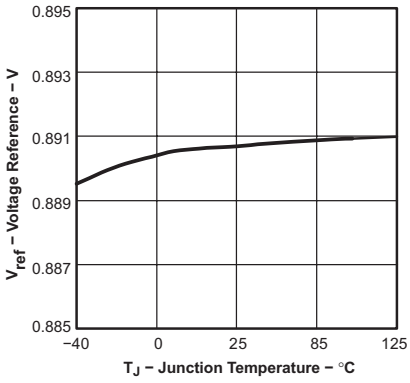


Figure 5. Voltage Reference vs Junction Temperature

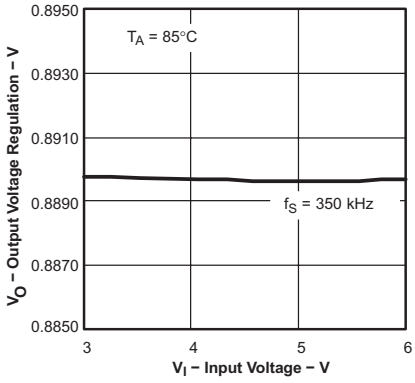


Figure 6. Output Voltage Regulation vs Input Voltage

Typical Characteristics (continued)

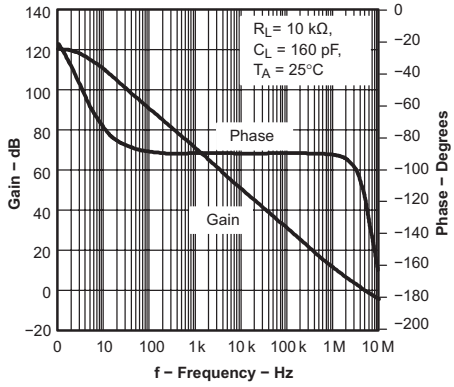


Figure 7. Error Amplifieropen Loop Response

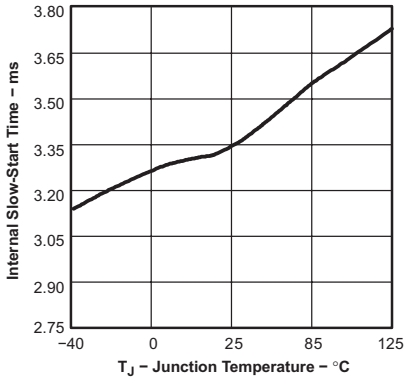


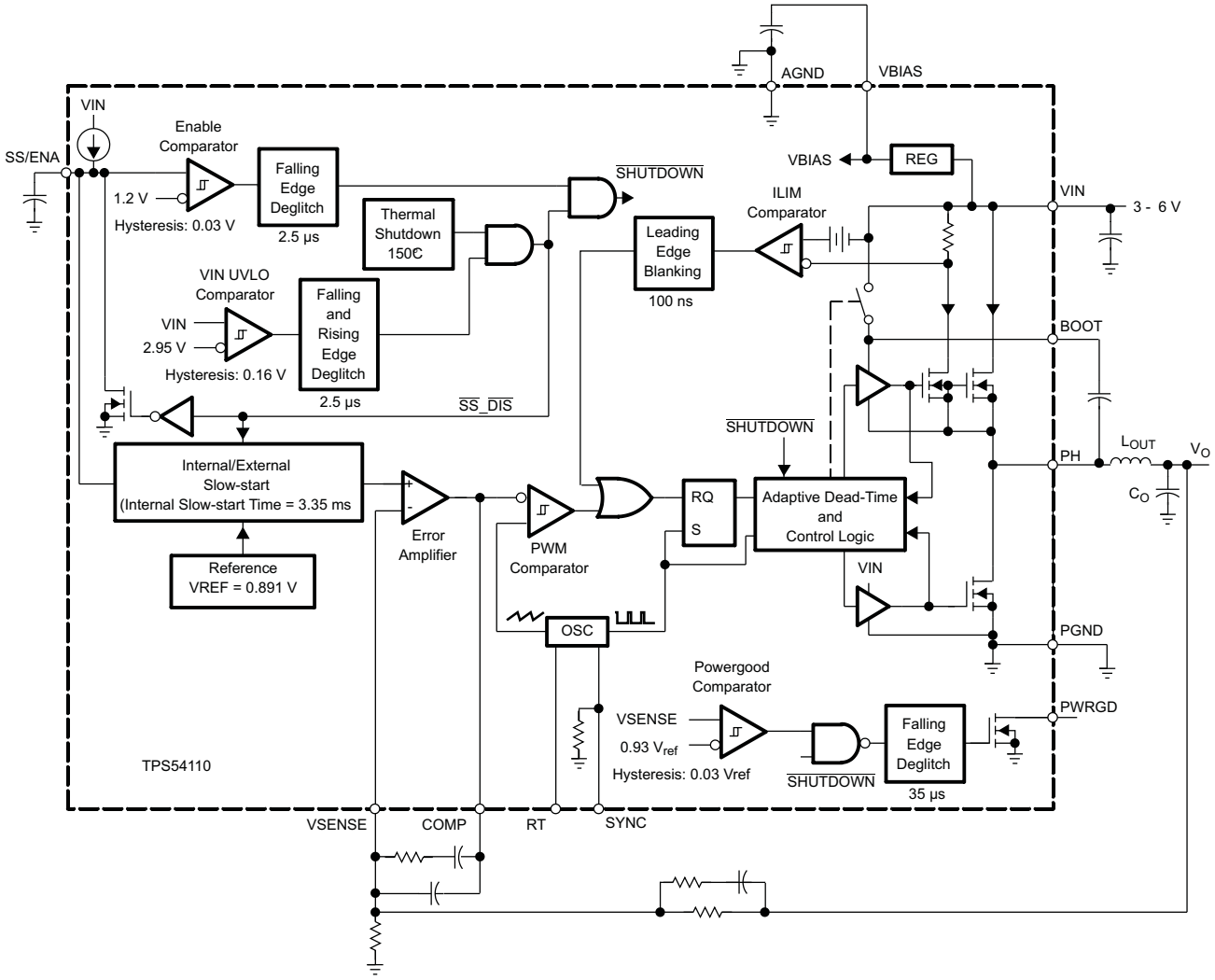
Figure 8. Internal Slow-Start Time vs Junction Temperature

8 Detailed Description

8.1 Overview

The TPS54110 low-input-voltage high-output-current synchronous-buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high- performance, voltage error amplifier that provides high performance under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 VBIAS Regulator (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. Place the bypass capacitor close to the VBIAS pin and returned to AGND. External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.7 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

8.3.2 Voltage Reference

The voltage reference system produces a precise V_{ref} signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54110 because it cancels offset errors in the scale and error amplifier circuits.

8.3.3 Oscillator and PWM Ramp

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the SYNC pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 kHz to 700 kHz by connecting a resistor from the RT pin to ground and floating the SYNC pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{SWITCHING FREQUENCY} = \frac{100\,\text{k}\Omega}{\text{R}} \times 500\,\text{kHz} \quad (1)$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 700 kHz by driving a synchronization signal into SYNC and connecting a resistor from RT to AGND. Choose an RT resistor that sets the free-running frequency to 80% of the synchronization signal. Table 1 summarizes the frequency selection configurations.

Table 1. Summary Of The Frequency Selection Configurations

SWITCHING FREQUENCY	SYNC PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	≥ 2.5 V	Float
Externally set 280 kHz to 700 kHz	Float	R = 68 k to 180 k
Externally synchronized frequency	Synchronization signal	R = RT value for 80% of external synchronization frequency

8.3.4 Error Amplifier

The high-performance, wide-bandwidth, voltage error amplifier sets the TPS54110 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L- and C-filter components to suit the particular application needs. Type-2 or type-3 compensation can be employed using external compensation components.

8.3.5 PWM Control

Signals from the error-amplifier output, oscillator, and current-limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control-logic block. During steady-state operation below the current-limit threshold, the PWM-comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse

duration. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error-amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error-amplifier output is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as V_{ref}. If the error-amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54110 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current-limit comparator remains tripped longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error-amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor, and consequently the output current. This process is repeated each cycle that the current-limit comparator is tripped.

8.3.6 Dead-Time Control and MOSFET Drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver does not turn on until the gate-drive voltage to the low-side FET is below 2 V. The low-side driver does not turn on until the voltage at the gate of the high-side MOSFETs is below 2 V. The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side driver is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external-component count.

8.3.7 Overcurrent Protection

Cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and differential amplifier and comparing it to the preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current-limit threshold. A 100-ns leading-edge blanking circuit prevents false tripping of the current limit. Current-limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current-sink operation is provided by thermal shutdown.

8.3.8 Thermal Shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown when the junction temperature decreases to 10°C below the thermal-shutdown trip point, and starts up under control of the slow-start circuit. Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. In a persistent-fault condition, the device cycles continuously; starting up under control of the soft-start circuit, heating up due to the fault, and then shutting down upon reaching the thermal-shutdown point.

8.3.9 Power Good (PWRDG)

The power-good circuit monitors for undervoltage conditions on VSENSE. If the voltage on VSENSE is 7% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if V_{IN} is less than the UVLO threshold, or SS/ENA is low, or if thermal shutdown asserts. When VIN = UVLO threshold, SS/ENA = enable threshold, and VSENSE > 93% of V_{ref}, the open-drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35-µs falling-edge deglitch circuit prevent tripping of the power-good comparator due to high frequency noise.

8.4 Undervoltage Lockout (UVLO)

The TPS54110 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until V_{IN} exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

8.5 Slow-Start/Enable (SS/ENA)

The slow-start/enable pin provides two functions; first, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND. Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2V}{5\mu a} \tag{2}$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7V}{5\mu a} \tag{3}$$

The actual slow-start is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS54110 low-input-voltage high-output-current synchronous-buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high- performance, voltage error amplifier that provides high performance under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power-good output useful for processor/logic reset, fault signaling, and supply sequencing.

9.2 Typical Applications

9.2.1 Typical TPS54110 Application

Figure 9 shows the schematic diagram for a typical TPS54110 application. The TPS54110 can provide up to 1.5 A of output current at a nominal output voltage of 3.3 V. For proper thermal performance, the exposed PowerPAD underneath the device must be soldered down to the printed-circuit board.

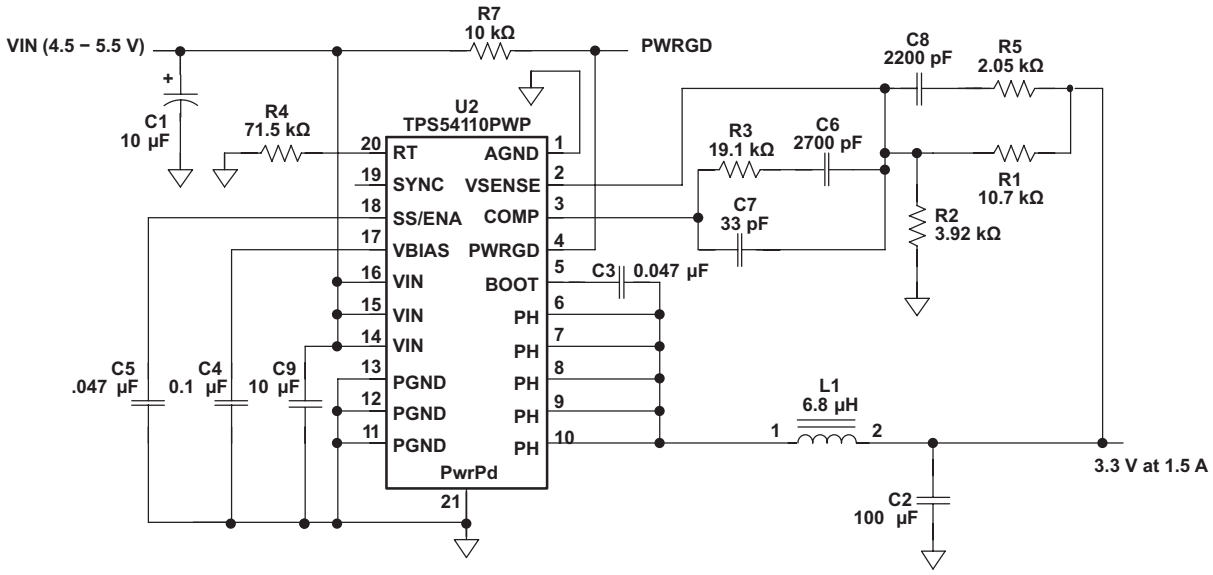


Figure 9. Application Schematic

Typical Applications (continued)

9.2.1.1 Design Requirements

The required parameters to begin the design process and values for this design example are listed in Table 2. As an additional constraint, the design is set up to be small size and low component height.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 5.5 V
Output voltage	3.3 V
Input ripple voltage	100 mV
Output ripple voltage	30 mV
Output current rating	1.5 A
Operating frequency	700 kHz

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Switching Frequency

The switching frequency is set within the range of 280 kHz to 700 kHz by connecting a resistor from the RT pin to AGND. Equation 4 is used to determine the proper RT value.

$$RT(k\Omega) = \frac{100 \times 500kHz}{f_{s(kHz)}} \quad (4)$$

In this example, the timing-resistor value chosen for R4 is 71.5 kΩ, setting the switching frequency to 700 kHz.

Alternately, the TPS54110 can be set to preprogrammed switching frequencies of 350 kHz or 550 kHz by connecting pins RT and SYNC as shown in Table 3.

Table 3. Design Parameters

FREQUENCY	RT	SYNC
350 kHz	Float	Float or AGND
550 kHz	Float	≥ 2.5 V

9.2.1.2.2 Input Capacitors

The TPS54110 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The minimum value for the decoupling capacitor, C9, is 10 uF. A high quality ceramic type X5R or X7R with a voltage rating greater than the maximum input voltage is recommended. A bulk input capacitor may be needed, especially if the TPS54110 circuit is not located within approximately 2 inches from the input voltage source. The capacitance value is not critical, but the voltage rating must be greater than the maximum input voltage including ripple voltage. The capacitor must filter the input ripple voltage to acceptable levels.

Input ripple voltage can be approximated by Equation 5:

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (5)$$

where

- $I_{OUT(MAX)}$ is the maximum load current
- f_{SW} is the switching frequency
- C_{BULK} is the bulk capacitor value
- ESR_{MAX} is the maximum series resistance of the bulk capacitor

Worst-case RMS ripple current is approximated by Equation 6:

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (6)$$

In this case the input ripple voltage is 66 mV with a 10-µF bulk capacitor. Figure 14 shows the measured ripple waveform. The RMS ripple current is 0.75 A. The maximum voltage across the input capacitors is V_{INMAX} + $\Delta V_{IN}/2$. The bypass capacitor and input bulk capacitor are each rated for 6.3 V and a ripple-current capacity of 1.5 A, providing some margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

9.2.1.2.3 Output Filter Components

Two components, L1 and C2, are selected for the output filter. Since the TPS54110 is an externally-compensated device, a wide range of filter-component types and values are supported.

9.2.1.2.3.1 Inductor Selection

Use Equation 7 to calculate the minimum value of the output inductor:

$$L_{MIN} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW}} \quad (7)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. For designs using low-ESR capacitors such as ceramics, use K_{IND} = 0.2. When using higher ESR output capacitors, K_{IND} = 0.1 yields better results. If higher ripple currents can be tolerated, K_{IND} can be increased allowing for a smaller output-inductor value.

This example design uses K_{IND} = 0.2, yielding a minimum inductor value of 6.29 µH. The next-higher standard value of 6.8 µH is chosen for this design. If a lower inductor value is desired, a larger amount of ripple current must be tolerated.

The RMS-current and saturation-current ratings of the output filter inductor must not be exceeded. The RMS inductor current can be found from Equation 8:

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8} \right)^2} \quad (8)$$

The peak inductor current is determined from Equation 9:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (9)$$

For this design, the RMS inductor current is 1.503 A and the peak inductor current is 1.673 A. The inductor chosen is a Coilcraft DS3316P-682 6.8 µH. It has a saturation current rating of 2.8 A and an RMS current rating of 2.2 A, easily meeting these requirements.

9.2.1.2.3.2 Capacitor Selection

The important design parameters for the output capacitor are dc voltage, ripple current, and equivalent series resistance (ESR). The dc-voltage and ripple-current ratings must not be exceeded. The ESR rating is important because along with the inductor current it determines the output ripple voltage level. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed-loop crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the closed-loop crossover frequency at less than 1/5 of the switching frequency. With high switching frequencies such as the 700 kHz frequency of this design, internal circuit limitations of the TPS54110 limit the practical maximum crossover frequency to about 100 kHz. To allow adequate phase gain in the compensation network, set the LC corner frequency to approximately one decade below the closed-loop crossover frequency. This limits the minimum capacitor value for the output filter to:

$$C_{OUT(MIN)} = \frac{1}{L_{OUT}} \times \left(\frac{K}{2\pi f_{CO}} \right)^2 \quad (10)$$

where

- K is the frequency multiplier for the spread between f_{LC}
- f_{CO}. K should be between 5 and 15, typically 10 for one decade of difference.

For a desired crossover of 60 kHz, K=10 and a 6.8 μH inductor, the minimum value for the output capacitor is 100 μF. The selected output capacitor must be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating factors must also be included. The maximum RMS ripple current in the output capacitor is given by Equation 11:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left[\frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C} \right]$$

where

- NC is the number of output capacitors in parallel (11)

The maximum ESR of the output capacitor is determined by the allowable output ripple specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter so the maximum specified ESR as listed in the capacitor data sheet is given by Equation 12:

$$ESR_{MAX} = N_C \times \left(\frac{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})} \right) \times \Delta V_{p\text{-}p(MAX)} \quad (12)$$

For this design example, a single 100-μF output capacitor is chosen for C2. The calculated RMS ripple current is 80 mA and the maximum ESR required is 87 mΩ. An example of a suitable capacitor is the Sanyo Poscap 6TPC100M, rated at 6.3 V with a maximum ESR of 45 mΩ and a ripple-current rating of 1.7 A.

Other capacitor types work well with the TPS54110, depending on the needs of the application.

9.2.1.2.4 Compensation Components

The external compensation used with the TPS54110 allows for a wide range of output-filter configurations. A large range of capacitor values and dielectric types are supported. The design example uses type 3 compensation consisting of R1, R3, R5, C6, C7 and C8. Additionally, R2 and R1 form a voltage-divider network that sets the output voltage. These component reference designators are the same as those used in the SWIFT Designer Software.

There are a number of different ways to design a compensation network. This procedure outlines a relatively simple procedure that produces good results with most output filter combinations. Use the SWIFT Designer Software for designs with unusually high closed-loop crossover frequencies; with low-value, low-ESR output capacitors such as ceramics; or if you are unsure about the design procedure.

A number of considerations apply when designing compensation networks for the TPS54110. The compensated error-amplifier gain must not be limited by the open-loop amplifier gain characteristics and must not produce excessive gain at the switching frequency. Also, the closed-loop crossover frequency must be set less than one fifth of the switching frequency, and the phase margin at crossover must be greater than 45 degrees. The general procedure outlined here meets these requirements without going into great detail about the theory of loop compensation.

First, calculate the output filter LC corner frequency using Equation 13:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} C_{OUT}}} \quad (13)$$

For the design example, f_{LC} = 6103 Hz.

Choose a closed-loop crossover frequency greater than f_{LC} and less than one fifth of the switching frequency. Also, keep the crossover frequency below 100 kHz, as the error amplifier may not provide the desired gain at higher frequencies. The 60-kHz crossover frequency chosen for this design provides comparatively wide loop bandwidth while still allowing adequate phase boost to ensure stability.

Next, the values for the compensation components that set the poles and zeros of the compensation network are calculated. Assuming an R1 value > than R5 and a C6 value > C7, the pole and zero locations are given by Equation 14 through Equation 17:

$$f_{Z1} = \frac{1}{2\pi R3 C6} \quad (14)$$

$$f_{Z2} = \frac{1}{2\pi R1 C8} \quad (15)$$

$$f_{P1} = \frac{1}{2\pi R5 C8} \quad (16)$$

$$f_{P2} = \frac{1}{2\pi R3 C7} \quad (17)$$

Additionally there is a pole at the origin, which has unity gain at a frequency:

$$f_{INT} = \frac{1}{2\pi R1 C6} \quad (18)$$

This pole is used to set the overall gain of the compensated error amplifier and determines the closed loop crossover frequency. Since R1 is given as 10 kΩ and the crossover frequency is selected as 60 kHz, the desired f_{INT} is calculated from Equation 19:

$$f_{INT} = \frac{10^{-0.74} \times f_{CO}}{2} \quad (19)$$

And the value for C6 is given by Equation 20:

$$C6 = \frac{1}{2\pi R1 f_{INT}} \quad (20)$$

Since C6 is calculated to be 2900 pF, and the location of the integrator crossover frequency is important in setting the overall loop crossover, adjust the value of R1 so that C6 is a standard value of 2700 pF, using Equation 21:

$$R1 = \frac{1}{2\pi C6 f_{LC}} \quad (21)$$

The value for R1 is 10.7 KΩ

The first zero, f_{Z1} is located at one half the output filter LC corner frequency, so R3 is calculated from:

$$R3 = \frac{1}{\pi C6 f_{LC}} \quad (22)$$

The second zero, f_{Z2} is located at the output filter LC corner frequency, so C8 is calculated from:

$$C8 = \frac{1}{2\pi R1 f_{LC}} \quad (23)$$

The first pole, f_{P1} is located to coincide with output filter ESR zero frequency. This frequency is given by:

$$f_{ESR0} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

where

- R_{ESR} is the equivalent series resistance of the output capacitor (24)

In this case, the ESR zero frequency is 35.4 kHz, and R5 is calculated from:

$$R5 = \frac{1}{2\pi C8 f_{ESR}} \quad (25)$$

The final pole is placed at a frequency high enough above the closed-loop crossover frequency to avoid causing an excessive phase decrease at the crossover frequency while still providing enough attenuation so that there is little or no gain at the switching frequency. The f_{P2} pole location for this circuit is set to 4 times the closed-loop crossover frequency and the last compensation component value C7 is derived:

$$C7 = \frac{1}{8\pi R3 f_{CO}} \tag{26}$$

Finally, calculate the R2 resistor value for the output voltage of 3.3 V using Equation 27:

$$R2 = \frac{R1 \times 0.891}{V_{OUT} - 0.891} \tag{27}$$

For this TPS54110 design, use R1 = 10.7 kΩ instead of 10.0 kΩ. R2 is then 3.92 kΩ.

Since capacitors are only available in a limited range of standard values, the nearest standard value was chosen for each capacitor. The measured closed-loop response for this design is shown in Figure 18.

9.2.1.2.5 Bias and Bootstrap Capacitors

Every TPS54110 design requires a bootstrap capacitor (C3), and a bias capacitor (C4). The bootstrap capacitor must be between 0.022 µF and 0.1 µF. This design uses 0.047 µF. The bootstrap capacitor is located between the PH pins and BOOT. The bias capacitor is connected between the VBIAS pin and AGND. Recommended values are 0.1 µF to 1 µF. This design uses 0.1 µF. Use high-quality ceramic capacitors with X7R or X5R grade dielectric for temperature stability. Place them as close to the device pins as possible.

9.2.1.3 Application Curves

All performance data shown for V_I = 5 V, V_O = 3.3 V, f_s = 700 kHz, T_A = 25°C, Figure 9

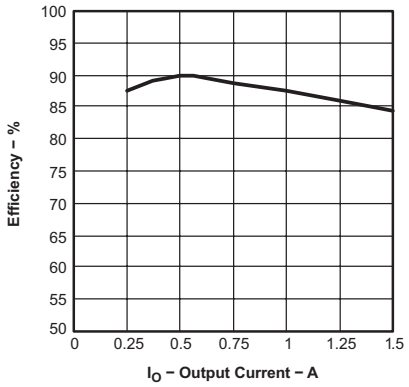


Figure 10. Efficiency vs Output Current

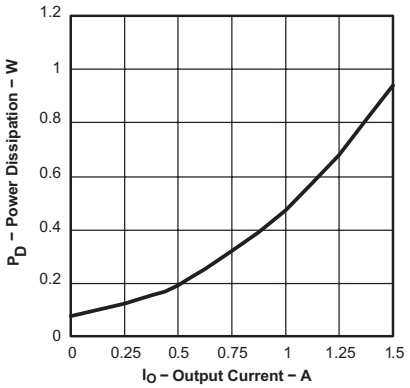


Figure 11. Power Dissipation vs Output Current

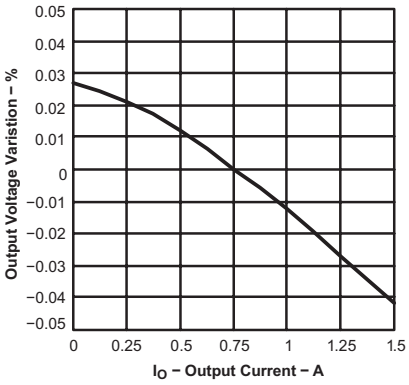


Figure 12. Load Regulation vs Output Current

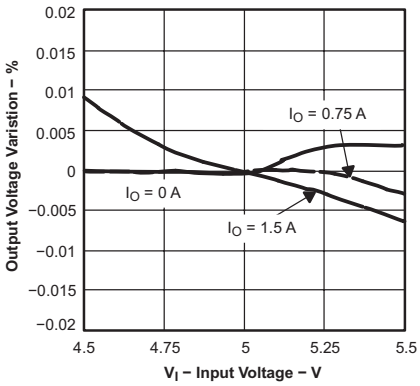


Figure 13. Line Regulation vs Input Voltage

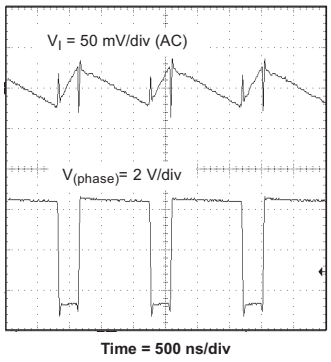


Figure 14. Input Voltage Ripple

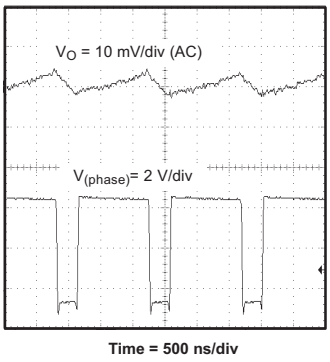


Figure 15. Output Voltage Ripple

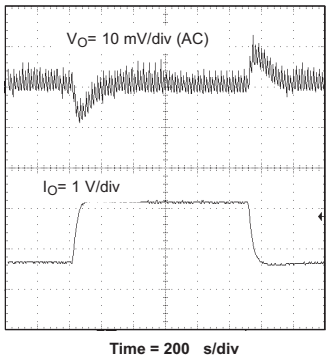


Figure 16. Output Voltage Transient Response

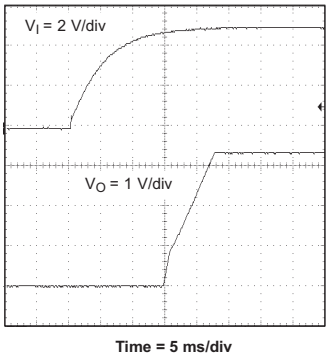


Figure 17. Start Up Waveform

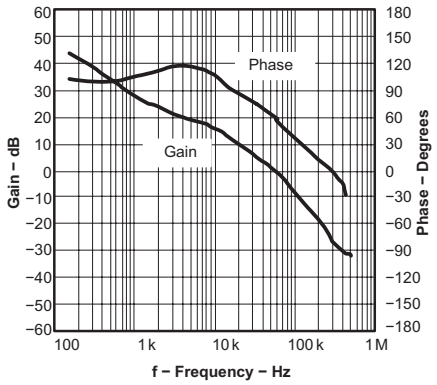


Figure 18. Measured Loop Response

9.2.2 Very-Small Form-Factor Application

Figure 19 shows an application schematic for a TPS54110 application designed for extremely small size. To achieve this goal, the design procedure given in the previous application circuit is modified. For example, in order to use a small-footprint Coilcraft DO3314-103MX inductor, the maximum-allowable inductor ripple current was increased above that normally specified. A small 0805 10-µF ceramic capacitor is used in the output filter. All the additional components are 0402 case size.

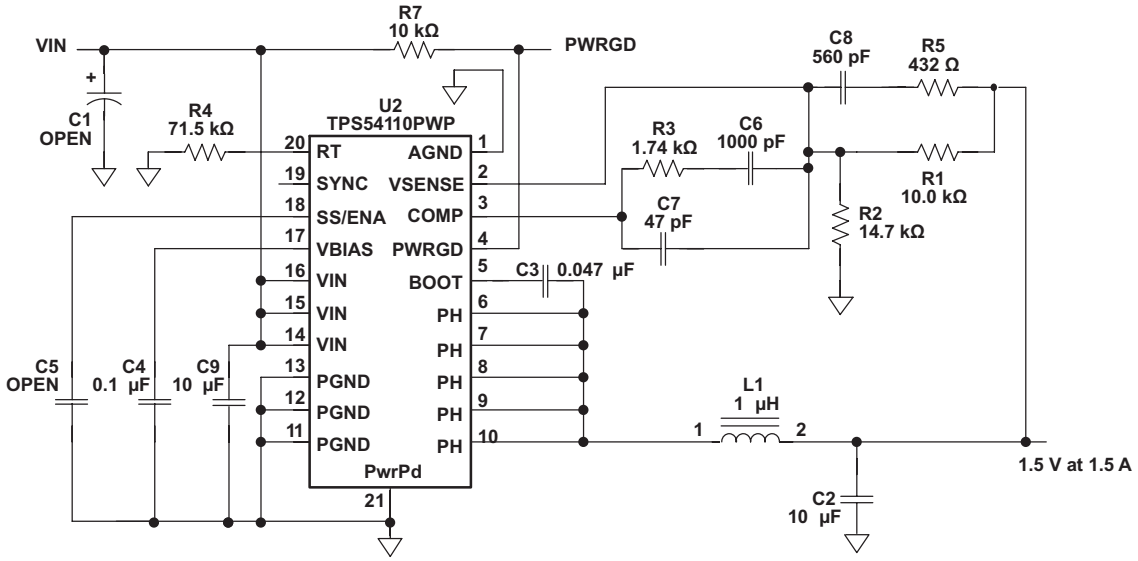


Figure 19. Small Form-Factor Reference Design

9.2.2.1 Design Requirements

See *Design Requirements*

9.2.2.2 Detailed Design Procedure

See *Detailed Design Procedure*

9.2.2.3 Application Curves

All performance data shown for V_I = 5 V, V_O = 1.5 V, F_S = 700 kHz, T_A = 25°C, Figure 19

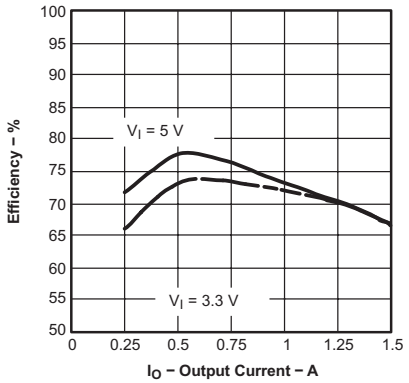


Figure 20. Efficiency vs Output Current

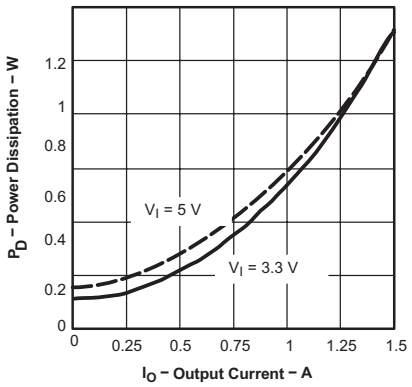


Figure 21. Power Dissipation vs Output Current

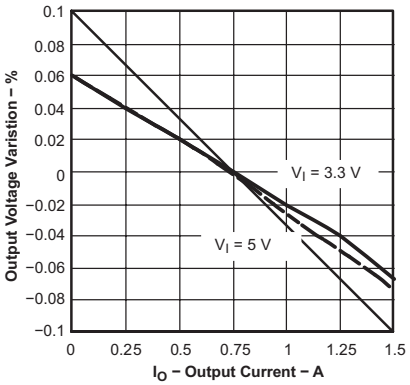


Figure 22. Load Regulation vs Output Current

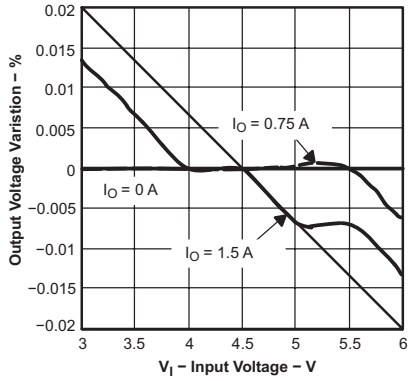


Figure 23. Line Regulation vs Input Voltage

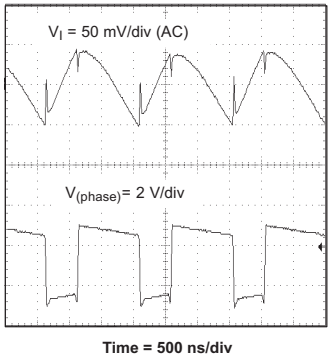


Figure 24. Input Voltage Ripple

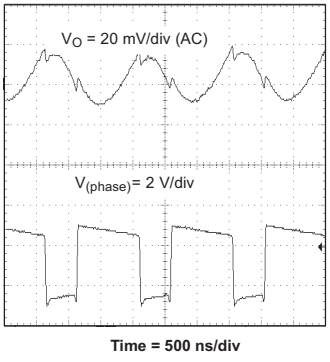


Figure 25. Output Voltage Ripple

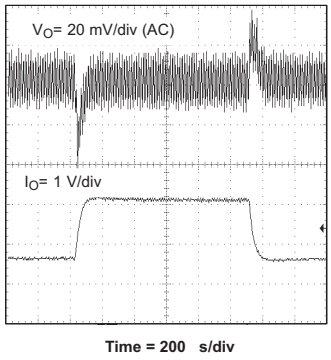


Figure 26. Output Voltage Transientresponse

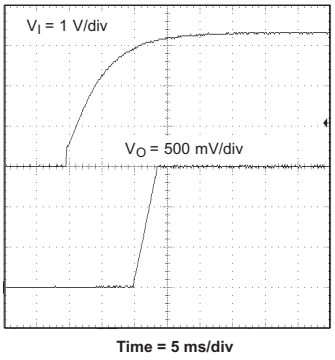


Figure 27. Start Up Waveform

9.2.3 Two-Output Sequenced-Startup Application

In Figure 28, the power-good output of U1 is used as a sequencing signal in a two-output design. Connecting the PWRGD pin of U1 to the SS/ENA pin of U2 causes the 1.5-V output to ramp up after the 3.3-V output is within regulation. Figure 29 shows the start-up waveforms associated with this circuit.

When V_{IN} reaches the UVLO-start threshold, the U1 output ramps up towards the 3.3-V set point. After the output reaches 90 percent of 3.3 V, the U1 asserts the power-good signal driving the U2 SS/ENA input high. The output of U2 then ramps up towards the final output set point of 1.5 V.

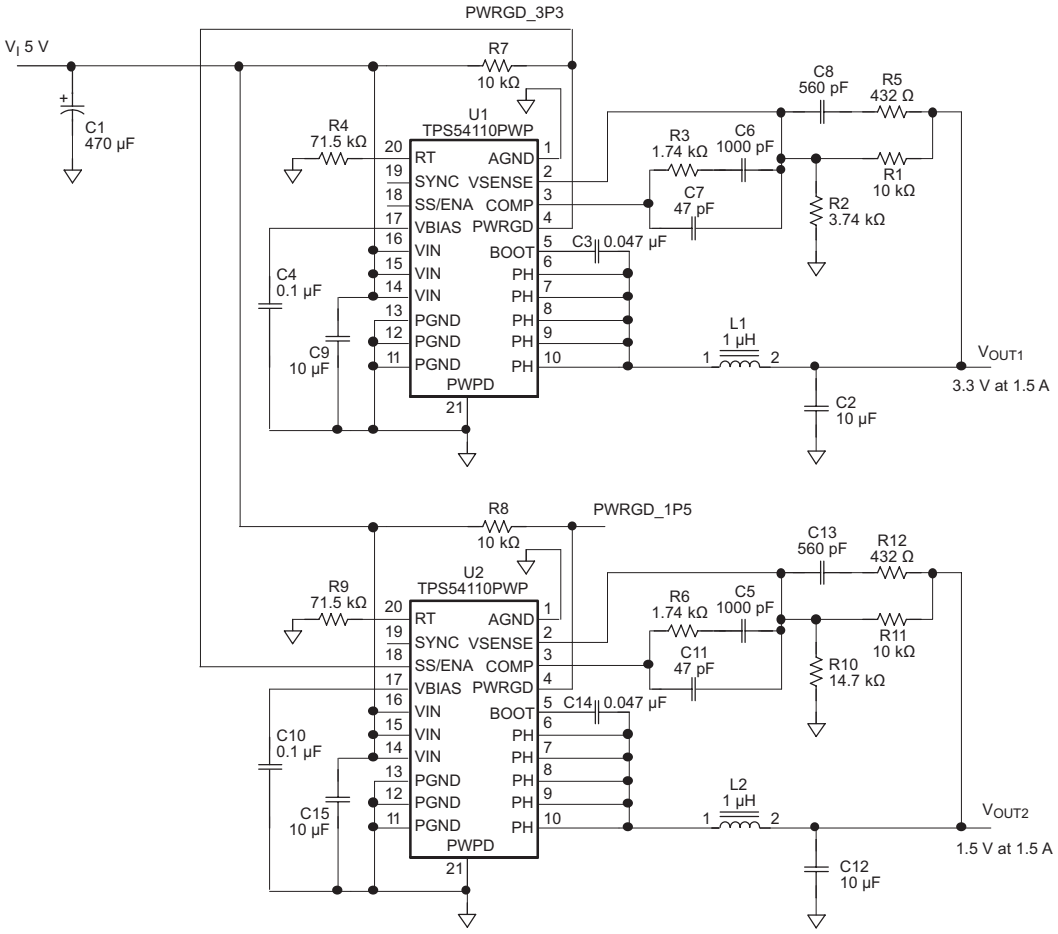


Figure 28. TPS54110 Sequencing Application Circuit

9.2.3.1 Design Requirements

See *Design Requirements*

9.2.3.2 Detailed Design Procedure

See *Detailed Design Procedure*

9.2.3.3 Application Curve

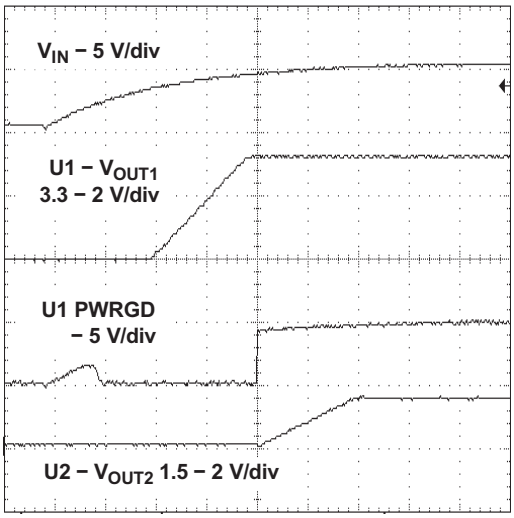


Figure 29. Sequencing Start-Up Waveforms

10 Layout

10.1 Layout Guidelines

The VIN pins are connected together on the printed board (PCB) and bypassed with a low-ESR ceramic bypass capacitor. Minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54110 ground pins. The recommended bypass capacitor is 10-μF (minimum) ceramic with X5R or X7R dielectric. The optimum placement is closest to the VIN pins and the AGND and PGND pins. See Figure 30 for an example layout. It has an area of ground on the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. Tie the AGND and PGND pins to the PCB ground area under the device as shown. Use a separate wide trace for the analog-ground path, connecting the voltage set-point divider, timing resistor RT, slow-start capacitor and bias-capacitor grounds. Tie the PH pins together and route to the output inductor. Since the PH connection is the switching node, locate the inductor very close to the PH pins, and minimize the area of the conductor to prevent excessive capacitive coupling. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. Connect the output-filter capacitor(s) as shown between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, L_{OUT}, C_{OUT}, and PGND as small as is practical. Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pin-out, they must be somewhat closely routed while maintaining as much separation as possible, yet keeping the layout compact. Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If a slow-start capacitor or RT resistor is used, or if the SYNC pin is used to select 350-kHz operating frequency, connect them to this trace as well.

10.2 Layout Example

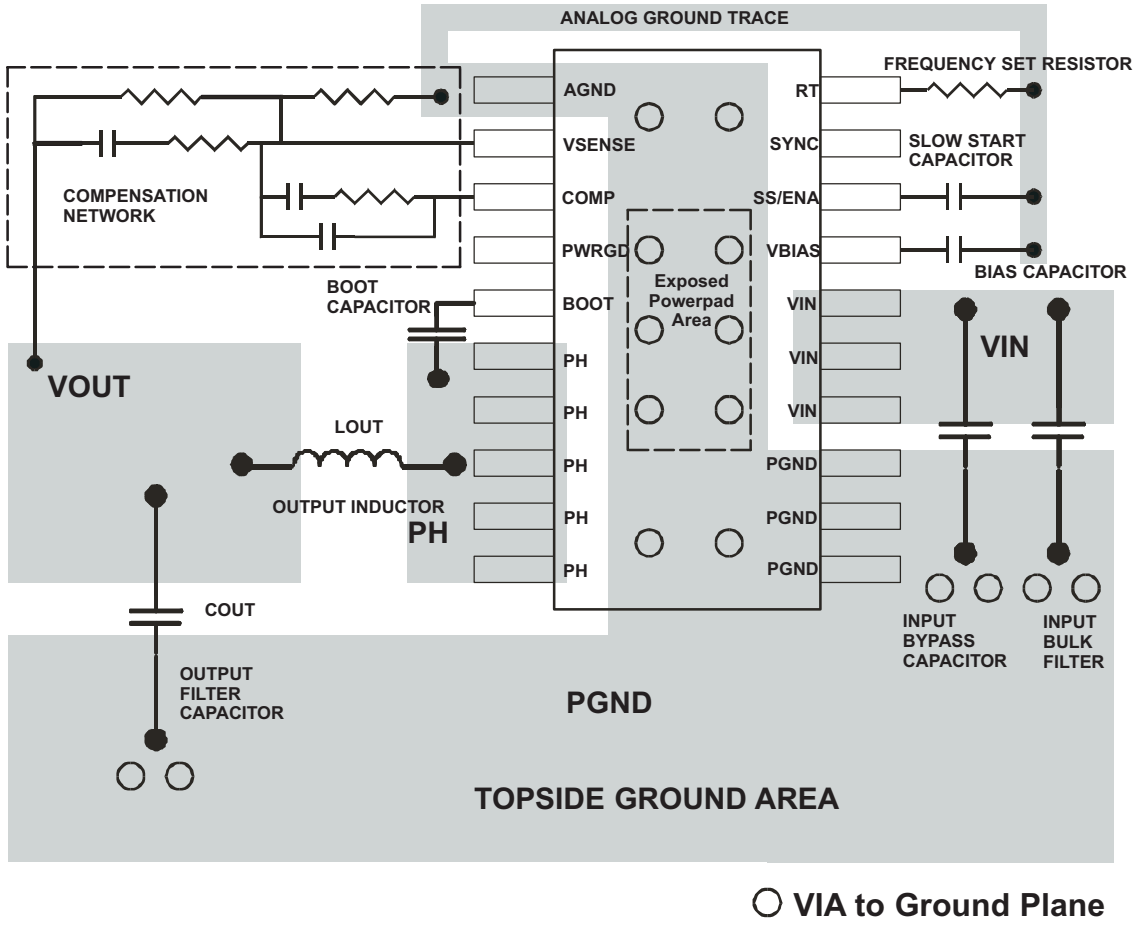


Figure 30. PC Board Layout Example

10.3 Layout Considerations For Thermal Performance

For operation at full rated load current, the analog ground plane must provide adequate heat dissipation area. A 3-inch-by-3-inch plane of 1-ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available. Connect the PowerPAD to the largest area available. Additional areas on the top or bottom layers also help dissipate heat. Use any area available when 1.5-A or greater operation is desired. Connect the exposed area of the PowerPAD to the analog ground-plane layer with 0.013-inch-diameter vias to avoid solder wicking through the vias. An adequate design includes six vias in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias in areas not under the device package enhance thermal performance.

10.4 Grounding and Powerpad Layout

The TPS54110 has two internal grounds (analog and power). Inside the TPS54110, the analog ground connects all noise-sensitive signals, while the power ground connects the noisier power signals. The PowerPAD must be tied directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54110, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground planes are recommended. Tie these two planes together directly at the IC to reduce noise between the two grounds. The only components that tie directly to the power-ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54110. The layout of the TPS54110 evaluation module represents recommended layout for a 2-layer board. Documentation for the TPS54110 evaluation module is obtained from the Texas Instruments web site under the TPS54110 product folder and in the application note, TI literature number SLVA109.

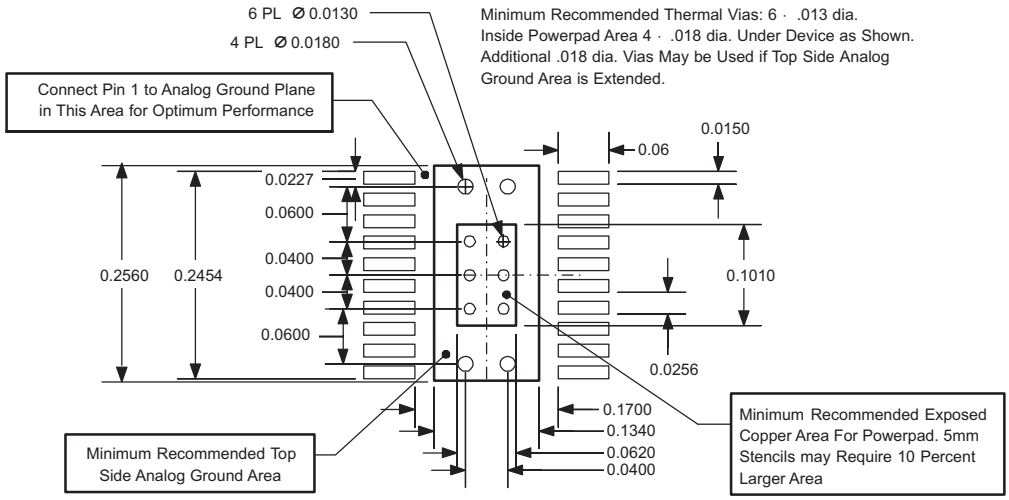


Figure 31. Recommended Land Pattern for 20-Pin PWP Powerpad

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54110PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS54110	Samples
TPS54110PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS54110	Samples
TPS54110PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS54110	Samples
TPS54110PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS54110	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS54110 :

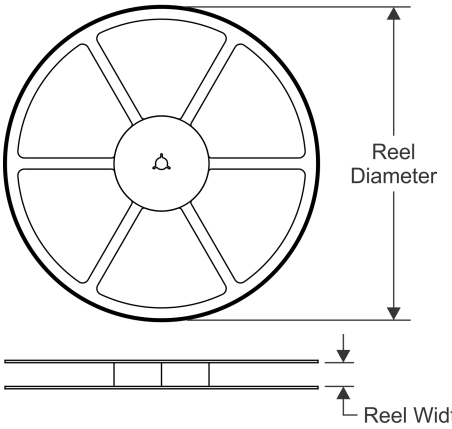
- Automotive: TPS54110-Q1

NOTE: Qualified Version Definitions:

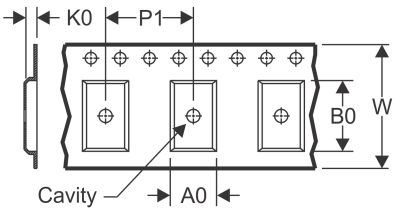
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

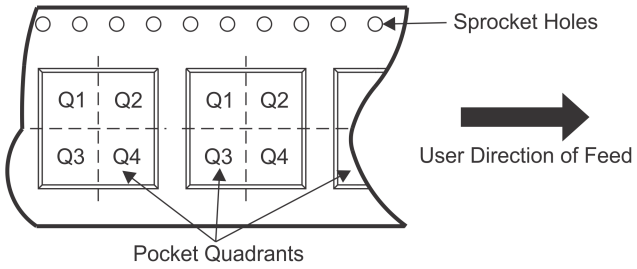


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

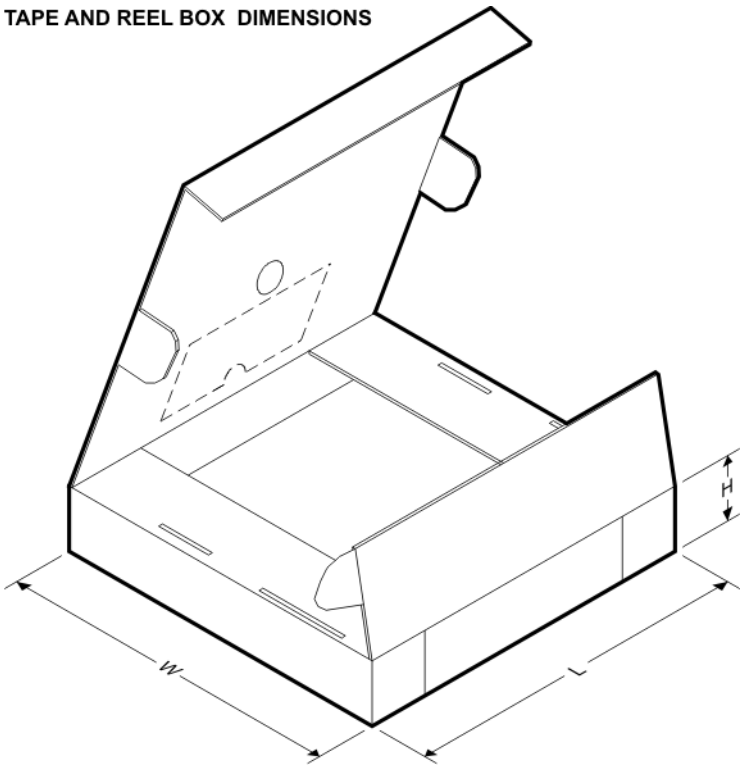
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54110PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

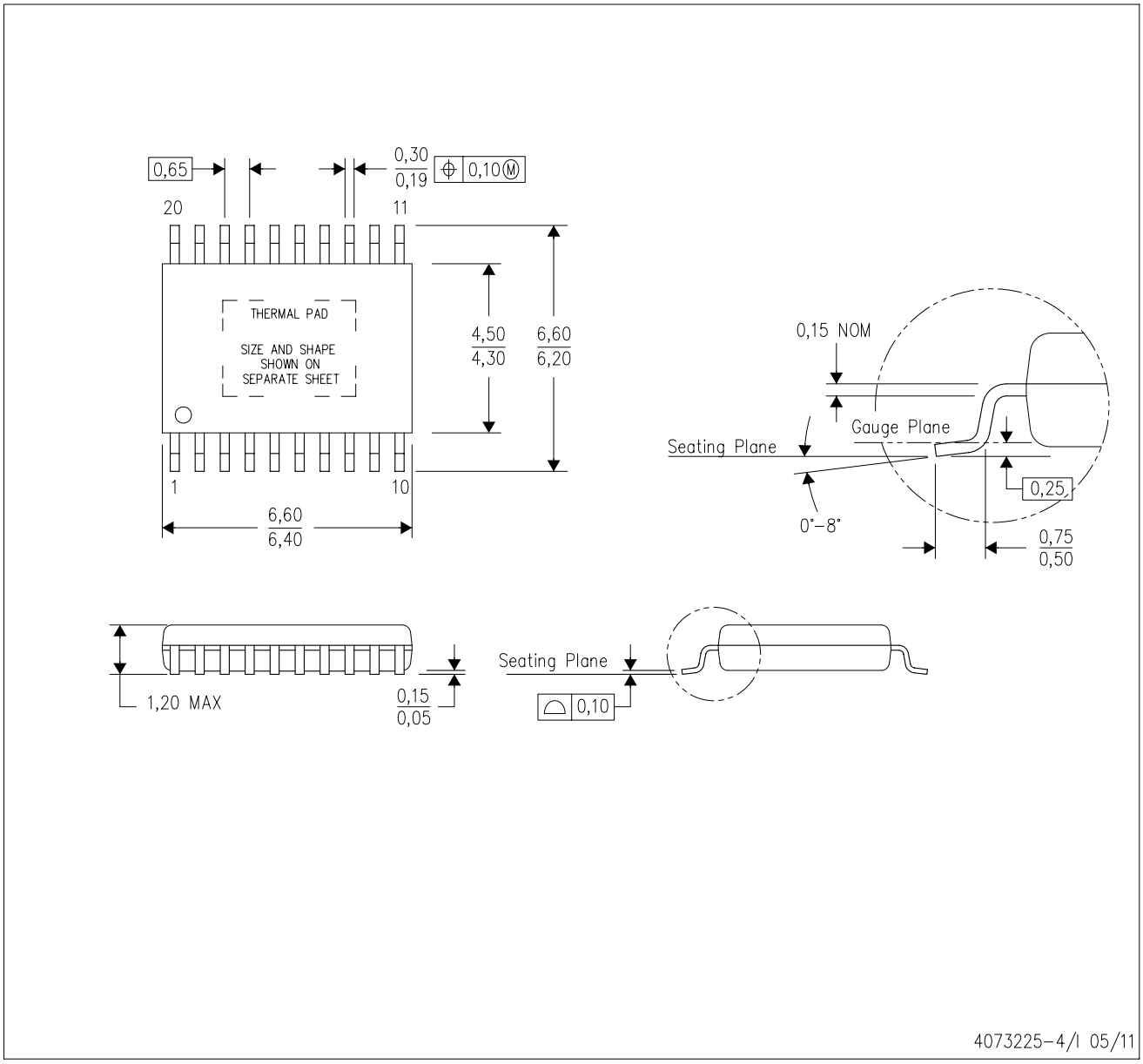
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54110PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

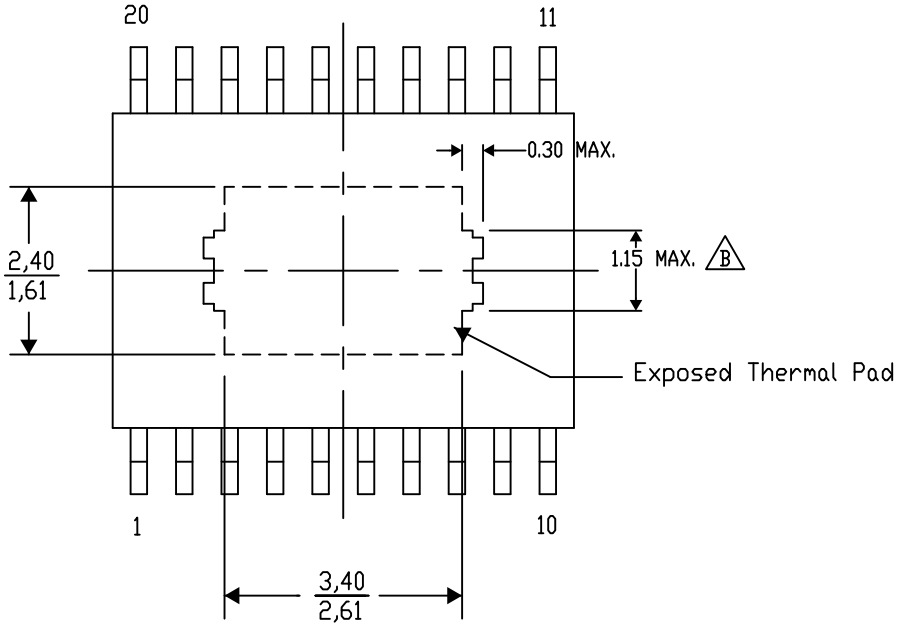
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

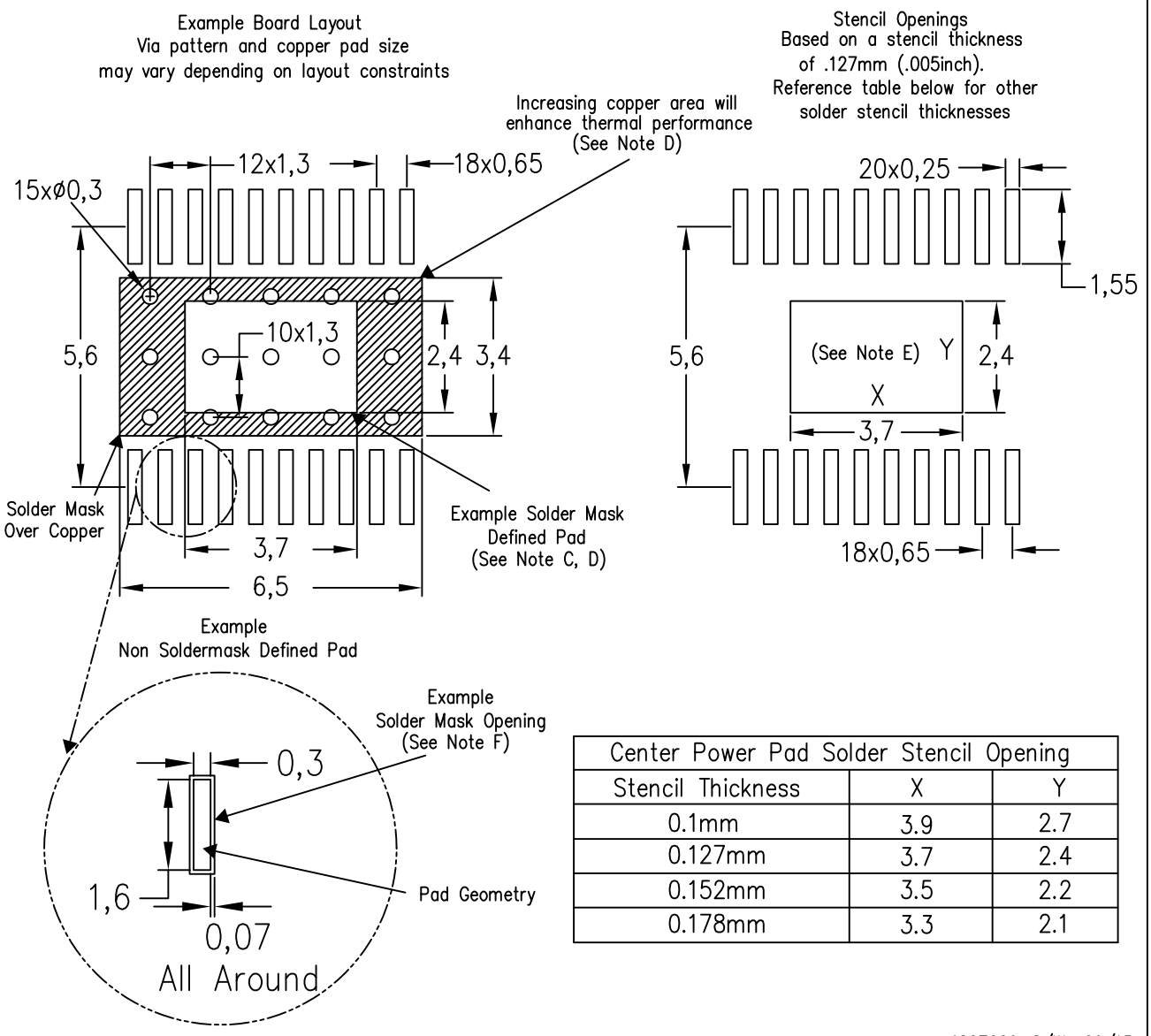
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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