Using the TPS43061 Boost Evaluation Module (EVM)

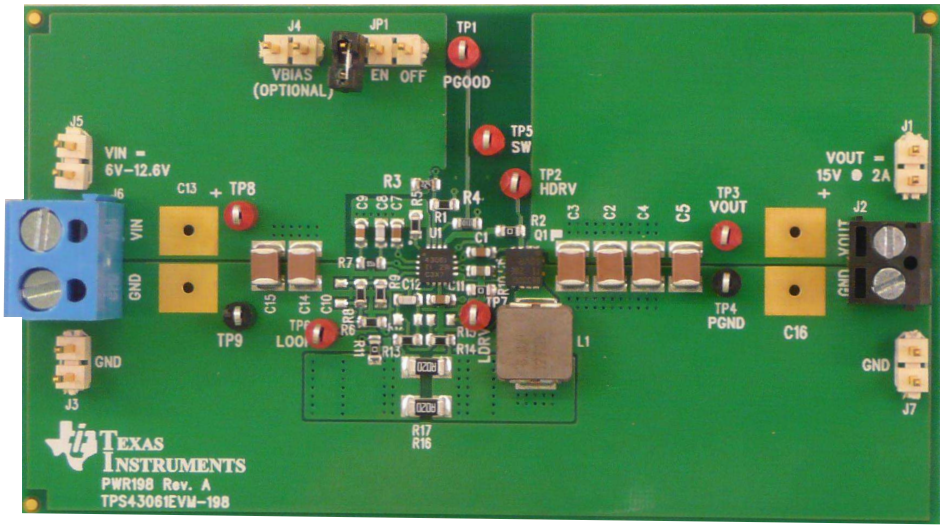


Figure 1. TPS43061EVM-198 EVM Board

This user's guide contains information for the TPS43061EVM-198 evaluation module (PWR198) including the performance specifications, schematic, and the bill of materials.

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1 Introduction

This user's guide contains background information for the TPS43061 as well as support documentation for the TPS43061EVM-198 evaluation module (PWR198). Also included are the performance specifications, schematic, and the bill of materials for the EVM.

1.1 Background

The TPS43061 is a DC-DC synchronous boost controller designed for a maximum output voltage of 60 V from an input voltage source of 4.5 V to 38 V. It has a 5.5-V gate-drive supply optimized for use with low Qg NexFETs. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small, printed-circuit-board areas that are possible when designing with the TPS43061 controller. The switching frequency is externally set at a nominal 750 kHz. The gate-drive circuitry for the external high-side and low-side FET is incorporated inside the TPS43061 package. The PWR198 uses the CSD86330Q3D NexFET power block integrating both the high-side and low-side FETs. External inductor DCR or resistor current sensing allows for an adjustable cycle-by-cycle current limit. The compensation components are external to the integrated circuit (IC), and an external resistor divider allows for an adjustable output voltage. Additionally, the TPS43061 provides an adjustable undervoltage lockout with hysteresis through an external resistor divider, adjustable slow-start time with an external capacitor and a power good output voltage indicator. The absolute maximum input voltage for the PWR198 based on the selected external components is 25 V.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS43061EVM-198	V_{IN} = 6 V to 12.6 V	I_{OUT} = 0 A to 2 A

1.2 Performance Specification Summary

A summary of the EVM performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 9 V and an output voltage of 15 V, unless otherwise specified. This EVM is designed and tested for V_{IN} = 6 V to 12.6 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS43061EVM-198 Performance Specification Summary

Specification	Test Conditions		MIN	TYP	MAX	Unit
V_{IN} voltage range			6	9	12.6	V
Output voltage set point				15		V
Output current range	V_{IN} = 6 V to 12.6 V		0		2	A
Line regulation	I_{OUT} = 2 A, V_{IN} = 6 V to 12.6 V			±0.1%		
Load regulation	V_{IN} = 9 V, I_{OUT} = 0.001 A to 2 A			±0.1%		
Load transient response	I_{OUT} = 0.5 A to 1.5 A	Voltage change		–300		mV
		Recovery time		400		µs
	I_{OUT} = 1.5 A to 0.5 A	Voltage change		210		mV
		Recovery time		400		µs
Loop bandwidth	V_{IN} = 9 V, I_{OUT} = 2 A			19		kHz
Phase margin	V_{IN} = 9 V, I_{OUT} = 2 A			68		°
Input voltage ripple	I_{OUT} = 2 A			10		mVpp
Output voltage ripple	I_{OUT} = 2 A			70		mVpp
Output rise time				25		ms
Operating frequency				750		kHz

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Table 2. TPS43061EVM-198 Performance Specification Summary (continued)

Specification	Test Conditions	MIN	TYP	MAX	Unit
Peak efficiency	TPS43061EVM-198, V_{IN} = 12 V, I_{OUT} = 2 A		97%		
DCM threshold	V_{IN} = 9 V		360		mA
Pulse skipping threshold	V_{IN} = 9 V		12		mA
No load input current	V_{IN} = 9 V		1.3		mA
UVLO start threshold			5.3		V
UVLO stop threshold			4.3		V

1.3 Modifications

These EVMs are designed to provide access to the features of the TPS43061. Some modifications can be made to this module. For further details please see the product data sheet.

1.3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R8. The value of R8 for a specific output voltage can be calculated using Equation 1, where R_{HS} is R8, R_{LS} is R9 and V_{FB} is 1.22 V. It s recommended to use a value of R9 near 10 kΩ.

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - V_{FB}}{V_{FB}} \quad (1)$$

Note: V_{IN} must be in a range so the minimum on-time is greater than the typical 100 ns and the minimum off-time is greater than the largest of typical 250 ns and 5% of the switching period.

1.3.2 Current Sensing

The default configuration of the EVM is for resistor current sensing. R13 and R14 are populated with R15 open. When adjusting the input voltage, output voltage or desired maximum output voltage, the current sense resistors R16 and R17 may need to be adjusted. The peak inductor current should first be calculated with Equation 2. Equation 3 is then used to calculate the required current sense resistor where V_{CS}typ is the current sense threshold. V_{CS}typ should be determined from the TPS43061 data sheet with the maximum duty cycle in the application. Ensure the current sense resistor is rated for the expected power dissipation. For inductor DCR current sensing, R14 should be left open while R15, R16 and R17 are shorted.

$$I_L peak = \frac{I_{OUT}}{1 - \frac{V_{OUT} - V_{IN}\,min}{V_{OUT}}} + \frac{V_{IN}\,min \times \frac{V_{OUT} - V_{IN}\,min}{V_{OUT}}}{2 \times L \times f_{SW}} \quad (2)$$

$$R_{CS} = \frac{V_{CS}typ}{1.2 \times I_L peak} \quad (3)$$

1.3.3 Slow-Start Time

Adjust the slow-start time by changing the value of C7. Equation 4 can be used to calculate the required capacitance based on a desired slow-start time, t_{SS}. I_{SS} is the charging current of 5-µA typical and V_{REF} is the internal reference voltage of 1.22 V. The EVM is set for a slow-start time of 25 ms using C7 = 0.1 µF.

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}} \quad (4)$$

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1.3.4 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R3 and R4. The EVM is set for a start voltage of 5.34 V and stop voltage of 4.31 V using R3 = 221 kΩ and R4 = 59.0 kΩ. Use Equation 5 and Equation 6 to calculate the required resistor values for R3 and R4 respectively for different start and stop voltages. The typical values of the constants in the two equations are as follows: V_{EN_DIS} = 1.14 V, V_{EN_ON} = 1.21 V, I_{EN_pup} = 1.8 µA, and I_{EN_hys} = 3.2 µA.

$$R_{UVLO_H} = \frac{V_{START} \times \left(\frac{V_{EN_DIS}}{V_{EN_ON}} \right) - V_{STOP}}{I_{EN_pup} \times \left(1 - \frac{V_{EN_DIS}}{V_{EN_ON}} \right) + I_{EN_hys}} \quad (5)$$

$$R_{UVLO_L} = \frac{R_{UVLO_H} \times V_{EN_DIS}}{V_{STOP} - V_{EN_DIS} + R_{UVLO_H} \times \left(I_{EN_pup} + I_{EN_hys} \right)} \quad (6)$$

1.3.5 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the VIN inputs are the same with R11 shorted. The single input voltage is supplied to J6. If desired, the two input voltage rails may be separated by removing R11. The control logic input voltage can be supplied to J4 and the power stage input voltage to J6.

1.3.6 Further Modification

Be aware, changing the input and output of conditions of the EVM will impact the design. It may also be necessary to modify the inductor, output capacitor and compensation components for the desired performance in the application. Additionally the CSD86330Q3D power block limits the output voltage to a maximum recommend output voltage of 22 V. Please see the data sheet or the excel design spreadsheet located in the product folder for details.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the EVM. The section also includes test results typical for the EVM covering efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start up and shutdown.

2.1 Input/Output Connections

This EVM includes input/output connectors and test points as shown in Table 3. A power supply capable of supplying at least 6 A must be connected to J6 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load-current capability must be 2 A. Wire lengths must be minimized to reduce losses in the wires. If any modification is done to the EVM design, an input supply and load rated for the new design are required. Test point TP8 provides a place to monitor the V_{IN} input voltages with TP9 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

Table 3. EVM Connectors and Test points

Reference Designator	Function
J1	2-pin header for V_{OUT} voltage connections
J2	V_{OUT}, 15 V at 2-A maximum
J3	2-pin header for GND connections
J4	2-pin header for optional V_{BIAS} input voltage connections (see Section 1.3.5)
J5	2-pin header for V_{IN} input voltage connections
J6	V_{IN} (see Table 1 for V_{IN} range)
J7	2-pin header for GND connections
JP1	3-pin header for EN jumper. Install jumper from pins 1-2 to enable or pins 2-3 to disable.

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Table 3. EVM Connectors and Test points (continued)

Reference Designator	Function
TP1	PGOOD test point for power good output voltage indicator
TP2	HDRV test point for high-side gate-drive voltage
TP3	V_{OUT} test point at V_{OUT} connector
TP4	GND test point at V_{OUT} connector
TP5	SW test point for switch node voltage
TP6	Test point between voltage divider network and output used for loop response measurements.
TP7	LDRV test point for low-side gate-drive voltage
TP8	V_{IN} test point at V_{IN} connector
TP9	GND test point at V_{IN}

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 2 A with V_{IN} = 12 V, and then decreases as the load current increases towards maximum load. Figure 2 shows the efficiency for the EVM brought to current limit for each input voltage. Dotted-line efficiency data was measured with Wurth Elektroniks 744311330. Measurements are taken at ambient temperature of 25°C. The efficiency may be lower at higher ambient temperatures due to temperature variation in the drain-to-source resistance of the selected external MOSFETs.

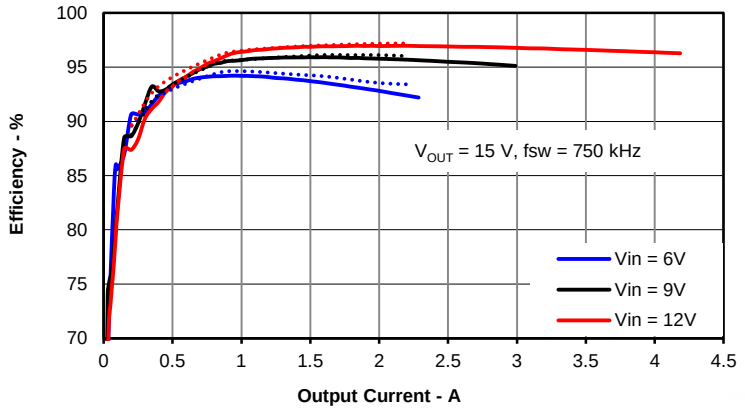


Figure 2. Efficiency Versus Load Current

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2.3 Output Voltage Regulation

The load regulation for the EVM is shown in Figure 3. The line regulation for the EVM is shown in Figure 4. Measurements are given for an ambient temperature of 25°C.

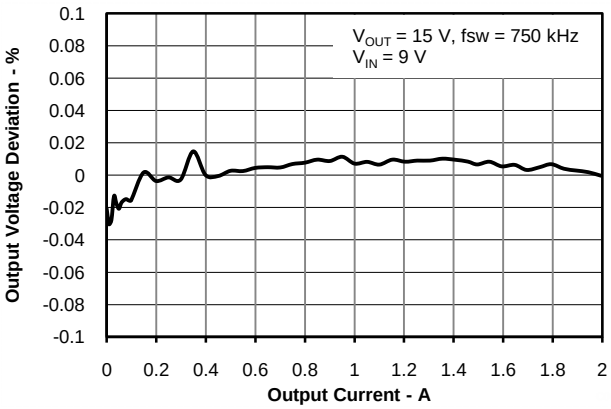


Figure 3. Regulation Versus Output Current

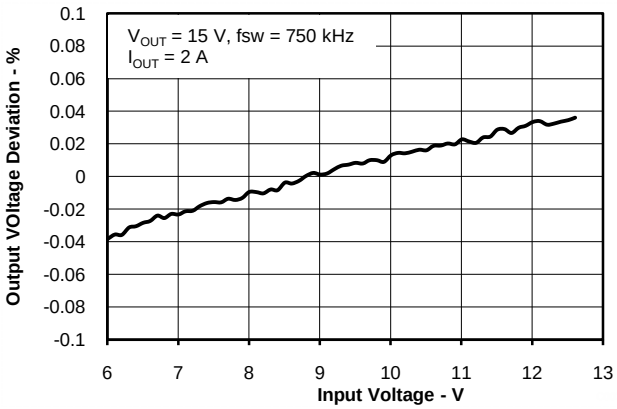


Figure 4. Regulation Versus Input Voltage

2.4 Load Transients and Loop Response

The EVM response to load transients is shown in Figure 5. The current step is from 25% to 75% of maximum rated load at 9 V input. The current step-slew rate is 100 mA/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

The EVM loop-response characteristics are shown in Figure 6. Gain and phase plots are shown for V_{IN} voltage of 9 V. Load current for the measurement is 2 A.

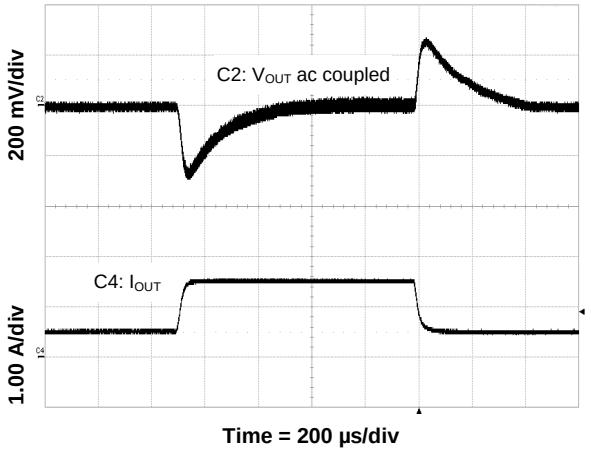


Figure 5. Load Transient Response

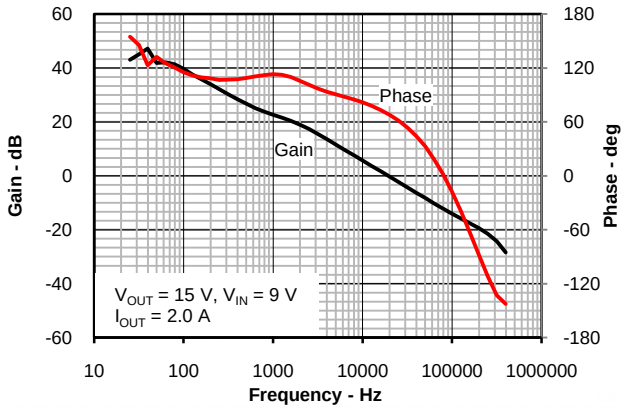


Figure 6. Loop Response

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2.5 Output Voltage Ripple

The EVM continuous conduction mode (CCM) output voltage ripple is shown in Figure 7. The output current is the rated full load of 2 A and V_{IN} = 9 V. The voltage ripple is measured directly across the output capacitors.

The discontinuous conduction mode (DCM) output voltage ripple is shown in Figure 8. The output current is 0.15 A and V_{IN} = 9 V.

The pulse skip mode output voltage ripple is shown in Figure 9. There is no external load on the output and V_{IN} = 9 V.

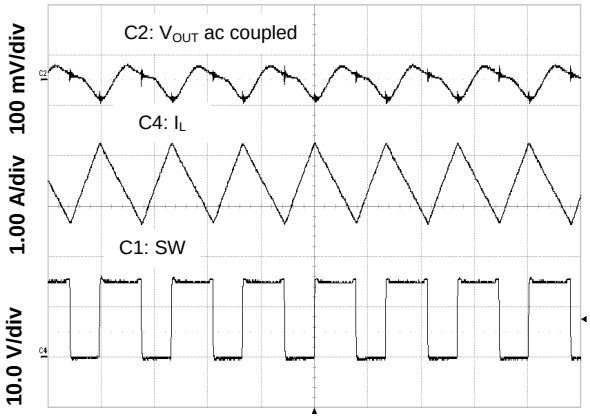


Figure 7. Output Voltage Ripple CCM

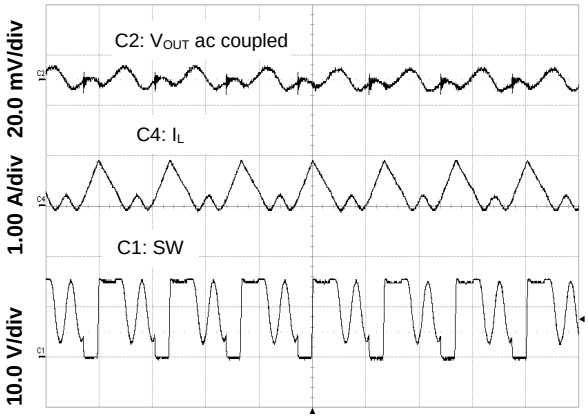


Figure 8. Output Voltage Ripple DCM

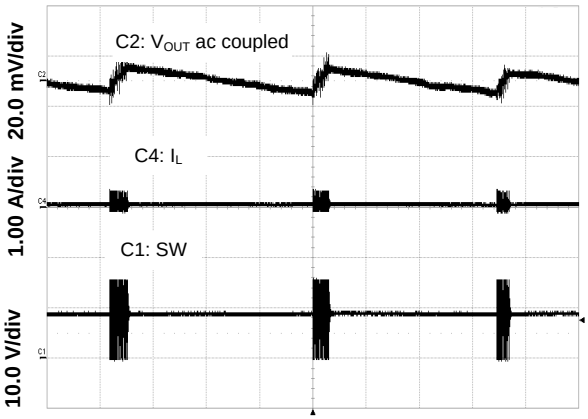


Figure 9. Output Voltage Ripple Pulse Skip Mode

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2.6 Input Voltage Ripple

The EVM CCM input voltage ripple is shown in Figure 10. The output current is the rated full load of 2 A and V_{IN} = 9 V. The voltage ripple is measured directly across the input capacitors.

The DCM input voltage ripple is shown in Figure 11. The output current is 0.15 A and V_{IN} = 9 V.

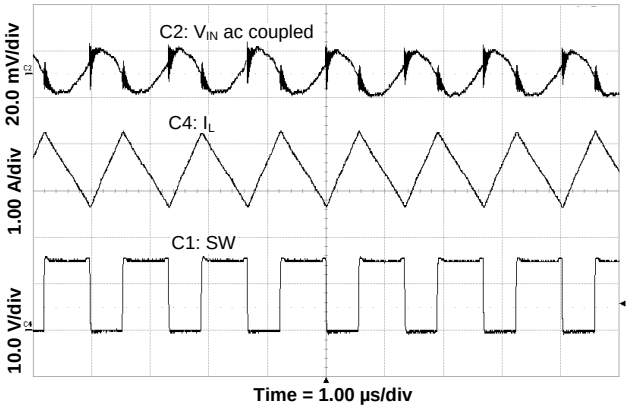


Figure 10. Input Voltage Ripple CCM

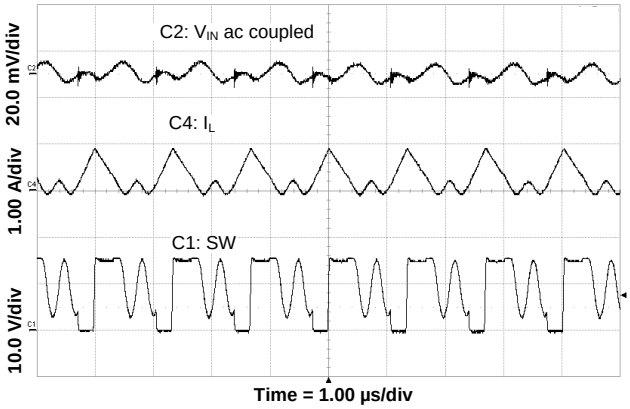


Figure 11. Input Voltage Ripple DCM

2.7 Start Up

The start up waveforms are shown in Figure 12 and Figure 13. The input voltage for these plots is 9 V and the output has a 2-A resistive load. In Figure 12 the input voltage supply is turned on and V_{IN} begins rising. Both the VCC and VOUT rail initially rise with V_{IN}. When the input reaches the undervoltage lockout threshold set by the external resistor divider, the device can begin switching and the output ramps up to the set value of 15 V with the slow-start voltage. PGOOD goes high when VOUT is in regulation.

In Figure 13 the input voltage is applied with EN held low. The output voltage is a diode drop below the input voltage and VCC is disabled. When EN is released, the start up sequence begins with VCC coming into regulation and the output ramps up to the set value of 15 V. PGOOD goes high when VOUT is in regulation.

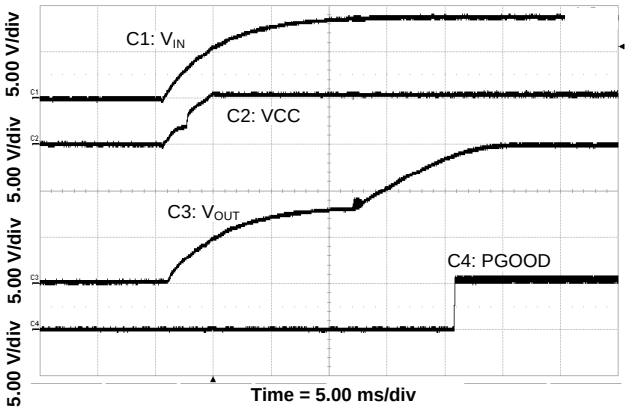


Figure 12. Start Up Relative to V_{IN}

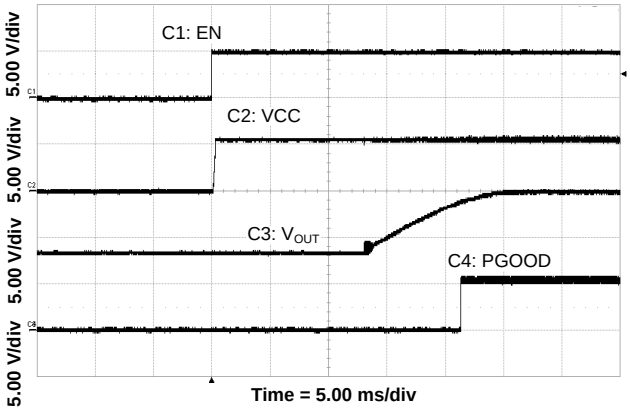


Figure 13. Start Up Relative to EN

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2.8 Shutdown

The shutdown waveforms are shown in Figure 14 and Figure 15. In Figure 14 the input voltage is removed, and when the input falls below the undervoltage lockout threshold set by the EN resistor divider, the TPS43061 shuts down, PGOOD is pulled low and the output falls to ground. The output has a 2-A resistive load.

In Figure 15 the input voltage is held at 9 V with no load and EN is shorted to ground. When EN is grounded, the TPS43061 is disabled, PGOOD is pulled low and the output voltage discharges to VIN.

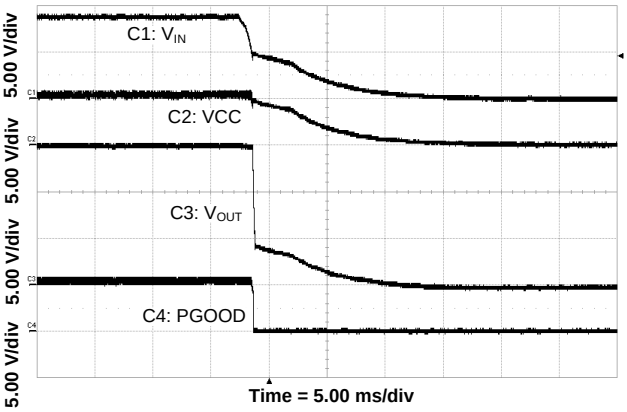


Figure 14. Shutdown Relative to V_{IN}

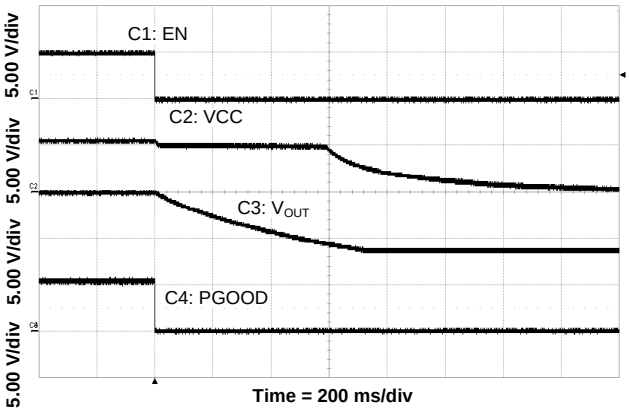


Figure 15. Shutdown Relative to EN

2.9 Gate-Drive Signals

In Figure 16 the gate-drive signals for the high-side and low-side FETs can be seen with the switching node are shown. The input voltage is 9 V and the output has a 2-A load.

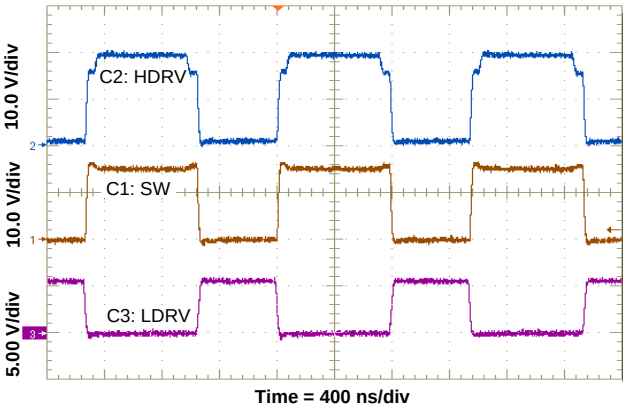


Figure 16. Gate-Drive Signals

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3 Schematic and Bill of Materials

This section presents the EVM schematic and bill of materials.

3.1 Schematic

Figure 17 is the schematic for the EVM.

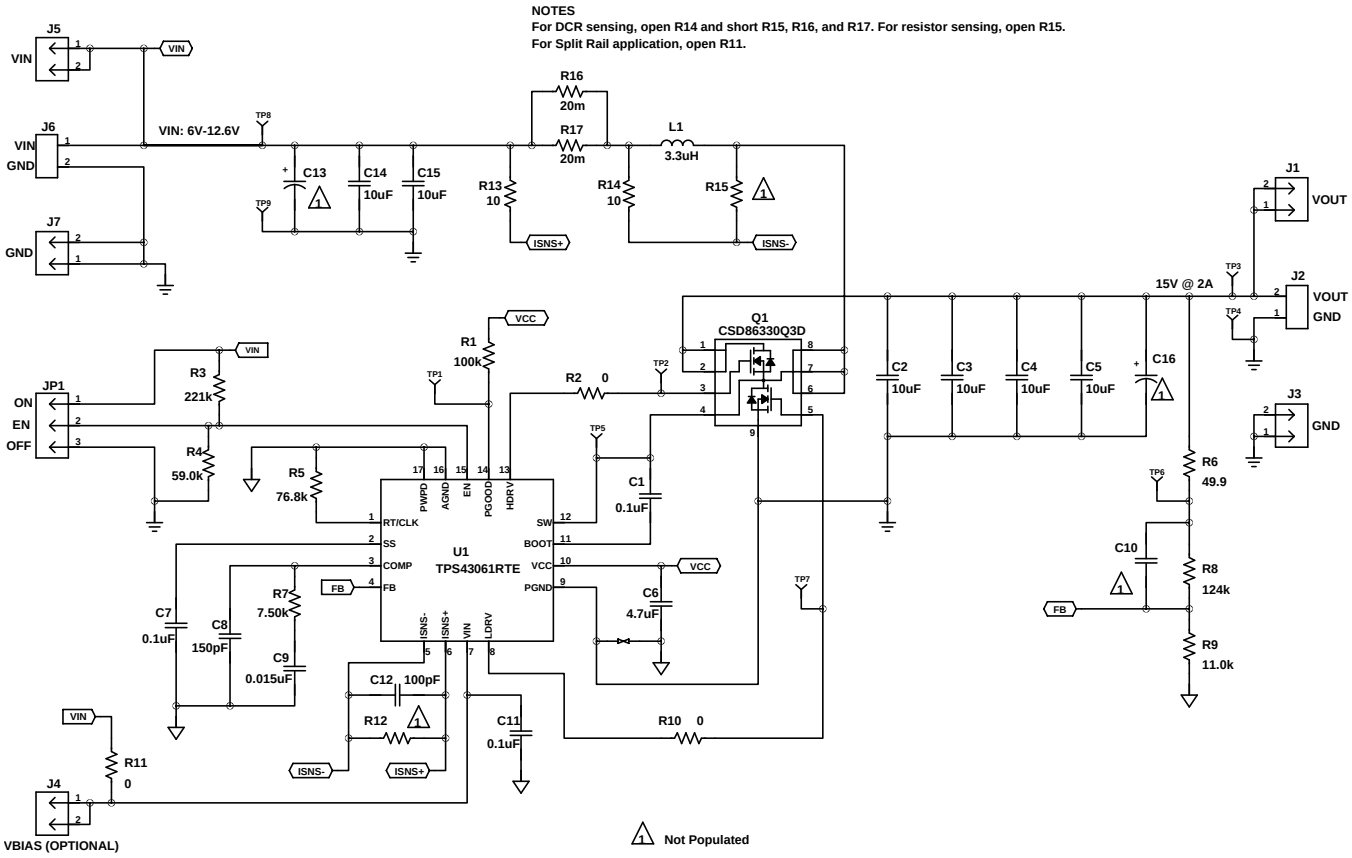


Figure 17. TPS43061EVM-198 Schematic

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3.2 Bill of Materials

Table 4 presents the bill of materials for the EVM.

Table 4. TPS43061EVM-198 Bill of Materials

Qty	RefDes	Value	Description	Size	Part Number	MFR
1	C6	4.7uF	Capacitor, Ceramic, 16V, X5R, 10%	0603	STD	STD
1	C8	150pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	STD	STD
1	C9	0.015uF	Capacitor, Ceramic, 50V, X7R, 10%	0603	STD	STD
0	C10	Open	Capacitor, Ceramic, 10V, X7R, 10%	0603	STD	STD
1	C12	100pF	Capacitor, Ceramic, 25V, X7R, 20%	0603	STD	STD
3	C1 C7 C11	0.1uF	Capacitor, Ceramic, 25V, X7R, 10%	0603	STD	STD
5	C2-5 C14-15	10uF	Capacitor, Ceramic Chip, 25V, X5R, 10%	1210	STD	STD
0	C13 C16	Open	Capacitor	Multi sizes	Engineering Only	STD
5	J1 J3-5 J7	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	J2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
1	J6	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
1	JP1	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	L1	3.3uH	Inductor, SMT, 6.0A, 30-milliohm	0.255 x 0.270 inch	IHLP2525CZER3R3M01 or 744311330	Vishay Wurth Elektronik
1	Q1	CSD86330Q3D	MOSFET, Synchronous Buck NexFET Power Block	QFN-8 POWER	CSD86330Q3D	TI
1	R1	100k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R3	221k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R4	59.0k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R5	76.8k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R6	49.9	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R7	7.50k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R8	124k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R9	11.0k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
0	R12 R15	Open	Resistor, Chip, 1/16W, 1%	0603	STD	STD
2	R13-14	10	Resistor, Chip, 1/16W, 1%	0603	STD	STD
2	R16-17	20m	Resistor, Chip, 1/2W, 1%, 100ppm	1206	PF1206FRF070R02L	Yageo
3	R2 R10-11	0	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	SH1		Short jumper, 100mil	0.100 inch	929950-00	3M
2	TP4 TP9	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
7	TP1-3 TP5-8	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
1	U1	TPS43061RTE	IC, Wide VIN Current Mode Synchronous Boost Controller	VQFN	TPS43061RTE	TI
1	--		PCB, 3.2 In x 1.8 In x 0.062 In		PWR198	Any
Notes:	1. These assemblies are ESD sensitive, ESD precautions shall be observed.					
	2. These assemblies must be clean and free from flux and all contaminants.					
	Use of no clean flux is not acceptable.					
	3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.					
	4. Ref designators marked with an asterisk ('**') cannot be substituted.					
	All other components can be substituted with equivalent MFG's components.					

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4 Board Layout

This section provides a description of the EVM, board layout, and layer illustrations.

4.1 Layout

The board layout for the EVM is shown in Figure 18 through Figure 22. This design has 4 layers of 2-oz copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and SW. Also on the top layer are all other components to allow the user to easily view, probe, and evaluate the TPS43061 control IC. The remaining area is filled with ground. The remaining three layers have additional copper for VIN, VOUT, AGND, and PGND connected with multiple vias. Additional copper is also connected to the sense resistor to aid with thermal dissipation. The second internal layer and bottom layer contain signal routes. Five vias directly under the TPS43061 device provide a thermal path from the top-side ground plane to the bottom-side and internal AGND plane. Lastly, the layout guidelines should be followed for the CSD86330Q3D which includes 12 vias beneath the device to the internal and bottom PGND planes to aid with thermal dissipation.

All noise-sensitive analog circuitry are placed as close as possible to the IC. The voltage divider network ties to the output voltage at the point of regulation on the bottom layer, near the output capacitors. Q1 is also placed as close as possible to the IC to keep the gate-drive traces as short as possible. The output capacitors are placed next to Q1 to limit the length of the high frequency switching current path. The SW copper is kept as small as possible to limit radiated noise from the high-frequency switching voltage node. The power pad is connected to the AGND pin and all noise-sensitive circuitry must use this as the ground return path. The ground return for the power components are connected to the PGND pin. The AGND and PGND are connected at one point near the PGND pin. The bypass capacitors for VIN and VCC are placed next to their respective pins. The filter capacitor between ISNS+ and ISNS- is located next to the pins to help filter out switching noise. An additional input bulk capacitor may be required (C13) depending on the connection to the EVM from the input supply. See the product datasheet for all layout recommendations.

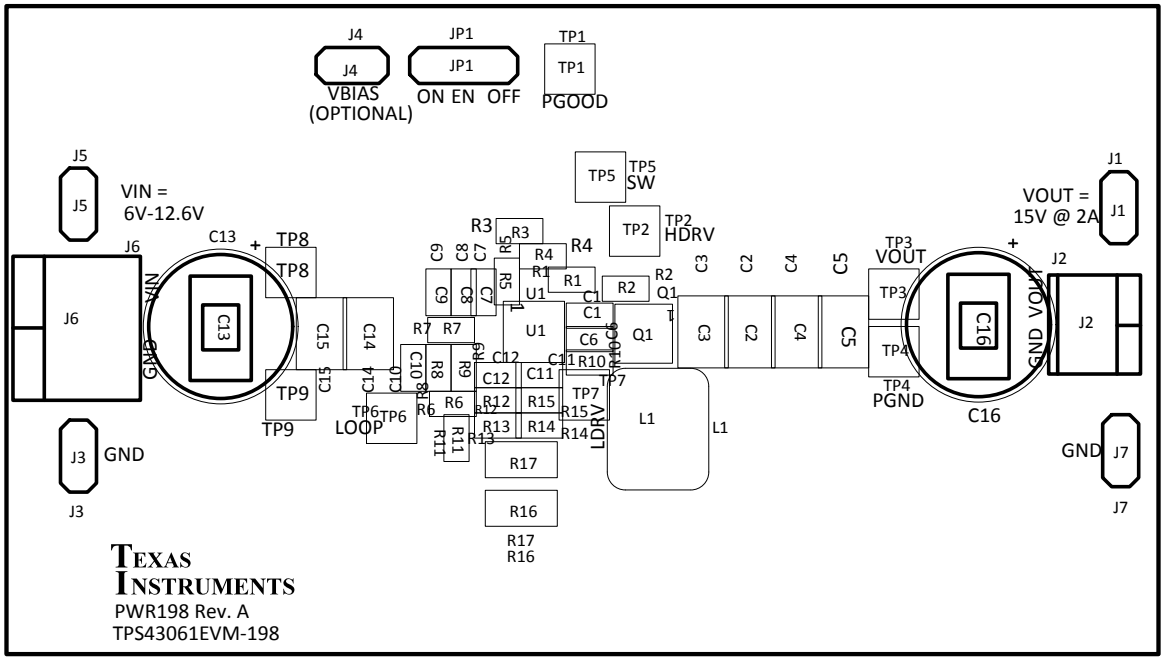


Figure 18. TPS43061EVM-198 Top Assembly and Silkscreen

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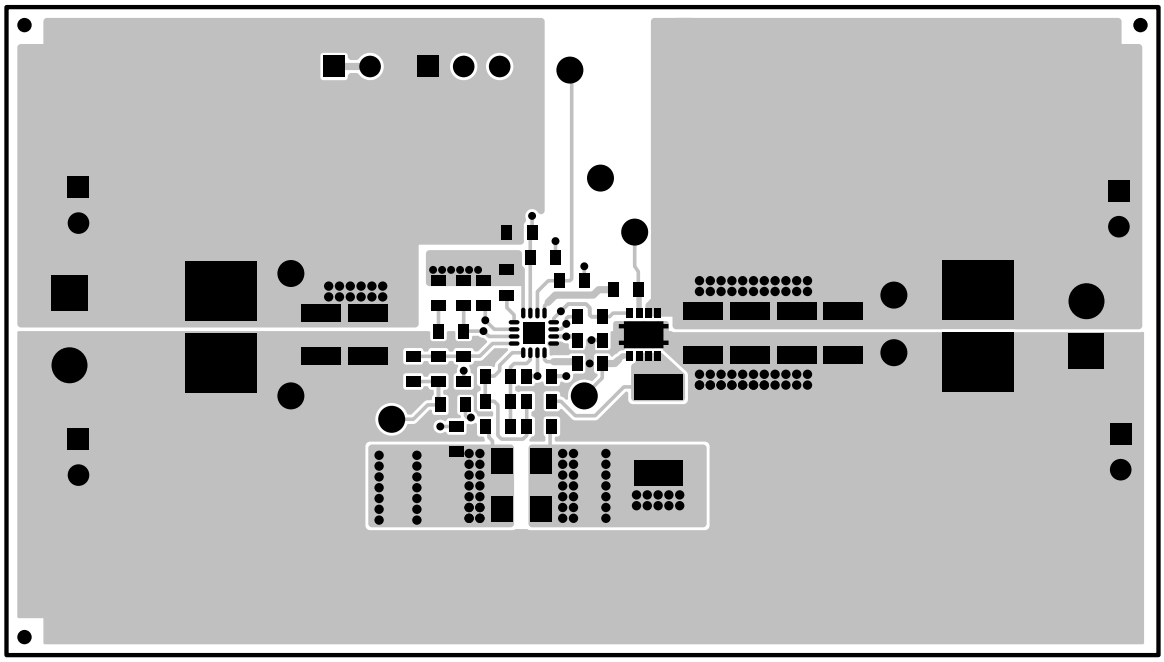


Figure 19. TPS43061EVM-198 Top-Side Layout

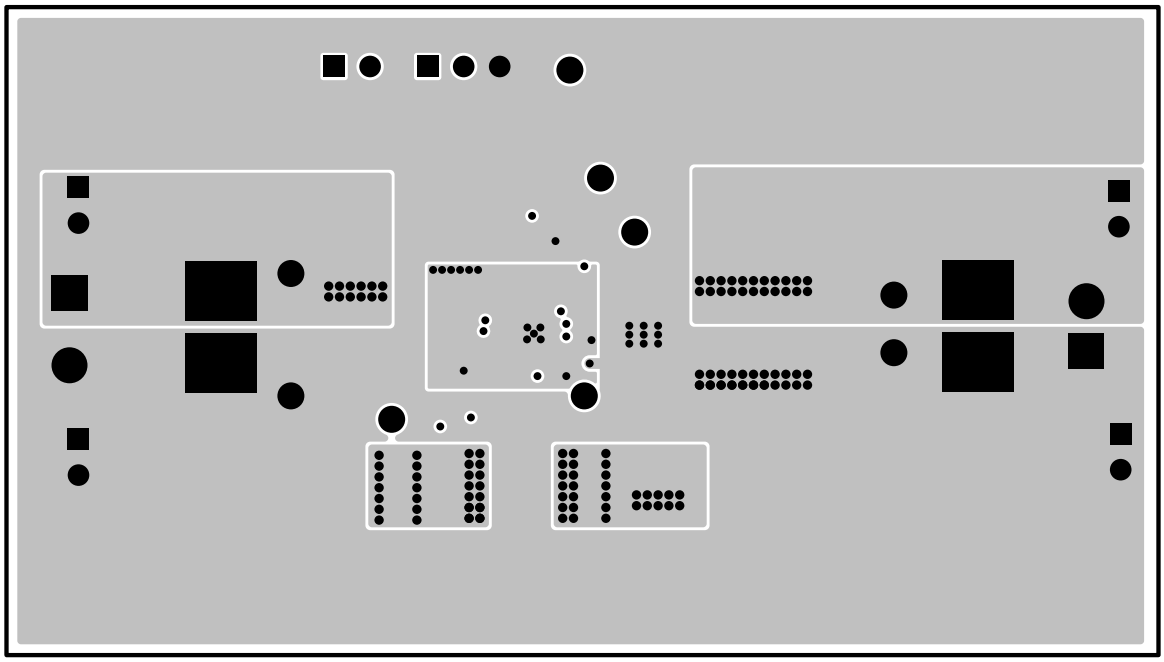


Figure 20. TPS43061EVM-198 Layer 2 Layout

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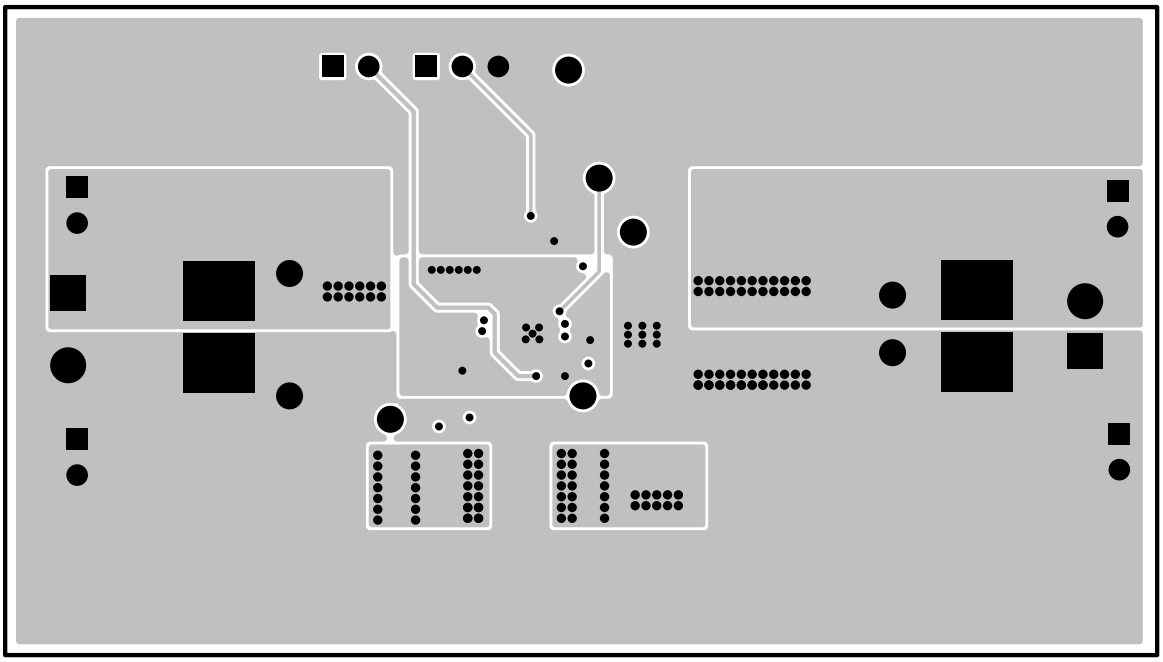


Figure 21. TPS43061EVM-198 Layer 3 Layout

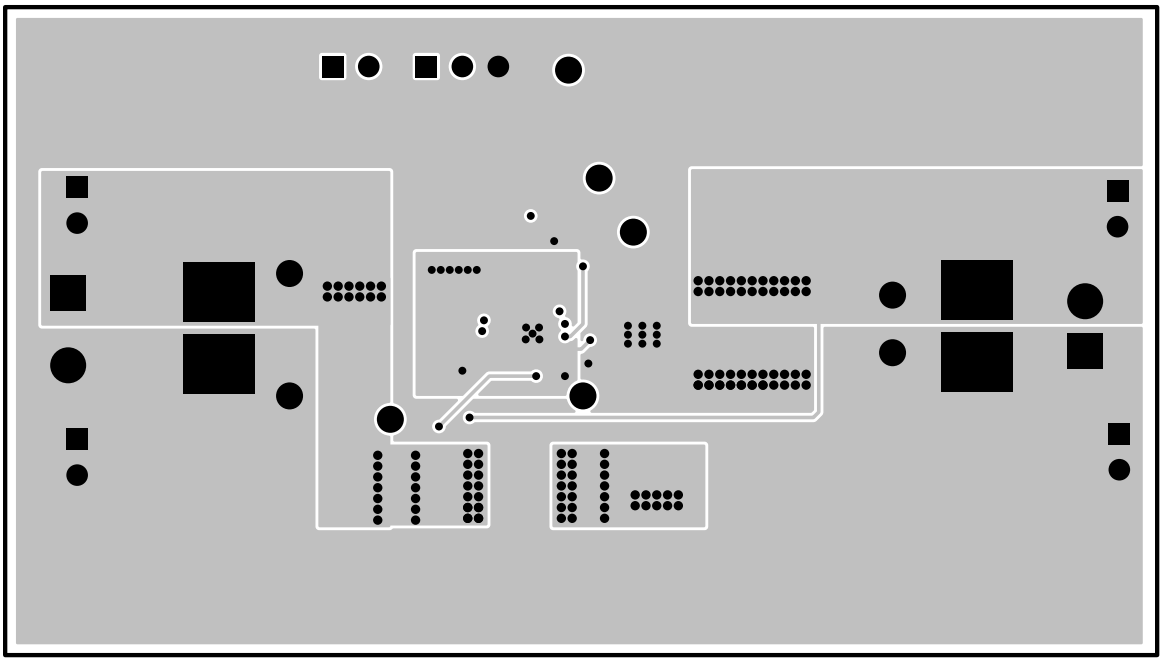


Figure 22. TPS43061EVM-198 Bottom-Side Layout

4.2 Estimated Circuit Area

The estimated printed-circuit-board area by outlining the components used in this design and the routing between them is 0.91 in^2 (590 mm^2). This area does not include test points or connectors. Also note, this design uses 0603 components for easy modifications and places all components on one layer so this area may be reduced.

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General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

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4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

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